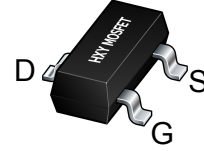




## Description

The LP2309LT1G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is well suited for use as a load switch or in PWM applications.



SOT-23

## General Features

$V_{DS} = -60V, I_D = -2A$

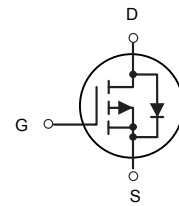
$R_{DS(ON)} < 160m\Omega @ V_{GS} = -10V$

$R_{DS(ON)} < 200m\Omega @ V_{GS} = -4.5V$

## Application

Load switch

PWM application



P-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
LP2309LT1G	SOT-23	N9ADE	3000

## Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	-2	A
$I_{DM}$	Drain Current-Pulsed (Note 1)	-8	A
$P_D$	Maximum Power Dissipation	1.5	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 150	°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	83.3	°C/W



### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.4	-2.0	-2.6	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-1.5A	-	140	160	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1.5A	-	160	200	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-1.5A	-	3	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, F=1.0MHz	-	444.2	-	PF
Output Capacitance	C <sub>oss</sub>		-	19.6	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	17.9	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-30V, I <sub>D</sub> =-1.5A, V <sub>GS</sub> =-10V, R <sub>G</sub> =3Ω	-	40	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	35	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-30V, I <sub>D</sub> =-1.5A, V <sub>GS</sub> =-10V	-	11.3	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.7	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	1.6	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.5A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	-1.6	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = -1.5A	-	25		nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100A/μs (Note 3)	-	31		nC

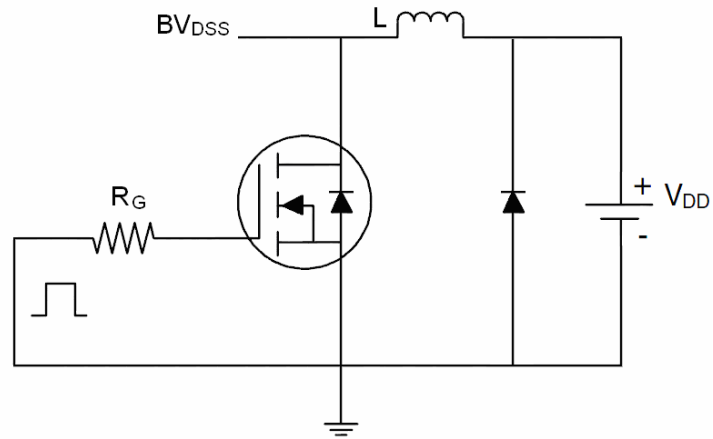
#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

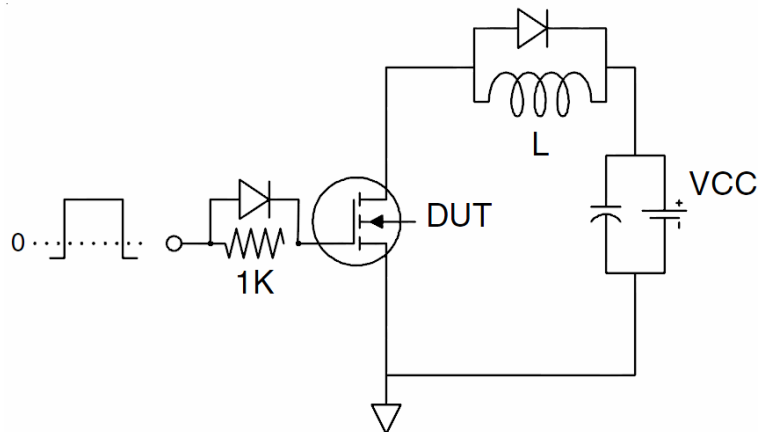


## Test Circuit

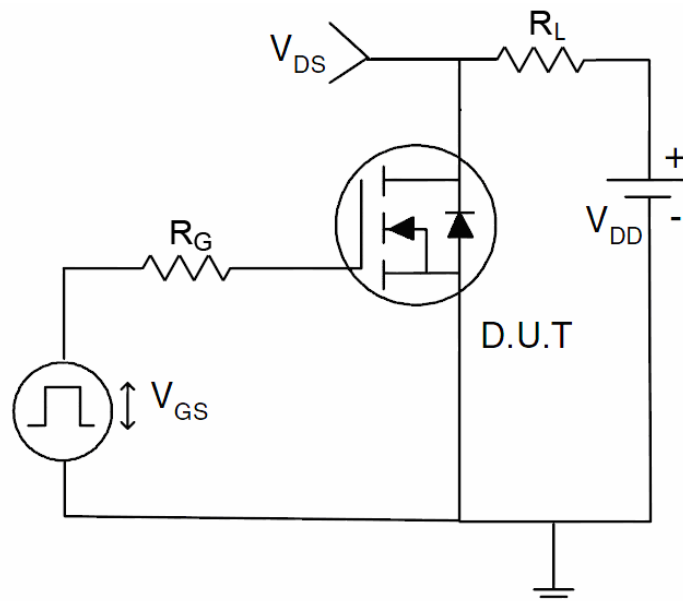
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit





### Typical Electrical and Thermal Characteristics (Curves)

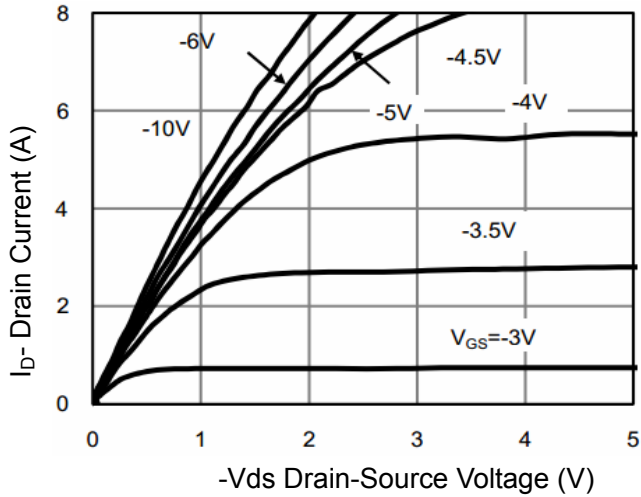


Figure 1 Output Characteristics

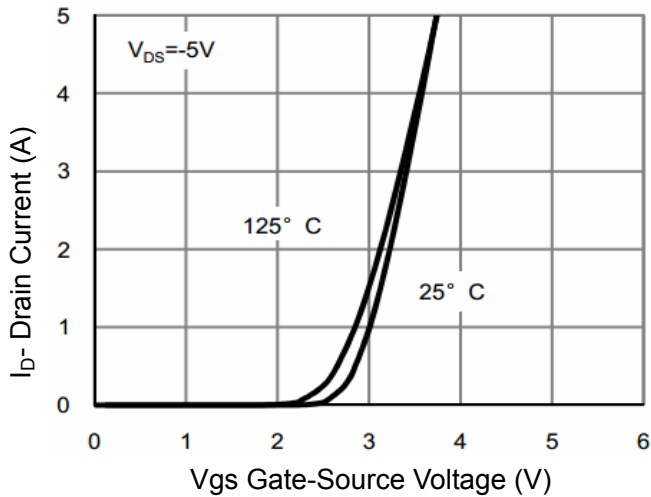


Figure 2 Transfer Characteristics

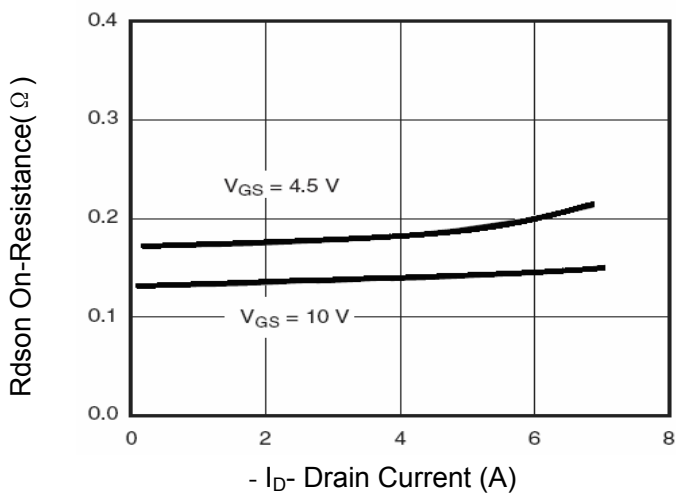


Figure 3 Rdson- Drain Current

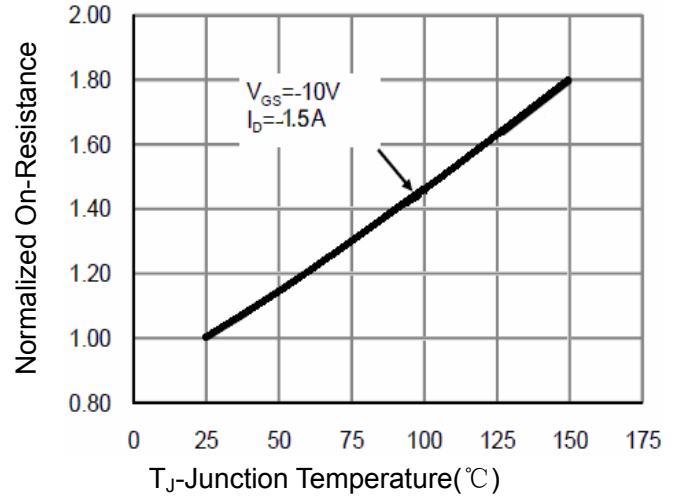


Figure 4 Rdson-Junction Temperature

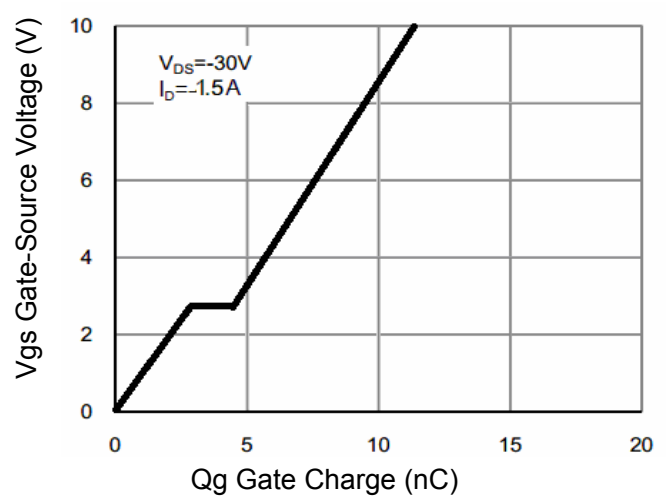


Figure 5 Gate Charge

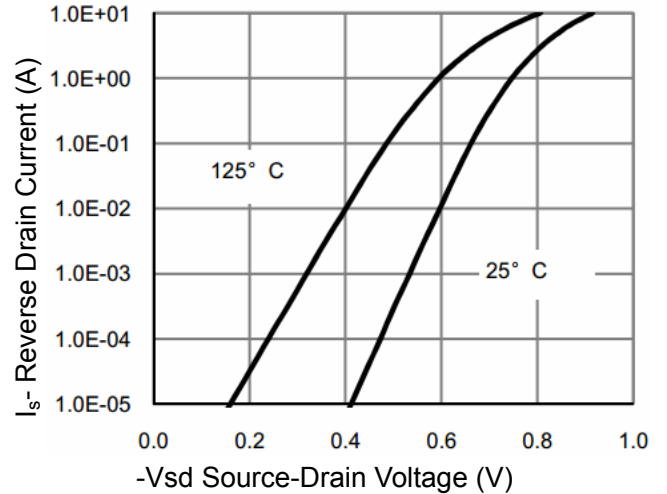


Figure 6 Source- Drain Diode Forward

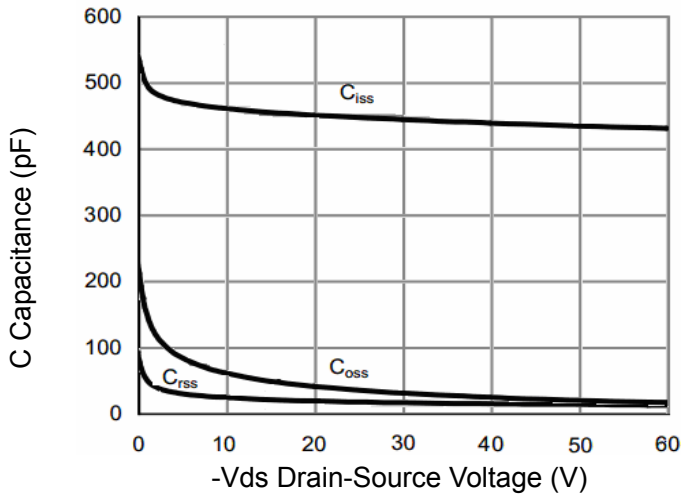


Figure 7 Capacitance vs Vds

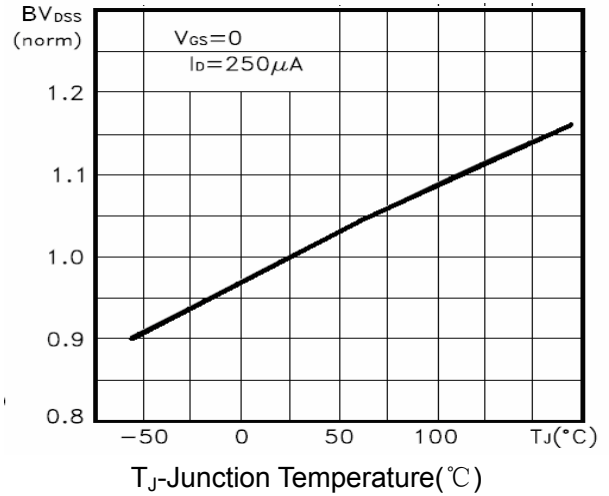


Figure 9  $BV_{DSS}$  vs Junction Temperature

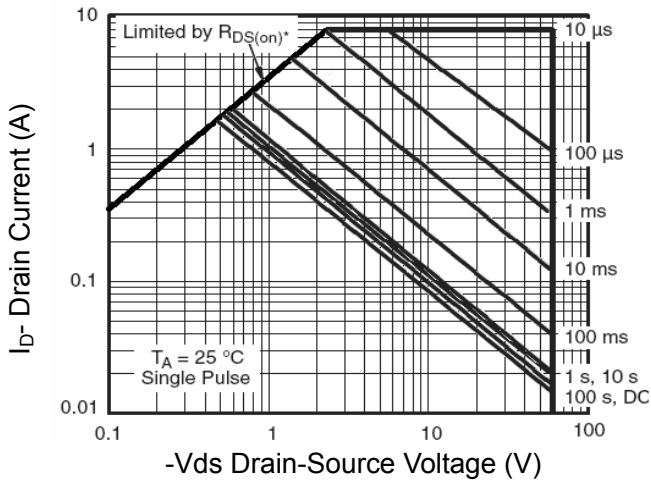


Figure 8 Safe Operation Area

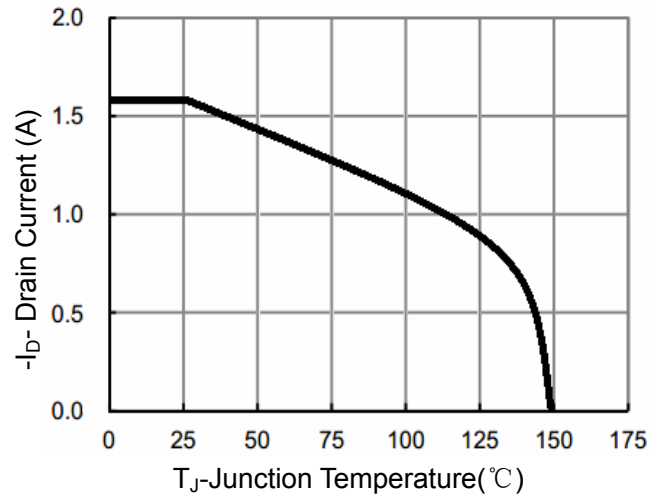


Figure 10  $I_D$  Current De-rating

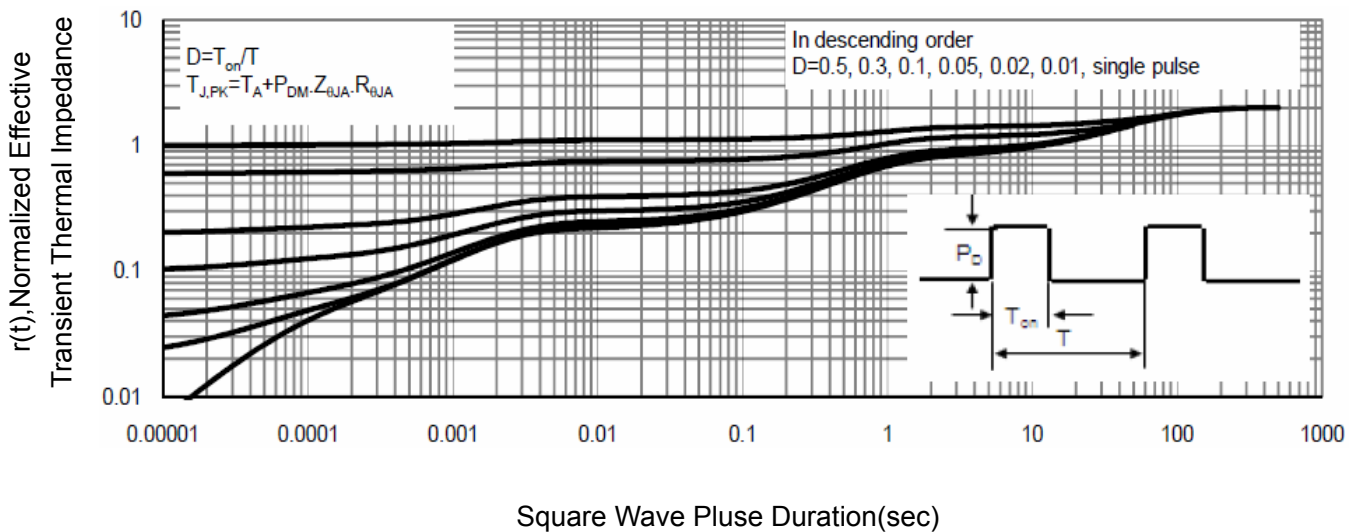
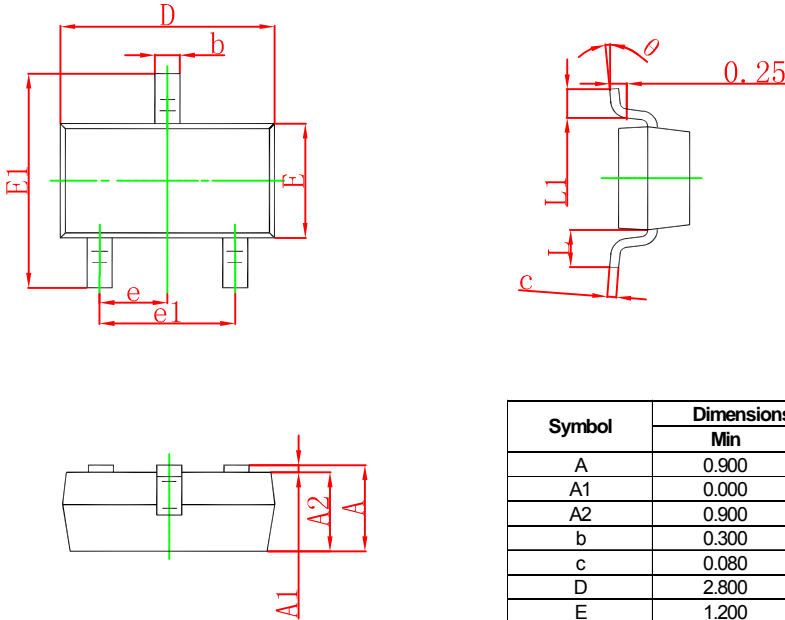


Figure 11 Normalized Maximum Transient Thermal Impedance

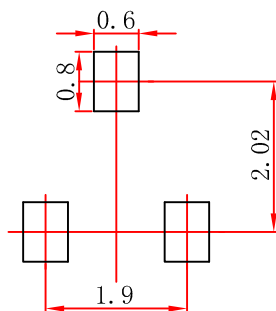


### SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

### SOT-23 Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.05\text{mm}$ .
  3. The pad layout is for reference purposes only.



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