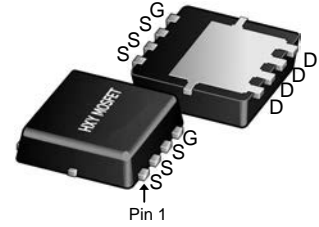




General Description

The NVTFS5C471NL use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable.

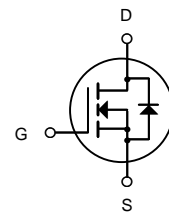


DFN3X3-8L

General Features

$V_{DS} = 40V$ $I_D = 60A$

$R_{DS(ON)} < 8.5m\Omega @ V_{GS} = 10V$



N-Channel MOSFET

Applications

Consumer electronic power supply Motor control
Synchronous-rectification Isolated DC
Synchronous-rectification applications

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
NVTFS5C471NL	DFN3X3-8L	HXY MOSFET	5000

Absolute Maximum Ratings at $T_j = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V _{DS}	40	V
Gate source voltage	V _{GS}	±20	V
Continuous drain current ¹⁾	I _D	60	A
Pulsed drain current ²⁾	I _{D, pulse}	130	A
Power dissipation ³⁾	P _D	39	W
Single pulsed avalanche energy ⁵⁾	EAS	48	mJ
Operation and storage temperature	T _{stg} , T _j	-55 to 150	°C
Thermal resistance, junction-case	R _{θJC}	3.2	°C/W
Thermal resistance, junction-ambient ⁴⁾	R _{θJA}	60	°C/W



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12A$	---	6.9	8.5	m Ω
		$V_{GS}=4.5V, I_D=10A$	---	10.0	15	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.35	---	3	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	---	5.8	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	1.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=1A$	---	14.3	---	ns
T_r	Rise Time		---	5.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	20	---	
T_f	Fall Time		---	11	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	690	---	μF
C_{oss}	Output Capacitance		---	193	---	
C_{rss}	Reverse Transfer Capacitance		---	38	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	60	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=31A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

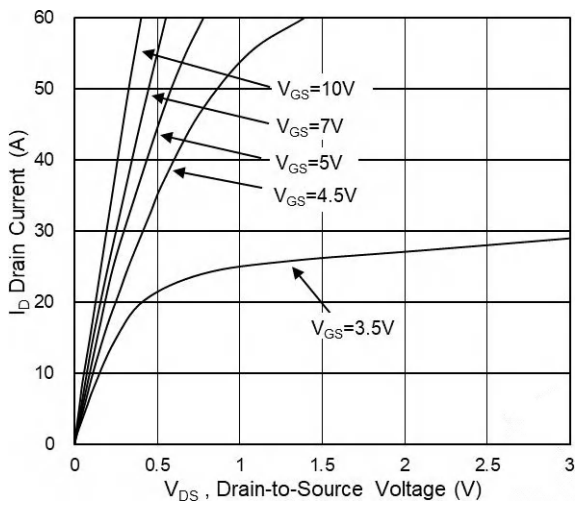


Fig.1 Typical Output Characteristics

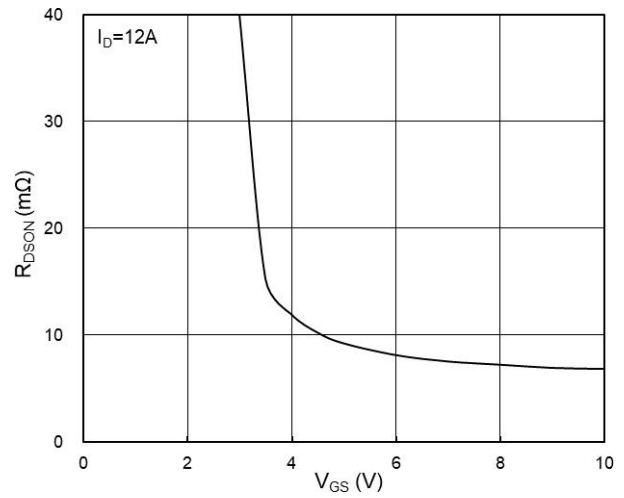


Fig.2 On-Resistance vs G-S Voltage

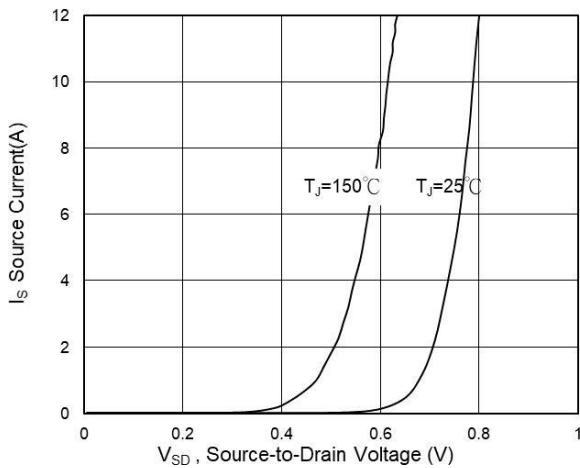


Fig.3 Source Drain Forward Characteristics

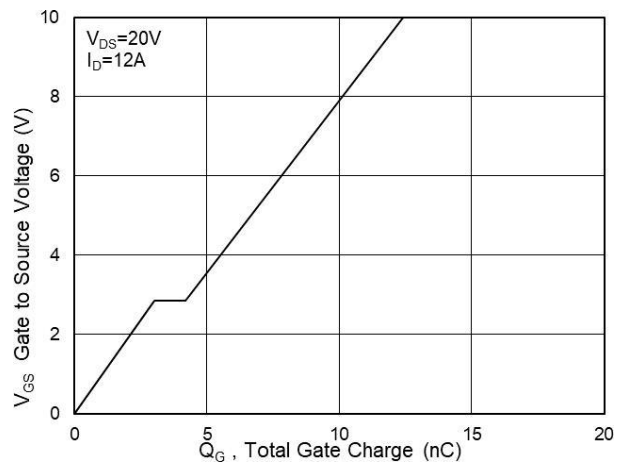


Fig.4 Gate-Charge Characteristics

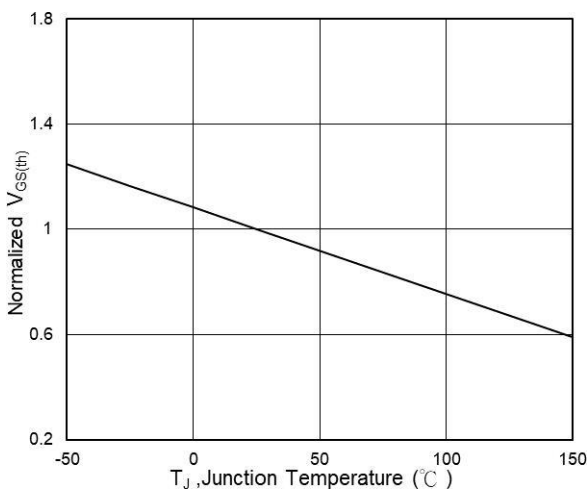


Fig.5 Normalized $V_{GS(th)}$ vs T_J

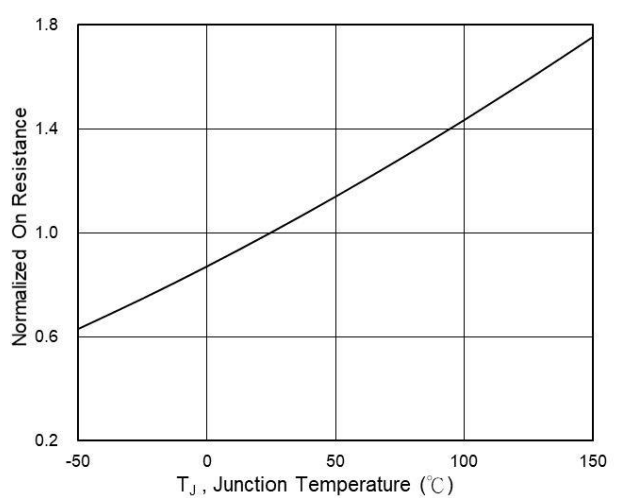


Fig.6 Normalized $R_{DS(on)}$ vs T_J

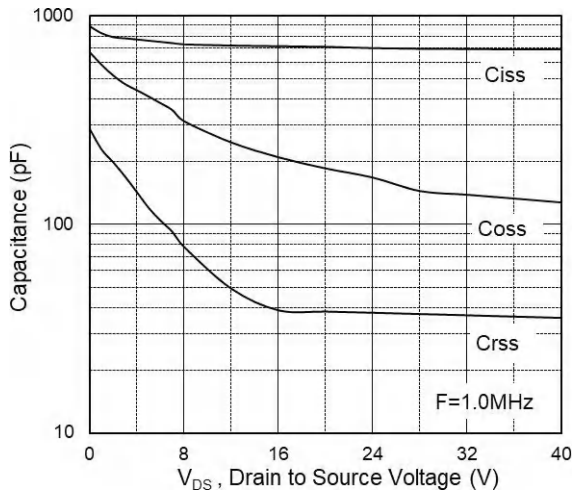


Fig.7 Capacitance

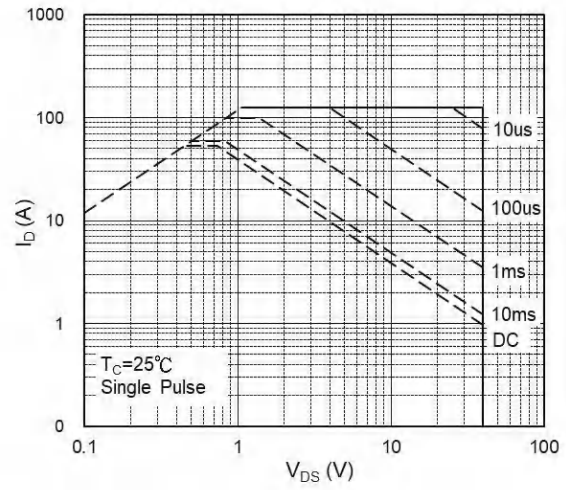


Fig.8 Safe Operating Area

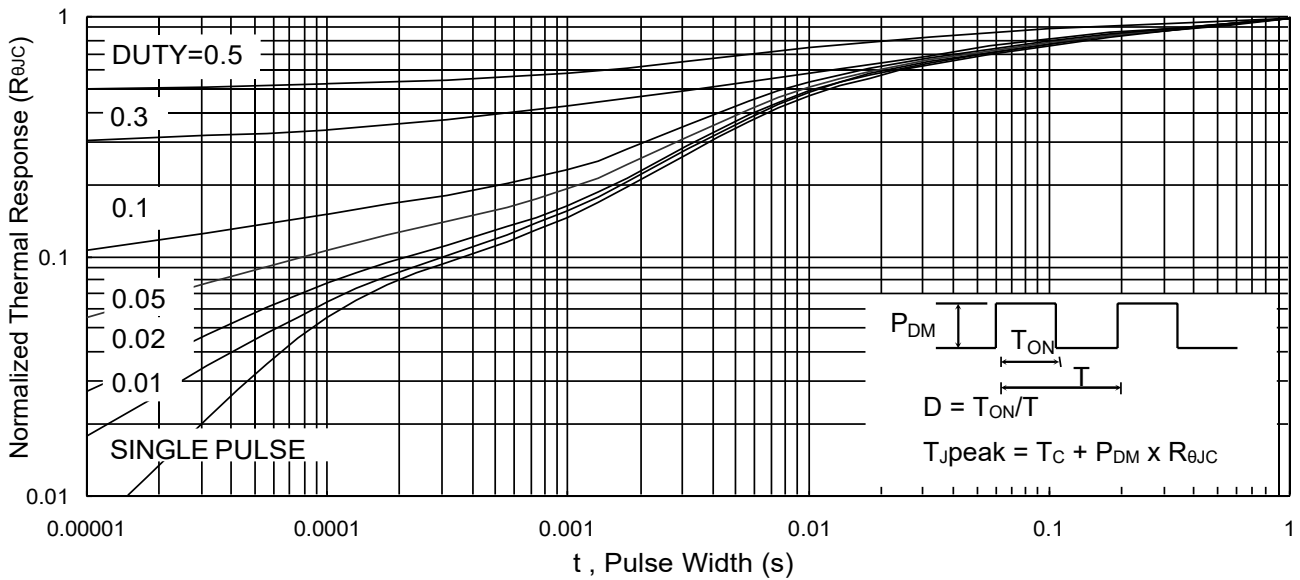


Fig.9 Normalized Maximum Transient Thermal Impedance

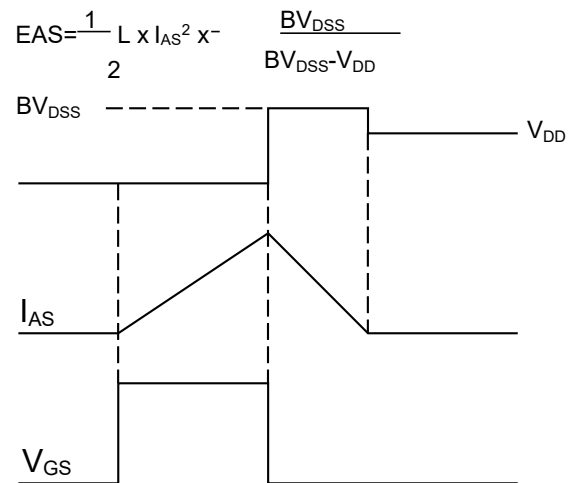
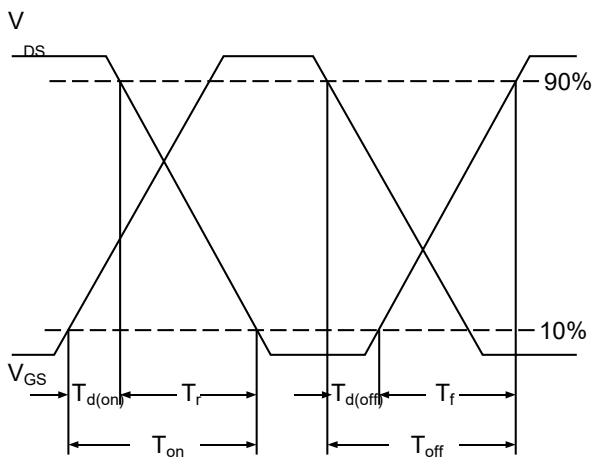
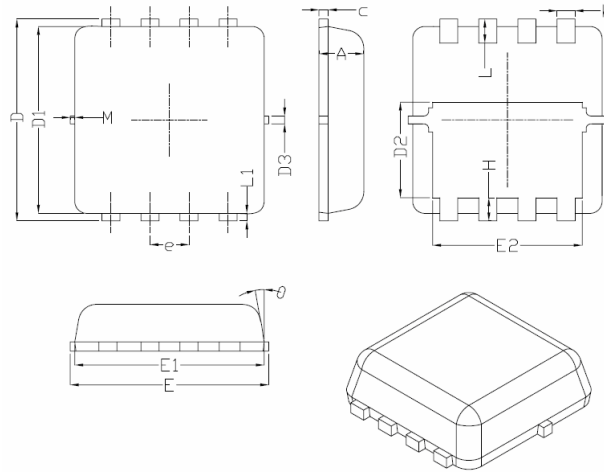


Fig.11 Unclamped Inductive Waveform



DFN3X3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°



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