



## Description

The SI4447DY-T1-E3 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

## General Features

$V_{DS} = -40V$   $I_D = -13A$

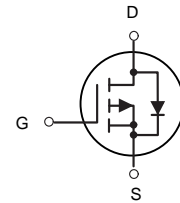
$R_{DS(ON)} < 19m\Omega @ V_{GS}=10V$

## Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI4447DY-T1-E3	SOP-8	HXY MOSFET	3000

## Absolute Maximum Ratings (Tc=25°C unless otherwise noted )

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	- 40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ C$	Drain Current <sup>3</sup> , $V_{GS} @ 10V$	-13	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	-52	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation	3	W
TSTG	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	41	°C/W



**Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-40	-	-	V
Gate-body Leakage current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T <sub>J</sub> =25°C	I <sub>DSS</sub> V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V	-	-	-1	μA
	T <sub>J</sub> =100°C		-	-	-100	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.0	-1.5	-2.2	V
Drain-Source On-Resistance <sup>4</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	14.0	19	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -5 A	-	19.5	25	
Forward Transconductance <sup>4</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -10A	-	44	-	S
<b>Dynamic Characteristics<sup>5</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, f = 1MHz	-	2525	-	pF
Output Capacitance	C <sub>oss</sub>		-	190	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	172	-	
Gate Resistance	R <sub>g</sub>	f = 1MHz	-	10	-	Ω
<b>Switching Characteristics<sup>5</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -20V, I <sub>D</sub> = -10A	-	35	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	8	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -10V, V <sub>DD</sub> = -20V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = -10A	-	14.5	-	ns
Rise Time	t <sub>r</sub>		-	20.2	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	32	-	
Fall Time	t <sub>f</sub>		-	10	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>4</sup>	V <sub>SD</sub>	I <sub>S</sub> = -10A, V <sub>GS</sub> = 0V	-	-	-1.2	V
Continuous Source Current	I <sub>S</sub>	T <sub>C</sub> =25°C	-	-	-13	A

Note :

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C.
2. The EAS data shows Max. rating . The test condition is V<sub>DD</sub>= -25V, V<sub>GS</sub>= -10V, L= 0.1mH, I<sub>AS</sub>= -34A.
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.



### Typical Characteristics

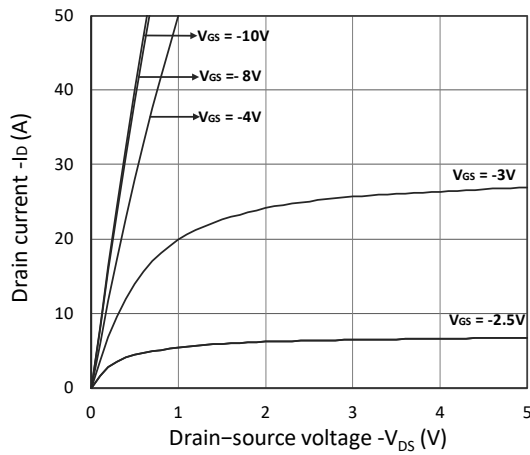


Figure 1. Output Characteristics

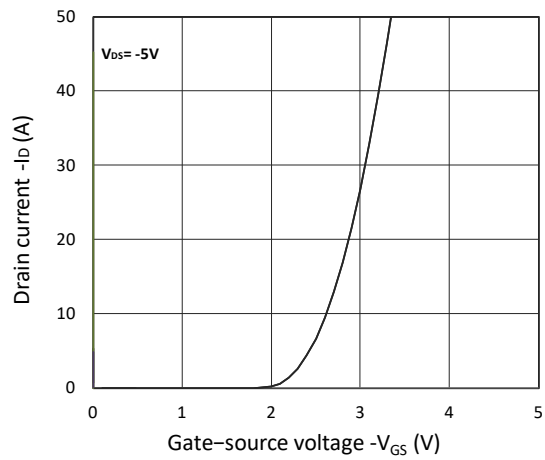


Figure 2. Transfer Characteristics

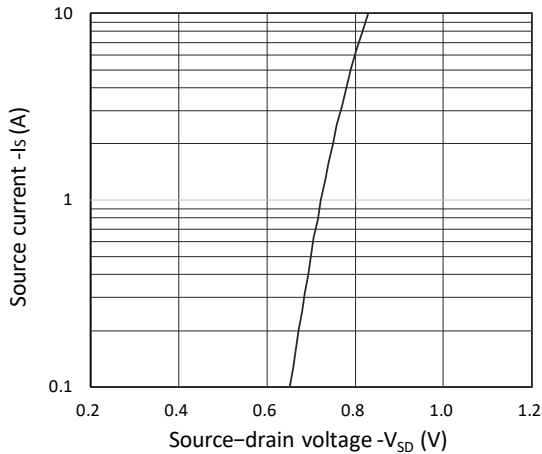


Figure 3. Forward Characteristics of Reverse

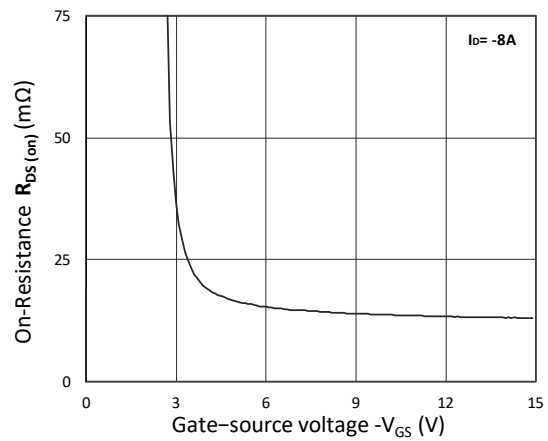


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

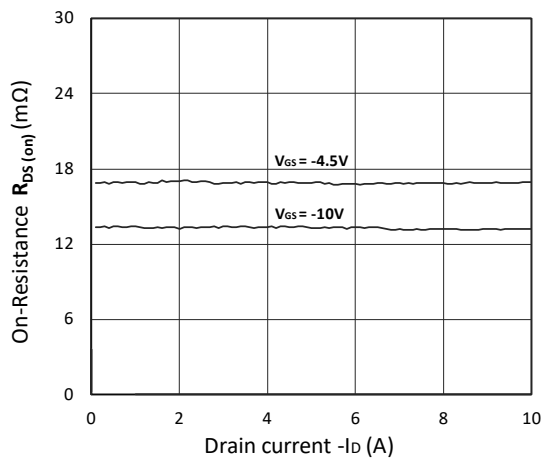


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

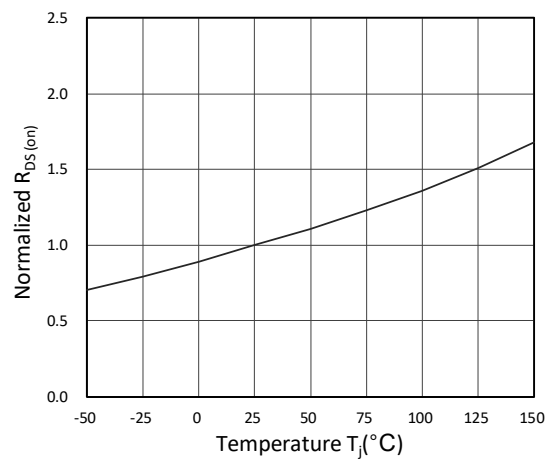


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

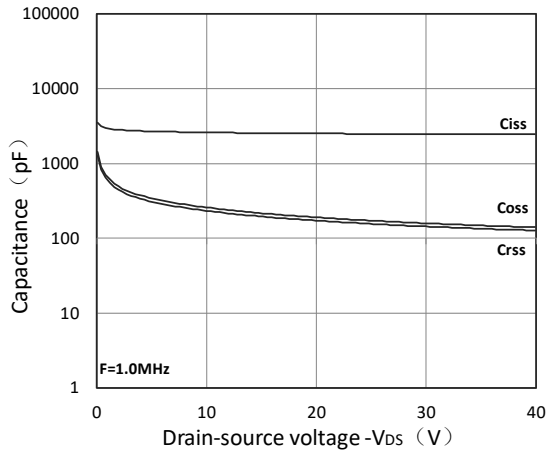


Figure 7. Capacitance Characteristics

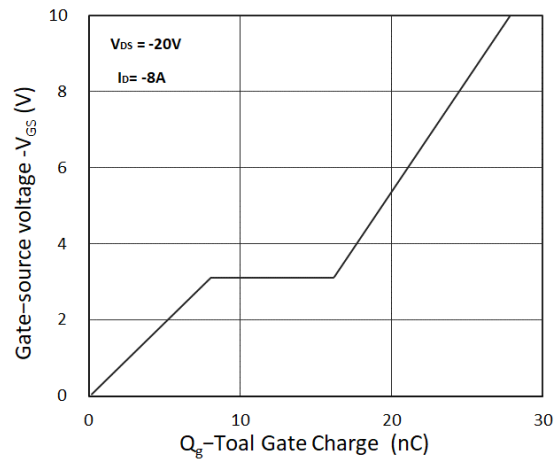


Figure 8. Gate Charge Characteristics

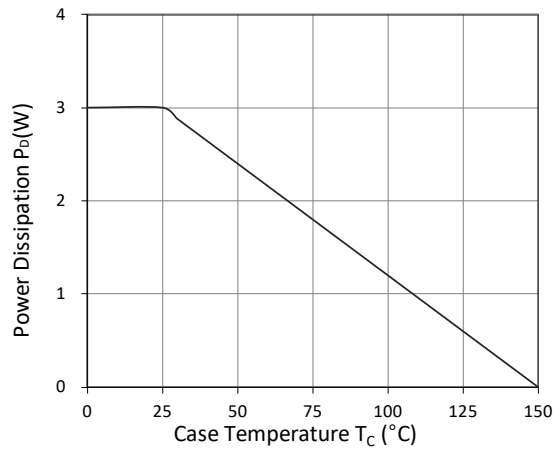


Figure 9. Power Dissipation

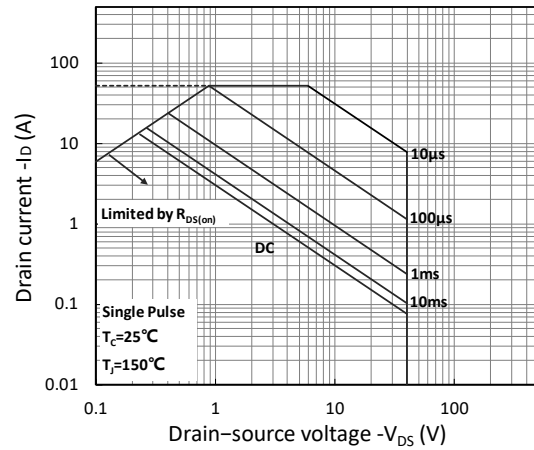


Figure 10. Safe Operating Area

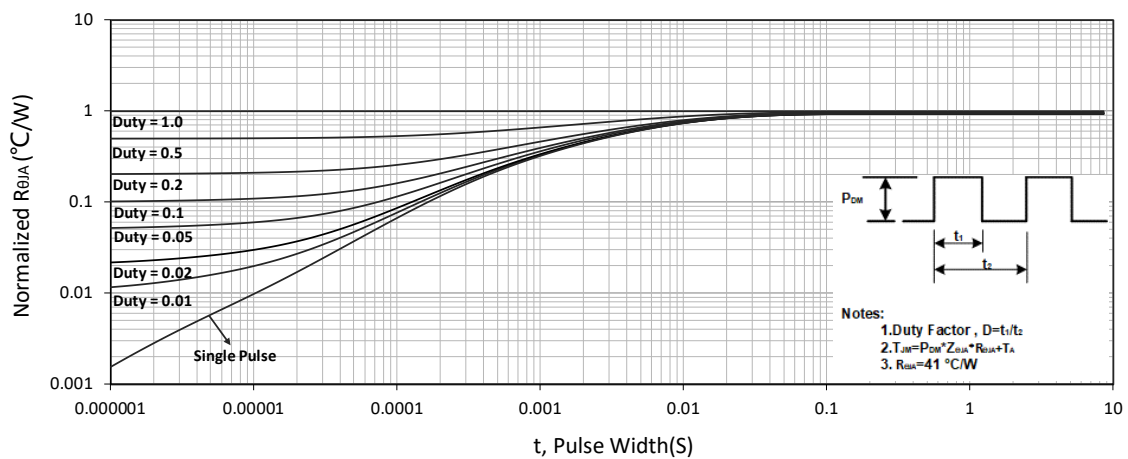


Figure 11. Normalized Maximum Transient Thermal Impedance



### Test Circuit

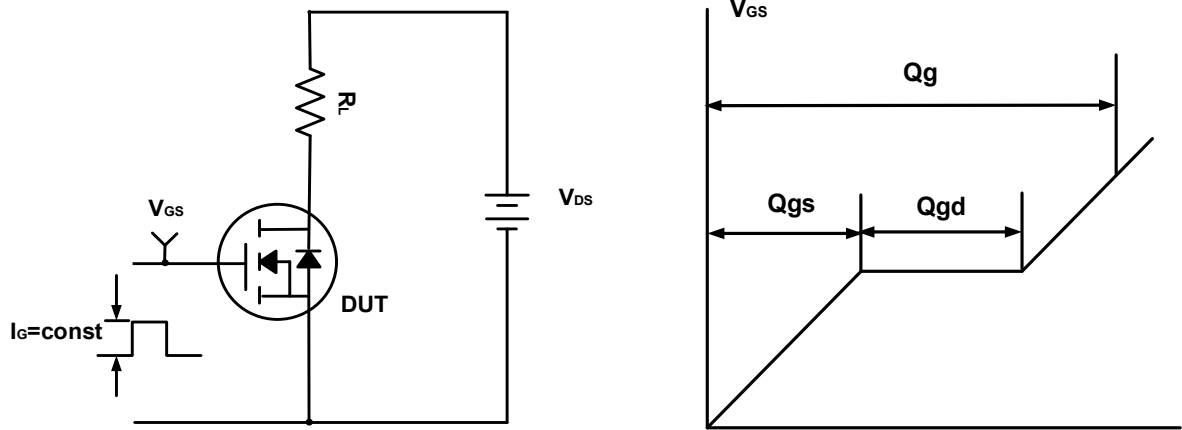


Figure A. Gate Charge Test Circuit & Waveforms

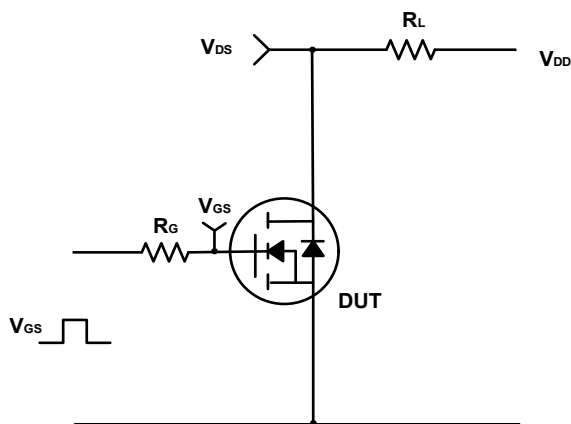


Figure B. Switching Test Circuit & Waveforms

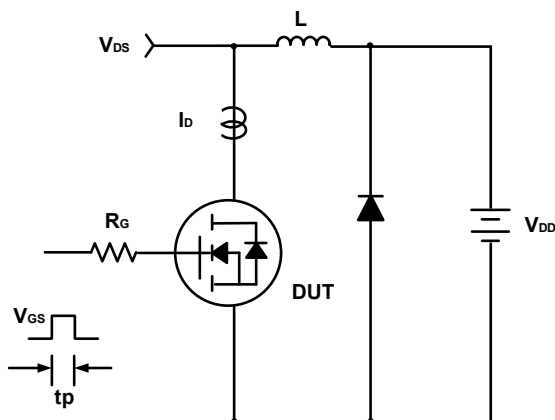
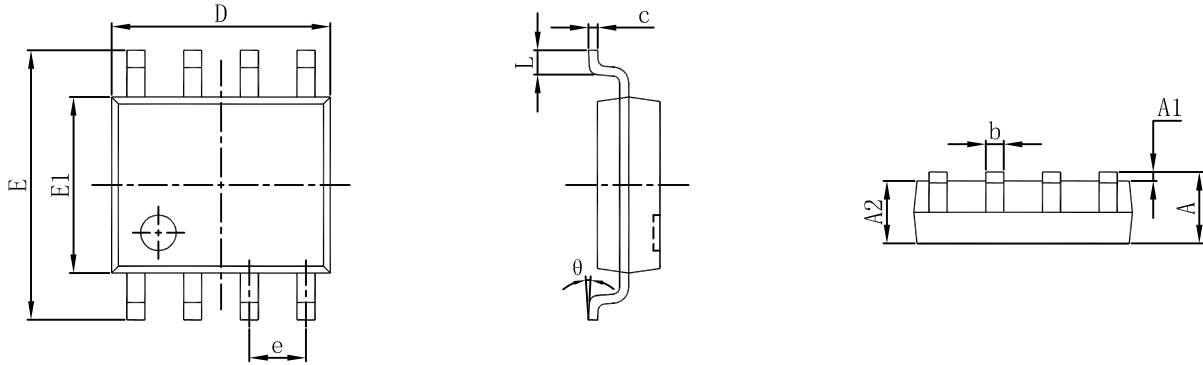


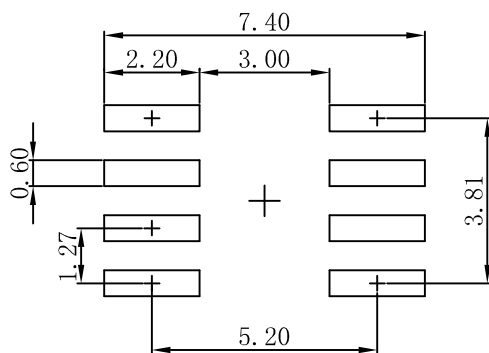
Figure C. Unclamped Inductive Switching Circuit & Waveforms



### SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.05\text{mm}$ .  
 3. The pad layout is for reference purposes only.



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