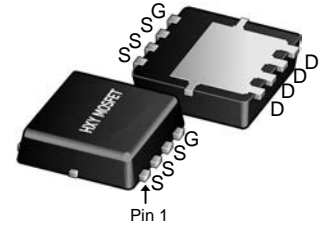




Description

The SI7121ADN-T1-GE3 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.



DFN3X3-8L

General Features

$V_{DS}=-30V, I_D=-40A$

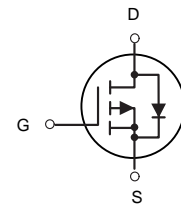
$R_{DS(ON)}<15m\Omega @V_{GS}=-10V$

$R_{DS(ON)}<26m\Omega @ V_{GS}=-4.5V$

Application

High side switch for full bridge converter

DC/DC converter for LCD display



P-Channel MOSFET

Package Marking and Ordering Information

| Product ID | Pack | Brand | Qty(PCS) |
|------------------|-----------|------------|----------|
| SI7121ADN-T1-GE3 | DFN3X3-8L | HXY MOSFET | 5000 |

Absolute Maximum Ratings@ $T_j=25^\circ C$ (unless otherwise specified)

| Symbol | Parameter | Rating | Units |
|----------------------|---|------------|--------------|
| VDS | Drain-Source Voltage | -30 | V |
| VGS | Gate-Source Voltage | +25 | V |
| $I_D@T_A=25^\circ C$ | Drain Current ³ , $V_{GS} @ 10V$ | -40 | A |
| $I_D@T_A=70^\circ C$ | Drain Current ³ , $V_{GS} @ 10V$ | -25 | A |
| IDM | Pulsed Drain Current ¹ | -120 | A |
| $P_D@T_A=25^\circ C$ | Total Power Dissipation | 15 | W |
| TSTG | Storage Temperature Range | -55 to 150 | $^\circ C$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ C$ |
| Rthj-c | Maximum Thermal Resistance, Junction-case | 6 | $^\circ C/W$ |
| Rthj-a | Maximum Thermal Resistance, Junction-ambient ³ | 66 | $^\circ C/W$ |



Electrical Characteristics (T_J=25°C unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|----------------------|--|---|------|------|------|-------|
| V _{(BR)DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D = -250μA | -30 | - | - | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = -30V, V _{GS} =0V, | - | - | -1 | μA |
| I _{GSS} | Gate to Body Leakage Current | V _{DS} =0V, V _{GS} = ±20V | - | - | ±100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D = -250μA | -1.0 | -1.6 | -2.5 | V |
| R _{DS(on)} | Static Drain-Source on-Resistance Note3 | V _{GS} = -10V, I _D = -10A | - | 12 | 15 | mΩ |
| | | V _{GS} = -4.5V, I _D = -5A | - | 18 | 26 | |
| C _{iss} | Input Capacitance | V _{DS} = -15V, V _{GS} =0V, f=1.0MHz | - | 1330 | - | pF |
| C _{oss} | Output Capacitance | | - | 183 | - | pF |
| C _{rss} | Reverse Transfer Capacitance | | - | 156 | - | pF |
| Q _g | Total Gate Charge | V _{DS} = -15V, I _D = -5A, V _{GS} = -10V | - | 22 | - | nC |
| Q _{gs} | Gate-Source Charge | | - | 1.0 | - | nC |
| Q _{gd} | Gate-Drain("Miller") Charge | | - | 1.8 | - | nC |
| t _{d(on)} | Turn-on Delay Time | V _{DD} = -15V, I _D = -10A, V _{GS} =-10V, R _{GEN} =2.5Ω | - | 9 | - | ns |
| t _r | Turn-on Rise Time | | - | 13 | - | ns |
| t _{d(off)} | Turn-off Delay Time | | - | 48 | - | ns |
| t _f | Turn-off Fall Time | | - | 20 | - | ns |
| I _S | Maximum Continuous Drain to Source Diode Forward Current | | - | - | -40 | A |
| I _{SM} | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | -90 | A |
| V _{SD} | Drain to Source Diode Forward Voltage | V _{GS} =0V, I _S = -15A | - | -0.8 | -1.2 | V |
| t _{rr} | Reverse Recovery Time | T _J =25°C, | - | 64 | - | ns |
| Q _{rr} | Reverse Recovery Charge | V _{DD} = -24V, I _F =-2.8A, di/dt=-100A/μs | - | 25 | - | nC |

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_{GS}=10V, R_G=25Ω, L=0.5mH, I_{AS}=-12.7A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

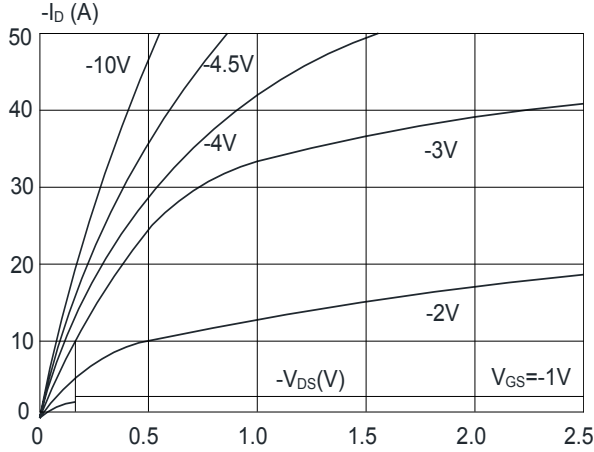


Figure 2: Typical Transfer Characteristics

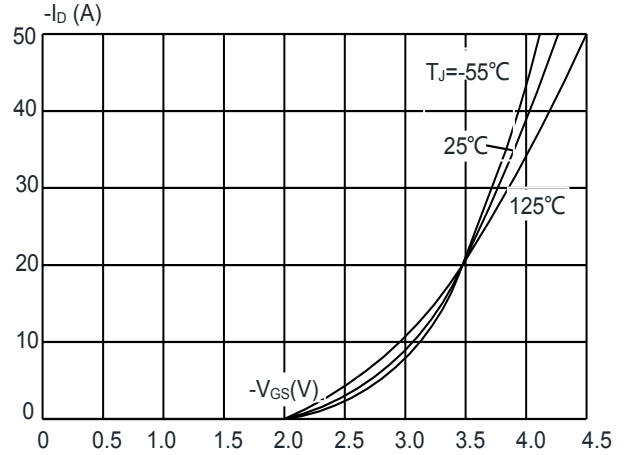


Figure 3: On-resistance vs. Drain Current

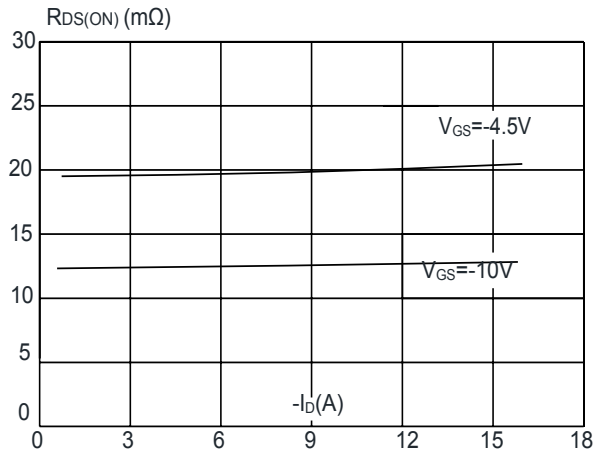


Figure 4: Body Diode Characteristics

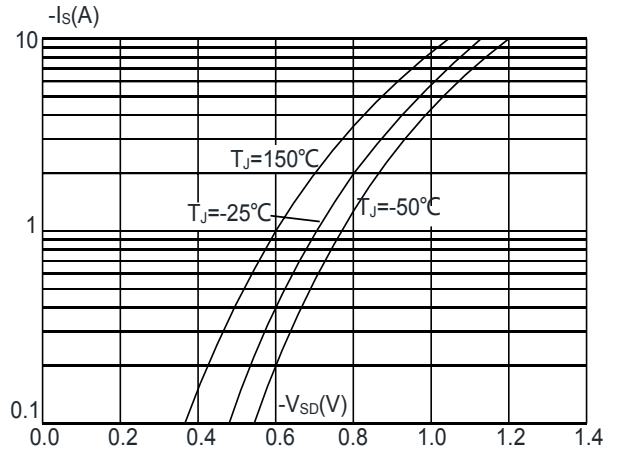


Figure 5: Gate Charge Characteristics

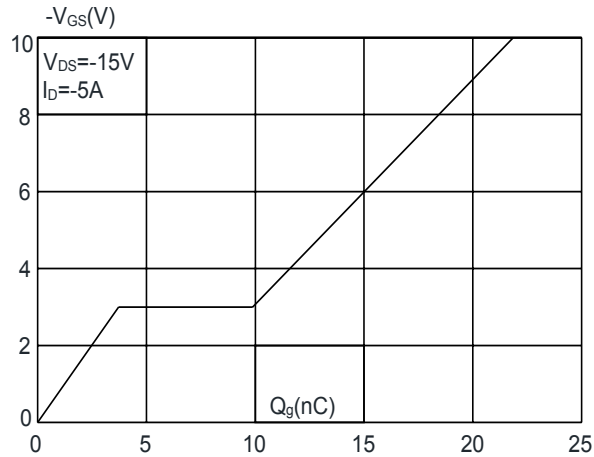


Figure 6: Capacitance Characteristics

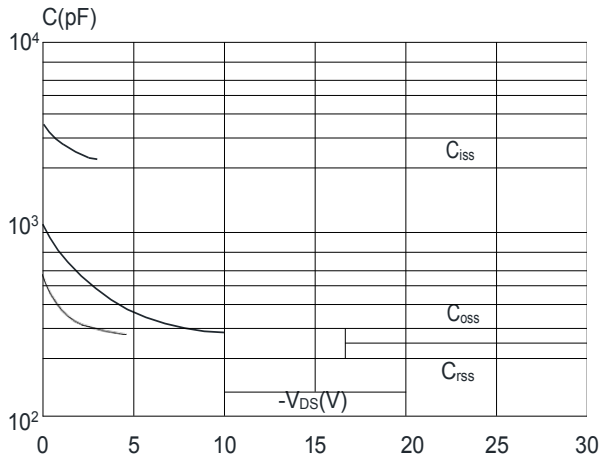




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

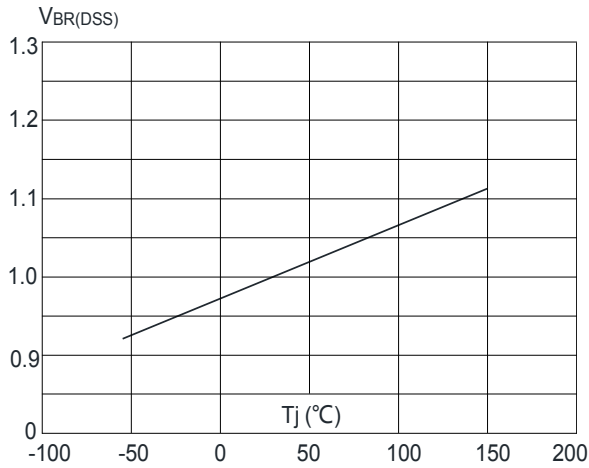


Figure 8: Normalized on Resistance vs. Junction Temperature

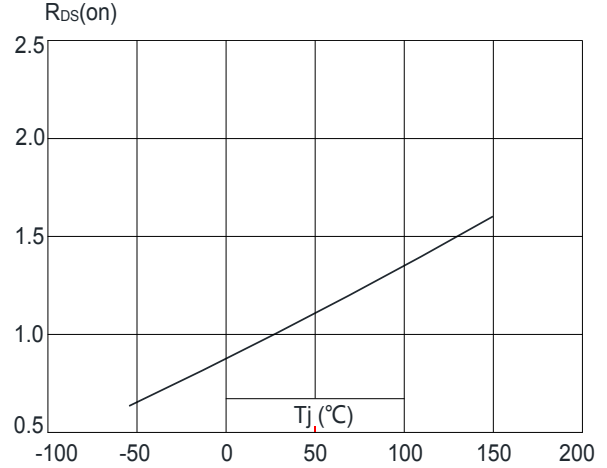


Figure 9: Maximum Safe Operating Area

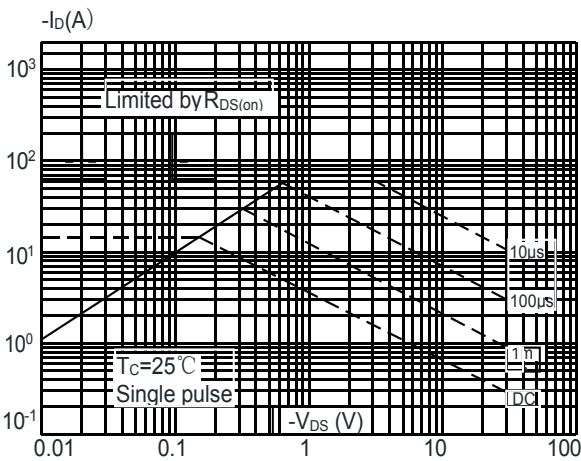


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

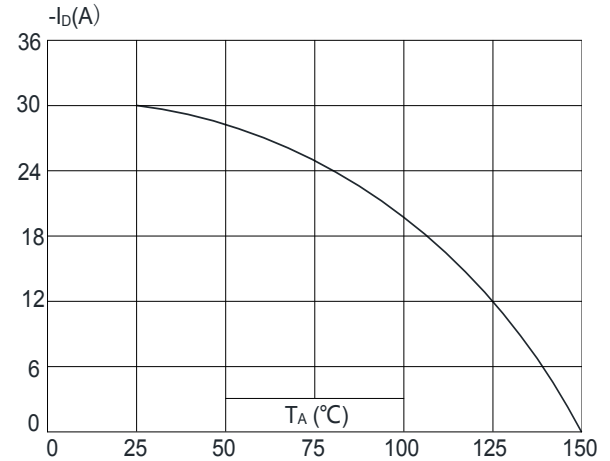
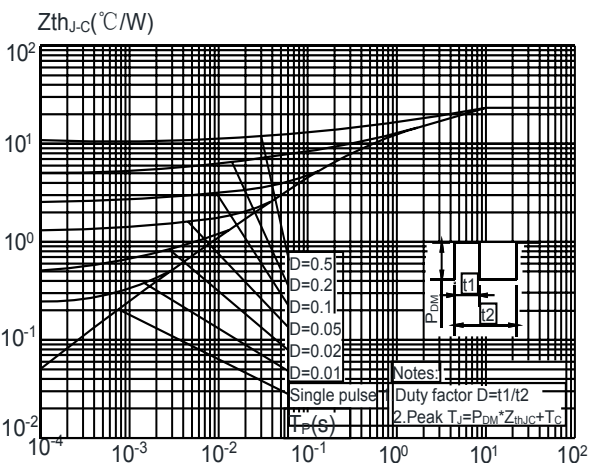


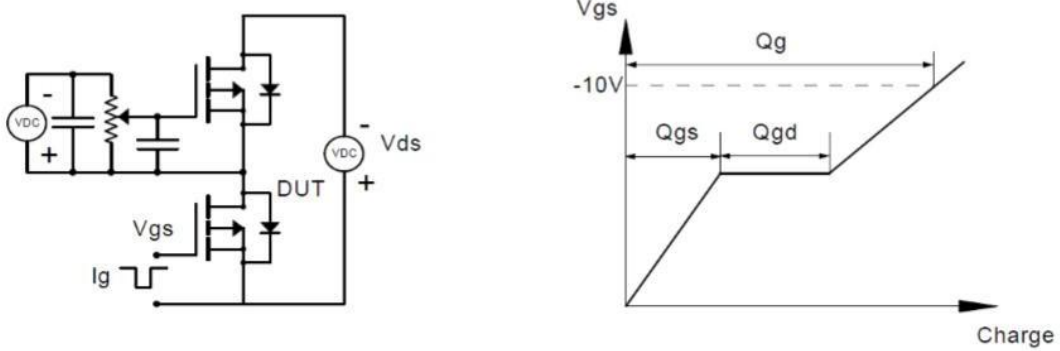
Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



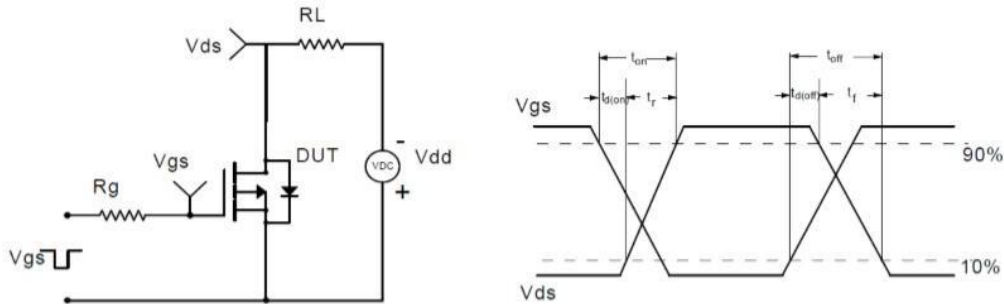


Test Circuit

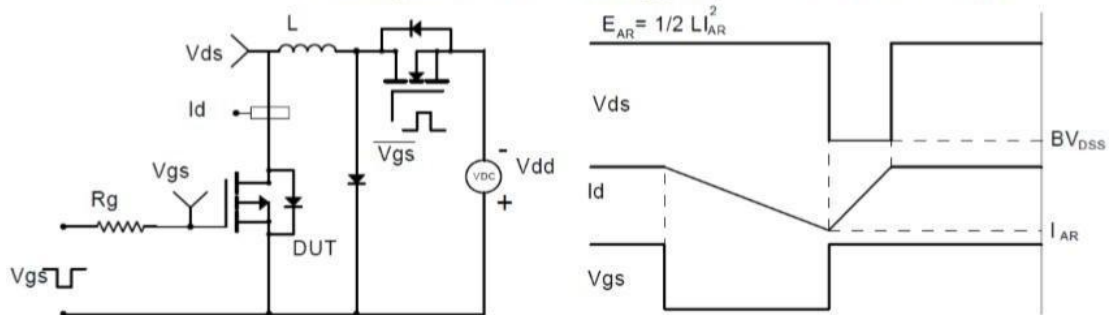
Gate Charge Test Circuit & Waveform



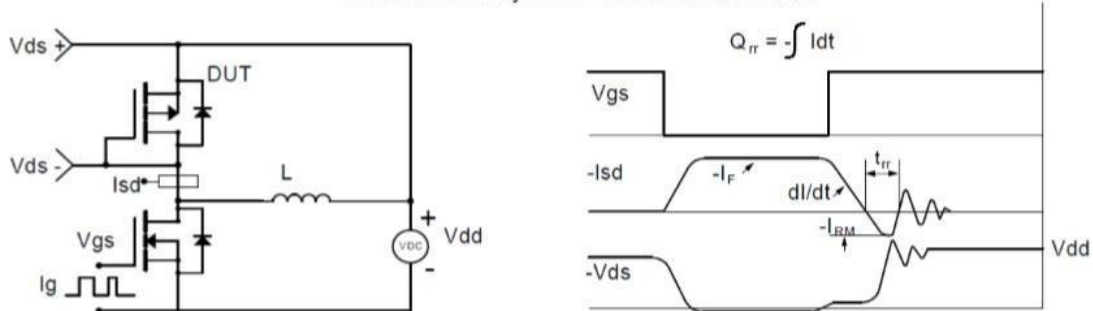
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

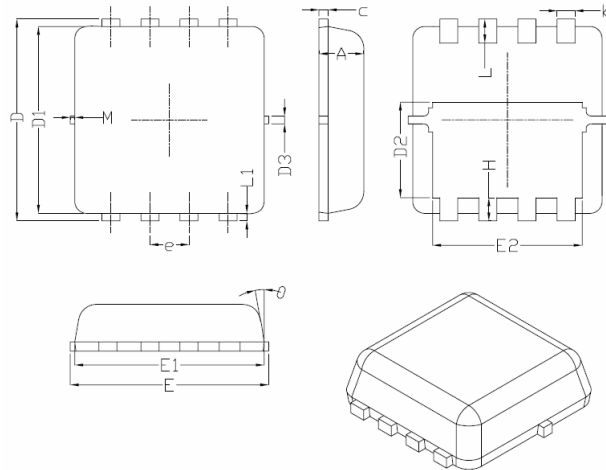


Diode Recovery Test Circuit & Waveforms





DFN3X3-8L Package Information



| Symbol | Dimensions In Millimeters | | |
|----------|---------------------------|------|------|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.25 | 0.30 | 0.35 |
| c | 0.10 | 0.15 | 0.25 |
| D | 3.25 | 3.35 | 3.45 |
| D1 | 3.00 | 3.10 | 3.20 |
| D2 | 1.48 | 1.58 | 1.68 |
| D3 | - | 0.13 | - |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 3.00 | 3.15 | 3.20 |
| E2 | 2.39 | 2.49 | 2.59 |
| e | 0.65BSC | | |
| H | 0.30 | 0.39 | 0.50 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | - | 0.13 | - |
| M | * | * | 0.15 |
| θ | | 10° | 12° |



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