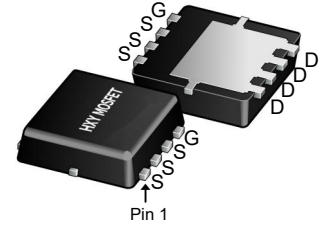




Description

The SISA96DN-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



DFN3X3-8L

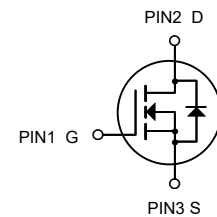
General Features

$V_{DS} = 30V$ $I_D = 50 A$

$R_{DS(ON)} < 10m\Omega$ @ $V_{GS}=10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SISA96DN-T1-GE3	DFN3X3-8L	HXY MOSFET	5000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	11	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	9	A
I_{DM}	Pulsed Drain Current ²	112	A
EAS	Single Pulse Avalanche Energy ³	24.2	mJ
I_{AS}	Avalanche Current	22	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	37.5	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2.42	W
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 175	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	$^\circ C/W$



Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.0193	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	---	7.5	10	mΩ
		V _{GS} =4.5V, I _D =15A	---	11	18	
V _{GS(th)}	Gate Threshold Voltage		1.2	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =250uA	---	-3.97	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	34	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.8	---	Ω
Q _g	Total Gate Charge (4.5V)		---	9.8	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	---	4.2	---	
Q _{gd}	Gate-Drain Charge		---	3.6	---	
T _{d(on)}	Turn-On Delay Time		---	4	---	ns
T _r	Rise Time	V _{DD} =15V, V _{GS} =10V, R _G =3.3	---	8	---	
T _{d(off)}	Turn-Off Delay Time	I _D =15A	---	31	---	
T _f	Fall Time		---	4	---	
C _{iss}	Input Capacitance		---	940	---	pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	131	---	
C _{rss}	Reverse Transfer Capacitance		---	109	---	
I _S	Continuous Source Current ^{1,5}		---	---	43	A
I _{SM}	Pulsed Source Current ^{2,5}	V _G =V _D =0V, Force Current	---	---	112	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	I _F =30A, di/dt=100A/μs, T _J =25°C	---	8.5	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.2	---	nC

Note :

- 1 .The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3 .The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=22A
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

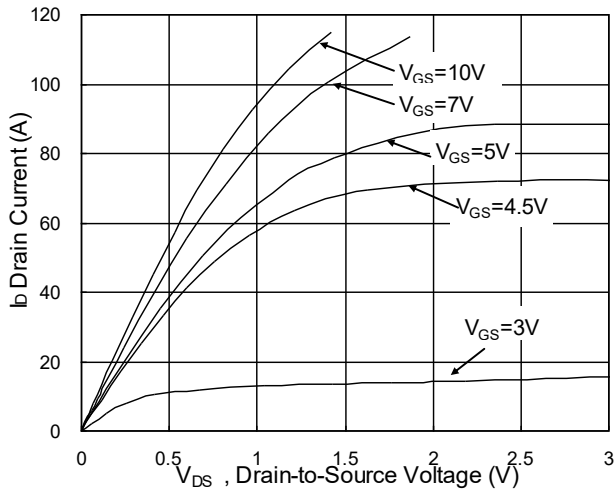


Fig.1 Typical Output Characteristics

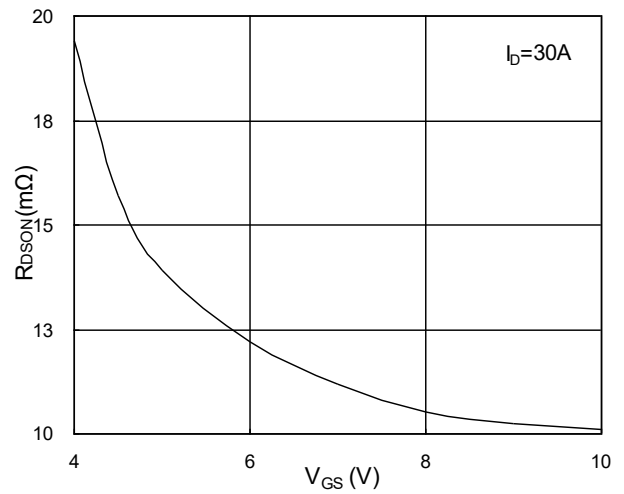


Fig.2 On-Resistance vs. G-S Voltage

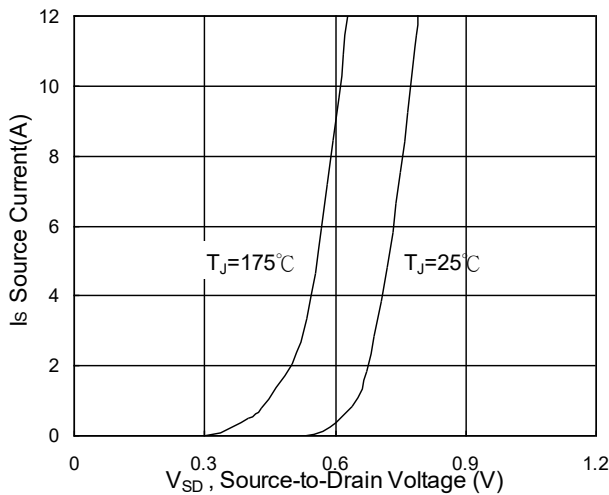


Fig.3 Forward Characteristics of Reverse

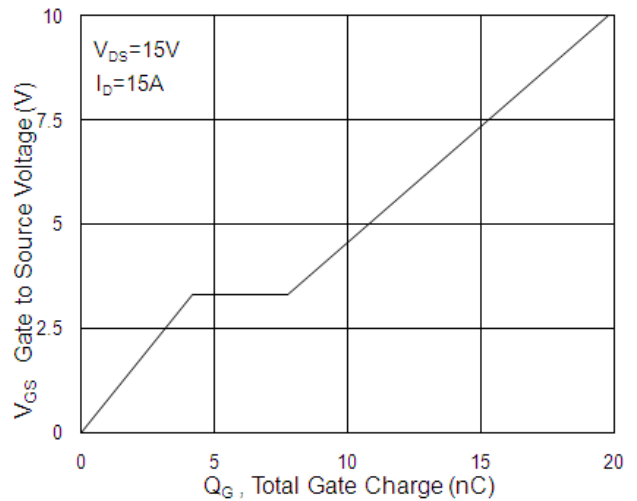


Fig.4 Gate-Charge Characteristics

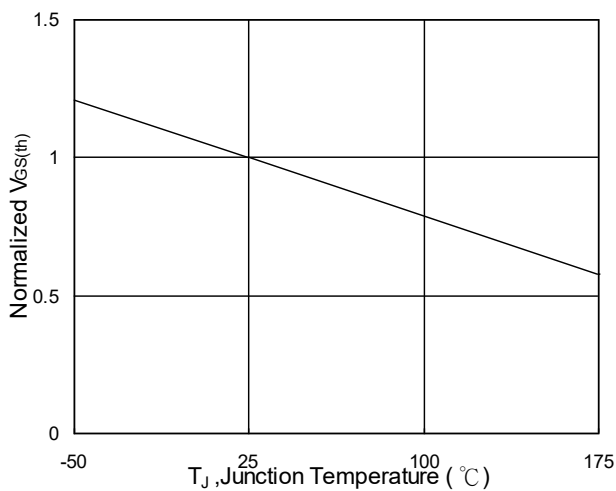


Fig.5 Normalized V_{GS(th)} vs. T_J

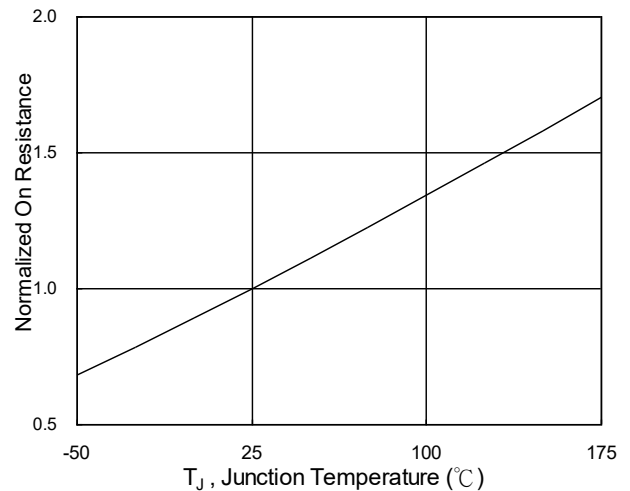


Fig.6 Normalized R_{DS(on)} vs. T_J

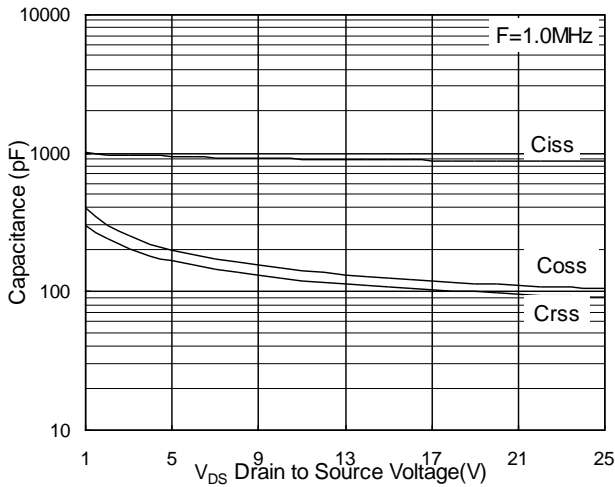


Fig.7 Capacitance

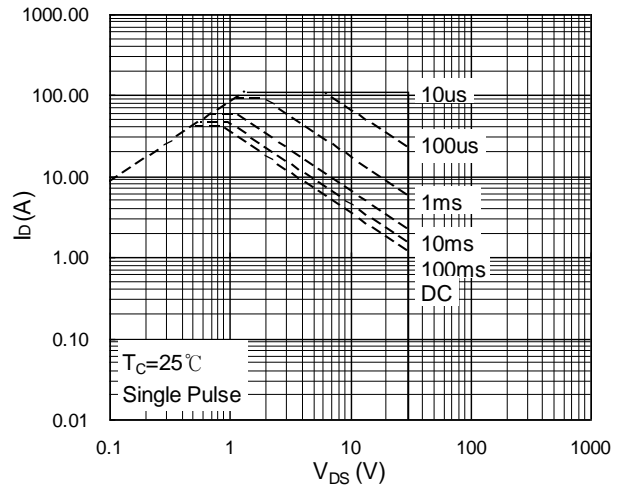


Fig.8 Safe Operating Area

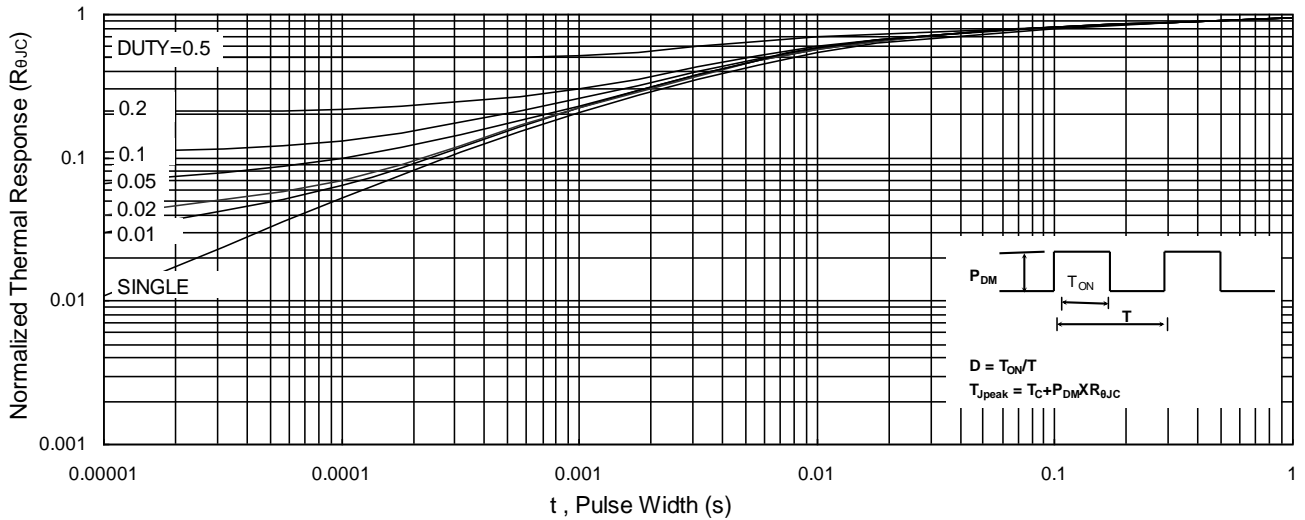


Fig.9 Normalized Maximum Transient Thermal Impedance

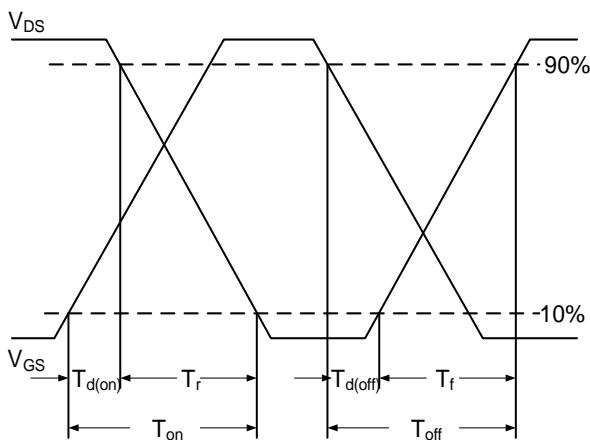


Fig.10 Switching Time Waveform

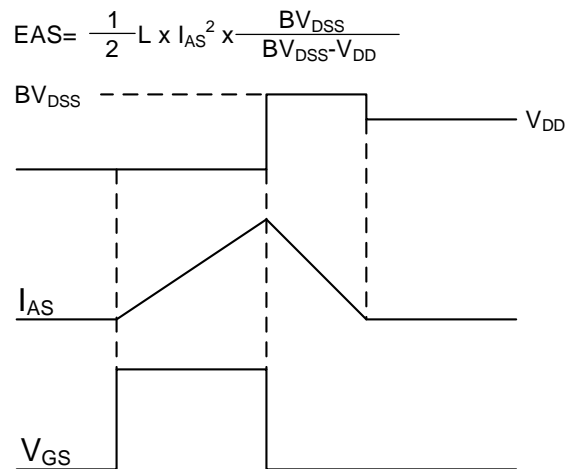
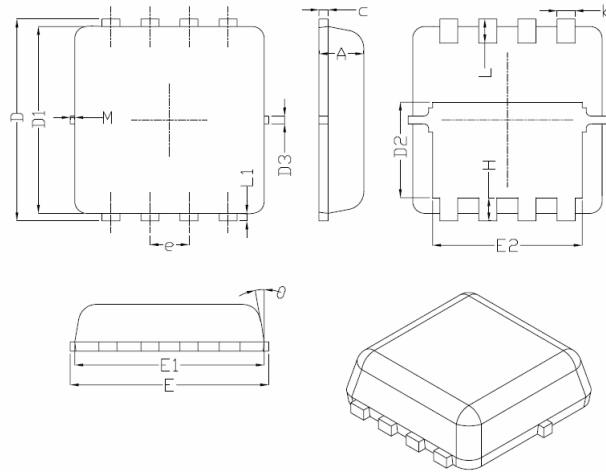


Fig.11 Unclamped Inductive Switching Waveform



DFN3X3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°



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