



### DESCRIPTION

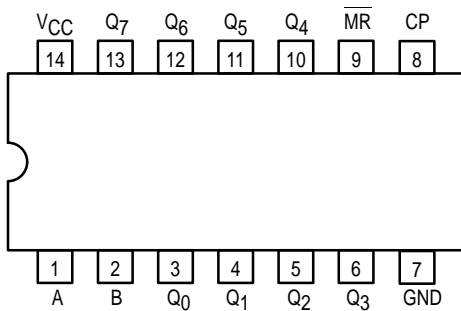
The SN74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock.

It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

### FEATURES

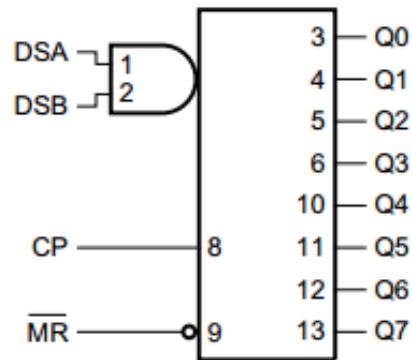
- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Fully Synchronous Data Transfers
- Gated Serial Data Input
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

### PIN ASSIGNMENT

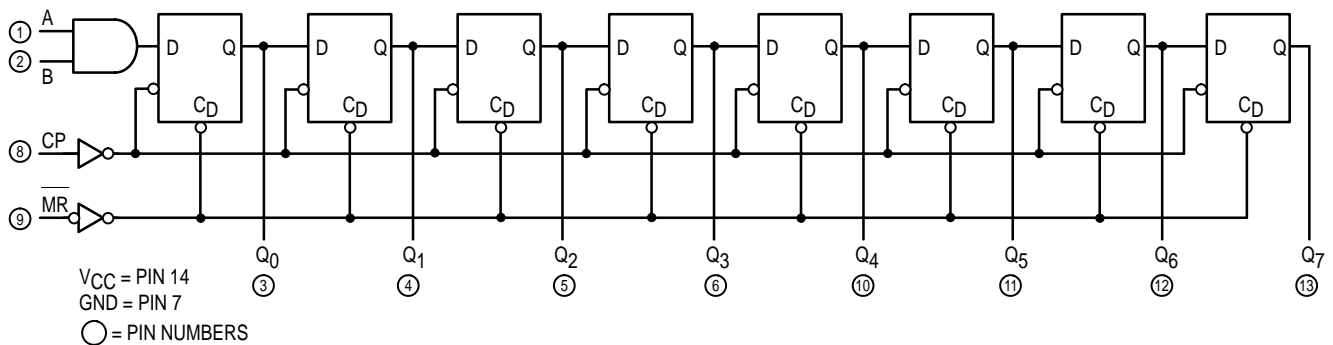


SOP/DIP-14

### LOGIC SYMBOL



### LOGIC DIAGRAM





## FUNCTIONAL DESCRIPTION

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{\text{MR}}$	DSA	DSB	Q0	Q1~Q7
Reset (Clear)	L	X	X	L	L~L
Shift	H	l	l	L	q0~q6
	H	l	h	L	q0~q6
	H	h	l	L	q0~q6
	H	h	h	H	q0~q6

L (l) = LOW Voltage Levels

H (h) = HIGH Voltage Levels

X = Don't Care

q<sub>n</sub> = Lower case letters indicate the state of the referenced input or output one

q<sub>n</sub> = set-up time prior to the LOW to HIGH clock transition.

## GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.75	V
Input Voltage	I <sub>OH</sub>			-0.4	mA
Storage Temperature	I <sub>OL</sub>			8	mA
Operating Ambient Temperature Range	T <sub>A</sub>	0		70	°C



**DC CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs			0.8	V
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}, I_{IN} = 48 \text{ mA}$		-0.65	-1.5	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	2.7		3.5	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = V_{CC} \text{ MIN},$ $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table		0.35	0.5	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7 \text{ V}$			20	$\mu\text{A}$
		$V_{CC} = \text{MAX}, V_{IN} = 7.0 \text{ V}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.4 \text{ V}$			-400	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{MAX}$	-20		-100	mA
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX}$			27	mA

**AC CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ )

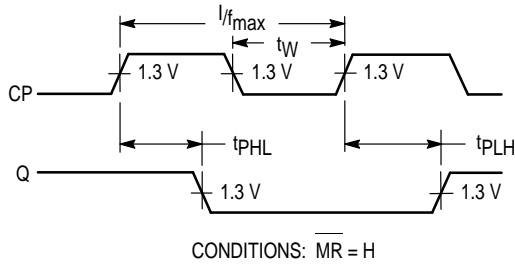
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 5.0 \text{ V}$ $CL = 15 \text{ pF}$	25	36		MHz
$t_{PHL}$	Propagation Delay MR to Output Q			24	36	ns
$t_{IK}$	Propagation Delay Clock to Output Q			17	27	ns
$t_{PHL}$				21	32	ns

**AC SETUP REQUIREMENTS** ( $T_A = 25^\circ\text{C}$ )

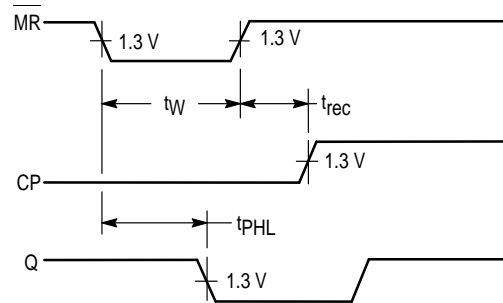
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_w$	CP, MR Pulse Width	$V_{CC} = 5.0 \text{ V}$	25	36		ns
$t_s$	Data Setup Time			24	36	ns
$t_h$	Data Hold Time			17	27	ns
$t_{rec}$	MR to Clock Recovery Time			21	32	ns



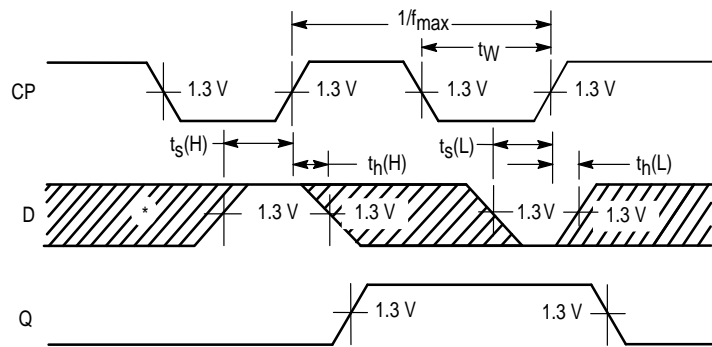
### AC WAVEFORMS



**Clock to Output Delays  
and Clock Pulse Width**



**Master Reset Pulse Width,  
Master Reset to Output Delay and  
Master Reset to Clock Recovery Time**



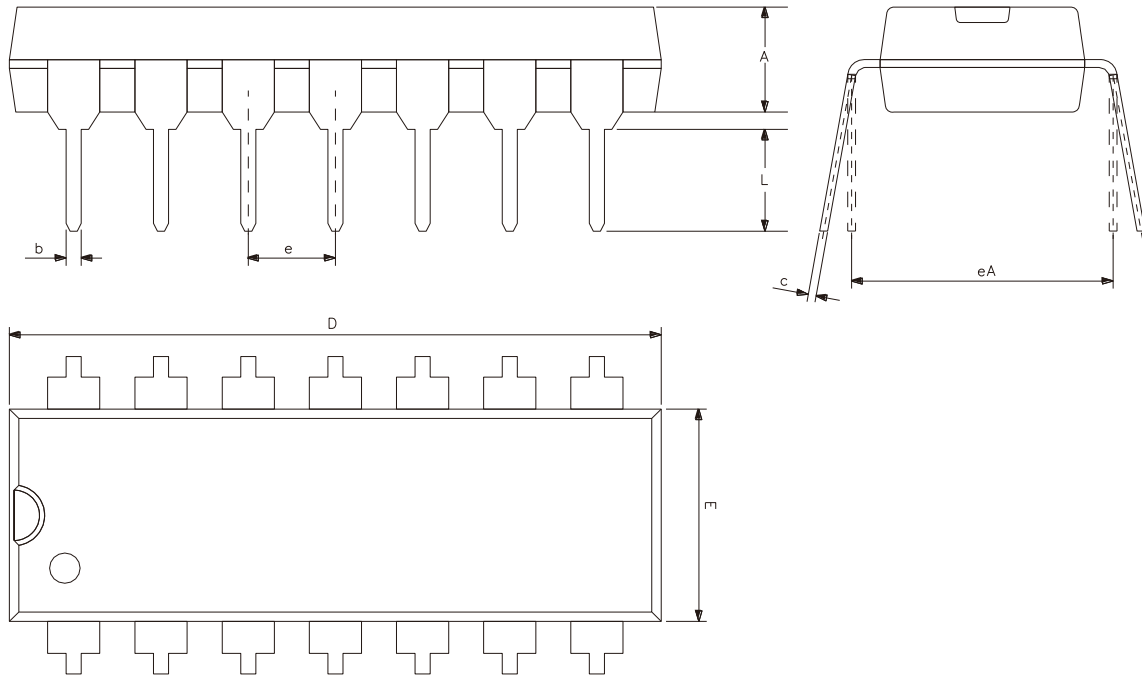
**Data Setup and Hold Times**

### ORDERING GUIDE

Model	Package Description	Qty(PCS)
SN74LS164DR	SOP-14	2500
SN74LS164N	DIP-14	25



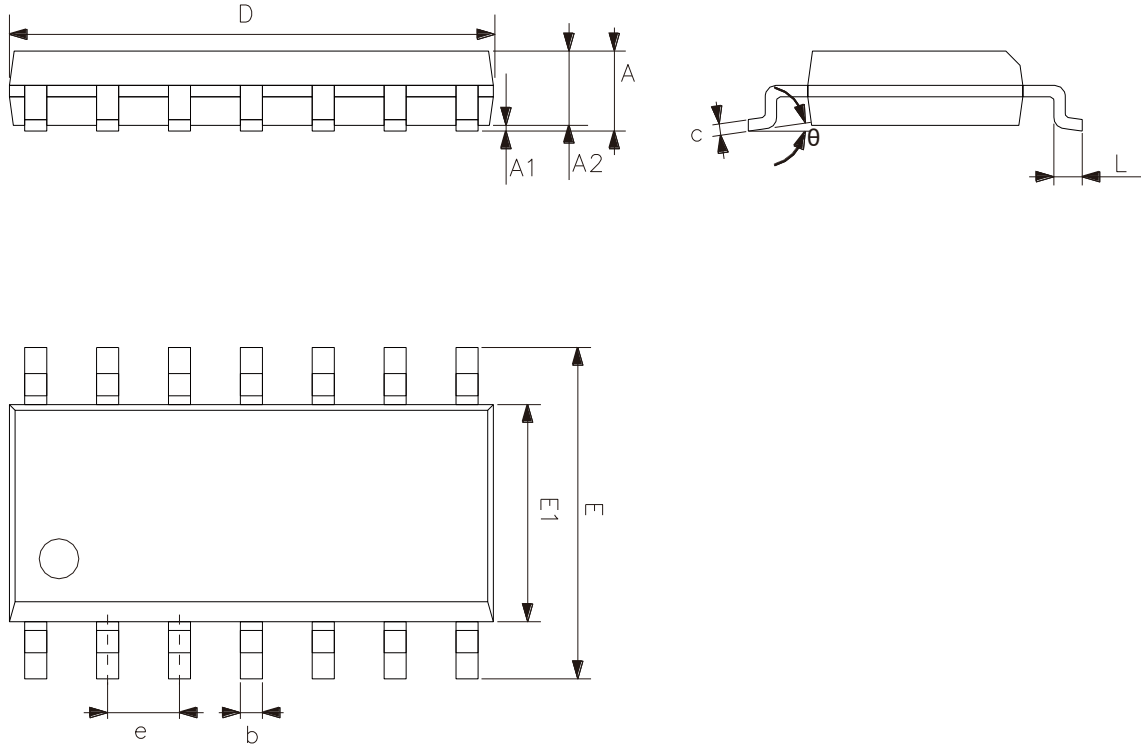
**PACKAGE OUTLINE DIMENSIONS**  
**DIP-14**



SYMBOL	COMMON DIMENSIONS (mm)	
	MIN	MAX
A	3.05	3.60
b	0.33	0.56
c	0.20	0.36
D	18.80	19.40
E	6.20	6.60
e	2.54	
eA	7.62	10.90
L	2.92	—



**PACKAGE OUTLINE DIMENSIONS**  
**SOP-14**



SYMBOL	COMMON DIMENSIONS (mm)	
	MIN	MAX
A	1.50	1.75
A1	0.05	0.25
A2	1.30	—
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°



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