

### **Description**

The ZXMN10A07F uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



**SOT-23** 

#### **General Features**

 $V_{DS}$  = 100V  $I_D$  =3 A

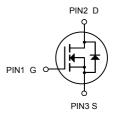
 $R_{DS(ON)}$  < 248m $\Omega$  @  $V_{GS}$ =10V

## **Application**

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

**Package Marking and Ordering Information** 

Product ID	Pack	Brand	Qty(PCS)
ZXMN10A07F	SOT-23	HXY MOSFET	3000

## Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Symbol Parameter		Units
VDS	Drain-Source Voltage	100	V
Vgs	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>A</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	3	А
I <sub>D</sub> @T <sub>A</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	1	
Ідм	Pulsed Drain Current <sup>2</sup>	5	А
PD@Ta=25°C	Total Power Dissipation <sup>3</sup>	1	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
R <sub>θ</sub> JA	Thermal Resistance Junction-ambient <sup>1</sup>	125	°C/W
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	80	°C/W



# Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
△BVbss/△TJ	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.067		V/°C
	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =1A		210	248	
RDS(ON)		V <sub>GS</sub> =4.5V , I <sub>D</sub> =0.5A		244	290	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient			-4.2		mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			1	uA
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C			5	uA
Igss	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20V$ , $V_{DS}$ = $0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =1A		2.4		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2.8	5.6	
Qg	Total Gate Charge (10V)			9.7	13.6	
Qgs	Gate-Source Charge	V <sub>DS</sub> =80V , V <sub>GS</sub> =10V , I <sub>D</sub> =1A		1.6	2.2	nC
$Q_{gd}$	Gate-Drain Charge			1.7	2.4	
Td(on)	Turn-On Delay Time			1.6	3.2	
Tr	Rise Time	V <sub>DD</sub> =50V , V <sub>GS</sub> =10V ,		19	34	
T <sub>d(off)</sub>	Turn-Off Delay Time	R <sub>G</sub> =3.3 I <sub>D</sub> =1A		13.6	27	ns
T <sub>f</sub>	Fall Time			19	38	
Ciss	Input Capacitance			508	711	
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		29	41	pF
Crss	Reverse Transfer Capacitance			16.4	23	
Is	Continuous Source Current <sup>1,4</sup>				1.2	Α
Іѕм	Pulsed Source Current <sup>2,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			5	Α
VsD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V
trr	Reverse Recovery Time	IE-10 41/4t-1000/		14		nS
Qrr	Reverse Recovery Charge	IF=1A , dI/dt=100A/μs , TJ=25°C		9.3		nC

#### Note:

<sup>1.</sup> The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

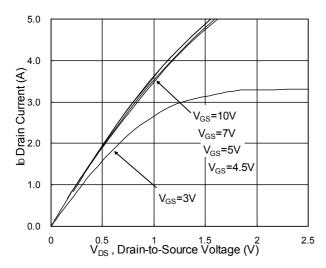
<sup>2.</sup>The data tested by pulsed , pulse width  $\leq 300 us$  , duty cycle  $\leq 2\%$ 

<sup>3.</sup> The power dissipation is limited by 150°C junction temperature

<sup>4 .</sup>The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



## **Typical Characteristics**



**Fig.1 Typical Output Characteristics** 

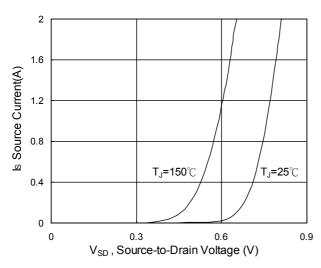


Fig.3 Forward Characteristics of Reverse

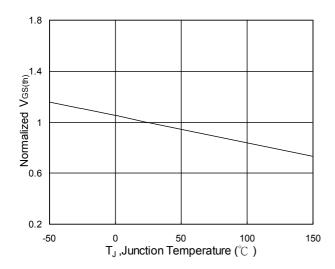


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$ 

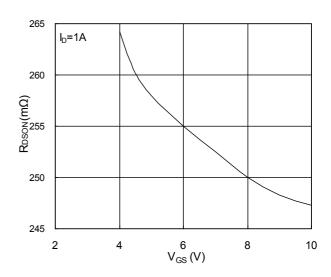


Fig.2 On-Resistance vs. Gate-Source

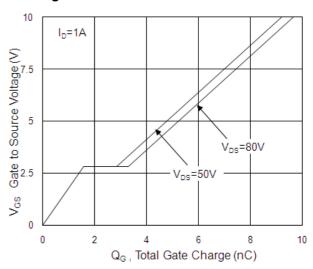


Fig.4 Gate-Charge Characteristics

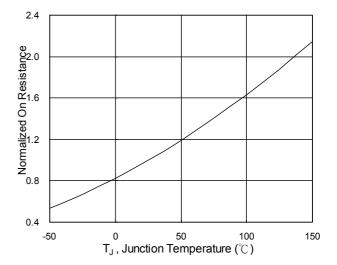
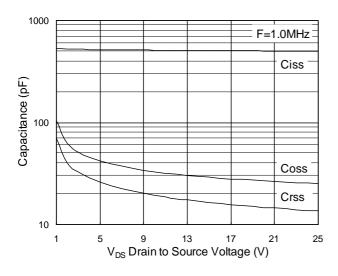


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>





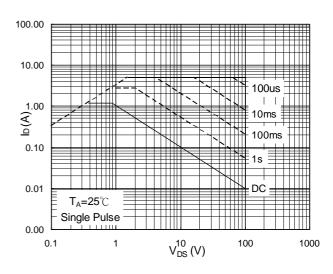


Fig.7 Capacitance

Fig.8 Safe Operating Area

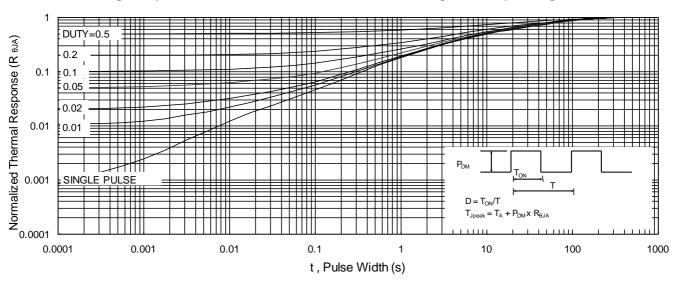
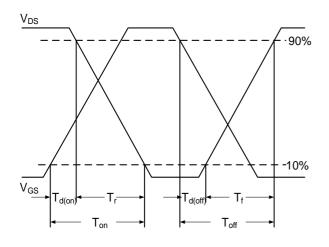


Fig.9 Normalized Maximum Transient Thermal Impedance



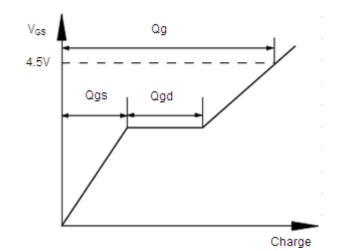
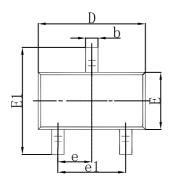


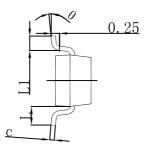
Fig.10 Switching Time Waveform

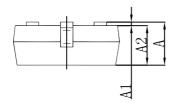
Fig.11 Gate Charge Waveform



# **SOT-23 Package Outline Dimensions**

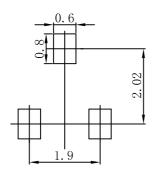






Symbol	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
Е	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550	REF	0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

# **SOT-23 Suggested Pad Layout**



- Note:
  1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
  3.The pad layout is for reference purposes only.

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STF5N65M6 IRF40H233XTMA1 STU5N65M6 DMN6022SSD-13 DMN13M9UCA6-7 DMTH10H4M6SPS-13 DMN2990UFB-7B
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