AiP16C22
Ram Mapping 44 SEG/4 COM LCD Controllers with 2-line Serial Interface

Product Specification

Specification Revision History：

Version	Date	Description
2021-04-A1	2021-04	New
2021-09-A2	2021-09	Update Ordering Information

1、General Description

AiP16C22 is a standard I^2C interface communication LCD controller/driver. The device provides one display mode: 1/4 duty display modes. The maximum display segments of the device are 176 patterns (44×4).

AiP16C22 has a built-in clock generator, LCD bias voltage generation module, LCD drive voltage follower and standard I^2C interface.

Features:

- Operating voltage: 2.4 to 5.5V
- I^2C interface
- Low power consumption
- Versatile blinking modes
- Read/Write address auto increment
- Internal 32kHz RC oscillator
- Bias: 1/2 or 1/3; duty: 1/4
- 16-step V_{LCD} voltage adjustable
- 44×4 bit display data register
- Internal LCD bias generator with voltage follower
- Two selectable LCD frame frequencies: 80Hz or 160Hz
- LCD drive voltage can be adjusted by external resistor
- Maximum display pattern 44×4：44 SEGs×4 COMs
- Packaging information: LQFP48/LQFP52

Ordering Information:

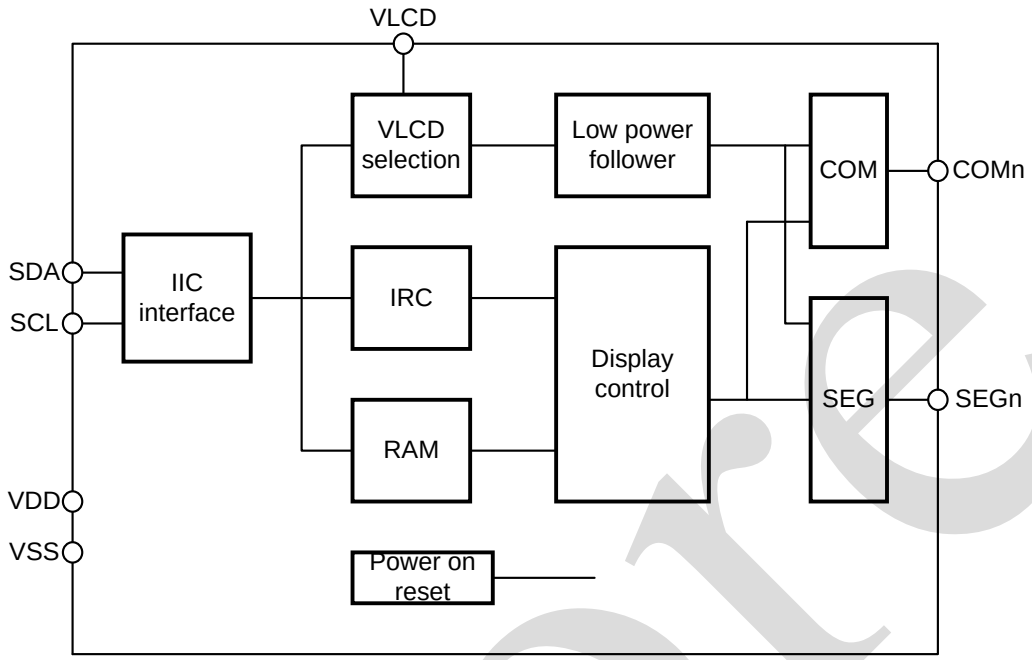
Tube packing specifications:

Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
AiP16C22LA.TB	LQFP48	AiP16C22	250 PCS/plate	10 plate/box	2500 PCS/box	6 box/pack	15000 PCS/pack	Dimensions of plastic enclosure: 7.0mm×7.0mm Pin spacing: 0.5mm
AiP16C22LD.TB	LQFP52	AiP16C22	90 PCS/plate	10 plate/box	900 PCS/box	6 box/pack	5400 PCS/pack	Dimensions of plastic enclosure: 14.0mm×14.0mm Pin spacing: 1.0mm

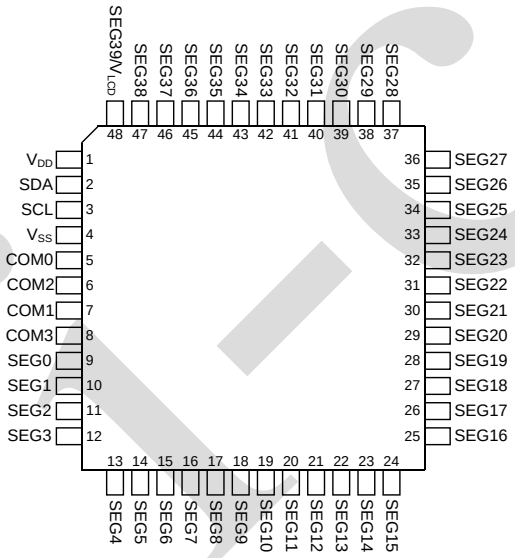
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

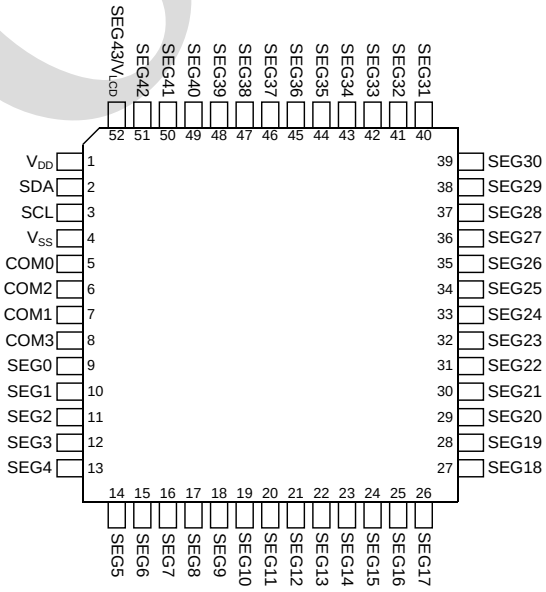
2.1、Block Diagram



2.2、Pin Configurations



LQFP48



LQFP52

2.3、Pin Description

Pin No.		Pin Name	Type	Description
LQFP48	LQFP52			
2	2	SDA	I/O	Serial data input/output for I^2C interface
3	3	SCL	I	Serial clock input for I^2C interface
1	1	V_{DD}	-	Positive power supply
4	4	V_{SS}	-	Negative power supply, ground
48	52	V_{LCD}	-	● One external resistor is connected between the V_{LCD} pin and the V_{DD} pin to determine the bias voltage for the V_{LCD} pin. Internal voltage adjustment function is disabled. ● Internal voltage adjustment function can be used to adjust the V_{LCD} voltage. If the V_{LCD} pin is used as voltage detection pin, an external power supply should not be applied to the V_{LCD} pin. ● An external MCU can detect the voltage of the V_{LCD} pin and program the internal voltage adjustment for the packages with a V_{LCD} pin.
6~8	6~8	COM0~COM3	O	LCD COM outputs
9~48	9~48	SEG0~SEG39	O	LCD SEG outputs
-	49~52	SEG40~SEG43	O	LCD SEG outputs

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Conditions	Value	Unit
supply voltage	-	-	V_{SS}-0.3 to V_{SS}+6.5	V
input voltage	V_{IN}	-	V_{SS}-0.3 to V_{DD}+0.3	V
operating temperature	T_{amb}	-	-40 to +85	℃
storage temperature	T_{stg}	-	-55 to +150	℃

3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(T_{amb}=-40 to +85℃, V_{DD}=2.4 to 5.5V, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
operating voltage	V_{DD}	-	-	2.4	-	5.5	V
operating voltage	V_{LCD}	-	-	-	-	V_{DD}	V
operating current	I_{DD}	3V	no load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display on, internal system oscillator on, DA0~DA3 are set to “0000”	-	18	27	uA
		5V		-	25	40	uA
operating current	I_{DD1}	3V	no load, V_{LCD}=V_{DD}, 1/3 bias, f_{LCD}=80Hz, LCD display off,	-	2	5	uA

		5V	internal system oscillator on, DA0~DA3 are set to “0000”	-	4	10	uA
standby curent	I_{STB}	3V	no load, $V_{LCD}=V_{DD}$, LCD display off, internal system oscillator off	-	-	1	uA
		5V		-	-	2	uA
HIGH level intput current	V_{IH}	-	SDA, SCL	$0.7V_{DD}$	-	V_{DD}	V
LOW level intput current	V_{IL}	-	SDA, SCL	0	-	$0.3V_{DD}$	V
input leakage curent	I_{IL}	-	$V_{IN}=V_{SS}$ or V_{DD}	-1	-	1	uA
LOW level output current	I_{OL}	3V	V_{OL}=0.4V, SDA	3	-	-	mA
		5V		6	-	-	mA
LCD COM sink current	I_{OL1}	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	-	uA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	-	uA
LCD COM source current	I_{OH1}	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	-	uA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	-	uA
LCD SEG sink current	I_{OL2}	3V	V_{LCD}=3V, V_{OL}=0.3V	250	400	-	uA
		5V	V_{LCD}=5V, V_{OL}=0.5V	500	800	-	uA
LCD SEG source current	I_{OH2}	3V	V_{LCD}=3V, V_{OH}=2.7V	-140	-230	-	uA
		5V	V_{LCD}=5V, V_{OH}=4.5V	-300	-500	-	uA

3.2.2、AC Characteristics 1

(T_{amb}=-40 to +85℃, V_{DD}=2.4 to 5.5V, V_{SS}=0V, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
LCD frame frequency	f_{LCD1}	4V	1/4 duty, T_{amb}=+25℃	72	80	88	Hz
LCD frame frequency	f_{LCD2}	4V	1/4 duty, T_{amb}=+25℃	52	80	124	Hz
LCD frame frequency	f_{LCD3}	4V	1/4 duty, T_{amb}=-40 to +85℃	144	160	176	Hz
LCD frame frequency	f_{LCD4}	4V	1/4 duty, T_{amb}=-40 to +85℃	104	160	248	Hz
V_{DD} off time	t_{OFF}	-	V_{DD} drop down to 0V	20	-	-	ms
V_{DD} slew rate	t_{SR}	-	-	0.05	-	-	V/ms

Note:

1. During the power on/off period, if the conditions of the power-on reset sequence are not met, the internal power-on reset (POR) circuit cannot work normally.

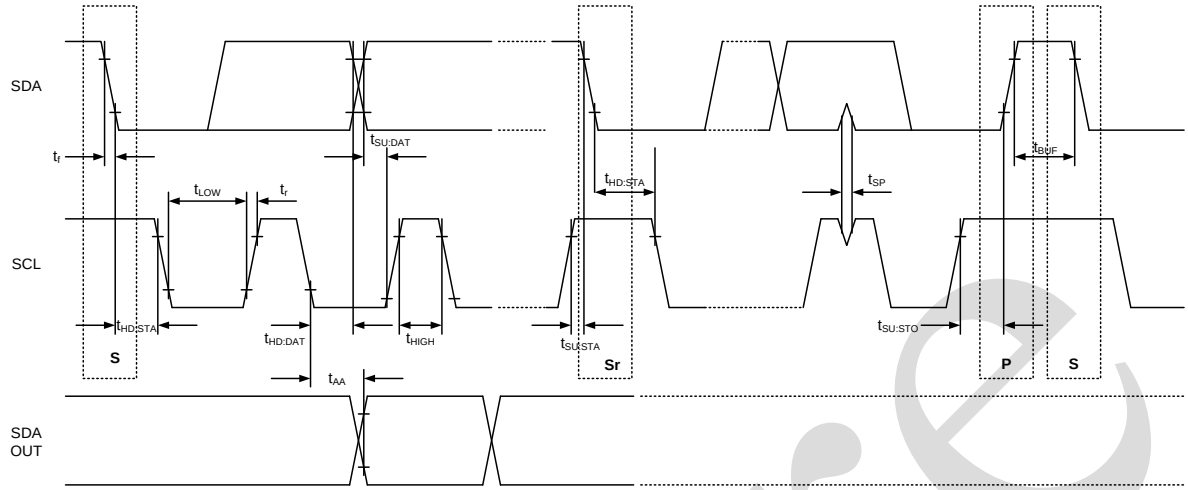
2. During operating, if the V_{DD} voltage drops below the specified minimum operating voltage, the power-on reset sequence conditions must be satisfied. In other words, the V_{DD} voltage must drop to 0V and must maintain a 0V voltage of at least 20ms before rising to the normal operating voltage.

3.2.3、AC Characteristics 2 (I^2C Interface)

Parameter	Symbol	Conditions	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
clock frequency	f_{SCL}	-	-	100	-	400	kHz
bus free time	t_{BUF}	during this period the bus must be free until a new transmission starts	4.7	-	1.3	-	us
Start condition hold time	$t_{HD: STA}$	after this period, the first clock pulse is generated	4.0	-	0.6	-	us
SCL LOW time	t_{LOW}	-	4.7	-	1.3	-	us
SCL HIGH time	t_{HIGH}	-	4.0	-	0.6	-	us
Start condition setup time	$t_{SU: STA}$	only relevant for repeated START condition	4.7	-	0.6	-	us
data hold time	$t_{HD: DAT}$	-	0	-	0	-	ns
data setup time	$t_{SU: DAT}$	-	250	-	100	-	ns
SDA and SCL rise time	t_R	-	-	1	-	0.3	us
SDA and SCL fall time	t_F	-	-	0.3	-	0.3	us
Stop condition setup time	$t_{SU: STO}$	-	4	-	0.6	-	us
effective clock output time	t_{AA}	-	-	3.5	-	0.9	us
input filter time constant (SDA, SCL)	t_{SP}	noise suppression time	-	100	-	50	ns

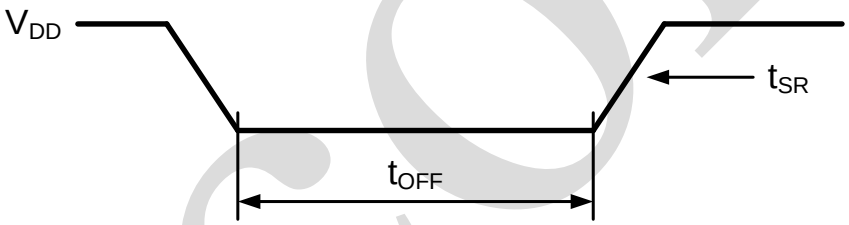
4、Timing Diagrams

4.1、I²C Timing



Note: The write cycle time t_{WR} is the time from a valid Stop condition of a write sequence to the end of the valid Start condition of a sequential command.

4.2、Power-on Reset Timing



5、Function Description

5.1、Power-on Reset

After power-on, the device is initialized by the internal power-on reset circuit. The state of the internal circuit after initialization is as follows:

- All COM/SEG outputs are set to V_{LCD}.
- The drive mode 1/4 duty output and 1/3 bias is selected.
- Both the system oscillator and LCD bias generator are off state.
- The LCD display is off sate.
- The internal voltage adjustment function is enabled.
- The detection switch function of the V_{LCD} pin is disabled.
- The frame frequency is set to 80Hz.
- The blinking function is switched off.

After power-on, Data transfers on the I²C bus within 1ms should be avoided to complete the reset action.

5.2、Display Memory—RAM Structure

AiP16C22 has a 44×4-bit static RAM for storing LCD display data. Write "1" to it to turn on the corresponding LCD, and write "0" to turn off the corresponding LCD.

The contents of the RAM data are directly mapped to the LCD. The 44 SEGs in the first column of RAM operate together with their corresponding COM0. In multiplexed LCD applications, SEGs in columns 2, 3, and 4 are time-multiplexed with their corresponding COM1, COM2, and COM3, respectively. The mapping relationship between RAM data and LCD pattern is as follows:

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG43					SEG42					21H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

Display data transfer format for I^2C interface

5.3、Address Pointer

Display RAM addressing technology is realized by address pointer. This mechanism allows single or multiple display data bytes to be loaded at any location in the display RAM. The address pointer sequence is initialized by the address pointer command.

5.4、System Oscillator

The internal oscillator provides timing for the internal logic and LCD drive signals. The system clock frequency (f_{SYS}) determines LCD frame frequency. During the system power-on initialization, the system oscillator will be in the stop state.

5.5、Frame Frequency

The AiP16C22 provides two frame frequencies, which can be selected by the mode setting command to be 80Hz or 160Hz.

5.6、Blinker Function

The device contains versatile blinking modes. The whole display can be blinked at frequencies selected by blink command. The ratio between the system frequency and the blinking frequency depends on the blinking mode, as shown in the following table:

Blinking Mode	Operating Mode Ratio	Blinking Frequency (Hz)
0	0	blink off
1	f_{SYS}/16384Hz	2
2	f_{sys}/32768Hz	1
3	f_{sys}/65536Hz	0.5

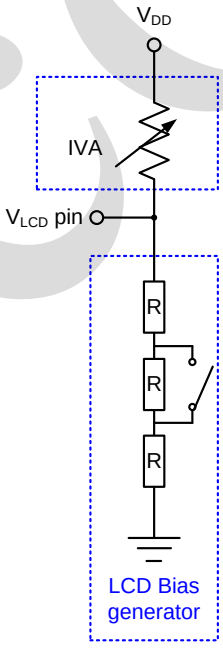
5.7、LCD Bias Generator

LCD full voltage (V_{OP}) comes from (V_{LCD}-V_{SS}). The LCD voltage can be externally compensated for temperature through the voltage provided by the V_{LCD} pin.

1/2 or 1/3 bias voltage can be obtained from an internal voltage divider of four series resistors connected between V_{LCD} and V_{SS}. The centre resistor can be switched out of circuits to provide a 1/4, 1/2 bias voltage .

5.8、Internal V_{LCD} Voltage Adjustment

- The internal V_{LCD} adjustment contains four series resistors and a 4-bit programmable analog switch which can provide 16-level voltage adjustment options using the V_{LCD} voltage adjustment command.
- The internal V_{LCD} adjustment as shown below:



5.9、SEG Drive Output

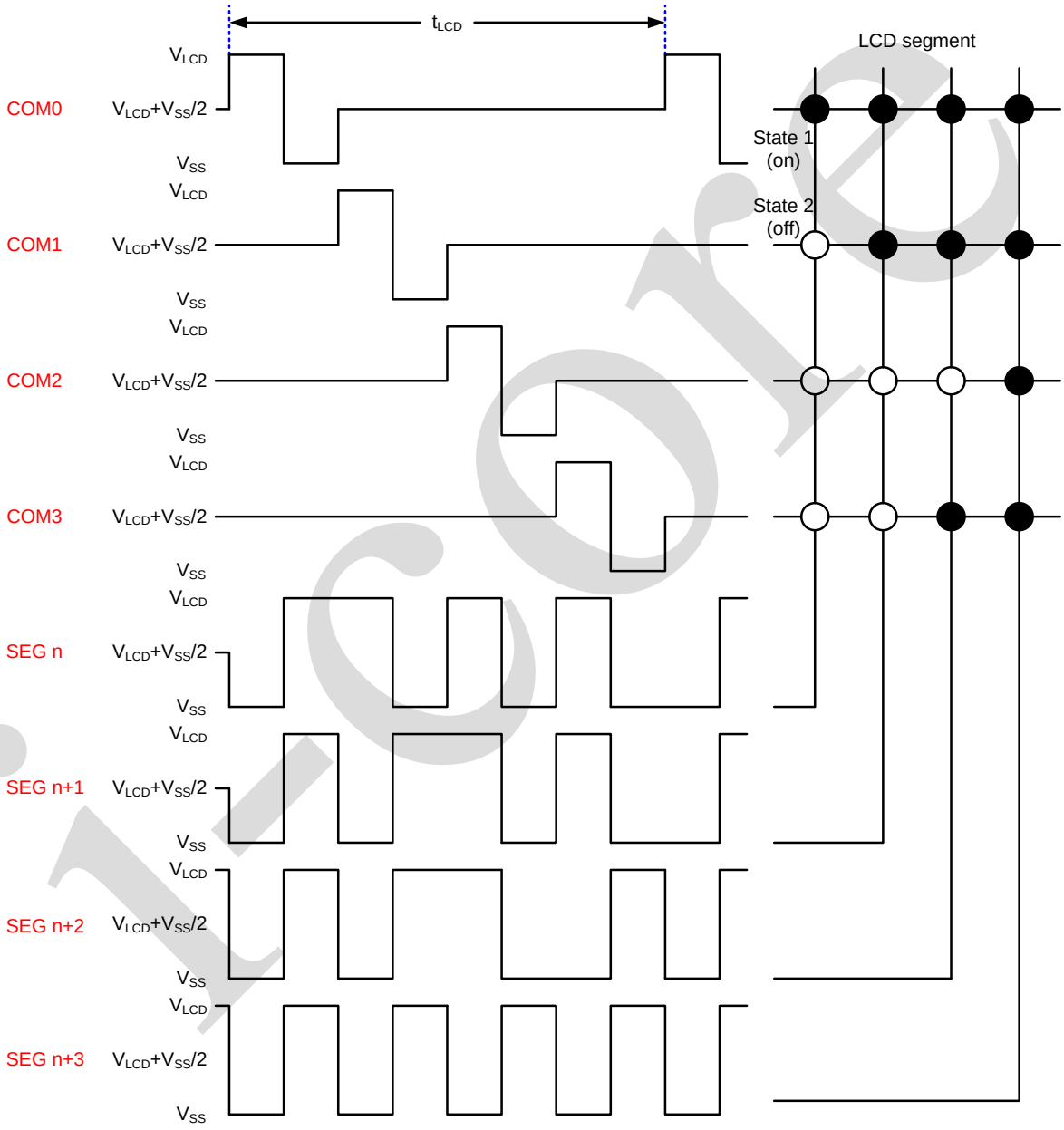
The LCD drive module contains 44 SEG outputs SEG0~SEG43, these SEGs should be directly connected to the LCD panel. The SEG output signals are generated according to the multiplexed COM signals and the data in the display latch. If the number of SEG used is less than 44, the unused SEG outputs should be left open-circuit.

5.10、COM Drive Output

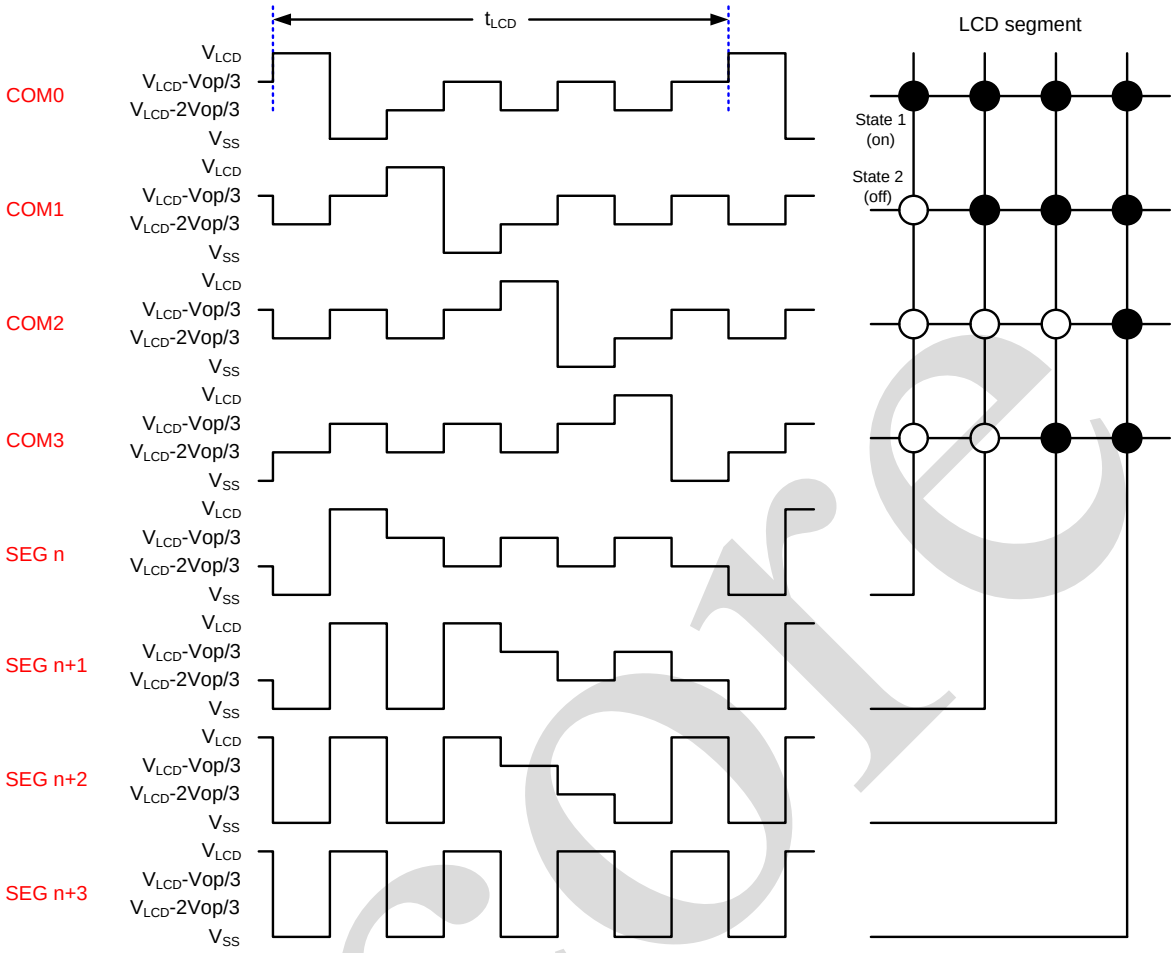
The LCD drive section contains 4 COM outputs (COM0~COM3). These COMs should be directly connected to the LCD panel. The COM output signals are generated according to the selected LCD drive mode. If the number of COMs used is less than 4, the unused COM output should be left open-circuit.

5.11、LCD Drive Mode Waveforms

● When the LCD drive mode selects 1/4 duty, AiP16C22 can select 1/2 or 1/3 bias, the waveform and LCD display is shown as follows:



1/4 duty and 1/2 bias drive mode waveform ($V_{OP}=V_{LCD}-V_{SS}$)



1/4 duty and 1/3 bias drive mode waveform ($V_{OP}=V_{LCD}-V_{SS}$)

● The relationship between the 4-bit programmable analog switch and V_{LCD} output voltage is shown in the following table:

Bias / DA3~DA0	1/2	1/3	Note
00H	1.000×V_{DD}	1.000×V_{DD}	default value
01H	0.9375×V_{DD}	0.957×V_{DD}	—
02H	0.882×V_{DD}	0.918×V_{DD}	—
03H	0.833×V_{DD}	0.882×V_{DD}	—
04H	0.789×V_{DD}	0.849×V_{DD}	—
05H	0.750×V_{DD}	0.818×V_{DD}	—
06H	0.714×V_{DD}	0.789×V_{DD}	—
07H	0.682×V_{DD}	0.763×V_{DD}	—
08H	0.652×V_{DD}	0.738×V_{DD}	—
09H	0.625×V_{DD}	0.714×V_{DD}	—
0AH	0.600×V_{DD}	0.692×V_{DD}	—
0BH	0.577×V_{DD}	0.672×V_{DD}	—
0CH	0.556×V_{DD}	0.652×V_{DD}	—

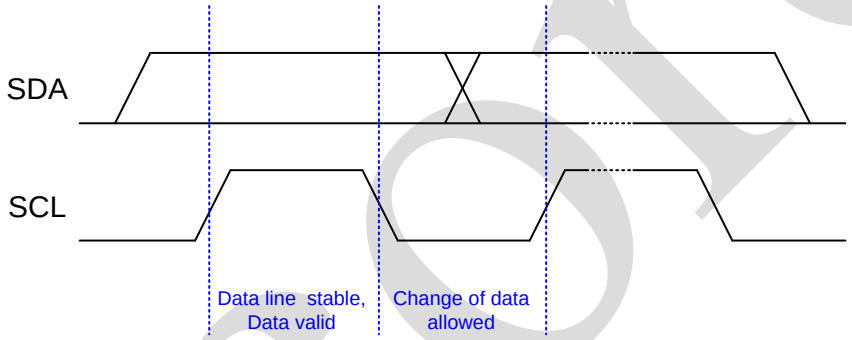
0DH	0.536×V_{DD}	0.634×V_{DD}	—
0EH	0.517×V_{DD}	0.616×V_{DD}	—
0FH	0.500×V_{DD}	0.600×V_{DD}	—

5.12、I²C Serial Interface

The device provides I²C serial interface, and the device is only used as a slave for I²C communication. The I²C interface is for bidirectional, two-line communication between different ICs or modules, that is, a serial data line SDA and a serial clock line SCL. These two lines are respectively connected to the positive power supply through a pull-up resistor with a typical value of 4.7KΩ. When the I²C bus is free, both lines are HIGH. The microcontroller connected to the I²C interface must have an open-drain or open-collector output to realize the wired-or function. Data transmission starts only when the I²C interface is not busy.

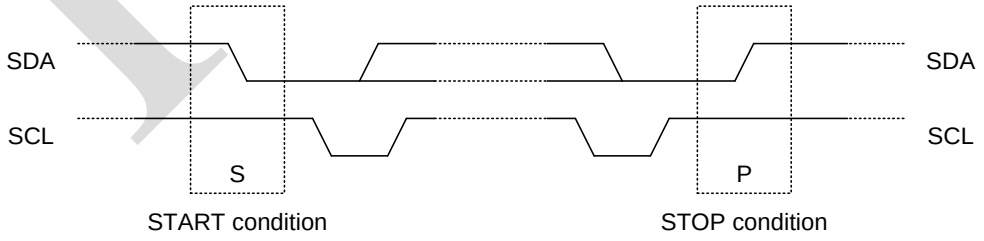
5.13、Data Validity

When SCL=1, the data on the SDA pin must be stable. Only when SCL=0, the level of the SDA pin will change, as shown in the diagram below:



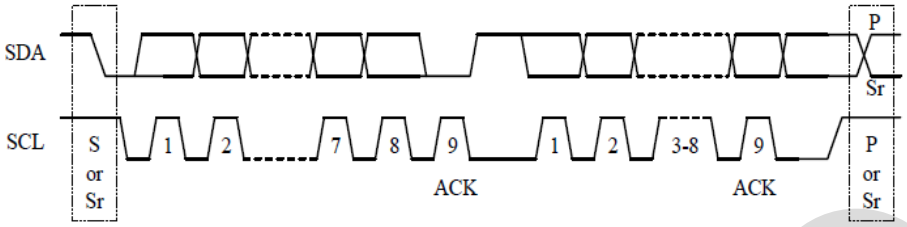
5.14、START And STOP Conditions

- When SCL=1, a high to low transition on the SDA line defines a START condition.
- When SCL=1, a low to high transition on the SDA line defines a STOP condition.
- START and STOP conditions are always generated by the master. The I²C interface is considered to be busy after the START condition. The I²C interface is considered to be free again a certain time after the STOP condition.
- The I²C interface stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START and repeated START (Sr) conditions are functionally identical.



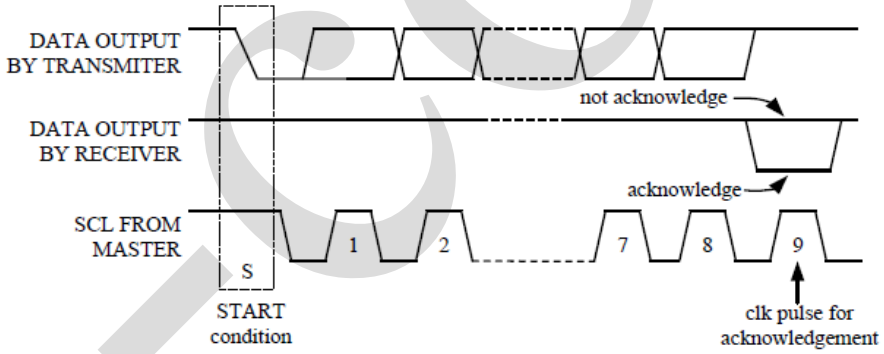
5.15、Byte Format

Every byte on the SDA line must be 8-bit long. The number of bytes that can be transmitted at a time is unlimited. Each byte has to be followed by an acknowledge bit. Data transmission starts from the highest bit.



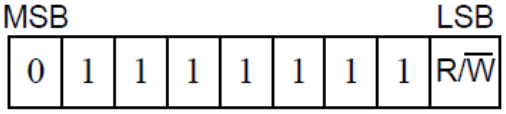
5.16、Acknowledge (ACK)

- Each bytes of eight bits is followed by one acknowledge bit. This acknowledge bit is a LOW level placed on the I^2C interface by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the receiving each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.
- A master receiver generates a not-acknowledge (NACK) when the slave sends the last byte and has told the slave to end data transmission. In this case, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



5.17、Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the $R/\overline{W}$ bit is "1", then a read operation is selected. When the $R/\overline{W}$ bit is "0", then a write operation is selected.
- AiP16C22 address bit is "0111111". When an address byte is sent, the device compares with its internal address. If they match, the device outputs an acknowledge on the SDA line.

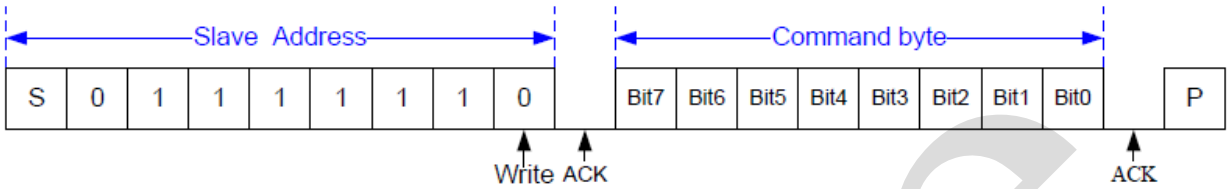


5.18、Write Operation

5.18.1、Byte Writes Operation

- **Command Byte**

A Command Byte write operation consists of a START condition, a slave address with an R/$\overline{W}$ bit, a valid register byte, a data byte and a STOP condition. After each of the three bytes, the device responds with an ACK.



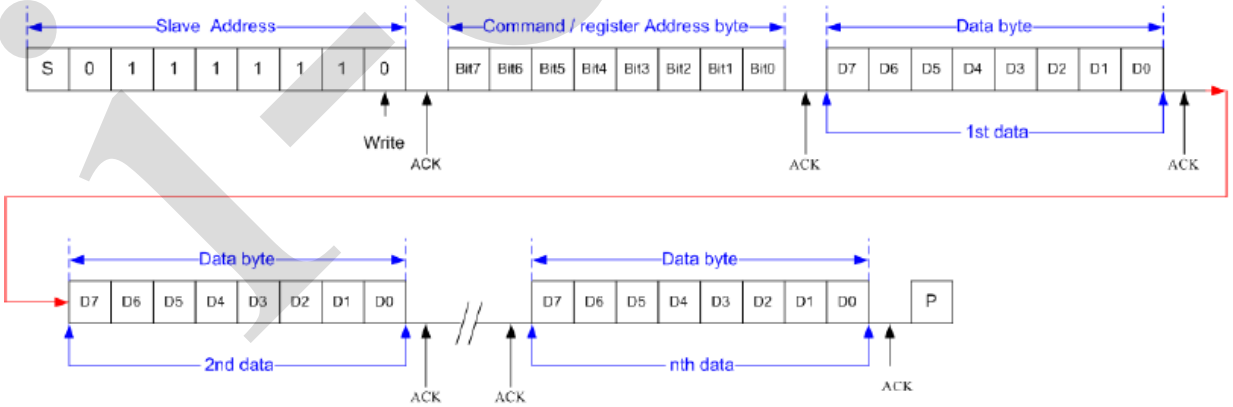
Command Byte Received

Single data Byte Received

Note: If the byte following the slave address is a command code, the byte following the command code will be ignored.

5.18.2、Display RAM Page Write Operation

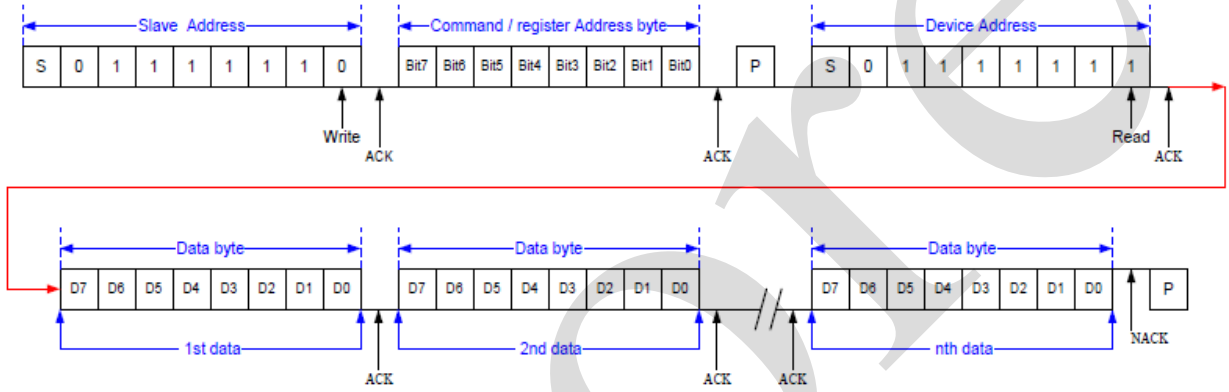
After a START condition the slave address with the R/$\overline{W}$ bit is sent to the I^2C interface followed with the Register Address of which the contents are written to the internal address pointer. The data to be written to the memory will be transmitted next and then the address pointer will be automatically incremented by 1, so it can write to the next address after receiving an acknowledge. After the internal address pointer reaches the maximum address, which is 15H, the address pointer will be reset to 00H.



N Data Bytes Received

5.19、Read Operation

- In this mode, the master reads the AiP16C22 data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit, a command byte and the register address byte which is written to the internal address pointer. After configuring the start address of the Read Operation, another START condition and the slave address are transferred on the I^2C interface followed by the R/$\overline{W}$ bit ("1"). Then the MSB of the data which was addressed is transmitted first on the I^2C interface. The address pointer is incremented by 1 after the receiving an acknowledge. That means that if the device sends the data at the address of A_{N+1}, the master will read and acknowledge the transferred new data byte and the address pointer is incremented to A_{N+2}. After the internal address pointer reaches the maximum address, which is 15H, the address pointer will be reset to 00H.
- The cycle of reading consecutive addresses will continue until the master sends a STOP condition.



Reading N Data Bytes

5.20、Command Summary

- **Drive Mode Command**

These commands are set to the frame frequency output, internal system oscillator on/off and display on/off and driver mode.

Function	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note
mode set	1	0	0	F	S	E	**0**	M0	reset value: 0x00
description	1	0	0	0	-	-	0	-	frame frequency: 80Hz
				1					frame frequency: 160Hz
				-	0	0		-	internal system oscillator off, LCD display off
					0	1			internal system oscillator off, LCD display off
					1	0			internal system oscillator on, LCD display off
					1	1			internal system oscillator on, LCD display on
				-	-	-		0	1/3 bias
								1	1/2 bias

- **Display Data Input Command**

This command is used to send data from MCU to memory map of the AiP16C22.

Function	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note
address pointer	0	0	0	A4	A3	A2	A1	A0	reset value: 0x00 display data start address of memory map

Note:
- Power on status: The address is set to 00H.
- If the address pointer reaches 15H, the pointer will reset to 00H.
- If the command is not defined, the function will not be affected.

- **Blinking Frequency Command**

This command defines the blinking frequency of the display modes.

Function	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note
blinking frequency command	1	1	0	0	0	0	BK1	BK0	reset value: 0xC0
description	1	1	0	0	0	0	0	0	blinking off
							0	1	blinking on, 2Hz
							1	0	blinking on, 1Hz
							1	1	blinking on, 0.5Hz

Internal Voltage Adjustment (IVA) Setting Command

The internal voltage (V_{LCD}) can provide sixteen kinds of regulator voltage adjustment options by setting the LCD operating voltage adjustment command.

Function	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Note
internal voltage adjust setting	0	1	DE	VE	DA3	DA2	DA1	DA0	reset value: 0x70
description	0	1	DE	-	-	-	-	-	select SEG/V_{LCD} shared pin function
			-	VE	-	-	-	-	enable or disable the internal voltage adjustment
			-	-	DA3	DA2	DA1	DA0	adjust the V_{LCD} output voltage.

Note:

Bit 5 DE	Bit 4 VE	SEG/V_{LCD} Shared Pin Select	Internal Voltage Adjustment	Note
0	0	V_{LCD} pin	off	● SEG/V_{LCD} pin is set as the V_{LCD} pin. ● The LCD drive voltage is input from the external to the V_{LCD} pin. ● Disable the internal voltage adjustment function ● If an external resistor is connected between the V_{LCD} pin and the V_{DD} pin, the resistor can be used to adjust the bias voltage, and the A3~A0 bits must be set as the value other than "0000". ● If the V_{LCD} pin is connected to V_{DD} pin, the DA3~DA0 bits must be set as "0000".
0	1	V_{LCD} pin	on	● SEG/V_{LCD} pin is set as the V_{LCD} pin. ● The LCD drive voltage is independently generated internally. ● Enable the internal voltage adjustment function. ● The V_{LCD} pin is an output pin of which the voltage can be detected by the external MCU host.
1	0	SEG pin	off	● SEG/V_{LCD} pin is set as the SEG pin. ● Disable the internal voltage adjustment function. ● The bias voltage is supplied by the internal V_{DD}. ● DA3~DA0 can be any value.
1	1	SEG pin	on	● SEG/V_{LCD} pin is set as the SEG pin. ● The LCD drive voltage is independently generated internally. ● Enable the internal voltage adjustment function.

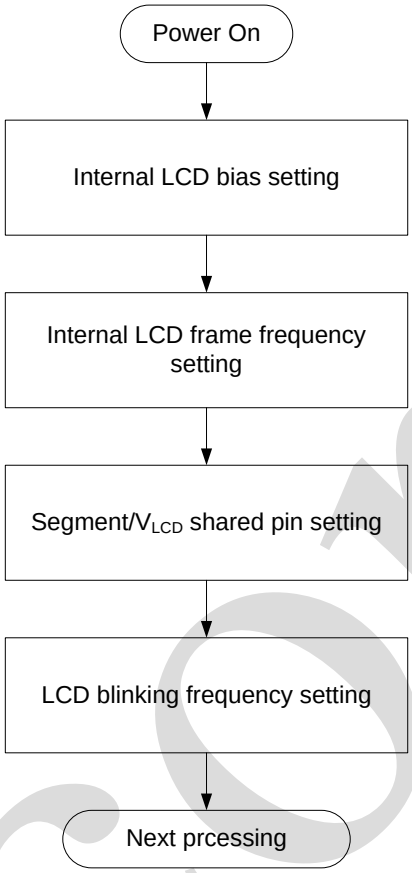
● When the DA0~DA3 bits are set to "0000", the internal voltage-follower (OP3) is disabled. When the DA0~DA3 bits are set to other values except "0000", the internal voltage follower (OP3) is enabled.

● Power on status: Disable the internal voltage adjustment and the SEG/V_{LCD} pin is set as the SEG pin.

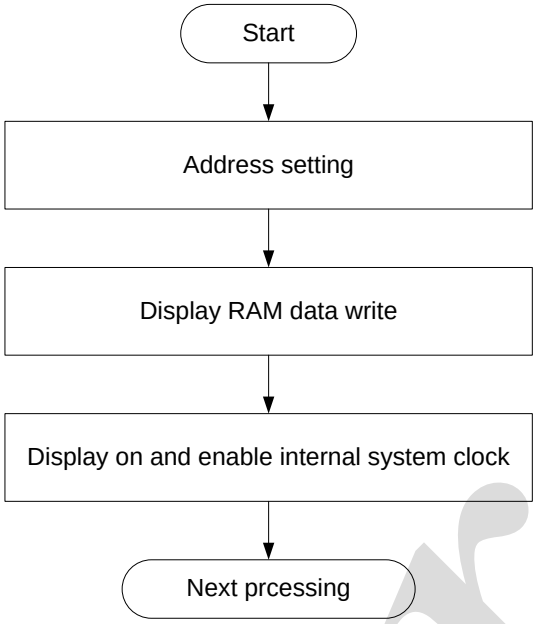
5.21、Operation Flow Chart

The flow charts of the access procedures are shown below.

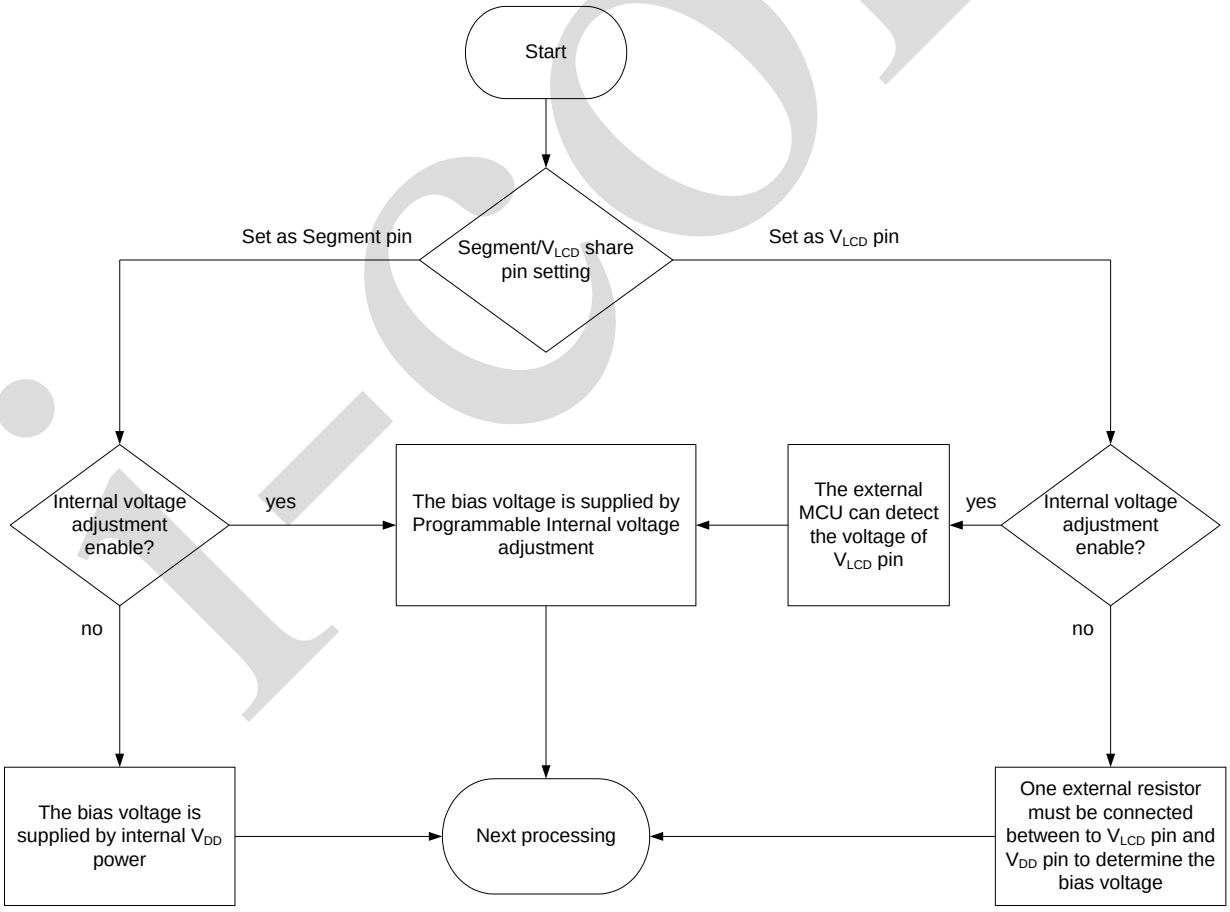
- **Initialization**



- **Display Data Read/Write (Address Setting)**



- **SEG/V_{LCD} Shared Pin And Internal Voltage Adjustment Setting**



5.21、Power Supply Sequence

● If the LCD and V_{DD} pin are powered separately, it is strongly recommended to follow the power supply sequence requirements.

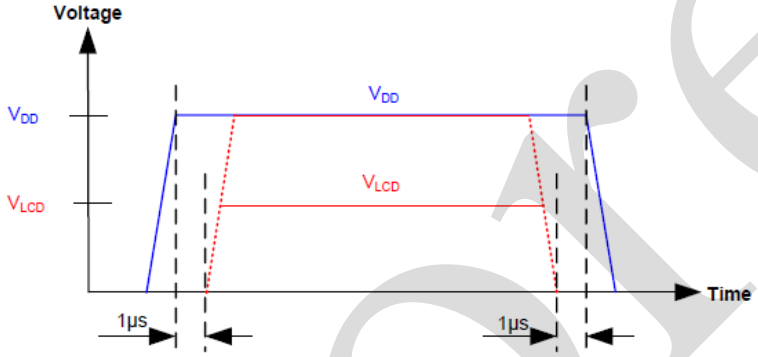
● Failure to follow the requirements of the power supply sequence may cause malfunctions.

Power supply sequence requirements:

1. Power-on sequence: First turn on the logic power supply voltage V_{DD}, then turn on the LCD drive voltage V_{LCD}.

2. Power-off sequence: First turn off the LCD drive voltage V_{LCD}, then turn off the logic power supply voltage V_{DD}.

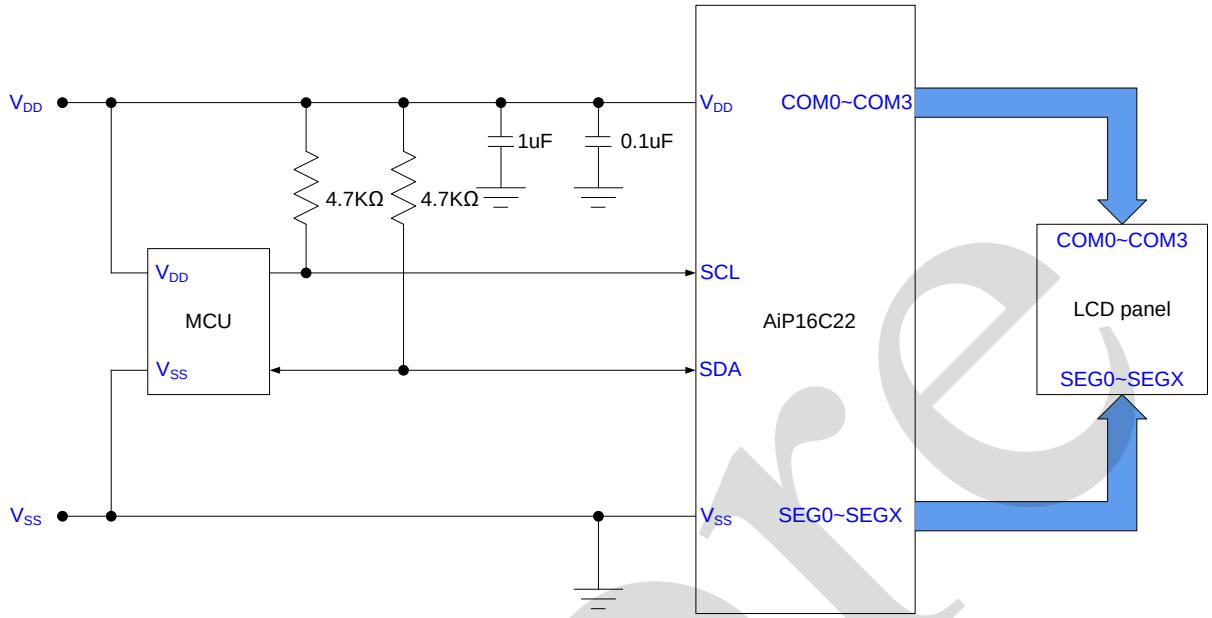
3. Regardless of whether the V_{LCD} voltage is higher than the V_{DD} voltage, the power supply sequence must be followed.



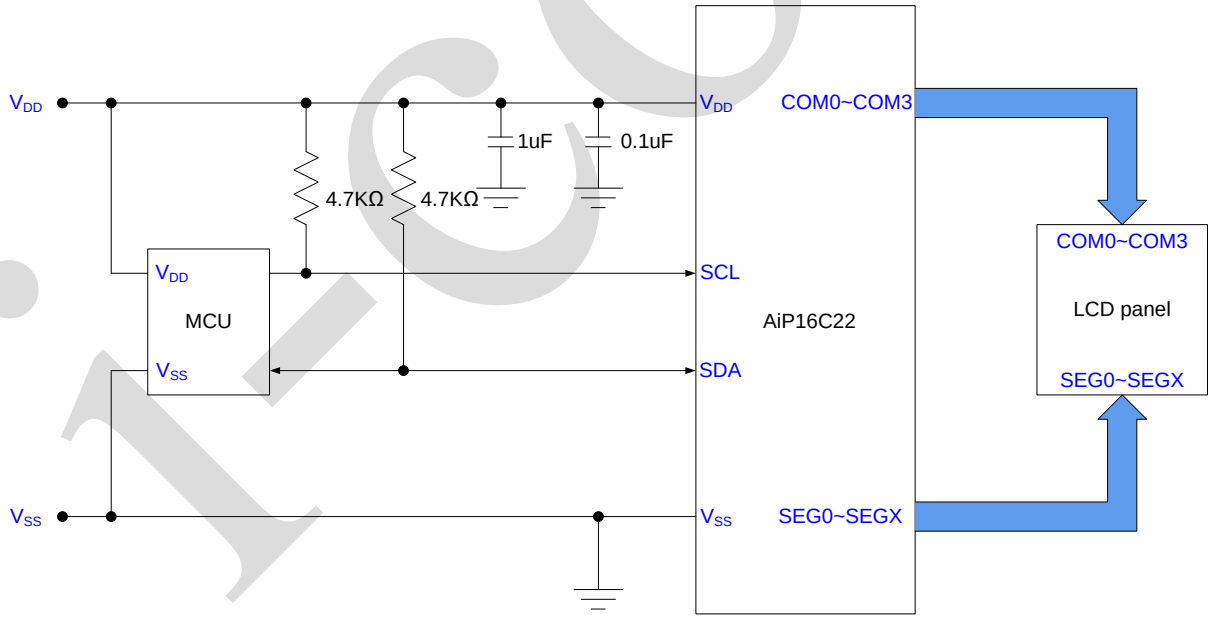
6、Typical Application Circuit And Application Note

6.1、Set As SEG Pin

Disable internal voltage adjustment. The bias voltage is supplied by internal V_{DD} power.

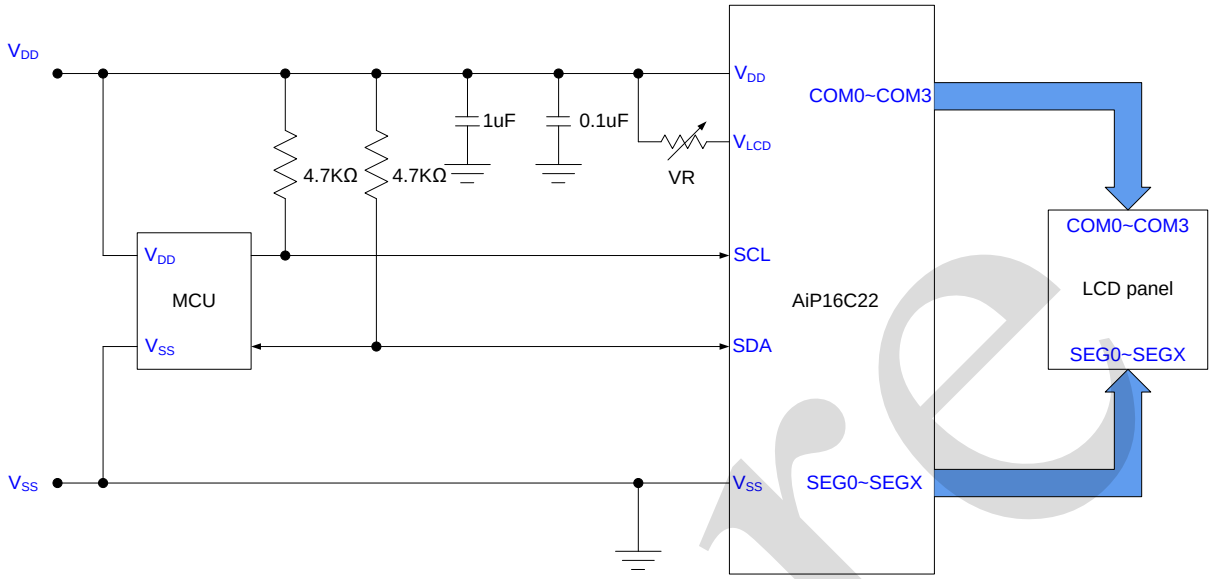


Enable internal voltage adjustment. The bias voltage is supplied by internal adjustment.

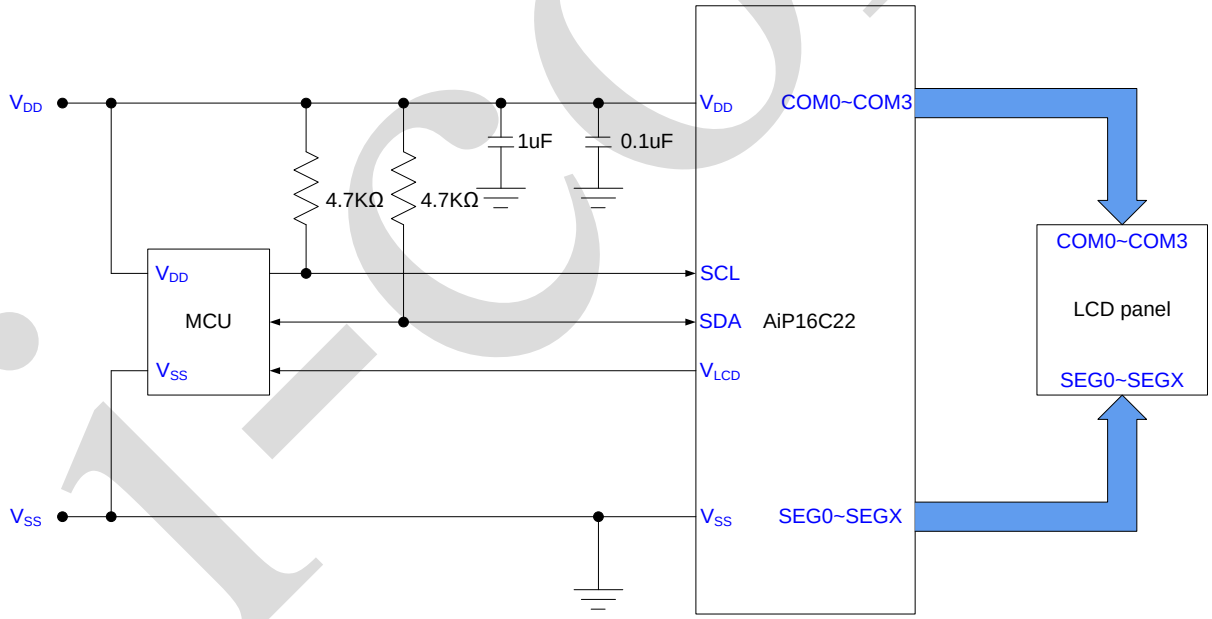


6.2、Set As V_{LCD} Pin

Disable internal voltage adjustment. One external resistor must be connected between V_{LCD} pin and V_{DD} pin to determine the bias voltage

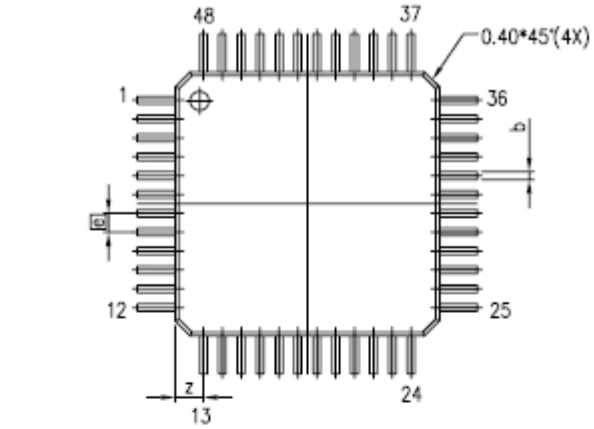


Enable internal voltage adjustment. The external MCU can detect the voltage of V_{LCD} pin.

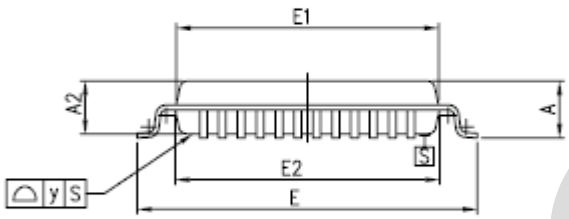


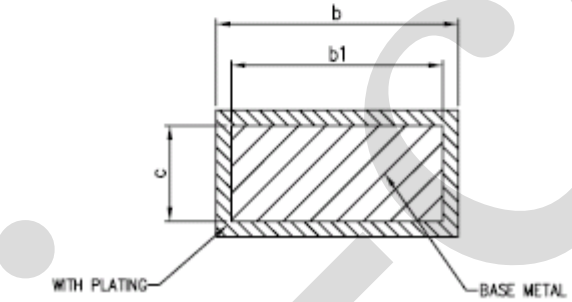
7、Package Information

7.1、LQFP48

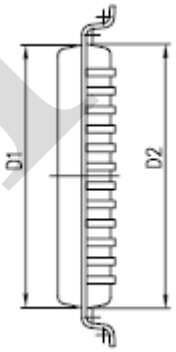


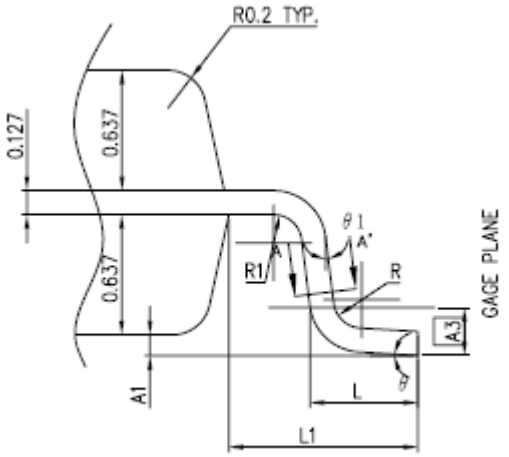
Symbol	Min	Nom	Max
A	----	----	1.63
A1	0.01	----	0.21
A2	1.30	1.40	1.50
A3	----	0.254	----
b	0.18	0.23	0.28
b1	0.15	0.20	0.25
c	----	0.127	----
D1	6.85	6.95	7.05
D2	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.85	6.95	7.05
E2	6.90	7.00	7.10
e	----	0.50	----
L	0.43	----	0.71
L1	0.90	1.00	1.10
R	0.1	----	0.25
R1	0.1	----	----
θ	0	----	10°
θ1	0	----	----
y	----	----	0.1
Z	----	0.75	----





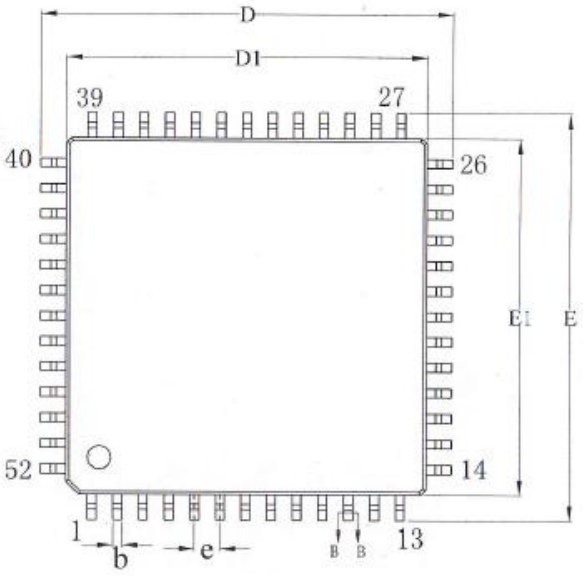
SECTION A–A'



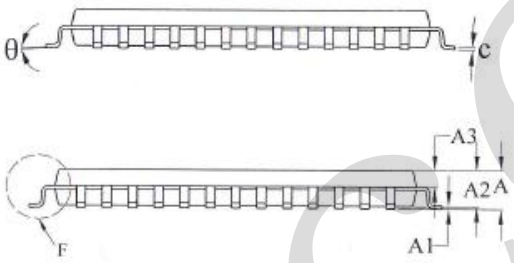


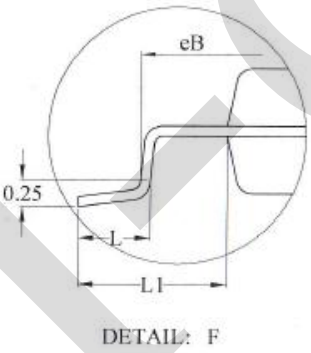
DETAIL A

7.2、LQFP52

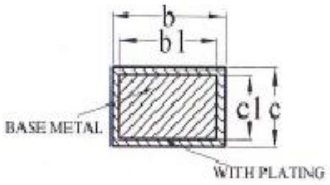


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.38	—	0.46
b1	0.37	0.40	0.43
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	1.00BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°





DETAIL: F



SECTION B-B

8、Statements And Notes

8.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

8.2、Notion

Recommended carefully reading this information before the use of this product；

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