AiP74ALVC164245
16-bit Dual Supply Translating Transceiver; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-02-A1	2020-02	New
2021-12-A2	2021-12	Modify Ordering Information
2022-02-A3	2022-02	Modify ambient temperature to -40℃~+105℃ and add electrical characteristics of -40℃~+105℃
2022-11-A4	2022-11	Modify soldering temperature; modify ordering information

1、General Description

The AiP74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device,superior to most advanced CMOS compatible TTL families.

The AiP74ALVC164245 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3V and 5V bus in a mixed 3V and 5V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow.nDIR (active HIGH) enables data from nAn ports to nBn ports. nDIR (active LOW) enables data from nBn ports to nAn ports.

The output enable inputs ($1\overline{OE}$ and $2\overline{OE}$), when HIGH, disable both nAn and nBn ports by placing them in a high-impedance OFF-state. Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$.

In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non-zero supply towards the zero supply. The nAn-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7V). $V_{CC(B)} \geq V_{CC(A)}$ (except in suspend mode).

Features:

- 5V tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range:
  3V port ($V_{CC(A)}$):1.5V to 3.6V
  5V port ($V_{CC(B)}$):1.2V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs voltage range from 2.7V to 5.5V
- Inputs accept voltages up to 5.5V
- High-impedance outputs when $V_{CC(A)}$ or $V_{CC(B)}$=0V
- Specified from -40℃ to +105℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74ALVC164245 TA48.TB	TSSOP48	74ALVC164245	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74ALVC164245 TA48.TR	TSSOP48	74ALVC164245	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing:0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

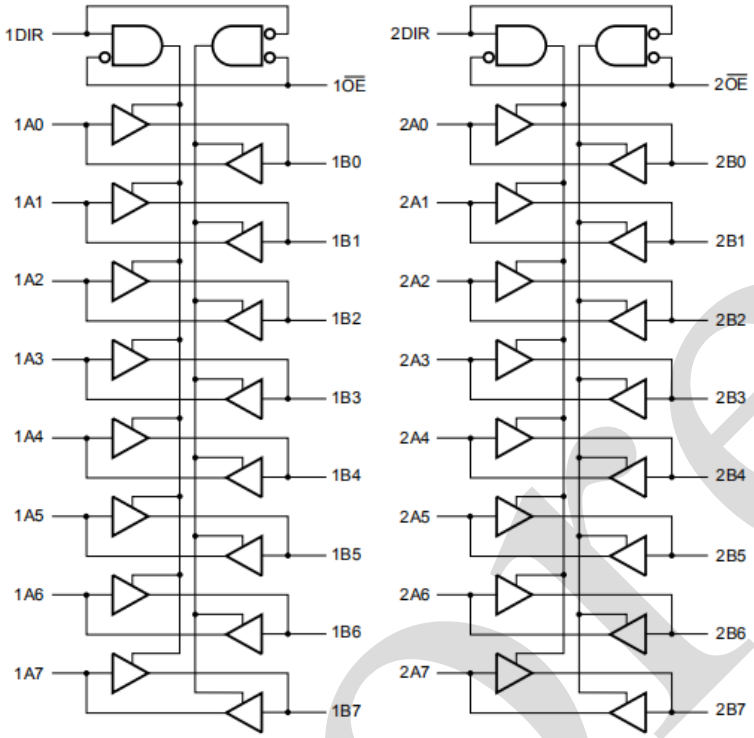


Figure 1. Logic symbol

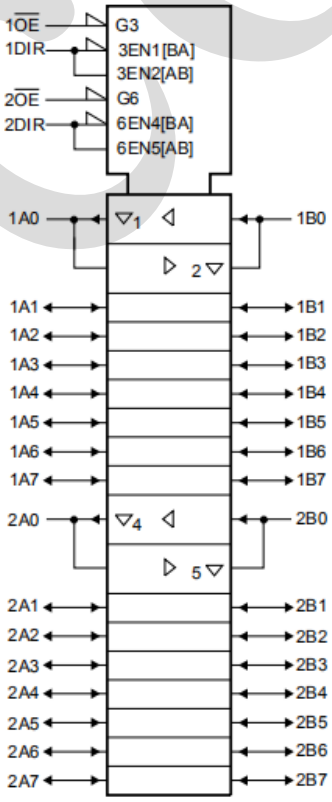
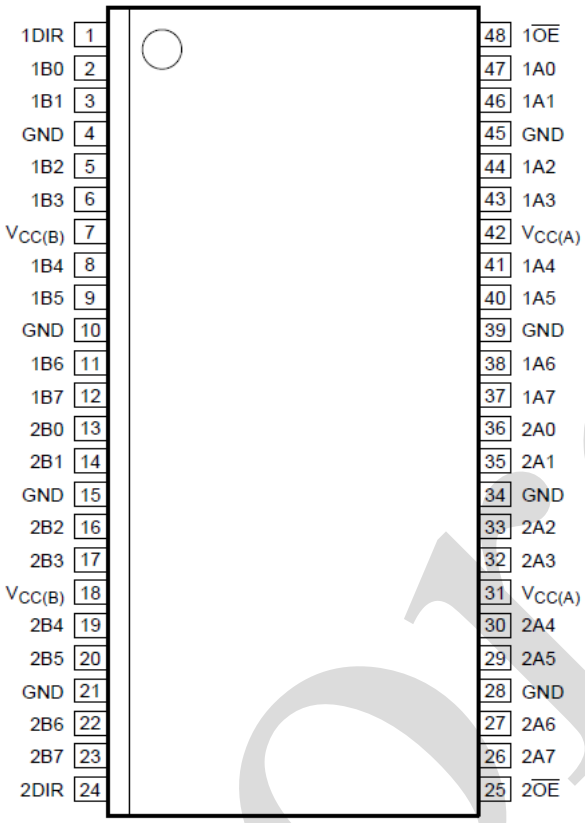


Figure 2. IEC logic symbol

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1,24	1DIR,2DIR	direction control inputs
2,3,5,6,8,9,11,12	1B0,1B1,1B2,1B3,1B4,1B5,1B6,1B7	data inputs/outputs
13,14,16,17,19,20,22,23	2B0,2B1,2B2,2B3,2B4,2B5,2B6,2B7	data inputs/outputs
4,10,15,21,28,34,39,45	GND	ground (0V)
7,18	$V_{CC(B)}$	supply voltage B(5V bus)
48,25	$1\overline{OE}$,$2\overline{OE}$	output enable inputs(active LOW)
47,46,44,43,41,40,38,37	1A0,1A1,1A2,1A3,1A4,1A5,1A6,1A7	data inputs/outputs
36,35,33,32,30,29,27,26	2A0,2A1,2A2,2A3,2A4,2A5,2A6,2A7	data inputs/outputs
31,42	$V_{CC(A)}$	supply voltage A(3V bus)

2.4、Function Table

Control		Input/output	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	nAn=nBn	inputs
L	H	inputs	nBn=nAn
H	X	Z	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage B	$V_{CC(B)}$	$V_{CC(B)} \geq V_{CC(A)}$	-0.5	+6.0	V
supply voltage A	$V_{CC(A)}$	$V_{CC(B)} \geq V_{CC(A)}$	-0.5	+4.6	V
input clamping current	I_{IK}	$V_I<0V$	-50	-	mA
input voltage	V_I	-[1]	-0.5	+6.0	V
Input/output voltage	$V_{I/O}$	-	-0.5	V_{CC}+0.5	V
output clamping current	I_{OK}	$V_O>V_{CC}$ or $V_O<0V$	-	±50	mA
output voltage	V_O	output HIGH or LOW [1]	-0.5	V_{CC}+0.5	V
		output 3-state[1]	-0.5	+6.0	V
output current	$I_{O(sink/source)}$	V_O=0V to V_{CC}	-	±50	mA
supply current	I_{CC}	-	-	100	mA
ground current	I_{GND}	-	-100	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-[2]	-	+150	℃
total power dissipation	P_{tot}	T_{amb}=-40℃ to +105℃	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
supply voltage B	$V_{CC(B)}$	$V_{CC(B)} \geq V_{CC(A)}$	maximum speed performance	2.7	-	5.5	V
			low-voltage applications	1.2	-	5.5	V
supply voltage A	$V_{CC(A)}$	$V_{CC(B)} \geq V_{CC(A)}$	maximum speed performance	2.7	-	3.6	V
			low-voltage applications	1.5	-	3.6	V
input voltage	V_I	control inputs: n$\overline{OE}$ and nDIR		0	-	5.5	V
Input/output voltage	$V_{I/O}$	nAn port		0	-	$V_{CC(A)}$	V
		nBn port		0	-	$V_{CC(B)}$	V
output voltage	V_O	nAn port		0	-	$V_{CC(A)}$	V
		nBn port		0	-	$V_{CC(B)}$	V
ambient temperature	T_{amb}	-		-40	-	+105	℃
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC(A)}$=2.7V to 3.0V		0	-	20	ns/V
		$V_{CC(A)}$=3.0V to 3.6V		0	-	10	ns/V
		$V_{CC(B)}$=3.0V to 4.5V		0	-	20	ns/V
		$V_{CC(B)}$=4.5V to 5.5V		0	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
HIGH-level input voltage	V_{IH}	nBn port	$V_{CC(B)}$=3.0V to 5.5V[2]	2.0	-	-	V
		nAn port, $\overline{n}OE$ and nDIR	$V_{CC(A)}$=3.0V to 3.6V	2.0	-	-	V
			$V_{CC(A)}$=2.3V to 2.7V[2]	1.7	-	-	V
LOW-level input voltage	V_{IL}	nBn port	$V_{CC(B)}$=4.5V to 5.5V[2]	-	-	0.8	V
			$V_{CC(B)}$=3.0V to 3.6V[2]	-	-	0.7	V
		nAn port, $\overline{n}OE$ and nDIR	$V_{CC(A)}$=3.0V to 3.6V	-	-	0.8	V
			$V_{CC(A)}$=2.3V to 2.7V[2]	-	-	0.7	V
HIGH-level output voltage	V_{OH}	nBn port; V_I=V_{IH} or V_{IL}	I_O=-24mA; $V_{CC(B)}$=4.5V	$V_{CC(B)}$-0.8	-	-	V
			I_O=-12mA; $V_{CC(B)}$=4.5V	$V_{CC(B)}$-0.5	-	-	V
			I_O=-18mA; $V_{CC(B)}$=3.0V	$V_{CC(B)}$-0.8	-	-	V
			I_O=-100uA; $V_{CC(B)}$=3.0V	$V_{CC(B)}$-0.2	$V_{CC(B)}$	-	V
		nAn port; V_I=V_{IH} or V_{IL}	I_O=-24mA; $V_{CC(A)}$=3.0V	$V_{CC(A)}$-0.7	-	-	V
			I_O=-100uA; $V_{CC(A)}$=3.0V	$V_{CC(A)}$-0.2	-	-	V
			I_O=-12mA; $V_{CC(A)}$=2.7V	$V_{CC(A)}$-0.5	-	-	V
			I_O=-8mA; $V_{CC(A)}$=2.3V	$V_{CC(A)}$-0.6	-	-	V
			I_O=-100uA; $V_{CC(A)}$=2.3V	$V_{CC(A)}$-0.2	$V_{CC(A)}$	-	V
LOW-level output voltage	V_{OL}	nBn port; V_I=V_{IH} or V_{IL}	I_O=24mA; $V_{CC(B)}$=4.5V	-	-	0.55	V
			I_O=12mA; $V_{CC(B)}$=4.5V	-	-	0.40	V
			I_O=100uA; $V_{CC(B)}$=4.5V	-	-	0.20	V
			I_O=18mA; $V_{CC(B)}$=3.0V	-	-	0.55	V
			I_O=100uA; $V_{CC(B)}$=3.0V	-	-	0.20	V
		nAn port; V_I=V_{IH} or V_{IL}	I_O=24mA; $V_{CC(A)}$=3.0V	-	-	0.55	V
			I_O=100uA; $V_{CC(A)}$=3.0V	-	-	0.20	V
			I_O=12mA; $V_{CC(A)}$=2.7V	-	-	0.40	V
			I_O=12mA; $V_{CC(A)}$=2.3V	-	-	0.60	V
			I_O=100uA; $V_{CC(A)}$=2.3V	-	-	0.20	V
input leakage current	I_I	V_I=5.5V or GND		-	±0.1	±5	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL};V_O=V_{CC} or GND[3]		-	±0.1	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A		-	0.1	40	uA
additional supply current	ΔI_{CC}	per control pin; V_I=V_{CC}-0.6V;I_O=0A [4]		-	5	500	uA
input capacitance	C_I	-		-	4.0	-	pF
input/output capacitance	$C_{I/O}$	nAn and nBn port		-	5.0	-	pF

Note:

[1] All typical values are measured at $V_{CC(B)}$=5.0V,$V_{CC(A)}$=3.3V and T_{amb}=25℃.

[2] If $V_{CC(A)}$<2.7V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

[4] $V_{CC(A)}$=2.7V to 3.6V:other inputs at $V_{CC(A)}$ or GND;$V_{CC(B)}$=4.5V to 5.5V:other inputs at $V_{CC(B)}$ or GND.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
HIGH-level input voltage	V_{IH}	nBn port	$V_{CC(B)}$=3.0V to 5.5V[2]	2.0	-	-	V
		nAn port, $n\overline{OE}$ and nDIR	$V_{CC(A)}$=3.0V to 3.6V	2.0	-	-	V
			$V_{CC(A)}$=2.3V to 2.7V[2]	1.7	-	-	V
LOW-level input voltage	V_{IL}	nBn port	$V_{CC(B)}$=4.5V to 5.5V[2]	-	-	0.8	V
			$V_{CC(B)}$=3.0V to 3.6V[2]	-	-	0.7	V
		nAn port, $n\overline{OE}$ and nDIR	$V_{CC(A)}$=3.0V to 3.6V	-	-	0.8	V
			$V_{CC(A)}$=2.3V to 2.7V[2]	-	-	0.7	V
HIGH-level output voltage	V_{OH}	nBn port; V_I=V_{IH} or V_{IL}	I_O=-24mA; $V_{CC(B)}$=4.5V	$V_{CC(B)}$-1.2	-	-	V
			I_O=-12mA; $V_{CC(B)}$=4.5V	$V_{CC(B)}$-0.8	-	-	V
			I_O=-18mA; $V_{CC(B)}$=3.0V	$V_{CC(B)}$-1.0	-	-	V
			I_O=-100uA; $V_{CC(B)}$=3.0V	$V_{CC(B)}$-0.3	-	-	V
		nAn port; V_I=V_{IH} or V_{IL}	I_O=-24mA; $V_{CC(A)}$=3.0V	$V_{CC(A)}$-1.0	-	-	V
			I_O=-100uA; $V_{CC(A)}$=3.0V	$V_{CC(A)}$-0.3	-	-	V
			I_O=-12mA; $V_{CC(A)}$=2.7V	$V_{CC(A)}$-0.8	-	-	V
			I_O=-8mA; $V_{CC(A)}$=2.3V	$V_{CC(A)}$-0.6	-	-	V
			I_O=-100uA; $V_{CC(A)}$=2.3V	$V_{CC(A)}$-0.3	-	-	V
LOW-level output voltage	V_{OL}	nBn port; V_I=V_{IH} or V_{IL}	I_O=24mA; $V_{CC(B)}$=4.5V	-	-	0.60	V
			I_O=12mA; $V_{CC(B)}$=4.5V	-	-	0.80	V
			I_O=100uA; $V_{CC(B)}$=4.5V	-	-	0.30	V
			I_O=18mA; $V_{CC(B)}$=3.0V	-	-	0.80	V
			I_O=100uA; $V_{CC(B)}$=3.0V	-	-	0.30	V
		nAn port; V_I=V_{IH} or V_{IL}	I_O=24mA; $V_{CC(A)}$=3.0V	-	-	0.80	V
			I_O=100uA; $V_{CC(A)}$=3.0V	-	-	0.30	V
			I_O=12mA; $V_{CC(A)}$=2.7V	-	-	0.60	V
			I_O=12mA; $V_{CC(A)}$=2.3V	-	-	0.60	V
			I_O=100uA; $V_{CC(A)}$=2.3V	-	-	0.20	V
input leakage current	I_I	V_I=5.5V or GND		-	-	±10	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL};V_O=V_{CC} or GND[3]		-	-	±20	uA
supply current	I_{CC}	V_I=V_{CC} or GND;I_O=0A		-	-	80	uA
additional supply current	ΔI_{CC}	per control pin; V_I=V_{CC}-0.6V;I_O=0A [4]		-	-	5000	uA

Note:

[1] All typical values are measured at $V_{CC(B)}$=5.0V,$V_{CC(A)}$=3.3V and T_{amb}=25℃.

[2] If $V_{CC(A)}$<2.7V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

[4] $V_{CC(A)}$=2.7V to 3.6V:other inputs at $V_{CC(A)}$ or GND;$V_{CC(B)}$=4.5V to 5.5V:other inputs at $V_{CC(B)}$ or GND.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, GND=0V; t_r=t_f ≤2.5ns; C_L=50pF; voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	nAn to nBn; see Figure 4[2]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	3.3	7.6	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.0	3.0	5.9	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	2.9	5.8	ns
		nBn to nAn; see Figure 4[2]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.0	3.0	7.6	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.0	4.3	6.7	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.2	2.5	5.8	ns
enable time	t_{en}	$n\overline{OE}$ to nBn; see Figure 5[3]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	4.1	11.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	3.6	9.2	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	3.2	8.9	ns
		$n\overline{OE}$ to nAn; see Figure 5[3]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	4.6	12.3	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	4.3	9.3	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	3.2	8.9	ns
disable time	t_{dis}	$n\overline{OE}$ to nBn; see Figure 5[4]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	2.0	2.7	10.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	2.5	4.6	9.0	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	2.1	4.9	8.6	ns
		$n\overline{OE}$ to nAn; see Figure 5[4]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.0	2.7	9.3	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	3.5	9.0	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	2.0	3.2	8.6	ns
power dissipation	C_{PD}	5V port:nAn to nBn; V_I=GND to V_{CC};	outputs enabled	-	30	-	pF

capacitance		$V_{CC(B)}$=5V; $V_{CC(A)}$=3.3V[5]	outputs disabled	-	15	-	pF
		3V port:nBn to nAn; V_I=GND to V_{CC}; $V_{CC(B)}$=5V; $V_{CC(A)}$=3.3V[5]	outputs enabled	-	40	-	pF
			outputs disabled	-	5	-	pF

Note:

[1] All typical values are measured at nominal voltage for $V_{CC(B)}$ and $V_{CC(A)}$ and at T_{amb}=25℃.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\Sigma(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\Sigma(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +105℃, GND=0V; $t_r=t_f$ ≤2.5ns; C_L=50pF; voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{pd}	nAn to nBn; see Figure 4[2]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	-	9.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.0	-	7.5	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	-	7.5	ns
		nBn to nAn; see Figure 4[2]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.0	-	9.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.0	-	8.5	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.2	-	7.5	ns
enable time	t_{en}	$n\overline{OE}$ to nBn; see Figure 5[3]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	-	14.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	-	11.5	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	-	12.0	ns
		$n\overline{OE}$ to nAn; see Figure 5[3]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.5	-	15.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	-	12.0	ns

			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	1.0	-	11.5	ns
disable time	t_{dis}	$n\overline{OE}$ to nBn; see Figure 5[4]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	2.0	-	13.5	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	2.5	-	11.5	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	2.1	-	11.0	ns
		$n\overline{OE}$ to nAn; see Figure 5[4]	$V_{CC(A)}$=2.3V to 2.7V; $V_{CC(B)}$=3.0V to 3.6V	1.0	-	12.0	ns
			$V_{CC(A)}$=2.7V; $V_{CC(B)}$=4.5V to 5.5V	1.5	-	11.5	ns
			$V_{CC(A)}$=3.0V to 3.6V; $V_{CC(B)}$=4.5V to 5.5V	2.0	-	11.0	ns

Note:

[1] All typical values are measured at nominal voltage for $V_{CC(B)}$ and $V_{CC(A)}$ and at T_{amb}=25℃.

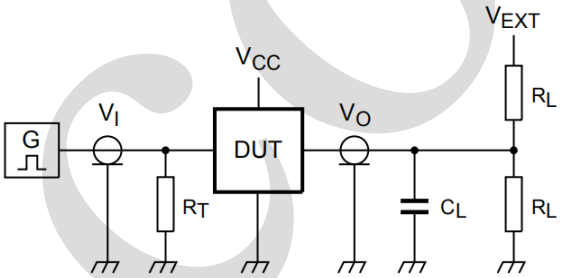
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

4、Testing Circuit

4.1、AC Testing Circuit



Definitions test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

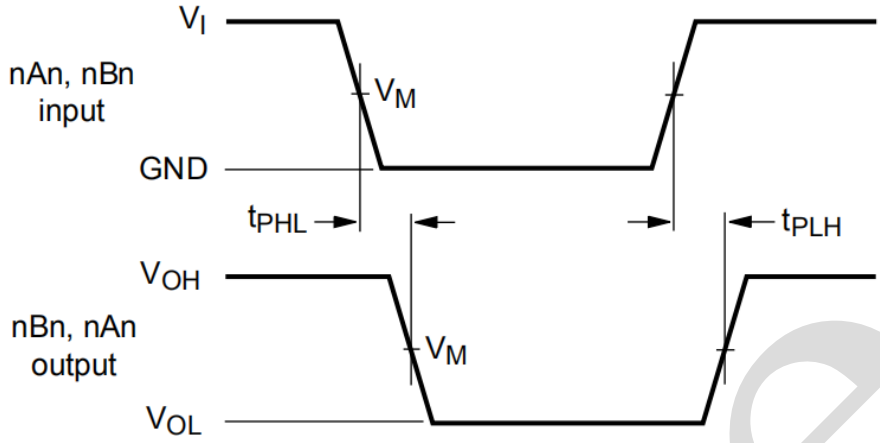
R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

Figure 3. Test circuit for measuring switching times

4.2、Test Data

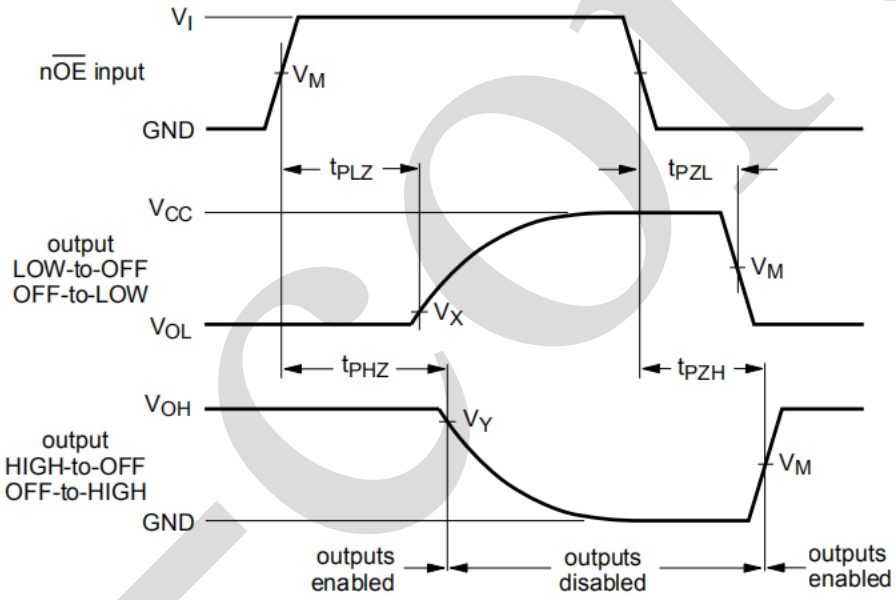
Direction	Supply voltage		Load		V_{EXT}		
	$V_{CC(A)}$	$V_{CC(B)}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
nAn port to nBn port	2.3V to 2.7V	2.7V to 3.6V	50pF	500Ω	open	GND	2×V_{CC}
nBn port to nAn port	2.3V to 2.7V	2.7V to 3.6V	50pF	500Ω	open	GND	6.0V
nAn port to nBn port	2.7V to 3.6V	4.5V to 5.5V	50pF	500Ω	open	GND	2×V_{CC}
nBn port to nAn port	2.7V to 3.6V	4.5V to 5.5V	50pF	500Ω	open	GND	6.0V

4.3、AC Testing Waveforms



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. Input (nAn,nBn) to output (nBn,nAn) propagation delays



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

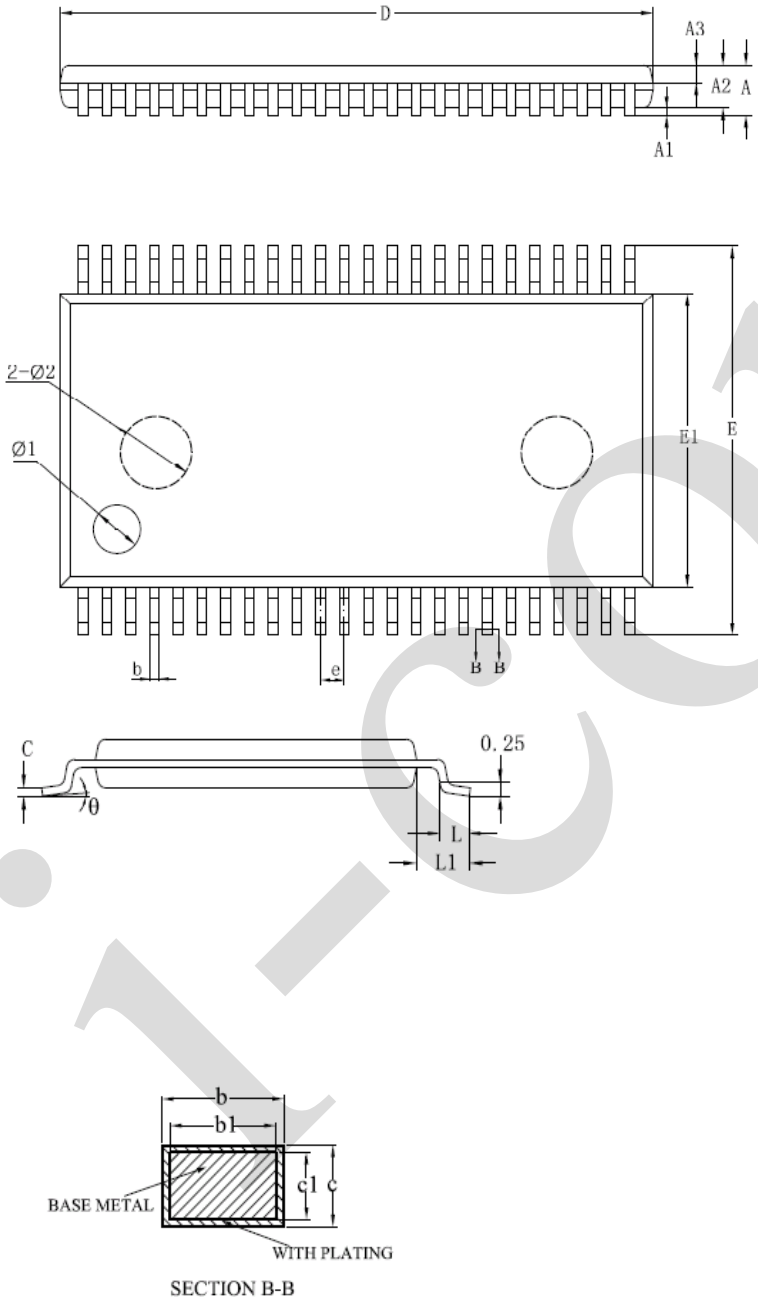
Figure 5. 3-state enable and disable times

4.4、Measurement points

Direction	Supply voltage		Input		Output		
	$V_{CC(A)}$	$V_{CC(B)}$	V_I	V_M	V_M	V_X	V_Y
nAn port to nBn port	2.3V to 2.7V	2.7V to 3.6V	$V_{CC(A)}$	$0.5\times V_{CC(A)}$	1.5V	$V_{OL(B)}$+0.3V	$V_{OH(B)}$-0.3V
nBn port to nAn port	2.3V to 2.7V	2.7V to 3.6V	2.7V	1.5V	$0.5\times V_{CC(A)}$	$V_{OL(A)}$+0.15V	$V_{OH(A)}$-0.15V
nAn port to nBn port	2.7V to 3.6V	4.5V to 5.5V	2.7V	1.5V	$0.5\times V_{CC(B)}$	$0.2\times V_{CC(B)}$	$0.8\times V_{CC(B)}$
nBn port to nAn port	2.7V to 3.6V	4.5V to 5.5V	3.0V	1.5V	1.5V	$V_{OL(A)}$+0.3V	$V_{OH(A)}$-0.3V

5、Package Information

5.1、TSSOP48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
A3	0.35	0.40	0.45
b	0.19	—	0.28
b1	0.18	0.20	0.23
c	0.15	—	0.21
c1	0.14	0.15	0.16
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°
Ø1	Ø1.00×0.10±0.05DP		
Ø2	Ø1.50×0.075±0.025DP		

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product；

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