16+1 ports Ethernet Switch Controller with Octal-PHYs (Priority, Security & Protocol)

Features

- **Built in 8 internal PHY, 8 SS-SMII, and one MII**
- **1.25Mbits packet buffer memory**
- **Support packet length up to 1600 Bytes**
- **Store & forward, share memory, non-blocking architecture**
- **Support flow control**
  - 802.3x in full duplex
  - Collision / Carrier sense based backpressure in half duplex
- **Provide up to 4K MAC address entries**
  - CRC/ direct hashing algorithm
  - Programmable aging timer (55s~1812070.4s)
  - Wire speed address learning and resolution
  - CPU accessible for security and static MAC
  - Learning enable/disable
- **Support Sniffer function (in, out, in & out)**
- **Support IGMP snooping function Version 1,2**
- **Support up to 2 trunk group**
  - Support up to 2 trunk groups
  - (Port 0~3, port 4~7)
  - Load balance based on (port, DA, SA, DA / SA)
- **Support VLAN(20 VLAN groups)**
  - Port based VLAN
  - Tag based VLAN based on Ports & VIDs
  - Add/ remove/ modify tag
- **Support Class of Service**
  - Port based COS function
  - 802.1Q priority tag based
  - IP TOS based (IPv4/IPv6)
  - TCP/UDP port based
  - 4 queues for per port
  - WRR/ FIFS/ SP algorithm
- **Broadcast storm control support**
  - Broadcast rate control per port
  - Block broadcast packet that not belongs to ARP or IPv4 packet to CPU port
- **Support port security**
  - MAC address based
  - TCP/UDP port based
- **Supports Bandwidth control**- 255 configurable levels for P0-P16, (from 32kbps to 7.96 Mbps) for low bandwidth
  - 255 configurable levels for P0-P16 (from 512kbps to 100 Mbps) for high bandwidth
  - With/without flow control
- **Support SMI auto-polling function**
  - Poll for speed, duplex, flow control, and link
  - Support Reverse MII 100M full duplex only
  - CPU accessible (interrupt support)
- **CPU R/W PHY registers**
- **Support SS-SMII mode**
- **Support 4 port states for Spanning Tree protocol**
  - Discarding/Blocking/learning/ forwarding
  - Forward BPDU to CPU port
- **Captures specific packet to CPU port**
- **BPDU, LACP, 802.1X, GMRP, GVRP, ARP**
- **ICMP, IGMP, TCP, UDP, OSPF, other IP protocols**
  - Packets with specific TCP/UDP port number
- **Flexible PHY address setting for CPU.**
- **Support three Configuration modes**
  - Pin initial setting
  - 2 wire serial interface for EEPROM
  - 2 wire serial interface for CPU
- **Statistic counters for each port**
  - RX/TX packet count
  - CRC error packet count
  - Drop packet count
  - Collision count
- **Support Non association port**
- **Support port based address flush**
- **Support LED functions (for p0~p7)**
  - Support 2 bit serial,3 bit serial, and 3 bit bi color mode
  - Support direct LED mode for Link/Activity, speed, duplex states
  - Support bi color direct LED mode
- **Only one 25MHz crystal is needed**
- **Adjustable IO voltage (3.3v MII1.95V SS-SMII)**
- **Programmable MAC address table through CPU interface**

- **128 pin LQFP EPAD package**

General Description

The IP1717 is a cost effective and fully integrated single chip. It integrates a 17-port switch controller, an octal PHY transceiver and SSRAM. Each of PHY transceiver complies with 802.3u specification and HP-license Auto MDI/MDIX.

The IP1717 also provides a 3S-MII interface to connect an octal PHY for a 16-port dumb switch application and a MII interface for a smart/management switch application.

It supports full smart switch functions, including IGMP snooping, 4 priority queues, TOS, TCP/UDP port number priority, 802.1Q VLAN, port security, protocol filter/forwarding and bandwidth control.

Block diagram

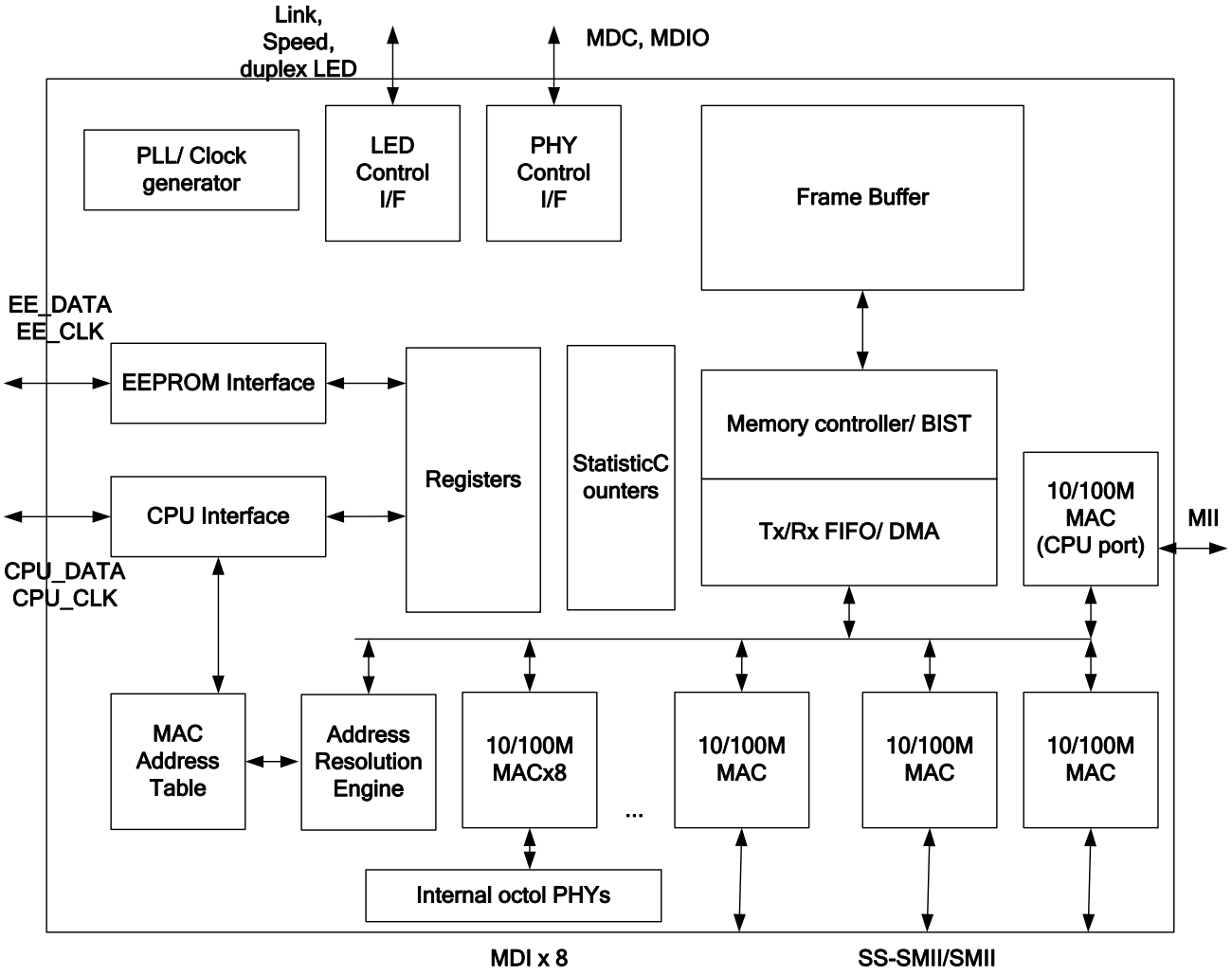

Table of Contents

Revision History

Revision #	Change Description
IP1717-DS-R01	Initial Release
IP1717-DS-R02	1.Modify COL LED blinking function in LEDMODE[1:0]=10 (page14 and 23)
	2.Remove SMII, Only SS-SMII is supported by IP1717
	3.Modify pin description of pin 99 BLK_TIME
	4.HOME_VLAN_OFF pin setting changed to pin 97
	5.Modify BPDU description, refer to General MAC operation behavior register(page 40) 6.Fix incorrect pin diagram(page 7)
IP1717-DS-R03	1.Fix P16 force link function description, refer to P16_FORCE_OFF pin description(Page11)
IP1717-DS-R04	1.Add interrupt events respond time description of CPU R/W EEPROM, SMI, and PHY link status change(page 23) 2.Support advanced power saving mode(page 26) 3.Add priority field of VLAN tag mapping to output queue description(page 30) 4.Add WRR ratio description of queue(page 30&50) 5.Fix MDC/MDIO timing(page 6) 6.Fix incorrect MII transmit and receive timing (page 69) 7.Add special tag description(page 42) 8.Fix incorrect register definition for backpressure(page 16) 9.Add DC characteristics description for VDDIO_1(page74) 10.Add the description of the TCP/UDP port number and the user-defined port number.(page 32) 11.Modify the description of the memory buffer size(page 1) 12.Add the description of the Switch ID(page 20) 13.Modify the description of IP TOS based COS(page 32) 14.Add DC characteristics description for crystal(X1)(page 74) 15.Add AC characteristics description for power sequence(page 65) 16.Modify the description of the uplink port(page 29) 17.Add TX pause description for switch(page 16) 18.Modify port number usage description for protocol(page 46) 19.Add MAC address description for CPU(page 48) 20.Modify the description for absolute maximum rating(page 68) 21.Add the description of the Spd/Duplex LEDs in force mode(page 24,62) 22.Modify the setting of register 02h[5] to be reserved(page 43) 23.Fix the error of 3-bit Bi-color LED setting(page 26) 24.Add junction temperature description(page 68) 25.Add RESETB threshold voltage description(page 74) 26.Add the register description of the internal octal PHY(page64~66) 27.Add Crystal specification description(page 75) 28.Modify Power On Sequence and Reset Timing(page 68) 29.Remove IP security function description(page1,38,52,56,57) 30.Modify VLAN group description(page1) 31.Add EEPROM timing specification(page 73) 32.Modify MDC/MDIO and CPUCLK/CPUDATA timing specification(page 70,71) 33.Modify Power On Sequence and Reset Timing(page 68)
IP1717-DS-R05	1.Package changed to LQFP EPAD(page2,75,76)

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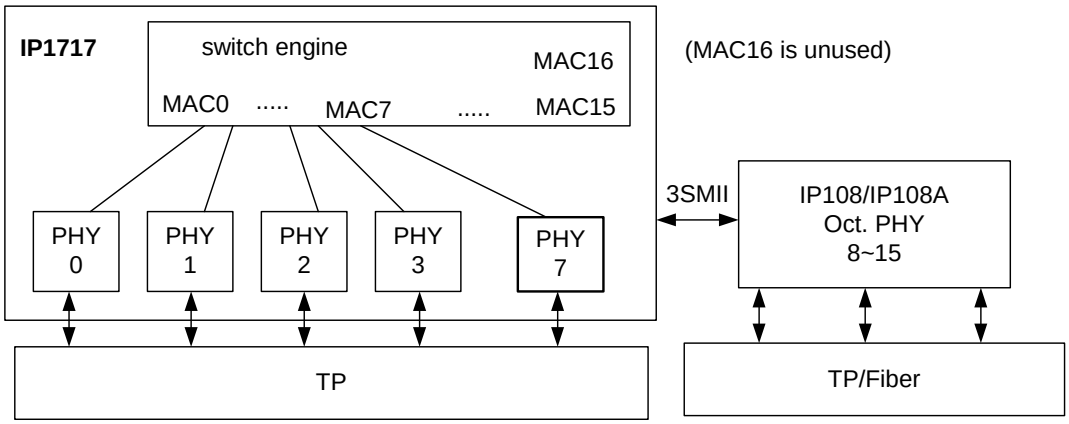
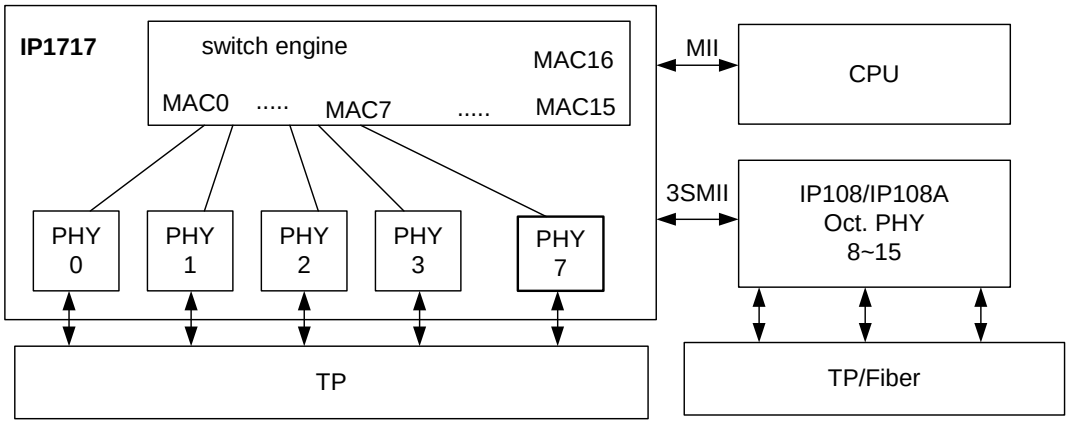
This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

Application Diagram

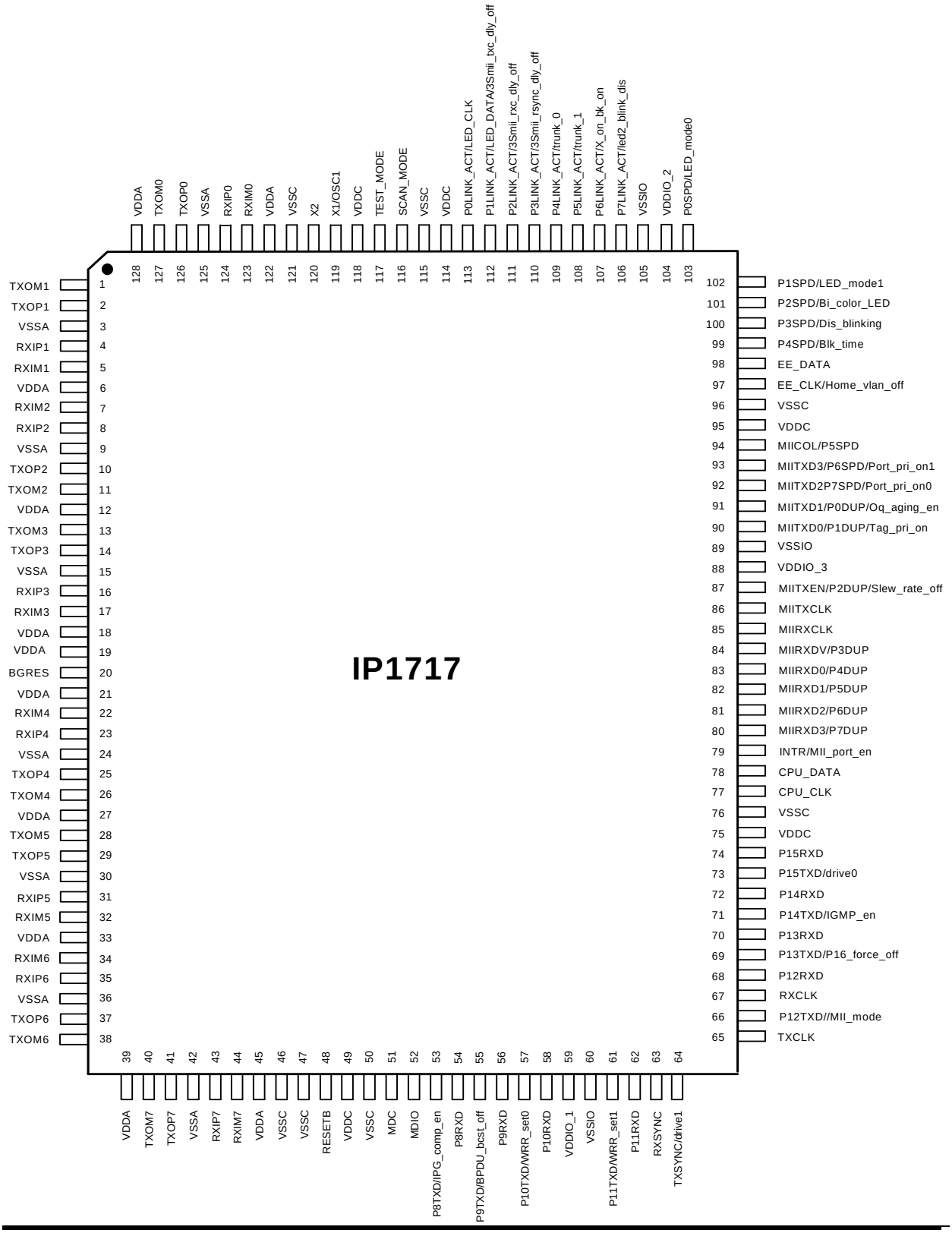
Dumb switch application



Smart/Management switch application



Pin diagram



1 Pin description

Pin No.	Label	Type	Description
SS-SMII			
73,71,69,66 61,57,55,53	P15TXD, P14TXD, P13TXD, P12TXD, P11TXD, P10TXD, P9TXD, P8TXD	O	SS-SMII transmit data output for port 8 to port 15
64	TXSYNC	O	SS-SMII synchronization output for transmit data
65	TXCLK	O	SS-SMII transmit clock output
74,72,70,68 62,58,56,54	P15RXD, P14RXD, P13RXD, P12RXD, P11RXD, P10RXD, P9RXD, P8RXD,	I	SS-SMII receive data input for port 8 to port 15
63	RXSYNC	I	SS-SMII receive synchronization input
67	RXCLK	I	SS-SMII receive clock input
MII/Reverse MII			
87	MIITXEN	O	MII (port 16) transmit enable
94	MIICOL	I/O	MII (port 16) collision is an input driven by PHY in PHY mode. When in reverse MII mode, it is a output pin driven by IP1717
93,92,91,90	MIITXD3~MIITXD0	O	MII (port 16) transmit data output
84	MIIRXDV	I	MII (port 16) receive valid
80,81,82,83	MIIRXD3~ MIIRXD0	I	MII (port 16) receive data input
86	MIITXCLK	I/O	MII (port 16) transmit clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII.
85	MIIRXCLK	I/O	MII (port 16) receive clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII.
SMI			
51	MDC	O	Clock for serial management bus. It's recommended to add a 30pf capacitor to ground for noise filtering.
52	MDIO	I/O	I/O data for serial management bus. It's recommended to add a 4.7K pull up resistor connecting to VDDIO_1 and a 30pf capacitor connecting to ground.

Pin description (continue)

Pin No.	Label	Type	Description
EEPROM			
97	EE_CLK	O	Serial EEPROM clock output
98	EE_DATA	I/O	Serial EEPROM data
PHY interface(Auto-MDI/MDIX, HP-License)			
40,38,28,26, 13,11,1,127	TXOM[7:0]	I/O	Transmit/Receive output/input differential negative signal
41,37,29,25, 14,10,2,126	TXOP[7:0]	I/O	Transmit/Receive output/input differential positive signal
44,34,32,22, 17,7,5,123	RXIM[7:0]	I/O	Receive/Transmit input/output differential negative signal
43,35,31,23, 16,8,4,124	RXIP[7:0]	I/O	Receive/Transmit input/output differential positive signal
CPU			
77	CPU_CLK	I	Serial CPU access clock input
78	CPU_DATA	I/O	Serial CPU data
Serial LED			
113	LED_CLK	O	Serial LED CLK
112	LED_DATA	I/O	Serial LED data
Direct LED (LED_MODE[1:0] must be set to 11 to support direct LED mode)			
113,112,111, 110,109,108, 107,106	P0LINK_ACT~ P7LINK_ACT	O	Direct LED link/activity for port0~7 The LED should be connected to VDDIO_2 through a 220 ohm resistor.
103,102,101, 100,99,94,93, 92	P0SPD~ P7SPD	O	Direct LED speed for port0~7 The LED of P0SPD~P4SPD should be connected to VDDIO_2 through a 220 ohm resistor. The LED of P5SPD~P7SPD should be connected to VDDIO_3 through a 220 ohm resistor. To support direct LED mode, MII port must be disabled by setting MII _PORT_EN to 0.
91,90,87,84 83,82,81,80	P0DUP~ P7DUP	O	Direct LED duplex for port0~7 The LED should be connected to VDDIO_3 through a 220 ohm resistor. To support direct LED mode, MII port must be disabled by setting MII _PORT_EN to 0.

Pin description (continue)

Pin No.	Label	Type	Description
Miscellaneous			
119	X1/OSCI	I	Crystal/ Oscillator 25MHz input
120	X2	O	Crystal output
48	RESETB	I	System reset (low active). Should be kept at “low” for at least 10 microseconds. The input voltage should be not higher than VDDIO_1.
79	INTR	O	Interrupt output. Active low. The pin can be either active low or high by writing REG E7h[4]
116	SCAN_MODE	I	Scan mode for testing
117	TEST_MODE	I	Test mode for testing
20	BGRES	I	Band gap reference voltage, it must be pull down by 6.19K ohm.
Power & Ground			
118,114,95,75, 49	VDDC	P	1.95V power for Core circuit
128,122,45,39, 33,27,21,19, 18,12,6	VDDA	P	1.95V power for analog circuit
59	VDDIO_1	P	1.95V power of I/O PAD of SS-SMII
104	VDDIO_2	P	3.3V power of I/O PAD of link and speed LED
88	VDDIO_3	P	3.3V power for I/O PAD of speed, duplex LED and MII
121,115,96,76, 50,47,46	VSSC	P	Core Ground
125,42,36,30, 2415,9,3	VSSA	P	Analog Ground
105,89,60	VSSIO	P	I/O Ground

Pin description (continue) latch in pins

<table>
<tr><th>Pin No.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Power On setting. The state of these pins will be latched upon reset.</td></tr>
<tr><td>53</td><td>IPG_COMP_EN</td><td>IL, PU</td><td>Enable IPG compensation
1: Enable (Default); 0: Disable
The function can be set by writing register 01h[1:0]</td></tr>
<tr><td>55</td><td>BPDU_BCST_OFF</td><td>IL, PU</td><td>Filter the packet with MAC destination address 01-80-c2-00-00-03 ~01-80-c2-00-00-0F
1: Filter (Default)
0: Broadcast
The function can be set by writing register 01h[2]</td></tr>
<tr><td>61,57</td><td>WRR_SET1,
WRR_SET0</td><td>IL, PD</td><td>Weight round robin setting of priority queues
<table><tr><td>00= First in first out</td><td>01= 8:1 ratio for 2 queues</td></tr><tr><td>10= 4:3:2:1 for 4 queues</td><td>11= 8:4:2:1 for 4 queues</td></tr></table>The function can be set by writing register 38h[15:0]</td></tr>
<tr><td>66</td><td>MII_MODE</td><td>IL, PU</td><td>Reverse MII mode
0:Reverse MII (IP1717 works as a PHY)
1:Normal MII (IP1717 works as a MAC`)
The function can be set by writing register E2h[2]</td></tr>
<tr><td>69</td><td>P16_FORCE_OFF</td><td>IL, PU</td><td>Port 16 force link
1: not force link(default)
0: force link
The function can be set by writing register BDh[6]
Port 16 only support 100M full duplex if port 16 force link and Reverse MII are enabled.</td></tr>
<tr><td>71</td><td>IGMP_EN</td><td>IL, PU</td><td>IGMP enable
1: Disable GMP function (default)
0: Enable IGMP function
The function can be set by writing register A5h[0]</td></tr>
<tr><td>64,73</td><td>DRIVE1,
DRIVE0</td><td>IL,PD,
PU</td><td>SS-SMII clock and data driving current setting
<table><tr><td></td><td>TXCLK/TXSYNC</td><td>TXD</td></tr><tr><td>00</td><td>4mA</td><td>2mA</td></tr><tr><td>01 (default)</td><td>8mA</td><td>4mA</td></tr><tr><td>10</td><td>11mA</td><td>8mA</td></tr><tr><td>11</td><td>11mA</td><td>11mA</td></tr></table>The function can be set by writing register EAh[4:3]</td></tr>
<tr><td>87</td><td>SLEW_RATE_OFF</td><td>IL,PD</td><td>Slew rate enable:
1: normal
0: fast (default)
The function can be set by writing register EAh[5]
If an external pull up resistor is used, it should be connected to VDDIO_3.</td></tr>
</table>

Pin description (continue) latch in pins

Pin No.	Label	Type	Description
Power On setting. The state of these pins will be latched upon reset.			
90	TAG_PRI_ON	IL,PD	Tag priority enable: 1: enable 0: disable (default) The function can be set by writing register 17h[15:0]~18h[0]. If an external pull up resistor is used, it should be connected to VDDIO_3.
91	OQ_AGING_EN	IL,PD	Output queue aging time enable 1:enable 0: disable (default) The function can be set by writing register 39h[7] If an external pull up resistor is used, it should be connected to VDDIO_3.
93,92	PORT_PRI_1, PORT_PRI_0	IL,PD	Port high priority enable setting 00: none (default) / 01: port1~port4 10: port 13~16 / 11: CPU port only The function can be set by writing register 14~15h[15:0] and 16h[1:0]. If an external pull up resistor is used, it should be connected to VDDIO_3.
79	MII_PORT_EN	IL,PU	MII port enable 1: MII port enable pin80~87,90~94 are changed to MII pins(default). 0:MII port disable pin80~87,90~94 are changed to LED pins.
97	HOME_VLAN_OFF	IL, PU	Home VLAN setting enable Port 0 ~ Port15 are all individual VLAN and only send to CPU port. 1: Disabled (Default) 0: Enabled
112	SS-SMII_TXC_DLY_OFF	IL,PU	SS-SMII TXCLK delay 1: No delay (default) 0:delay 4ns The function can be set by writing register EAh[0]
111	SS-SMII_RXC_DLY_OFF	IL,PU	SS-SMII RXCLK delay 1: No delay (default) 0:delay 4ns The function can be set by writing register EAh[1]
110	SS-SMII_RSYNC_DLY_OFF	IL,PU	SS-SMII RXSYNC delay 1: No delay (default) 0:delay 4ns The function can be set by writing register EAh[2]

108,109	TRUNK_1, TRUNK_0	IL,PU	Trunk port setting for trunk group 0 11: none (default) 10:port 1~2 01: port 1~3 00: port 1~4 The function can be set by writing register 46h[7:0]
107	X_ON_BK_ON	IL,PU	Flow control off for full and half mode 1: flow control on (default) 0: flow control off

Pin description (continue) latch in pins

Pin No.	Label	Type	Description
Power On setting. The state of these pins will be latched upon reset.			
106	LED2_BLINK_DIS	IL,PU	LED mode 2 blinking disable 1: COL LED not blinking during collision (default) 0: COL LED blinking during collision. This pin is valid for 3-bit serial bi-color mode only (LEDMODE[1:0]=10); the other LED modes are not affected.
102,103	LED_MODE1, LED_MODE0	IL,.PD	LED mode selection 00: 3 bit serial mode (default) 01: 2 bit serial mode 10: 3 bit serial Bi-color mode 11: mono direct LED mode If an external pull up resistor is used, it should be connected to VDDIO_2.
101	BI_COLOR_LED	IL,.PD	Direct bi color LED mode 1: bi color 0: mono color (default) If an external pull up resistor is used, it should be connected to VDDIO_2.
100	DIS_BLINKING	IL,.PD	Disable LED blinking: 1:enable 0: disable (default) LED will not be blinking upon power on if the pin set to one If an external pull up resistor is used, it should be connected to VDDIO_2.
99	BLK_TIME	IL,.PU	Blinking time period: 1: 40ms(default) 0:120ms Blinking time can be selected either 120ms or 40ms

Note:

1. All the trapped pins are latched upon reset and are pulled down or pulled up by a 50K resistor inside the chip.
2. The designer can connect a 4.7K ohms resistor to set these pins to “1” or “0” to change the default state.
3. The content of an EEPROM will override the pin setting.

2 Function description

2.1 Switch engine and queue management

Packet forwarding

IP1717 utilizes the “store & forward” method to handle packet transfer. IP1717 begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

2.1.1 Address learning and hashing

Related registers	3Bh[0], 40h

IP1717 can handle up to 4096 MAC address entries. And it provides two kinds of hash method to maintain the MAC address table; one is the direct mapping and the other is the CRC algorithm. When the direct mapping method is selected, register 3Bh[0] set to “1”, IP1717 recognizes the least significant 12 bits of the MAC address. When the CRC algorithm is used, register 3Bh[0] set to “0”,

The address learning function for each port can be either enabled or disabled by setting the corresponding bit in registers 40h.

Packets with the following conditions will not be stored in MAC address table.

- Erroneous packet
- 802.3x pause packet
- 802.1D Reserved Group packet
- Multicast source MAC address
- Under size and over size(>1600)

2.1.2 802.1D packet forward

Related registers	01h[2], 02h[2:1]

Besides the erroneous packet and the IEEE802.3x pause packet are not forwarded, 802.1D Reserved Group packet with MAC address from 01-80-c2-00-00-04 to 01-80-c2-00-00-0F can be optionally dropped by setting register 01h[2]. A packet with MAC address equal to 01-80-c2-00-00-00 can be forwarded to CPU or be dropped according to the setting in register 02h[1]. A packet with MAC address equal to 01-80-c2-00-00-03 can be forwarded to CPU or be dropped according to the setting in register 02h[2].

2.1.3 Inter frame gap compensation

Related registers	01h[1:0]

IP1717 supports an option to transmit a packet with IPG shrank 40PPM, 80PPM, 120PPM to compensate the data accumulation due to TX clock frequency difference between local machine and link partner. This function can be turned on by writing “01” ,“10”, and “11” to register 01h[1:0].

2.2 Aging time

2.2.1 Address aging

Related registers	3Fh, 3Bh[1]

IP1717 supports programmable aging time to meet various system requirement, ranging from 55.3 sec to 1812070.4sec ±3.8%. User can program aging time writing register 3Fh. The address aging function can be disabled by programming register 3Bh[1].

2.2.2 Packet aging

Related registers	39h

IP1717 supports packet aging (output queue aging). If a packet stays in IP1717 longer than output queue aging time defined in register 39h[5:0], IP1717 will drop the packet to improve the efficiency of packet buffer. The packet aging function can be enabled by programming register 39h[7].

2.3 Flow control

2.3.1 IEEE 802.3x

Related registers	B6h~B9h

When operating in full duplex mode, IP1717 supports IEEE802.3x flow control. IP1717 supports symmetric pause and asymmetric pause function. Each port's flow control function can be enabled individually by programming register B6h~B9h. When the packets in buffer reach the threshold, IP1717 generates a "Xon" pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP1717 from overrun. When the packets in buffer lower than threshold, IP1717 generates a "Xoff" pause packet to notify the link partner the receiving buffer is available.
The source MAC of the pause frame is 00:90:c3:00:00:01 if the pause frame comes from IP1717.

2.3.2 Backpressure

Related registers	BAh~BBh, 01h[4:3]

When operating in half duplex mode, the IP1717 supports backpressure flow control. Each port's backpressure function can be enabled individually by programming register BAh~BBh. When the packets in buffer reach the threshold, IP1717 generates a jam pattern to back off the link partner. IP1717 supports the collision based and carrier-based backpressure. When the collision based backpressure is enabled, register 01h[3] set to "0", IP1717 generates a jam pattern only when the link partner is transmitting data and the receiving buffer in IP1717 is not available. When detecting a collision on line, the link partner stops transmission until a back off time expires. When the carrier based backpressure is enabled, register 01h[3] set to "1", IP1717 transmits null packets continuously to prevent link partner's transmission when the buffer is not available.

Flow control off for high priority packets

To prevent the flow control function affects the high priority traffic, each port of IP1717 can turn off flow control function for a period of time automatically when it receiving a high priority packet. This function can be enabled by writing register 01h[7].

2.4 Bandwidth and broadcast storm control

2.4.1 Bandwidth control

Related registers	03h~13h, 01h[6]

IP1717 implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP1717 provides a variety of the bandwidth configuration. It limits the maximum byte counts, which a port can send or receive in a period of time. If the sending byte counts or receiving byte counts of a port reaches a pre-defined threshold, it will stop transmitting or receiving data.

Each port's egress/ingress data rate can be programmed individually. The maximum rate of port0~port 16 are defined in register 03h~13h. The high byte of the registers defines the receive rate and low byte defines transmission rate. Register 01h[6] defines the high /low throttle value using in bandwidth control function. It is note that the once the rate is set, it is independent of the status of link speed and flow control. The detail configuration is shown in the following table.

	Maximum output rate (transmit rate)	Maximum input rate (receive rate)
	Port 0~16	Port 0~16
H/L throttle	Register 03h~13h	Register 03h~13h
01h[6]=0	Bit [7:0] * 32 kbps	Bit [15:8] * 32 kbps
01h[6]=1	Bit [7:0] * 512 kbps	Bit [15:8] * 512 kbps

2.4.2 Broadcast storm control

Related registers	3Dh, 3Eh[0], 3Eh[6:1]

To prevent the broadcast storm, the IP1717 implement a broadcast storm control mechanism. When this function is enabled, a port begins to drop incoming broadcast packets if the received broadcast packet counts reach the threshold defined in register 3Eh[6:1]. Each port's broadcast storm protection function can be enabled individually by programming register 3Dh and 3Eh[0].

2.4.3 Block broadcast packets to CPU

Related registers	3Bh[4], E2h[0]

IP1717 supports an option to block broadcast packets to CPU port. To enable the function, user has to assign port 16 as a CPU port by programming register E2h[0], and then turn on the function by programming register 3Bh[4].

2.5 SS-SMII and MII interface

Related registers	EAh

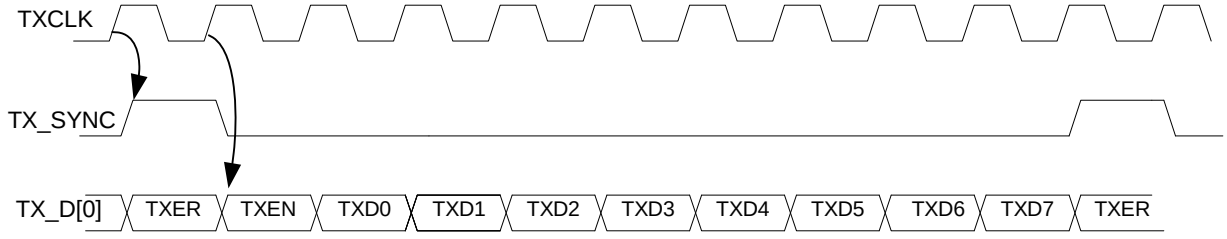
IP1717 supports an option for adjusting SS-SMII timing and output driving current, TXCLK input will be delayed if register EAh[0] is written to 1, RXCLK output will be delay if register EAh[1] is written to 1,and RXSYNC will be delayed if register EAh[2] is written to 1.port8~port16 of IP1717 driving current can be adjust by programming register EAh[4:3]. IP1717 also supports normal and fast for slew rate function by writing register EAh[5].

2.5.1 SS-SMII timing

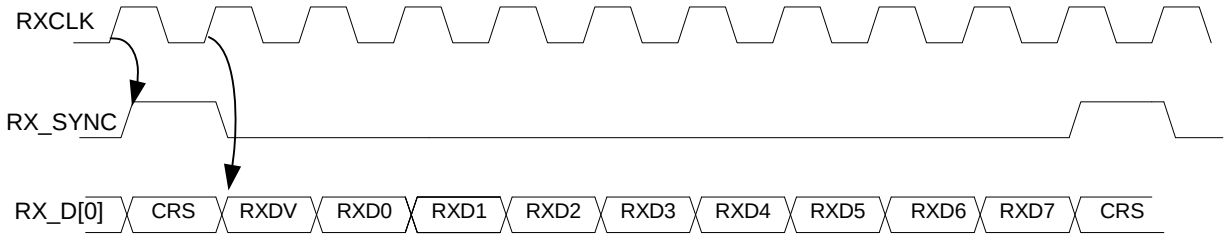
IP1717 sends out data on TX_D at the rising edge of TXCLK and uses TX_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the TX_SYNC, a PHY can capture the correct data stream. A PHY sends out data on RX_D at the rising edge of RXCLK and uses RX_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the RX_SYNC, IP1717 samples the correct data at the rising edge of RXCLK.

Accompanied by the high pulse of TX_SYNC, the TXEN, TX_ER and 8-bit TX data are present on the TX_D pin. For the RX part of SS-SMII, the CRS, RXDV, and 8-bit RX data are present on the RX_D pin.

To fit the timing requirement, the delay on TXCLK and RXCLK can be adjusted by programming register EAh. The driving current can be adjusted by pin DRIVE[1:0] and register EAh.



Transmit SS-SMII



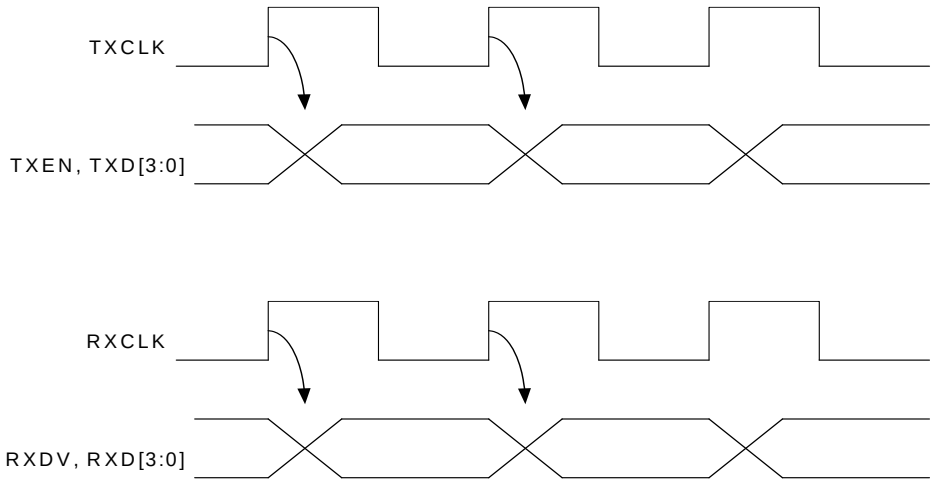
Receive SS-SMII

2.5.2 MII timing

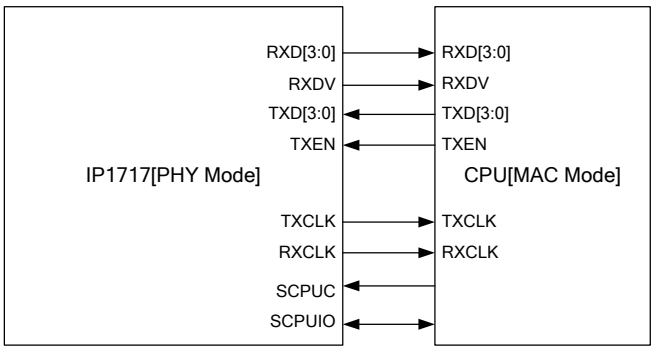
IP1717 sends out data RXDV and RXD[3:0] at the rising edge of RXCLK. By recognizing the RXDV and RXD[3:0], an external CPU can capture the correct data stream.

An external CPU sends out data TXD[3:0] and control signal TXEN at the rising edge of TXCLK. By recognizing the TXEN, TXD[7:0], IP1717 can capture the correct data stream. IP1717 samples the correct data at the rising edge of TXCLK.

MII



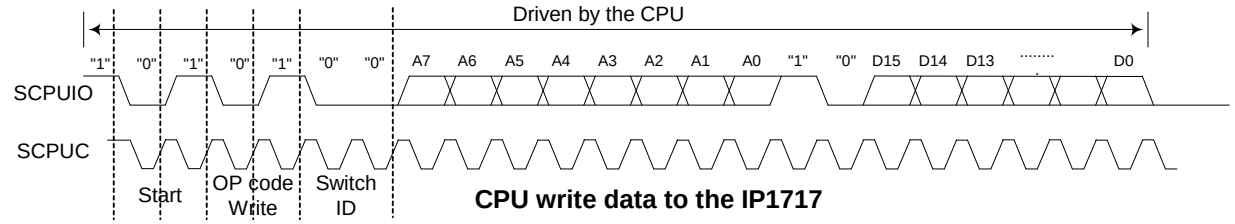
MII



2.6 CPU interface

There is no need to program the register of the IP1717 for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP1717 and the CPU is a serial bus, which comprises a clock and an I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the switch ID, the read/write command, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.



Switch ID is 2'b00 and is fixed

2.7 Configure and access the port status

Related registers	B0h~BBh, C0h~C5h

User can configure the property of each port through CPU I/F. The property of each port can be configured individually. User can set the auto-negotiation, speed, duplex, pause, and backpressure function by writing register B0h~BBh. Besides updating the property of IP1717, it also updates the property of the corresponding PHY through SMI.

User can get the status of a port by reading register C0h~C5h. The registers provide the status of Asymmetric pause function, symmetric pause function, duplex, speed and link of each port.

2.8 MII port force link

Related registers	BDh[6]

User can force MII port (port 16) always link by programming BDh[6]. This function is useful when IP1717 is connected to a PHY, which doesn't support SMI, such that, IP1717 can't get the link status by polling its MII registers. Because IP1717 doesn't receive / transmit a packet from/ to a un-link port, these port don't work. Force link function will solve the problem.

2.9 Read /Write address table(LUT)

Related registers	ACh~AFh

User can access IP1717's MAC address table. The address space is 4K, from 0~4095. To write an entry to the MAC address table, user has to fill the 46-bit data to register ADh-AEh, and AFh[13:0] and then specify the address of the entry and issues a write command by programming register ACh. To read an entry from MAC address table, user has to specify the address of the entry and issues a read command by programming register ACh. The entry can be read from register ADh~AEh, AFh[13:0]. It is note that the bit 14 and 15 of register AFh is not a MAC address; instead it defines the generation method of address of an entry.

Because IP1717 builds and accesses the MAC address table with the address derived with hashing algorithm, user has to calculate the address of an entry in the same way before accessing the table. That is, if direct hashing is selected, the address of an entry is the 12 lsb of a MAC address. If CRC hashing is selected, the address of an entry is the 12 lsb of CRC result of a MAC address. User can use IP1717 hardware to calculate the CRC-hashing address by register AFh.

2.10 CPU read /write PHY registers

Related registers	BEh, BFh

User can access the register of a PHY connected to IP1717 through CPU I/F. To read a register of PHY, user has to specify the address of the PHY, address of the MII register, read command by programming register BEh. The content of the register can be read from register BFh. To write a register of PHY, user has to specify the address of the PHY, address of the MII register, write command, and written data by programming register BEh~BFh.

The associated PHY addresses from port 0 to port 15 are 8~-23. Port 16 default setting is 1.

2.11 CPU read/write EEPROM

Related registers	EBh~ECh

User can access the EEPROM through CPU I/F. To read one byte from EEPROM, user has to specify the byte address, device address, read command by programming register EBh. The data can be read from register ECh. To write one byte to EEPROM through CPU I/F, user has to specify the byte address, device address, write command and written data by programming register EBh~ECh, the data should be written to register ECh, and then execute write command by programming register EBh.

2.12 EEPROM interface

IP1717 provides EEPROM I/F to access 24C016 for dumb and smart applications. After detecting the rising edge of reset input, the IP1717 will start to read the content of EEPROM (acting like an EEPROM master).

The register address of the IP1717 should comply with the address of EEPROM. Being an EEPROM master, the IP1717 downloads the content of EEPROM only if the first two bytes in EEPROM are “1717h”.User can write data to EEPROM by CPU, even if the first word of EEPROM isn’t 1717.

The mapping relationship between the IP1717 registers and the EEPROM address are depicted as the following table.

EEPROM address	EEPROM content	IP1717’s Register
00h	17h	XX
01h	17h	XX
02h	Expected value	01h[15:8]
03h	Expected value	01h[7:0]
04h	Expected value	02h[15:8]
05h	Expected value	02h[7:0]
••••••	••••••	••••••
••••••	••••••	••••••
1D8h	Expected value	ECh[15:8]
1D9h	Expected value	ECh[8:0]

Note:

1. The EEPROM ID should be set to “3’b000”; i.e. A2=0; A1=0; A0=0
2. IP1717 downloads the content of the EEPROM ranging from address 00h to 199h; i.e. the register beyond this range is not recognized by IP1717.

3. The ID for IP1717 recognition should be set at address 00h and address 01h as shown in the table.

2.13 Statistics counters

Related registers	01h[9:8], 34h, 35h[0], 31h~33h

IP1717 supports 34 statistic counters, two counters for one port. These counters are enabled if register 01h[9] is set to 1. User can select the function of counters to be RX packet count, TX packet count, collision count, or CRC error count by programming register 01h[8] and register 34h~35h. Each bit of register 34h and 35h[0] is corresponding to one port individually as shown in the following table.

	The function of counters of a port	
01h[8], one bit of 34h ~ 35h[0]	Counter 0	Counter 1
0,0	Receive packet count	Transmit packet count
0,1	Transmit packet count	Collision count
1,0	Receive packet count	Drop packet count (MAC)
1,1	Receive packet count	CRC error packet count

To read the content of a counter, user has to specify the address of counter in register 31h[5:0] and issue read command by setting register 31h bit 8 and bit 9. Then, user reads the content of the counter by reading register 32h and 33h. The address of counter of each port is shown in the following table.

Address of counter (31h[5:0])	Location of counter
0	Port 0 counter 0
1	Port 0 counter 1
2	Port 1 counter 0
3	Port 1 counter 1
……..	……..
……..	……..
30	Port 15 counter 0
31	Port 15 counter 1
32	Port 16 counter 0
33	Port 16 counter 1

To reset a counter, user can not specify the address of counter, because reset and update commands are global, just only issue reset command by setting register 31h bit 7 and bit 9 . To stop a counter updating, only issue updating stop command by setting register 31h bit 6 and bit 9.

2.14 Interrupt

Related registers	E7h[4:0], E8h[3:0]

IP1717 supports one interrupt pin to indicate status change. When one of the following conditions happen, IP1717 will asserts the interrupt signals depending on active low or high by programming register E7h[4].

Three interrupt events response time from command/event issued:
1. A CPU R/W SMI command is completed (256us)
2. A CPU R/W EEPROM command is completed(128us)
3. Link status changes on PHY of any port(1.5ms)

An interrupt function can be enabled by programming the corresponding bit of register E7h[3:0], the interrupt mask register. User can read register E8h[3:0] to identify the interrupt source.

2.15 LED description

2.15.1 LED Mode Settings

IP1717 also supports either serial or direct LED status streams schemes for port0~7 LED display. The format of LED status driving modes, as shown below, are controlled by LEDMODE[1:0] pins, which are latched upon reset. All LED statuses are represented as active-low under 3 bit and 2 bit serial modes, except Link/Act whose polarity depends on Spd status in bi-color mode or those LED pins whose polarity depends on the initial setting of pin under mono color direct mode.

LEDMODE[1:0]		Mode	Output sequences(pins)
00		3-bit serial stream	Col / Fulldup, Link/Act, Spd
01		2-bit serial stream	Spd, Link/Act
10		3-bit for Bi-color LED	Col / Fulldup, Link/Act, Spd
11		Mono-color LED direct-drive	Col / Fulldup, Link/Act, Spd

LED Indication	Description
Col / Fulldup	Col, Full duplex Indicator. Blinking every 40 or 120ms depends on LED_BLNK_TIME setting when collision happens. Low for full duplex, and high for half duplex mode. The blinking function is disabled in 3-bit bi-color LED mode (LEDMODE[1:0]=10) if pin 106 LED2_BLINK_DIS is set to 1.
Link / Act	Link, Activity Indicator. For 3-bit serial stream mode, low for link established. For 3-bit Bi-color LED mode and 100Mb/s, the Link/Act is high for link established. For 3-bit Bi-color LED mode and 10Mb/s, the Link/Act is low for link established. The LED blinks every 40 or 120ms when the corresponding port is transmitting or receiving.
Spd	Speed Indicator. Low for 100Mb/s, and high for 10Mb/s.

2.15.2 LED blinking setting time

The IP1717 also provides 40/120ms LED blinking time setting through LED_BLNK_TIME pin upon power on reset, The LED's blinking time of the Col/Fulldup and the Link/Act will change according to this pin setting.
For bi-color Link/Act/Spd, the LED blinking time is not affected by LED_BLNK_TIME.

2.15.3 Serial stream sequence

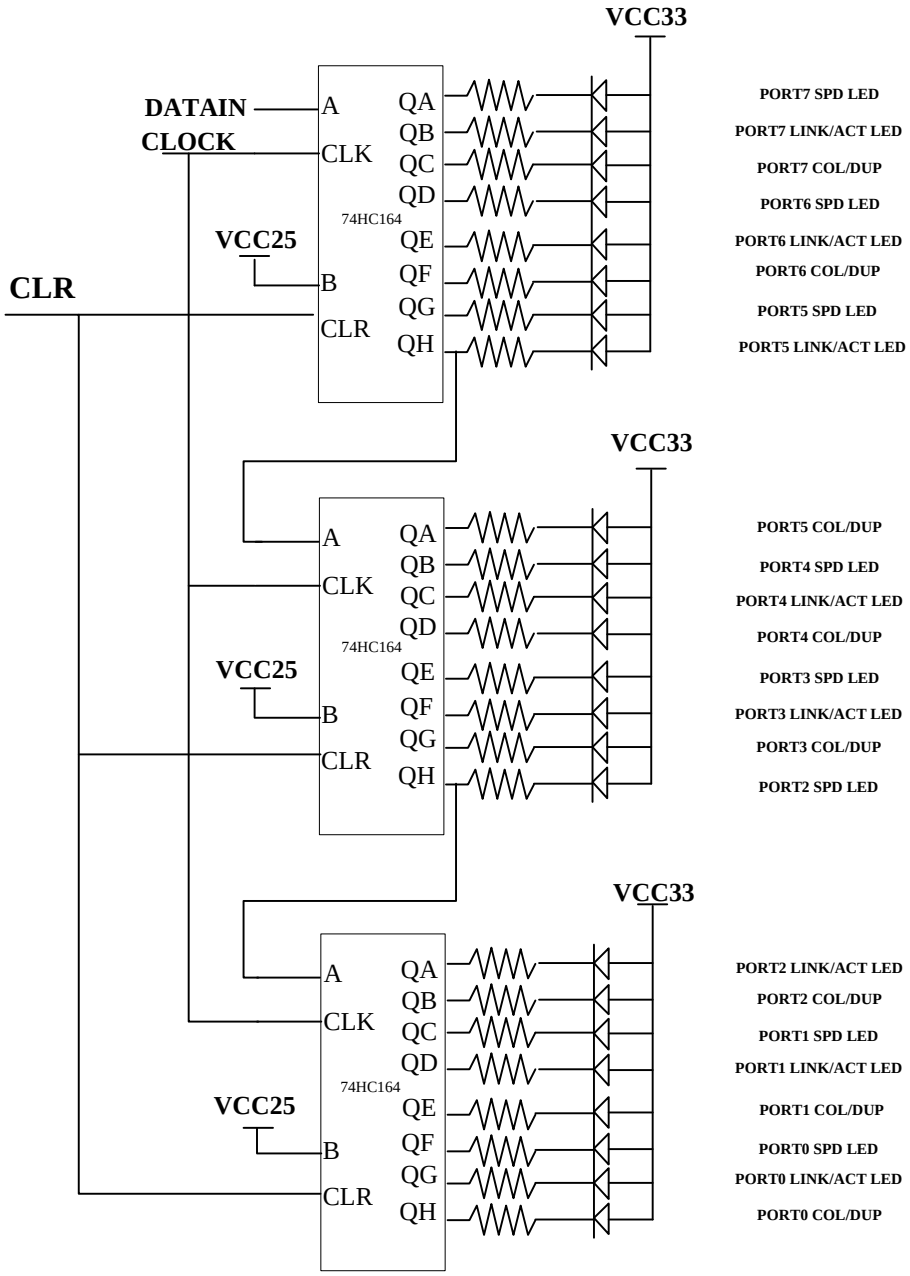
Bits stream are output sequentially from port0 to port7 .For 2-bit serial stream mode, the sequence is Spd at first and then Link/Act. For 3-bit serial stream mode, the sequence is Col/Fulldup, Link/Act, then Spd.

2.15.4 Direct LED mode

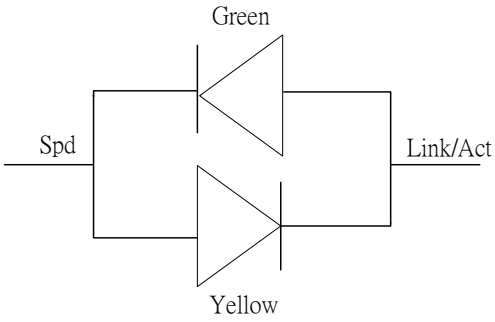
IP1717 also supports direct LED mode by setting LEDMODE[1:0]=11, IP1717 only drive port0~7 link/activity LEDs if MII_PORT_EN is set to high, IP1717 will drive port0~7 link/activity, Spd, duplex LEDs if MII_PORT_EN is set to low. Besides, direct LED mono color and bi color can be selected by DIR_BI_LED pin.

2.15.5 Spd/Duplex LEDs in force mode

When pin 102,103 LEDMODE[1:0] is set in serial LED mode, the bit[11] of the register F0h is used to select LED behavior in force mode. Register F0h[11]=0 means that Spd/Duplex LEDs will be light before link up. Register F0h[11]=1 means Spd/Duplex LEDs will not be light before link up. The default setting of the Register F0h[11] is 0



Exteranl TTL for 3 Bit Serial Stream LED Mode



Bi color configuration

Spd	Link/Act	LED indication	Bi-color state
0	0	10Mbps without link	None
1	1	100Mbps without link	None
0	1	100Mbps and Link	Green
1	0	10Mbps and Link	Yellow

2.15.6 Advanced power saving mode

IP1717 will enter advanced power saving(APS) mode during port is unlink state if MII register 16h[7]=1, IP1717's maximum system power consumption is about 4.27w basing on 16 ports are active state, IP1717's minimum system power consumption is about 0.98w on unlink state. Power saving percentage is about 77%.

APS mode

		IP1717 system	
Status		Link/Act	
Speed/Operating ports		Watt	**Saving**
100M Full	0	0.98	77%
	4	1.73	59%
	8	2.56	40%
	12	3.39	20%
	16	4.27	0%

Saving percentage based on 16 ports power consumption

2.16 VLAN configuration

2.16.1 Port based VLAN

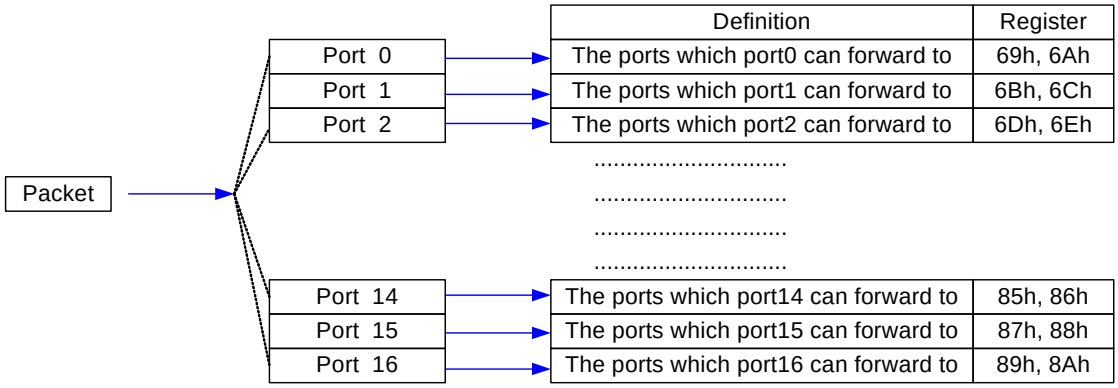
Related registers	69h~8Ah, 3Bh[6]

IP1717 supports port based VLAN and tag based VLAN..

The IP1717 provides various port based VLAN configurations. User can enable the function by writing 0 to register 3Bh bit 6. Each port uses two registers to describe its port base VLAN configuration. That is, a set of ports allowed to be forwarded from the source port. The overall number of VLAN groups that the IP1717 can support is 17. Thus, the registers, which define the port based VLAN are from 69h to 8Ah.

Take the following example for the detailed description. The data incoming from port 0 will be forwarded to the corresponding port defined in register 69h and 6Ah. For example, if register 69h and 6Ah are written with “000F” and “0001”, the packet from port 0 can be forwarded to port 16 and port 1~3 only. Similarly, the forwarding rule for the data incoming from port 1 will refer to the register 6Bh and 6Ch. The forwarding rule for the data incoming from port 1 will refer to the register 89h and 8Ah.

Note: The port ID is counted from 0 to 16.



2.16.2 Tag based VLAN

Related registers	4Fh~54h, 55h~68h, 69h~90h, 3Bh[6]

Tag based VLAN for port based
IP1717 supports a 20-entry VLAN table, VID table entry 0~19, to provide 20 active VLANs out of 4096 VLANs defined in IEEE802.1Q. User can define 20 VID entries in the VID table and enable the tag VLAN function by programming register 55h~68h and register 3Bh bit 6. When a tagged packet is received, IP1717 compares the VID field in the packet with the ones defined in the VID table. If it is not matched, IP1717 drops the packet. If it is matched, IP1717 uses the corresponding index to select one of the 20-entry in the VLAN table, defined in register 69h~90h, as an output port mask. That is, a set of ports, to which the packet can be forwarded to. IP1717 forwards the packet according to MAC address and the output port mask. If the source port is not one of the members in the VLAN table entry, IP1717 drops the packet. It is note that register 69h~ 8Ah define port base VLAN configuration and tag based VLAN table entry.

When an un-tagged packet is received, IP1717 uses the default PVID for the source port as index to the VID of the packet. The default PVID index of a port is defined in the register 4Fh~54h. IP1717 forwards the packet in the same way as mentioned above. For example, if port 0 receives an un-tag packet, IP1717 adopts the PVID index of port 0 defined in register 4Fh to select one of the VLAN table defined in register 69h~90h. A tagged packet with VID equal to “000” is handled as an un-tagged packet.

Tag based VLAN for VID based
IP1717 also support tag based VLAN based on VID, which can be configured by programming register 91h-A4h,it provides more flexible for tag based VLAN setting, for example, if untagged port will add tag with VID=1 from port 0 and register 91h by writing 000f, just only port2-4 of output ports will be added tag with VID=1, the other ports will not added tag.

2.16.3 Add/Remove/Modify Tag

Related registers	4Bh~4Eh, 4Fh~54h, 55h~68h

IP1717 inserts or removes a tag of a frame if tagging/ un-tagging function is enabled. Tagging function of a port is enabled if the corresponding bit in register 4B and 4C is set. A tag port always adds a tag to a forwarded packet with the VID selected by PVID. The tag information VID is defined in register 55h~68h and the PVID for each source port is defined in register 4Fh~54h. A packet with VID equal to 12’b0 will be handled as un-tag frame. Un-tagging function of a port is enabled if the corresponding bit in register 4Dh and 4Eh is set. A un-tag port always removes a tag from a forwarded packet. The operation is illustrated as follows. It is note that the VID defined in register 55h~68h for tagging is also used for 802.1Q tag based VLAN.

Frame type of the received packet	The operation of a port which forwards the packet	
	Forward to a untagged filed	Forward to a tagged field
Untagged	Forward the packet without modification	1. Insert a tag using the default VLAN tag value of the source port 2. Calculate new CRC 3. The default VLAN tag value is defined in the register 55h~68h.

Priority-tagged (VLAN ID=0)	1. Strip tag 2. Calculate new CRC	1. Keep priority field. 2. Replace the tag with the default VLAN tag value of the source port 3. Calculate new CRC 4. The default VLAN tag value is defined in the register 55h~68h.
VLAN-tagged	1. Strip tag 2. Calculate new CRC	Forward the packet without modification

2.16.4 Packet across a VLAN

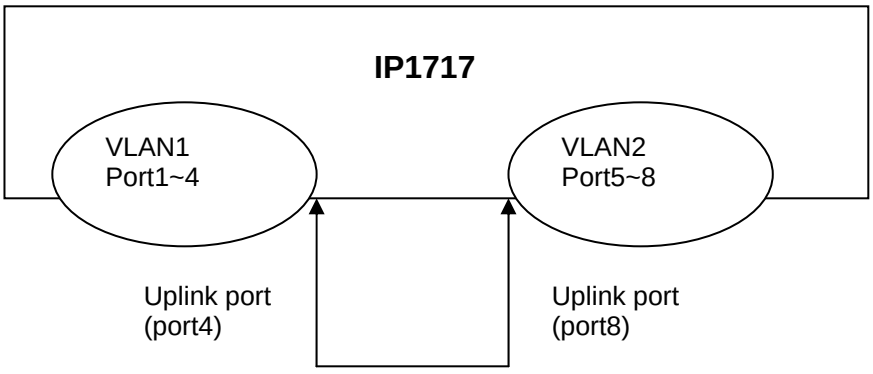
Related registers	3Bh[7]

Usually, a packet is not allowed to be forwarded across a VLAN. That is, if the destination port does not belong to the same VLAN, the packet is dropped. IP1717 provides an option to allow uni-cast packets to stride across a VLAN. This function is enabled by set bit 7 of register 3Bh.

2.16.5 VLAN up link

Related registers	3Bh[8], 44h, 45h

In normal operation, if destination and source are in different VLAN, the packet will be dropped.
IP1717 supports an option to forward the packets filtered by this condition to up-link ports in the same VLAN group if register 3Bh bit 8 is set to “1”, the up-link ports are defined in register 44h and 45h.
For example:
VLAN1: port1~4 and uplink port is port4, if packets come from port1~3 and the packets will forward to port4. VLAN2: port5~8 and uplink port is port8, if packets come from port5~7 and the packets will forward to port8.



2.17 Class of service

2.17.1 Output queue with scheduling priority

Relate registers	38h, 01h[7]

IP1717 implements 4 levels of priority queues, high priority and low priority. The priority for each packet is based on the following schemes:

1. Physical port
2. 802.1Q VLAN tag
3. IP TOS/DS
4. TCP/UDP port number

Each incoming packet is mapped to either a high priority queue or a low priority queue. When no COS function is enabled, the first-in/ first-out forwarding method is used. The weight function, for the ratio of high/low priority, the 3 bits of queue3~0 are set to 000 means WRR ratio =8, set to 001 means WRR ratio=1, …. set to 111 means WRR ratio= 7, is defined in register 38h.

In IP1717, the 4 kinds of COS have priority. TCP > IP > Tag > Port. Remember that IP1717 has 4 Queues.

IP1717 provides an option to pause flow control function to prevent the extra delay for a high priority packet. A port's flow control function is disabled for 1.5s automatically when it receives a high priority packet. This function can be enabled by writing "1" to register 01h[7].

2.17.2 Port base COS

Related registers	14h~16h.

The port-based priority only concerns the physical port location in a switch. A packet received by a high priority port is handled as a high priority packet. Each port of IP1717 can be configured as a high priority port individually by programming register 14h~16h. For example, the bit [1:0] of register 14h corresponds to port 0 and the bit [1:0] of register 15h corresponds to port 8.

2.17.3 802.1Q priority tag based COS

Related registers	17h~18h

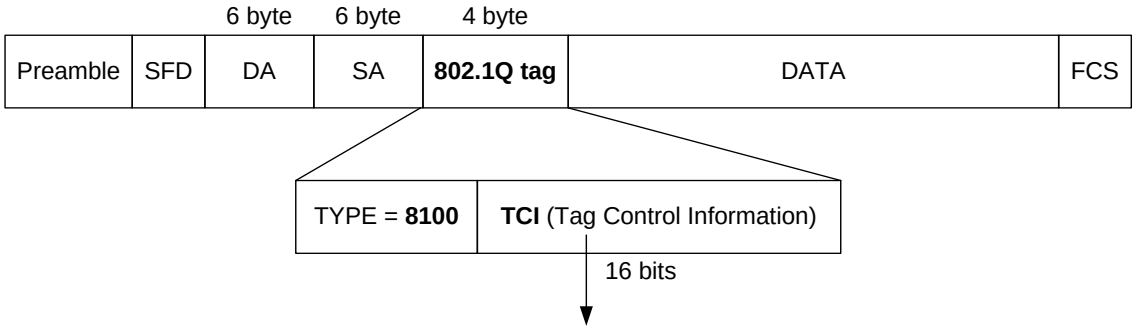
When the COS for 802.1Q VLAN tag is enabled, the IP1717 will examine the 3 bits of priority field carried by a VLAN tag and map it to the corresponding priority.

For 4 queue mode:
Priority (111,110)→queue3;
Priority (101,100)→queue2;
Priority (011,000)→queue1;
Priority (010,001)→queue0.

For 2 queue mode:
Priority (111,110,101,100,011,000)→queue1;
Priority (010,001)→queue0.

The Tag priority is following the 802.1Q 2003 Edition Table 8-2. Please refer this document. The COS function of each port can be enabled individually by programming register 17h and 18h. For example, the bit 0 of register 17h corresponds to port 0 and the bit 0 of register 18h corresponds to port 16.

802.1Q priority tag based CoS



Bit[15:13]: Priority
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.

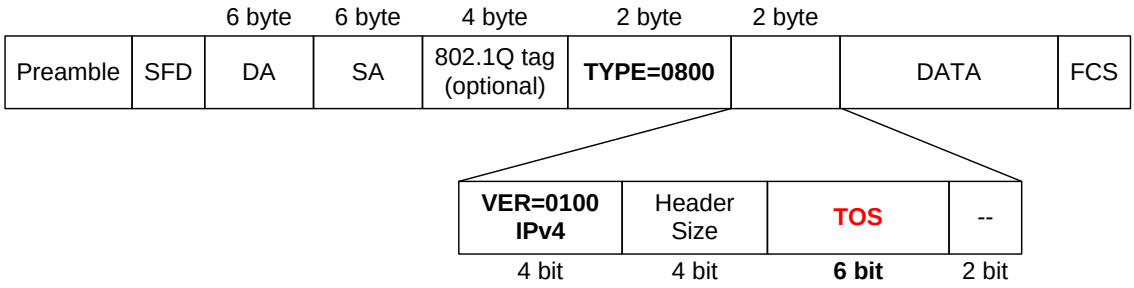
2.17.4 IP TOS based COS

Related registers	19h~1Bh

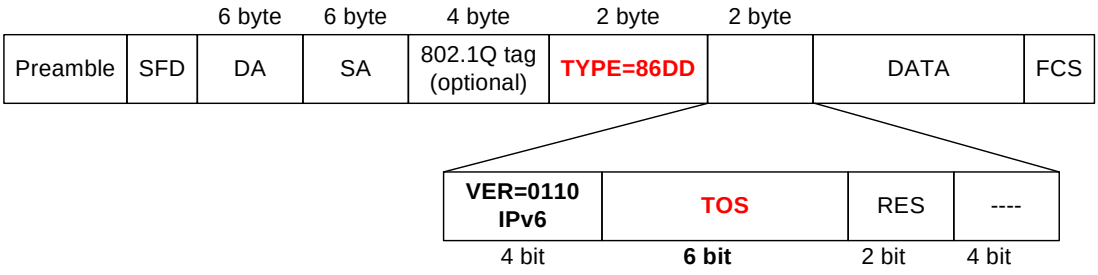
IP1717 provides the IP layer COS function by recognizing the priority octet and mapping it to the corresponding priority. For an IPv4 packet, it is embedded in the TOS (type of Service) Octet. For an IPv6 data packet, the Traffic Class is used to differentiate the Class of Service. When this function is enabled, the IP1717 will automatically recognize the IP version and capture the either the TOS field (IPv4) or Traffic Class field (IPv6).The priority settings are defined in register 1Bh.

According to the priority setting of register 1Bh, the IPv4/v6 packets can be forwarded to queue0, queue1, queue2 or queue3 if WRR function is enabled and the TOS field of the IPv4/v6 packets are set as b'001010, b'010010, b'011010, b'100010, b'101110, b'110000, b'111000, others will be forwarded to queue0. There are only two queues active in strictly priority mode, queue1and queue0, queue1 is for high priority and queue0 is for low priority.

IPv4 frame format



IPv6 frame format



The IP TOS/DS priority function of each port can be enabled individually by programming register 19h and 1Ah. For example, the bit 0 of register 19h corresponds to port 0 and the bit 0 of register 1Ah corresponds to port 16.

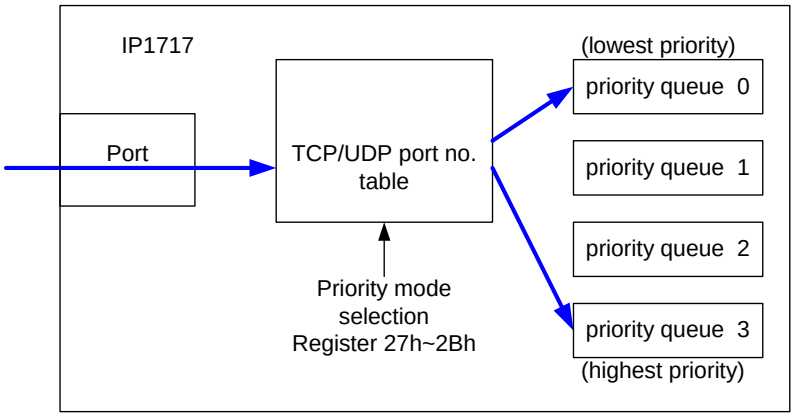
2.17.5 TCP/UDP port number based COS

Related registers	1Fh~2Bh

The COS based on TCP/UDP port number priority function will be enabled by programming register 25h and 26h. For example, the bit 0 of register 25h corresponds to port 0, and bit 0 of register 26h corresponds to port 16. IP1717 will examine the TCP/UDP destination port number in a packet to decide its priority.

User can define the priority of protocols, based on TCP/UDP port number; by programming register 27h~2Bh. A packet with TCP/UDP port number matched that listed in register 27h~2Bh will be treated as a high/low priority packet according to the corresponding setting in the registers. For example, a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a high priority packet if register 27h[2:0] is not set to “000. A packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a low priority packet if register 27h[2:0] is set to “000”. A packet with TCP/UDP port number equal to 20 or 21 (FTP) will be forwarded to CPU port if register 27h[2:0] is set to “100”. A packet with TCP/UDP port number equal to 20 or 21 (FTP) will be dropped if register 27h[2:0] is set to “101”.The priority of the TCP/UDP port number will override the priority of the user-defined port number if the priority of FTP (20, 21) is set to low and the priority of the port number (1~21) is set to high for user-defined setting, the priority of port number (20,21) will be treated as low priority rather than high priority.

A packet with TCP/UDP port number matched the user-defined port number range which defined in register 1Fh~24h will be treated as a high/low priority packet according to the setting in the register 2Bh[8:0]. For example, a packet with TCP/UDP port number matched the one defined in the register 1Fh and 20h will be handled as a high priority packet if register 2B[2:0] is set to “011”. IP1717 provides three groups for user define port number range.



2.18 Capture Ethernet protocol frame and IP packet to CPU port

IP1717 recognizes the following type of packets by examining the field listed in the following table.

	DA	Type	Protocol no. In IP Header	Port no. In UDP header	Note
In-band management	1717’s MAC address	--	--	--	Global setting
BPDU	01-80-C2-00-00-**00**	--	--	--	Global setting
LACP	01-80-C2-00-00-**02**	--	--	--	Global setting
802.1X	01-80-C2-00-00-**03**	888E	--	--	Global setting
GVRP, GMRP	01-80-C2-00-00-**20~21**	--	--	--	Global setting

OSPF	--	0800	89	--	Global setting
ARP	--	0806	--	--	Global setting
ICMP		0800	01	--	Global setting
IGMP	01-00-5E-XX-XX-XX	0800	02	--	Global setting
TCP	--	0800	06	--	Global setting
UDP	--	0800	17	--	Global setting

Note:
1. “--“ means don’t care.
2. Pause frame is not forwarded to CPU.

2.18.1 In band management frame

Related registers	02h[0], E2h[0], 2Eh~30h

IP1717 has a default MAC address 00-90-c3-00-00-01. If an incoming packet with DA equal to IP1717's MAC address will be dropped if register 02h[0] is set to "0" or forwarded to CPU port if register 02h[0] is set to "1" and register E2h[0] is set to "1". IP1717's MAC address can be updated by programming register 2Eh~30h.

2.18.2 ARP 802.1X

Related registers	1Eh, 02h[2], 02h[5]

A port only forwards ARP and 802.1X EAPOL frames and drops other packets if the corresponding bit in register 1Eh is set to "1" and 02h[2] is set "1", too. A port resumes to normal operation if the corresponding bits are cleared. Please refer to section 4.5.2 802.1X port based security for more detail information.

Besides forwarding ARP to its destination port, IP1717 can forward an ARP to CPU port if register 02h[5] is set to "1'.

2.18.3 BPDU, LACP, GVRP, GMRP

Related registers	01h[2],02h[4:1],E2h[0]

IP1717 recognizes an incoming BPDU, LACP, GVRP and GMRP packet and decides to forward it to CPU only or drop it according to the setting in register 02h[1], 01h[2] and 02h[4:3]. Register E2h[0] defines port 16 to be CPU port.

Protocol	GVRP, GMRP	GVRP, GMRP	LACP	LACP
Register	02h[4]=0 E2h[0]=1	02h[4]=1 E2h[0]=1	E2h[0]=1 02h[3]=0	E2h[0]=1 02h[3]=1
Behavior	Broadcast	To CPU port	Drop	To CPU port

Protocol	BPDU 01-80-C2-00-00-00	BPDU 01-80-C2-00-00-00	BPDU 01-80-C2-00-00-00
Register	01h[2]=1 02h[2]=1 E2h[0]=1	01h[2]=0 02h[1]=0 E2h[0]=1	01h[2]=0 02h[1]=1 E2h[0]=1
Behavior	Broadcast	Drop	To CPU port

Protocol	01-80-C2-00-00-03	01-80-C2-00-00-03	01-80-C2-00-00-03
Register	01h[2]=1	01h[2]=0 02h[2]=0 E2h[0]=1	01h[2]=0 02h[1]=1 E2h[0]=1
Behavior	Broadcast	Drop	To CPU port

2.18.4 ICMP TCP, UDP, OSPF

Related registers	02h[13:6], E2h[0]

IP1717 recognizes an incoming ICMP, TCP, UDP, and OSPF packet and decides to forward it to CPU, too or drop it according to the setting in register 02h[13:6]. Register E2h[0] defines port 16 to be CPU port.

Register 02h

bit	13:12	11:10	9:8	7:6
Protocol	OSPF	UDP	TCP	ICMP
definition	00: Send to its destination port. 01: Send to CPU port and its destination port. 10: Send to CPU port only. 11: drop			

2.18.5 The other IPV4

IP1717 handles the other IPv4 protocols not mentioned above according to the setting of 02h[15:14].

bit	02h[15:14]
Protocol	Other prorocols of IPv4
definition	00: Send to its destination port. 01: Send to CPU port and its destination port. 10: Send to CPU port only. 11: drop

2.18.6 Block broadcast packet to CPU

All broadcast frames will be inhibited to forwarded to CPU port except for broadcast packets with ARP protocol if register 3Bh[4] is set to “1”. When this function is enabled, IPv4 can be still forwarded to CPU port, if register 3Bh[5] is set to “1”.

2.19 Security

2.19.1 MAC address based security

Related registers	43h[2:0], 40h

IP1717 supports MAC address based security function if register 43h[1] is written with “0”. When the function is enabled, IP1717 drops the packet with a SA not found in the address table. This function is valid only if the address learning function is disabled by programming register 40h.
IP1717 provides an option to forward the un-known SA packets to CPU when the function is enabled. An un-known SA packet is forwarded to CPU, if bit 0 of register 43h is cleared.
IP1717 also supports SA associated with source port if register 43h[2] is set to 1, for example, if packets with specific SA send from Port 0, if change to port1, the packets will not be forwarded. The Packets with specific SA can send from any port if register 43h[2] is set to 0.

2.19.2 802.1X port based security

Related registers	02h[0] 02h[2], 1Eh E2h[0]

IP1717 supports 802.1X based security function. If the function is enabled, IP1717 only forwards 802.1X EAPOL packets (DA=01 80 C2 00 00 03 and packet type=88 8E or DA= switch's MAC address, packet type=88 8E and 02[0]=1) to CPU port and drops other types of packets. ARP packets are not affected by the function and are forwarded according to their destination address. This function can be enabled for each port individually by programming register 1Eh. User has to write "1" to register 02h[2] to enable 802.1X security function. If register 02h[2] is written with '0", all EAPOL packets will be dropped or broadcast depending on 01h[2].

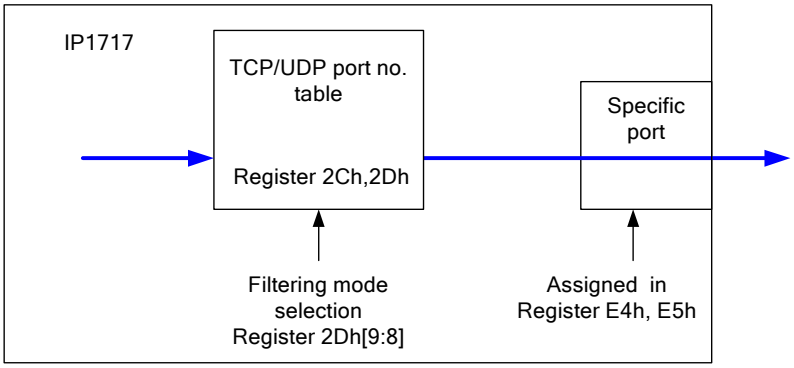
2.19.3 Specific port filtering

Related registers	2Ch, 2Dh, E4h, E5h, 1Fh~24h

IP1717 supports a function to enable/disable a specific port to send out packets with specific TCP/UDP port number. Each port can be configured to be a specific port individually by programming register E4h and E5h. When the function is enabled (2Dh[9]=1), IP1717 forwards or drops a packet with TCP/UDP port number, defined in register 2Ch and 2Dh, to specific port, defined in register E4h and E5h, according to the setting of 2Dh[8].

If user defined TCP/UDP port number is selected, 2Dh[6:4], IP1717 handles packets according to the TCP/UDP port number defined in register 1Fh~24h.

For example, a packet with TCP/UDP port number in the range defined in the register 1Fh and 20h will be dropped by a filtering port, if register 2Dh bit 8 and bit 4 are set to "01". A packet with TCP/UDP port number in the range defined in the register 23h and 24h will be sent by a filtering port, if register 2Dh bit 8 and bit 6 are set to "11".



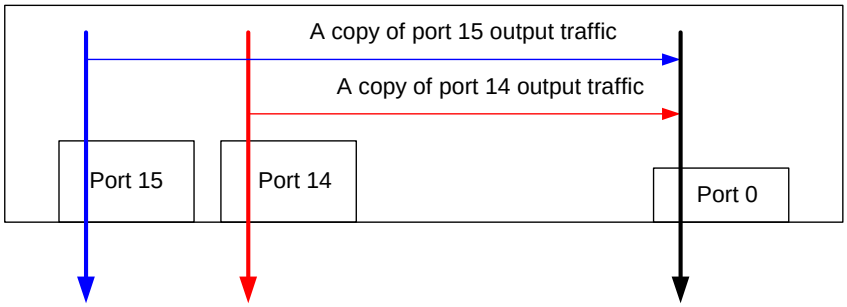
2.19.4 Port mirror security

Related registers	47h ~ 4Ah, 3Bh[11:10].

In some circumstances, the network administrator requires to monitor the network status. The port mirroring function helps the network administrator diagnose the network.

A port mirroring function is accomplished by assigning monitored ports (source ports), snooping ports (destination ports) and snooping method. IP1717 will copy the traffic of monitored ports to all snooping ports. That is, the snooped packets for all snooping ports are the same. The IP1717 supports three kinds of mirroring methods: the ingress, the egress and ingress plus egress. It is defined in register 3Bh[11:10]. Registers 49h and 4Ah define the ports to be monitored (mirroring source). Register 47h and 48h specifies the ports to snoop (mirroring destination).

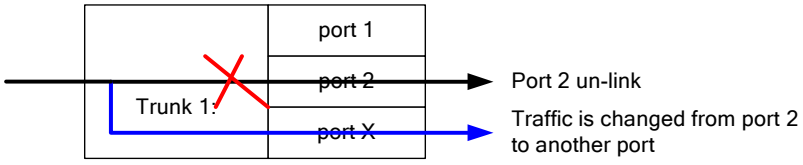
For example, if user wants to monitor the output traffic of port 14 and port 15 to port 0 as shown in the following figure. He has to write “01” to register 3Bh[11:10] to choose monitor method to be output traffic, write C000h and 0000h to register 49h and 4Ah to select port 14 and 15 to be monitored ports, write 0001h and 0000h to register 47h and 48h to select port 0 as a monitoring port. IP1717 will copy the traffic out of port 14 and port 15 to port 0.



2.20 Trunk channel

2.20.1 Trunk channel behavior

IP1717 supports 2 trunk channels consisting of port 0~3, and port 4~7. Each trunk channel may comprise 2 to 4 ports. User can configure the trunk channel individually by writing non-zero values to the corresponding bits of a port in the register 46h. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP1717 forwards the packet to the other port of the trunk.



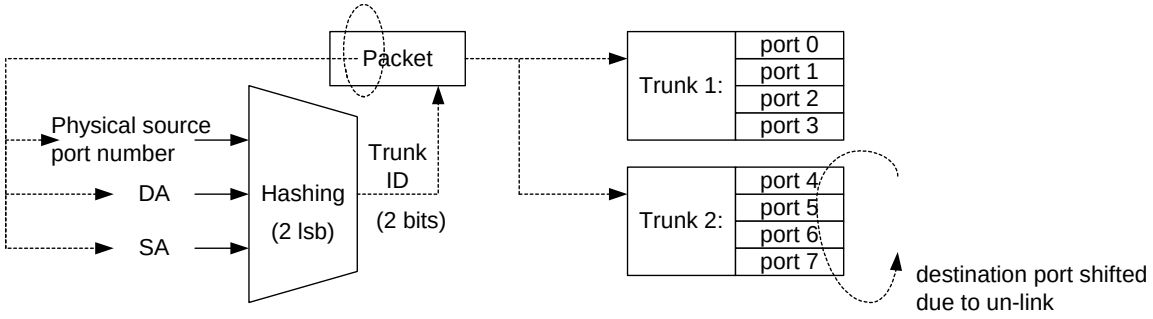
For example:

Trunk0 group consists of port2~3 if register 46h[15:0]=000c, trunk1group consists of port4~5 if register 46h[15:0]=0030.

2.20.2 Load balance

To fully utilize the bandwidth in a trunk channel, IP1717 supports load balance function. A physical port of a trunk forwards a packet only if the trunk ID of the packet matches the ID setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk ID.

IP1717 performs a hashing algorithm to calculate a 2-bit trunk ID of a packet basing on register 3Bh[3:2]. It is used to select one of the trunk ports to forward packets. If the destination port of a trunk is un-link, the packet will be forward another port of the same trunk.

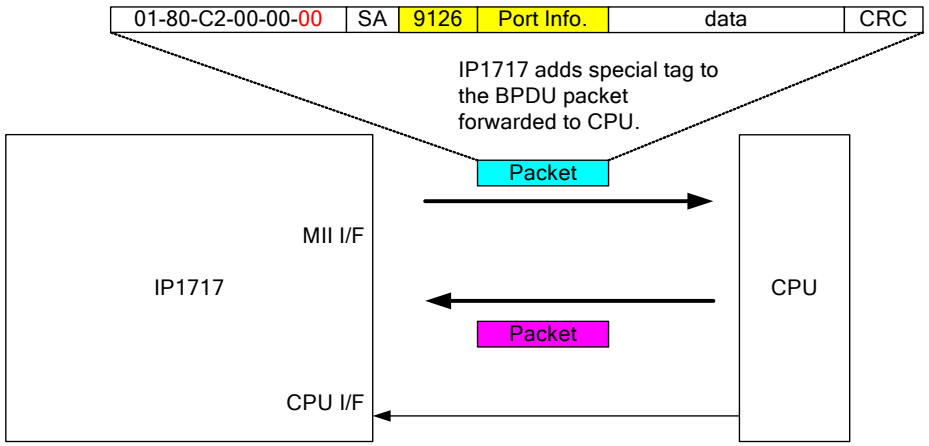


2.21 Spanning tree function

2.21.1 BPDU packet forwarding

Related registers	01h[2], 02h[1], E2h[1:0], 41h, 42h

IP1717 supports spanning tree function with the following features:
1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU and add special tag for source port information. The function is enabled by writing “1” to register 02h[1], “0” to register 01h[2] and “11” to register E2h[1:0].
3. CPU write 41h, 42h to set the spanning tree port state for each port.



2.21.2 Spanning tree setting

Related registers	01h[2],02h[1], E2h[0],41h, 42h

To support IEEE802.1D spanning tree protocol, each port of IP1717 supports four states defined in IEEE802.1D IP1717 not support listening state in 802.1D, states of spanning tree can be set by register 41h and 42h, for example, ports of IP1717 will be set to disabled state if the corresponding bit of register 41h and 42h are written to 00, ports of IP1717 will be set to blocking state if the corresponding bit of register 41h and 42h are written to 01, ports of IP1717 will be set to learning state if the corresponding bit of register 41h and 42h are written to 10, ports of IP1717 will be set to forwarding state if the corresponding bit of register 41h and 42h are written to 11.

	Disable state	Blocking state	Learning state	Forwarding state
corresponding bit of register 41h	0	1	0	1
corresponding bit of register 42h	0	0	1	1

2.22 Non association port

Related registers	A9h

IP1717 provide an option to support non association port function, these ports will not receive packets from each other if the function is enabled, even if the ports belong to same VLAN. The non association port can be set by writing register A9H, for example, port 0 and 15 of IP1717 will not be forwarded packets to each other if register A9h[15:0] is written to 8001.

2.23 Aging flush

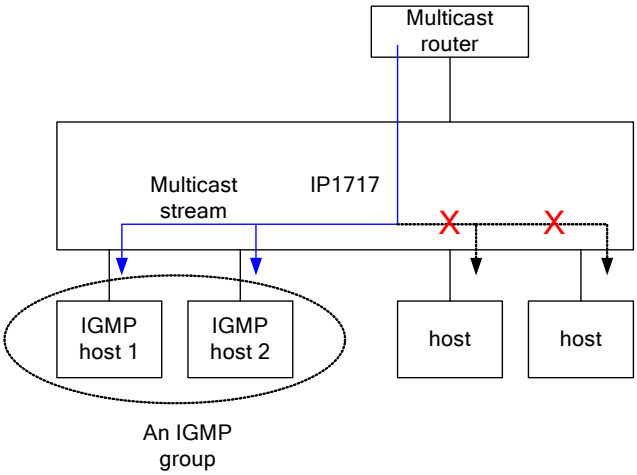
Related registers	ABh

IP1717 supports port based aging out individually, the aging port will be age out until learning again, the aging port can be set by writing register ABH. For example, port of IP1717 will be aged out if the register ABh[0] by writing to one, until learning again and read zero from register ABh[0].

2.24 IGMP snooping

Related registers	A5h

For a switch without IGMP snooping, a multicast packet is forwarded to all ports, that is, it is treated as a broadcast packet. With IGMP snooping, a multicast packet of a group is only forwarded to ports that are members of that group. IGMP (Internet Group Management Protocol) is used to establish membership in a Multicast group. It significantly reduces multicast traffic in a switch.

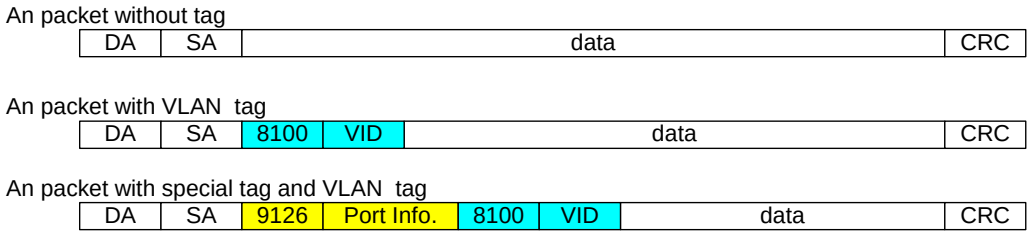


2.25 Special tag

Related registers	E2h,E3h

The special tag is inserted into packet and then the packet is identified by CPU port if register E2h[1:0]=3, the default setting of the special tag is 9126, which can be configured by writing register E3h[15:0].
The port information is followed with special tag. The port information of the packet is added by source port if the source port is port0, the port information is 0, and so on. Special tag is two bytes length and Port information is two bytes length.

Special tag format:



3 Register description

3.1 IP1717 switch register description

R = Read; W = Write; R/W = Read/Write; R/C: clear after reading

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
MAC control register				
01H	02H 03H	General MAC operation behavior Bit [1:0]: enable IPG compensation 00:disable IPG compensation 01:compensation 40 PPM 10:compensation 80 PPM 11compensation 120PPM Bit [2]: broadcast all BPDU packets (MAC address=0x0180C2000004~0x0180C200000F) But (0X0180C2000000/0X0180C2000003 must also ref 0x02[1]) Bit [3]: Back pressure method 0:Collision base 1:Carrier Sense base Bit [4]: Collision 16 times drop enable 0: not drop packet if exceed collision 16 times(default) 1: drop packet if exceed collision 16 times Bit [5]: Collision back off enable 0: collision back off is disabled 1:collision back off is enabled Bit [6]: High/Low bandwidth throttle select 0:32 kbps unit for low bandwidth 1:512 kbps unit for high bandwidth Bit [7]: Auto turn off flow control function if priority queue enable 0: the flow control will not be closed if packet is high priority 1: the flow control will automatically closed if packet is high priority Bit [8]: Port statistic counter method (ref. To 34H&35H) Bit [9]: Port statistic counter enable (ref. To 34H&35H) 0: port stats counter is disabled 1: port stats counter is enabled	R/W	16'h0021
02H	04H 05H	Ethernet protocol frames capture Bit [0]: In-band management (Destination MAC address = switch MAC address) 1:to CPU port 0:Drop (Switch MAC address define in offset address 0x2E, 2F, 30) Bit [1]: Spanning tree 0:Drop 1:to CPU port Drop or to CPU port will be effected only if broadcast BPDU packets are disabled Bit [2]: 802.1X protocol enable 0:Drop or broadcast based on broadcast BPDU packets are disabled or enabled 1:to CPU port only if broadcast BPDU packets are	R/W	16'h0001

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		disabled Bit [3]: LACP 0:Drop 1:Send to port 16 (CPU) only Bit [4]: GxRP 0:Broadcast 1:Send to port 16 (CPU) only Bit [5]: Reserved IP packet capture Bit [7:6]: ICMP Bit [9:8]: TCP Bit [11:10]: UDP Bit [13:12]:OSPF Bit [15:14]:IPv4 Other protocol, 00:Send to ports only 01:Send to port 16 (CPU) and ports 10:Send to port 16 (CPU) only 11:Drop IP1717 supports 4 options to capture IP packets to meet user's requirement 0x0180c2000003: 0x02[2] = 1, only to CPU 0x02[2] = 0, if Bit[2] = 1→ broadcast 0→drop		
03H~ 13H	06H~ 27H	Egress/Ingress Rate control Bit [7:0]: Output Rate control Bit [15:8]: Input Rate control The max. Input/Output rate =Rate control x 32 kbps (low bandwidth) =Rate control x 512 kbps(high bandwidth)	R/W	16'h0000
14H	28H 29H	Port base priority enable for port7~port00, 2 bit per port Ex: Bit [1:0]: port base priority setting for port 1 00 - to queue 0 (lowest priority) 01 - to queue 1 10 - to queue 2 11 - to queue 3 (highest priority) IP1717 provides 2 queues (low& high priority) and 4 queues (lowest priority~ highest priority)	R/W	16'h0000
15H	2AH 2BH	Port base priority enable for port15~port8, 2 bit per port	R/W	16'h0000
16H	2CH 2DH	Port base priority enable for port16	R/W	16'h0000
17H	2EH	VLAN Tag base priority enable for port15~port0, 1 bit per port	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
	2FH	Bit [15:0]: 0: disable 1: enable		
18H	30H 31H	VLAN Tag base priority enable for port16 Bit [0]: 0: disable(no tag priority) 1: enable(tag priority based on priority mapping table for 2 queues or 4 queues)	R/W	16'h0000
19H	32H 33H	IP COS base priority enable for port15~port0, 1 bit per port Bit [15:0]: 0: disable 1: enable If enable, the QoS of the packets into the enabled ports will also refer register 1BH settings.	R/W	16'h0000
1AH	34H 35H	IP COS base priority enable for port16 Bit [0]: 0: disable 1: enable	R/W	16'h0000
1BH	36H 37H	Differentiated Services (DS) priority setting Bit [1:0]: priority setting for CODEPOINT 6'b001010 Bit [3:2]: priority setting for CODEPOINT 6'b010010 Bit [5:4]: priority setting for CODEPOINT 6'b011010 Bit [7:6]: priority setting for CODEPOINT 6'b100010 Bit [9:8]: priority setting for CODEPOINT 6'b101110 Bit [11:10]: priority setting for CODEPOINT 6'b110000 Bit [13:12]: priority setting for CODEPOINT 6'b111000 Note: If the CODEPOINT is not defined above, it treat as priority "0"	R/W	16'h0000
1CH	38H 39H	Port receive enable for port15~port0, 1 bit per port Bit [15:0]: 0:disable(not receive packets) 1:enable(receive packets)	R/W	16'hFFFF
1DH	3AH 3BH	Port receive enable for port16 Bit [0]: 0:disable 1:enable	R/W	16'h0001
1EH	3CH 3DH	802.1X port lock enable (port 15~port0) Bit [15:0]: 0:normal operation (authorized state) 1:drop all frames except ARP & 802.1X EAPOL packets (unauthorized state)	R/W	16'h0000
1FH	3EH 3FH	User define TCP/UDP port number A upper ranger setting	R/W	16'h0000
20H	40H 41H	User define TCP/UDP port number A lower ranger setting IP1717 will check if the port number A in the following range lower ranger $\leqq$ port number A $\leqq$ upper ranger	R/W	16'h0000
21H	42H 43H	User define TCP/UDP port number B upper ranger setting	R/W	16'h0000
22H	44H 45H	User define TCP/UDP port number B lower ranger setting IP1717 will check if the port number B in the following range lower ranger $\leqq$ port number B $\leqq$ upper ranger	R/W	16'h0000
23H	46H 47H	User define TCP/UDP port number C upper ranger setting	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description		R/W	Default value
24H	48H 49H	User define TCP/UDP port number C lower ranger setting IP1717 will check if the port number C in the following range lower ranger ≦ port number C ≦ upper ranger		R/W	16'h0000
25H	4AH 4BH	TCP/UDP port number base priority for p15~p0, 1 bit per port Bit [15:0]: 0:disable(port number base priority will be disabled)) 1:enable(port number base priority will be enabled, and port number based priority setting based on register 1FH~24H,27H~2BH		R/W	16'h0000
26H	4CH 4DH	TCP/UDP port number base priority for p16 Bit [0]: 0:disable 1:enable		R/W	16'h0000
27H	4EH 4FH	TCP/UDP port number based priority setting: Port_No common used by Bit [2:0]: 20,21 (FTP) Bit [5:3]: 22 (SSH) Bit [8:6]: 23 (TELNET) Bit [11:9]: 25 (SMTP) Bit [14:12]:53 (DNS)	000: to queue 0 (dis) 001: to queue 1 010: to queue 2 011: to queue 3 100: to CPU 101: drop	R/W	16'h0000
28H	50H 51H	TCP/UDP port number based priority setting: Port_No common used by Bit [2:0]: 69 (TFTP) Bit [5:3]: 80,8080 (HTTP_0,1) Bit [8:6]: 110 (POP3) Bit [11:9]: 119 (NEWS) Bit [14:12]:123 (SNTP)	000: to queue 0 (dis) 001: to queue 1 010: to queue 2 011: to queue 3 100: to CPU 101: drop	R/W	16'h0000
29H	52H 53H	TCP/UDP port number based priority setting: Port_No common used by Bit [2:0]: 137,138,139 (NETBIOS 0,1,2) Bit [5:3]: 143,220 (IMAP_0,1) Bit [8:6]: 161,162 (SNMP_0,1) Bit [11:19]:443 (HTTPS) Bit [14:12]:1863 (MSN)	000: to queue 0 (dis) 001: to queue 1 010: to queue 2 011: to queue 3 100: to CPU 101: drop	R/W	16'h0000
2AH	54H 55H	TCP/UDP port number based priority setting: Port_No common used by Bit [2:0]: 3389 (XRD_RDP) Bit [5:3]: 4000,8000 (QQ_0,1) Bit [8:6]: 5190 (ICQ)		R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description		R/W	Default value
		Bit [11:19]: 5050 (YAHOO) Bit [14:12]: 67,68 (BOOTP/DHCP) The port number of the protocol can be modified by user.	000: to queue 0 (dis) 001: to queue 1 010: to queue 2 011: to queue 3 100: to CPU 101: drop		
2BH	56H 57H	TCP/UDP user defined port number based priority setting: Bit [2:0]: TCP/UDP_num_a Bit [5:3]: TCP/UDP_num_b Bit [8:6]: TCP/UDP_num_c (Corresponding to offset address 0x1F~0x24)	000: to queue 0 (dis) 001: to queue 1 010: to queue 2 011: to queue 3 100: to CPU 101: drop	R/W	16'h0000
2CH	58H 59H	TCP/UDP port number based filter select to specific port Port_No common used by Bit [0]: 20,21 (FTP) Bit [1]: 22 (SSH) Bit [2]: 23 (TELNET) Bit [3]: 25 (SMTP) Bit [4]: 53 (DNS) Bit [5]: 69 (TFTP) Bit [6]: 80,8080 (HTTP_0,1) Bit [7]: 110 (POP3) Bit [8]: 119 (NEWS) Bit [9]: 123 (SNTP) Bit [10]: 137,138,139 (NETBIOS 0,1,2) Bit [11]: 143,220 (IMAP_0,1) Bit [12]: 161,162 (SNMP_0,1) Bit [13]: 443 (HTTPS) Bit [14]: 1863 (MSN) Bit [15]: 3389 (XRD_RDP) Bit [15:0] : 0:don't care 1:select (Corresponding to offset address 0x27~0x2A)		R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
2DH	5AH 5BH	TCP/UDP port number based filter select to specific port Port_No common used by Bit [0]: 4000,8000 (QQ_0,1) Bit [1]: 5190 (ICQ) Bit [2]: 5050 (YAHOO) Bit [3]: 67,68 (BOOP/DHCP) Bit [4]: TCP/UDP_num_a Bit [5]: TCP/UDP_num_b Bit [6]: TCP/UDP_num_c Bit[6:0]: 0:don't care 1:select Bit [7]: Reserved Bit [8]: filter method to specific port 0:negative list, the setting "1"s above which routed to specific port will be filtered. 1:positive list, the setting "1"s above which routed to specific port can be passed, otherwise be filtered Bit [9]: filter function enable 1:enable (0x2C, 0x2D setting take effect) 0:disable (Bit [9:8]: Ref to offset address 0xE4, 0xE5)	R/W	16'h0000
2EH	5CH 5DH	Switch's MAC address [15:0]	R/W	16'h0001
2FH	5EH 5FH	Switch's MAC address [31:16]	R/W	16'hC300
30H	60H 61H	Switch's MAC address [47:32] The MAC address setting of IP1717 is for CPU usage	R/W	16'h0090
31H	62H 63H	CPU Read statistic counter command [5:0]: statistic counter read address (from counter 0~33) [6]: statistic counter data updating stop [7]: statistic counter reset [8]: statistic counter read (after read, counter will reset to 0) [9]: command enable	W R/C	16'h0000
32H	64H 65H	CPU Read low 16 bits statistic counter data When register 31H execute read command, the read back data will put in register 32H and 33H.	R	16'h0000
33H	66H 67H	CPU Read high 16 bits statistic counter data	R	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
34H	68H 69H	Port statistic counter selection (port15~port0) Ref: 0x01[8]=(Port statistic counter method) Address even odd {Method, Selection}: counter0 counter1 0 0, receive packet count, transmit packet count 0 1, transmit packet count, collision count 1 0, receive packet count, packet drop count (MAC) 1 1, receive packet count, CRC error packet count Ex: Port 0: addr = 0 (even addr), counter 0 1 (odd addr), counter 1 Port 1: addr = 2 (counter 0), 3 (counter 1) Port 16:addr= 32 (counter0), 33(counter1)	R/W	16'h0000
35H	6AH 6BH	Port statistic counter selection (port16)	R/W	16'h0000
36H	6CH 6DH	(Reserved)	R/W	16'hFFFF (R/C)
37H	6EH 6FH	(Reserved)	R/W	16'h0001 (R/C)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
Output queue register				
38H	70H 71H	Out queue schedule mode / weight selection Bit [1:0]: Schedule mode 00:Fist come Fist schedule 01:Strict Priority 10:2 queues WRR 11:4 queues WRR Bit [4:2]: priority queue 0 weight number when in WRR mode Bit [7:5]: priority queue 1 weight number when in WRR mode Bit [10:8]: priority queue 2 weight number when in WRR mode Bit [13:11]: priority queue 3 weight number when in WRR mode Priority queue 3 bits setting: 000→8,001→1,010→2,011→3,100→4,101→5,110→6,111->7(WRR ratio). Note: If 2 queues used only, queue 0 and 1 are the queues used.	R/W	16'h0000
39H	72H 73H	Out queue Aging timer configuration Bit [5:0]: output queue aging time = (1~2) x (value+1) x 100ms Bit [7]: output queue aging function enable	R/W	16'h0000
3AH	74H 75H	(Reserved for test)		16'h745E

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
Address resolution logic register				
3BH	76H 77H	ARL operation setting Bit [0]: Hash algorithm selection 0: CRC map base 1: Direct map base Bit [1]: Address table aging function disable 0: aging enable 1: aging disable Bit [3:2]: Trunk hash algorithm selection 2'b00: Port ID 2'b01: SA 2'b10: DA 2'b11: Both SA/DA Bit [4]: Block broadcast frames to CPU port except for ARP 0: disable blocking 1: enable blocking Bit [5]: Pass all ipv4 packet when block broadcast frame to CPU 0: disable pass 1: enable pass Bit [6]: VLAN type 0: port base VLAN 1: 802.1Q TAG based VLAN Bit [7]: Unicast packet stride across VLAN 0: unicast do not stride different VLAN 1: unicast strides different VLAN Bit [8]: VLAN blocked packet forward to uplink port enable 0: not forward to uplink port 1: forward to uplink port (Uplink port setting establish at offset address 0x44,45) Bit [9]: CPU route enable, if enable, the packets will route according to register 0xA8 Bit [11:10]: sniffer method 00:disable 01:egress 10:ingress 11:egress / ingress Corresponding to offset register 0x47h~0x4Ah Bit [12]: select the tag/untag method 0: base on ports(reg 4B~4E) 1: base on VIDS(reg 91~A4)	R/W	16'h0000
3CH	78H 79H	(reserved)	R/W	16'h0000
3DH	7AH 7BH	Broadcast storm control setting (p15~p0) Bit [15:0]: Broadcast storm control 1:enable 0:disable Broadcast packets reached to threshold will be dropped defined in register 3Eh	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
3EH	7CH 7DH	Broadcast storm control setting (p16) & broadcast threshold Bit [0]: Broadcast storm control 1:enable 0:disable Bit [6:1]: Broadcast storm control threshold The number of broadcast frames allowed in one period 100M :500us 10M :5 ms	R/W	16'h007E
3FH	7EH 7FH	Aging timer threshold setting Bit [14:0]: Aging timer, the aging time is about: (setting+1) x 55.3 sec. 3.8%	R/W	16'h0005
40H	80H 81H	Enable Source MAC address learning function port 15~port 0 Bit [15:0]: 0:disable learning 1:enable learning	R/W	16'hFFFF
41H	82H 83H	Spanning tree state configure bit 0 for port 15~port 0	R/W	16'hFFFF
42H	84H 85H	Spanning tree state configure bit 1 for port 15~port 0 {bit 1, bit 0} 00: discard state 01: block state 10: learning state 11: forwarding state	R/W	16'hFFFF
43H	86H 87H	Security configuration Bit [0]: disable forward unknown SA frame to CPU port 0:forward 1:not forward Bit [1]: forward unknown SA frame if source address learning function is disable 0:drop the unknown SA frame 1:forward the unknown SA frame Bit [2]: indicates the SA of input frame should match the original learning port or not 0: SA will not binding the original port 1: SA will binding the original port	R/W	16'h0006
44H	88H 89H	VLAN uplink function support for port15~port0 Bit [15:0]: uplink port configuration 0:normal port 1:uplink port	R/W	16'h0000
45H	8AH 8BH	VLAN uplink function support for port16 Bit [0]: uplink port configuration 0:normal port 1:uplink port	R/W	16'h0000
46H	8CH 8DH	Trunk function setting Bit [3:0]: for trunk 1 setting (p3~p0) Bit [7:4]: for trunk 2 setting (p7~p4) 0:port is not in trunk group 1:port is in trunk group	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
47H	8EH 8FH	Sniffer function configuration Bit [15:0]: the sniffering port select for port15~port0 0: this port is not monitoring port 1: this port is monitoring port Select the ports that sniffered packet send to.	R/W	16'h0000
48H	90H 91H	Sniffer function configuration Bit [0]: the sniffering port select for port16 0: this port is not monitoring port 1: this port is monitoring port Select the ports that sniffered packet send to.	R/W	16'h0000
49H	92H 93H	Sniffer function configuration Bit [15:0]: sniffered port config for port15~port0 0:this port is not be sniffered 1:this port is sniffered	R/W	16'h0000
4AH	94H 95H	Sniffer function configuration for port16 Bit [0]: sniffered port config 0:this port is not be sniffered 1:this port is sniffered	R/W	16'h0000
4BH	96H 97H	VLAN output port add tag operation configuration for port15~port0 Bit [15:0]: output frame add tag 0:disable 1:add VLAN tag to output frame	R/W	16'h0000
4CH	98H 99H	VLAN output port add tag operation configuration for port16 Bit [0]: output frame add tag 0:disable 1:add VLAN tag to output frame	R/W	16'h0000
4DH	9AH 9BH	VLAN output port remove tag operation configuration for port15~port0 Bit [15:0]: output frame remove tag 0:disable 1:remove VLAN tag of output frame	R/W	16'h0000
4EH	9CH 9DH	VLAN output port remove tag operation configuration for port16 Bit [0]: output frame remove tag 0:disable 1:remove VLAN tag of output frame	R/W	16'h0000
4FH	9EH 9FH	PVID index setting for p2~p0 Bit [4:0]: PVID indx configuration for port0 Bit [9:5]: PVID indx configuration for port1 Bit [14:10]: PVID indx configuration for port2 PVID index only support entry0~19 per port	R/W	15'h0820

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
50H	A0H A1H	PVID index setting for p5~p3 Bit [4:0]: PVID indx configuration for port3 Bit [9:5]: PVID indx configuration for port4 Bit [14:10]: PVID indx configuration for port5 PVID index only support entry0~19 per port	R/W	16'h1483
51H	A2H A3H	PVID index setting for p8~p6 Bit [4:0]: PVID indx configuration for port6 Bit [9:5]: PVID indx configuration for port7 Bit [14:10]: PVID indx configuration for port8 PVID index only support entry0~19 per port	R/W	16'h20E6
52H	A4H A5H	PVID index setting for p11~p9 Bit [4:0]: PVID indx configuration for port9 Bit [9:5]: PVID indx configuration for port10 Bit [14:10]: PVID indx configuration for port11 PVID index only support entry0~19 per port	R/W	16'h2D49
53H	A6H A7H	PVID index setting for p14~p12 Bit [4:0]: PVID indx configuration for port12 Bit [9:5]: PVID indx configuration for port13 Bit [14:10]: PVID indx configuration for port14 PVID index only support entry0~19 per port	R/W	16'h39AC
54H	A8H A9H	PVID index setting for p16~p15 Bit [4:0]: PVID indx configuration for port15 Bit [9:5]: PVID indx configuration for port16 PVID index only support entry0~19 per port	R/W	16'h020F
55H~ 68H	AAH D1H	VID configuration for VLAN table entry 0~19 Bit [11:0]: VID configuration 12bit VID can be configured 1~4094(dec) note: 0 and 4095 should not be used	R/W	16'h0001 ~0014
69H	D2H D3H	VLAN member configuration for VLAN table entry 0 or port 0 port base VLAN setting. Bit [15:0] 0: not in VLAN group 1: in VLAN group	R/W	16'hFFFF
6AH	D4H D5H	VLAN member configuration for VLAN table entry 0 or port 0 port base VLAN setting. Bit [0] 0: not in VLAN group 1: in VLAN group	R/W	16'h0001
6BH~ 90H	D6H 121H	VLAN member configuration for VLAN table entry 1~19 (1~16 also for port 1~16 port base VLAN) Bit [15:0] 0: not in VLAN group 1: in VLAN group For dumb switch, entry 17~19 must be set to all zeros	R/W	16'hFFFF 16'h0001
91H	122H 123H	Indicates the output ports with VID0 have tag or not Bit[15:0] 0: the output should not have tag 1: the output should have tag	R/W	16'hFFFF

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
92H~ A4H	124H~ 149H	Indicates the output ports with VID1~19 have tag or not Bit[15:0] 0: the output should not have tag 1: the output should have tag	R/W	16'hFFFF
A5H	14AH 14BH	IGMP snooping function configuration Bit [0]: enable IGMP snooping function Bit [15:1]: reserved	R/W	16'h0000
A6H	14CH 14DH	(reserved)		16'h0000
A7H	14EH 14FH	(reserved)		16h'0000
A8H	150H 151H	CPU send packets to specific ports Bit [15:0]: 0: packet from CPU is not sent to this port 1: packet from CPU is sent to this port	R/W	16'h0000
A9H	152H 153H	Non-association port Bit [15:0]: indicate which ports are non-association port If a port is the non-association port, it will not send packets to other non-association ports	R/W	16'h0000
AAH	154H 155H	(reserved)	R/W	16'h0000
ABH	156H 157H	Port base address flush for port15~0 Bit[15:0]: indicates that the address learning by the selected port should be flushed	R/W	16'h0000
ACH	158H 159H	CPU read/write address table configuration Bit [11:0]: the address table address Bit [12]: read/write configuration 0: read 1: write Bit [13]: the REG_CPU_DATA_0, REG_CPU_DATA_1, REG_CPU_DATA_2 data indicator 0: the contain is read back data 1: the contain is the data that want to write into address table Bit [14]: command enable 0: disable 1: read/write address table enable Bit [15]: command complete	R/W	16'h0000
ADH	15AH 15BH	CPU read/write address table data [15:0] If the command is read, store the read back data If the command is write, write this data to address table	R/W	16'h0000
AEH	15CH 15DH	CPU read/write address table data [31:16] If the command is read, store the read back data If the command is write, write this data to address table	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
AFH	15EH 15FH	CPU read/write address table data [45:32] If the command is read, store the read back data If the command is write, write this data to address table Bit [15:14]: Table address access method 00: address calculated by CPU 01: address calculated by HW for normal MAC entry 10 ~11:(reserved)	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
SMI control register				
B0H	160H 161H	Auto negotiation Configuration Bit [15:0]: Auto negotiation for port15~0 0: disable auto negotiation 1: enable auto negotiation	R/W	16'hFFFF
B1H	162H 163H	Auto negotiation configuration Bit [0]: Auto negotiation for port16 0: disable auto negotiation 1: enable auto negotiation	R/W	16'h0001
B2H	164H 165H	Speed setting for port 15~0, 1 Bit/port Bit [15:0] 0: 10 Mbps 1: 100 Mbps	R/W	16'hFFFF
B3H	166H 167H	Speed setting for port16 Bit [0]: 0: 10 Mbps 1: 100 Mbps	R/W	16'h0001
B4H	168H 169H	Duplex setting for Port15~Port0, 1bit/port Bit [15:0]: 0: half duplex 1: full duplex	R/W	16'hFFFF
B5H	16AH 16BH	Duplex setting for Port16 Bit [0]: 0: half duplex 1: full duplex	R/W	16'h0001
B6H	16CH 16DH	Pause setting for Port15~Port0, 1bit/port Bit [15:0]: 0: disable pause 1: enable pause	R/W	16'hFFFF
B7H	16EH 16FH	Pause setting for Port 16 Bit [0]: 0: disable pause 1: enable pause	R/W	16'h0001
B8H	170H 171H	Asymmetric pause setting for Port15~Port0, 1bit/port Bit [15:0] 0: disable asymmetric pause 1: enable asymmetric pause	R/W	16'hFFFF

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
B9H	172H 173H	Asymmetric pause setting for Port16 Bit [0] 0: disable asymmetric pause 1: enable asymmetric pause	R/W	16'h0001
BAH	174H 175H	Backpressure setting for Port15~Port0, 1bit/port Bit [15:0]: 0: backpressure function disable 1: backpressure function enable	R/W	16'hFFFF
BBH	176H 177H	Backpressure setting for Port16 Bit [0]: 0: backpressure function disable 1: backpressure function enable	R/W	16'h0001
BCH	178H 179H	Transmit setting for Port15~Port0, 1bit/port Bit [15:0]: 0: transmit disable 1: transmit enable	R/W	16'hFFFF
BDH	17AH 17BH	Bit [0]: transmit setting for Port 16 0: transmit disable 1: transmit enable Bit [5:1]: PHY address setting for CPU port PHY address can be set from 0 to31, the default is one. Bit [6]: CPU port force link 0: not force link 1:force link without SMI	R/W	16'h0003
BEH	17CH 17DH	CPU read/write PHY register command Bit [4:0]: PHY address(from PHY 0 to 31) Bit [9:5]: MII Register address(from MII register 0 to 31) Bit [12:10]: reserved Bit [13]: 0: command not complete 1: command complete Bit [14]: 0: read operation 1: write operation Bit [15]: 0: idle or command complete 1: start command	R/W	16'h0000
BFH	17EH 17FH	CPU read/write PHY register command data Bit [15:0]: in read command-the read back data In write command-data want to write	R/W	16'h0000
C0H	180H 181H	The port status of port 2~0, 5 bit/port Bit [4:0]: port 0 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 1 status Bit [14:10]: port 2 status Flow_Ctrl include backpressure in half duplex	R	16'h0000
C1H	182H 183H	The port status of port 5~3, 5 bit/port Bit [4:0]: port 3 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 4 status Bit [14:10]: port 5 status Flow_Ctrl include backpressure in half duplex	R	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C2H	184H 185H	The port status of port 8~6, 5 bit/port Bit [4:0]: port 6 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 7 status Bit [14:10]: port 8 status Flow_Ctrl include backpressure in half duplex	R	16'h0000
C3H	186H 187H	The port status of port 11~9, 5 bit/port Bit [4:0]: port 9 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 10 status Bit [14:10]: port 11 status Flow_Ctrl include backpressure in half duplex	R	16'h0000
C4H	188H 189H	The port status of port 14~12, 5 bit/port Bit [4:0]: port 12 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 13 status Bit [14:10]: port 14 status Flow_Ctrl include backpressure in half duplex	R	16'h0000
C5H	18AH 18BH	The port status of port 16~15, 5 bit/port Bit [4:0]: port 15 status {Asymmetric pause, flow_ctrl, duplex, speed, link} Bit [9:5]: port 16 status Flow_Ctrl include backpressure in half duplex	R	16'h0000
C6H	18CH 18DH	(reserved)		16'h0000
C7H	18EH 18FH	(reserved)		16'h0000
C8H	190H 191H	(reserved)		16'h0000
C9H	192H 193H	(reserved)		16'h0000
CAH	194H 195H	(reserved)		16'h0000
CBH	196H 197H	(reserved)		16'h0000
CCH	198H 199H	(reserved)		16'h0000
CDH	19AH 19BH	(reserved)		16'h0000
CEH	19CH 19DH	(reserved)		16'h0000
CFH	19EH 19FH	(reserved)		16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
D0H	1A0H 1A1H	(reserved)		16'h0000
D1H	1A2H 1A3H	(reserved)		16'h0000
D2H	1A4H 1A5H	(reserved)		16'h0000
D3H	1A6H 1A7H	(Reserved)		16'h0000
D4H	1A8H 1A9H	(Reserved for test)		16'h0032
D5H	1AAH 1ABH	(Reserved for test)		16'h0062
D6H	1ACH 1ADH	(Reserved for test)		16'h0001
D7H	1AEH 1AFH	(Reserved for test)		16'h0019
D8H	1B0H 1B1H	(Reserved for test)		16'h039E
D9H	1B2H 1B3H	(Reserved for test)		16'h0064
DAH	1B4H 1B5H	(Reserved for test)		16'h02EC
DBH	1B6H 1B7H	(Reserved)		16'h0000
DCH	1B8H 1B9H	(Reserved)		16'h0000
DDH	1BAH 1BBH	(Reserved)		16'h0000
DEH	1BCH 1BDH	(Reserved)		16'h0000
DFH	1BEH 1BFH	(Reserved)		16'h0000
E0H	1C0H 1C1H	(reserved)		16'h0000
E1H	1C2H 1C3H	(reserved for test)		16'h0F0F

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
Miscellaneous control register				
E2H	1C4H 1C5H	CPU mode setting Bit [0]: Port 16 linked to CPU 0: normal port 1: CPU port Bit [1]: Special TAG for CPU port enable 0: disable 1: enable, frame transmit out CPU port will be inserted special tag, special tag defined in register E3h Bit [2]: CPU interface RvMII mode 0: MAC mode 1: PHY mode	R/W	16'h0000
E3H	1C6H 1C7H	Special TAG Type/Len setting Bit [15:0]: special tag type/length item	R/W	16'h9126
E4H	1C8H 1C9H	Specific port setting for TCP/UDP port filter setting Bit [15:0]: P0~P15 port filter Ref offset address 0x2D [8]: 0: negative filtering mode (If TCP/UDP number matched, packet sent to filter setting port will be dropped) 1: positive filtering mode (If TCP/UDP port matched, packet sent to filter setting port will be allowed, others will be dropped) 0x2D [9]: filter enable 0: disable 1: enable	R/W	16'h0000
E5H	1CAH 1CBH	Specific port setting for TCP/UDP port filter setting Bit [0]: P16 port filter (same definition as above)	R/W	16'h0000
E6H	1CCH 1CDH	(Reserved)		16'h0000
E7H	1CEH 1CFH	Interrupt signal setting Bit [0]: enable interrupt for CPU r/w SMI command complete Bit [1]: enable interrupt for PHY link status notification Bit [2]: reserved Bit [3]: enable interrupt for CPU r/w EPROM command complete Bit [4]: Interrupt pin active mode (0: low active 1: high active) Note: Interrupt signal that is triggered by any event will assert until user read this register (0xE8h)	R/W	16'h0002
E8H	1D0H 1D1H	Interrupt signal setting Bit [0]: Interrupt of CPU r/w SMI command complete Bit [1]: PHY link status change notification Bit [2]: reserved Bit [3]: Interrupt of CPU r/w EPROM command complete	R/C R/C R/C R/C	16'h0000

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>E9H</td><td>1D2H
1D3H</td><td>(Reserved)</td><td></td><td>16’h0000</td></tr>
<tr><td>EAH</td><td>1D4H
1D5H</td><td>RMII/SS-SMII Interface signal Delay setting
Bit [0]: Port 8~Port 15 SS-SMII TX Clock input delay
0: no delay 1:delay 4 ns;
Bit [1]: Port 8~Port 15 SS-SMII RX Clock output delay
0: no delay 1:delay 4 ns;
Bit [2]: Port 8~Port 15 SS-SMII RX SYNC input delay
0: no delay 1:delay 4 ns;
Bit [4:3]: Port 8~Port 16, clock output driving current
<table>
<tr><td></td><td>TXCLK/TXSYNC</td><td>TXD</td></tr>
<tr><td>00</td><td>4mA</td><td>2mA</td></tr>
<tr><td>01 (default)</td><td>8mA</td><td>4mA</td></tr>
<tr><td>10</td><td>11mA</td><td>8mA</td></tr>
<tr><td>11</td><td>11mA</td><td>11mA</td></tr>
</table>
Bit [5]: Slew Rate
0: Normal, 1: Fast</td><td>R/W</td><td>16’h0020</td></tr>
<tr><td>EBH</td><td>1D6H
1D7H</td><td>CPU read/write EEPROM command
Bit [7:0]: Byte Address
Bit [10:8]: Device Address
Bit [12:11]: reserved
Bit [13]: 0: command not complete
1: command complete
Bit [14]: 0: read operation
1: write operation
Bit [15]: the read/write command trigger
0: idle or command complete
1: start command</td><td>R/W</td><td>16’h0000</td></tr>
<tr><td>ECH</td><td>1D8H
1D9H</td><td>CPU read/write EEPROM command data
Bit [7:0]: In read command – the read back data
In write command – data want to write</td><td>R/W</td><td>16’h0000</td></tr>
<tr><td>ED~EFH</td><td>1DAH
1DFH</td><td>(reserved)</td><td></td><td>16’h0000</td></tr>
<tr><td>F0H</td><td>1E0H
1E1H</td><td>Spd/Duplex LEDs in force mode.
Bit[11]=0(default)
When LEDMODE is set in serial LED mode, the Spd/Duplex LEDs will be light before link up.
Bit[11]=1
When LEDMODE is set in serial LED mode, the Spd/Duplex LEDs will not be light before link up.</td><td>R/W</td><td>16’h0000</td></tr>
<tr><td>F1~F2H</td><td>1E2H
1E5H</td><td>(reserved for test)</td><td></td><td>16’h0000</td></tr>
</table>

3.2 IP1717 internal octal PHY register description

The internal PHY can be only accessed by register BE~BF of IP1717, please refer to register BE~BF description of IP1717.The internal PHY address is from 8 to 15, the detailed setting of internal PHY is as follows.

Register16 : PHY Specification Control Register (default = 16'h45AC)

Reg.bit	Name	Description	Mode	Default
16[15]	PS_MODE_DIS	Disable 10M power saving mode 1: Disable 10M power saving mode 0: Enable 10M power saving mode (default)	RW	0
16[14]	PS_MODE_SEL	This bit is used to select the 10M power saving mode if 10M power saving mode is enable 1: 0 to 100 mA current switch (default) 0: 40 to 100 mA current switch	RW	1
16[13]	PS_10TX_EN	Enable 10M transmit power saving mode 1: Enable 10M transmit power saving mode 0: Disable 10M transmit power saving mode	RW	0
16[12]	Reserved		RO	0
16[11]	PS_10TX_MODE	This bit is used to select the 10M transmit power saving mode if 10M transmit power saving mode is enable. 1: Mode1 is selected 0: Mode 0 is selected	RW	0
16[10]	FORCE_MODE_LED	0: In force mode, IP1717 LED will not show the operating mode before link up. 1: In force mode, IP1717 LED will show the operating mode before link up.	RW	1
16[9]	CONSISTENCY_RF	When this bit is set to 0, IP1717 asserts consistency_match during auto negotiation process by ignoring RF bit. 0: RF bit is ignored. 1: RF bit is considered.	RW	0
16.[8]	MLT3_DET_EN	Set high to enable MLT3 detection function. When MLT3 detection function is enabled, IP1717 supports manually (without auto negotiation) speed change from 10Mbps to 100Mbps by link partner. 1: Enable MLT3 detection function 0: Disable MLT3 detection function	RW	1
16.[7]	APS_ON	This bit is used to activate Auto Power Saving (APS) mode 0: Disable 1: Enable	RW	1
16.[6]	NWAY_PWSV_OFF	Set high to disable the power saving during Auto-Negotiation procedure 0: Enable Power Saving 1: Disable Power Saving	RW	0

Reg.bit	Name	Description	Mode	Default
16[5]	AUTO_MDIX_ALL_EN	Auto-crossover for all ports 0: Disable auto-crossover function for all ports 1: Enable auto-crossover function for all ports When this bit is set to high, auto-crossover function can be disabled per port by MII register 23 bit 15~8.	RW	1
16.[4]	FEF_DISABLE	Set high to disable the functionality of Far-End Fault when the chip operates at fiber mode 0: Enable FEF 1: Disable FEF	RW	0
16.[3]	REPEAT_MODE	Set high to let IP1717 operate at repeat mode 0: Not Repeat mode 1: Repeat mode	RW	1
16.[2]	JABBER_ENA	Set high to enable jabber detection mechanism when IP1717 operates at 10BASE-T 0: Disable 1: Enable	RW	1
16.[1]	HEARTBEAT_ENA	Set high to enable heartbeat detection mechanism when IP1717 operates at 10BASE-T 0: Disable 1: Enable	RW	0
16.[0]	BYPASS_DSPRST	Set high to disable DSP reset watch-dog timer 0: Not Bypass 1: Bypass	RW	0

- **Register18 : PHY Status Monitoring Register**

Reg.bit	Name	Description	Mode	Default
18.[15]	LDSP_SLEEPING	When is set to high, indicates IP1717 is at link-down sleeping mode	RO	0
18.[14]	LINK_OK	When is set to high, indicates link status is OK	RO	0
18.[13]	DESCRAM_LOCK	When is set to high, indicates PCS de-scrambler is locked on data	RO	0
18.[12]	10BASE_POLARITY	When is set to high, indicates the cable polarity is reversal (this bit is meaningful only chip operates at 10BASE-T)	RO	0
18.[11]	RESLOVED_SPEED	To indicate the resolved speed mode 0: 10BASE-T 1: 100BASE-TX/FX	RO	0
18.[10]	RESLOVED_DUPLEX	To indicate the resolved duplex mode 0: Half Duplex 1: Full Duplex	RO	0
18.[9]	MDI/MDIX	To indicate either at MDI or MDIX state 0: MDI (Not Crossover) 1: MDIX(Crossover)	RO	0
18.[8:0]	NWAY_DEBUG_OUT	NWAY debug output	RO	0

Register23 : MDI/MDIX Control Register (default = 16'hff00)

Reg.bit	Name	Description	Mode	Default
23[15:8]	Auto_MDIX	Port7~port0 auto crossover enable 1: Enable auto crossover function. 0: Disable auto crossover function.	R/W	8'hff
23[7:0]	MDIX_SEL	Port7~port0 MDI/MDIX channel selection A port can force the channel to the MDI or MDIX when the port's auto crossover function is disabled. 1: select the MDIX channel. 0: select the MDI channel.	R/W	8'h00

EEPROM register mapping table for switch only

```
17 17 00 25 00 01 00 00 00 00 00 00 00 00 00 00 //0f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //1f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //2f
00 00 00 00 00 00 00 00 ff ff 00 01 00 00 00 00 //3f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //4f
00 00 00 00 00 00 00 00 00 00 00 00 00 01 c3 00 //5f
00 90 00 00 00 00 00 00 00 00 00 00 ff ff 00 01 //6f
00 00 00 00 74 5e 00 00 00 00 00 00 00 7e 00 05 //7f
ff ff ff ff ff ff 00 06 00 00 00 00 00 00 00 00 //8f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 08 20 //9f
14 83 20 e6 2d 49 39 ac 02 0f 00 01 00 02 00 03 //af
00 04 00 05 00 06 00 07 00 08 00 09 00 0a 00 0b //bf
00 0c 00 0d 00 0e 00 0f 00 10 00 11 00 12 00 13 //cf
00 14 ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff //df
00 01 ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff //ef
00 01 ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff //ff
00 01 ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff //10f
00 01 ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff //11f
00 01 ff ff ff ff ff ff ff ff ff ff ff ff ff ff //12f
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff //13f
ff ff ff ff ff ff ff ff ff ff 00 00 00 00 00 00 //14f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //15f
ff ff 00 01 ff ff 00 01 ff ff 00 01 ff ff 00 01 //16f
ff ff 00 01 ff ff 00 01 ff ff 00 03 00 00 00 00 //17f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //18f
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //19f
00 00 00 00 00 00 00 00 00 32 00 62 00 01 00 19 //1af
03 9e 00 64 02 ec 00 00 00 00 00 00 00 00 00 00 //1bf
00 00 0f 0f 00 00 91 26 00 00 00 00 00 00 00 02 //1cf
00 00 00 00 00 30 00 00 00 00 00 00 00 00 00 00 //1df
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 //1ef
```

4 Electrical Characteristics

4.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

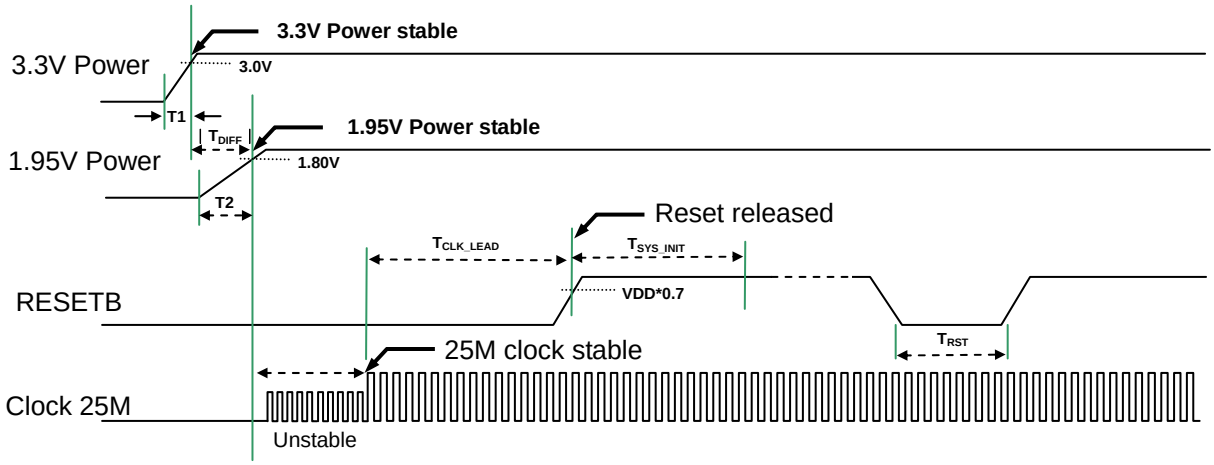
PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O_1	V_{DDIO_1}	– 0.5	+3.6V	V
	I/O_2&3	V_{DDIO_2} & V_{DDIO_3}	– 0.5	+3.6V	V
	Core	V_{DDC} & V_{DDA}	– 0.5	+2.2V	V
Input Voltage		V_I	– 0.5	V_{DDIO_1}, V_{DDIO_2} & V_{DDIO_3}	V
Output Voltage		V_O	– 0.5	V_{DDIO_1}, V_{DDIO_2} & V_{DDIO_3}	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	+70	°C
Junction Temperature		Tj	0	+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

4.2 AC Characteristics

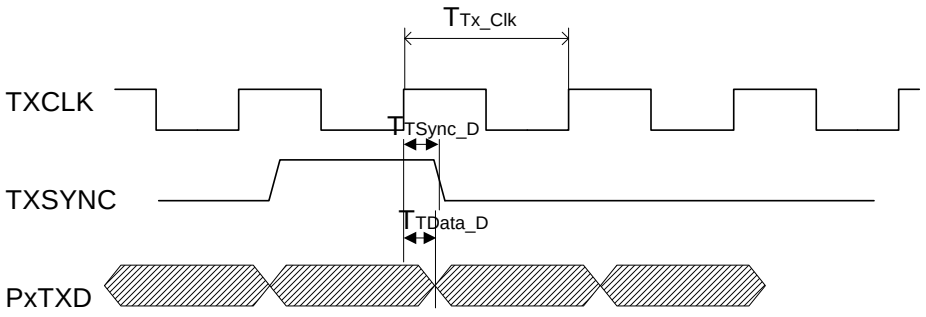
Power On Sequence and Reset Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T1	Rising time of 3.3V Power	1	-	-	ms
T2	Rising time of 1.95V Power	1	-	-	ms
$\lvert T_{DIFF} \rvert$	Time difference among power sources	0	-	30	ms
T_{CLK_LEAD}	X1 clock valid before reset released	10	-	-	ms
T_{SYS_INIT}	System initial completed, this time to keep silence.	100	-	-	ms
T_{RST}	Reset period for reset switch	10	-	-	ms



SS-SMII Transmit Timing

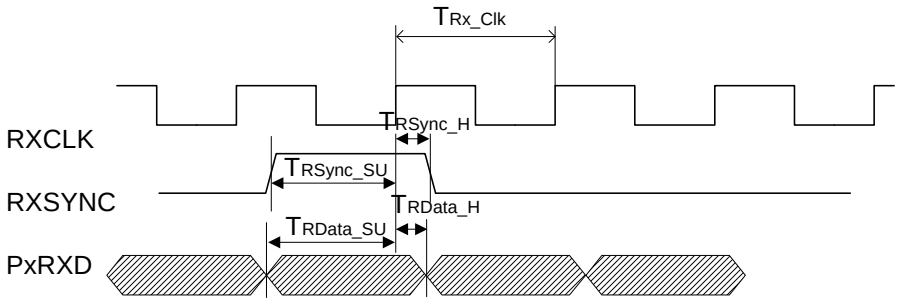
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tx_Clk}	Transmit clock cycle time	-	8	-	ns
T_{TSync_D}	TXCLK rising edge to TXSYNC output delay	1.0	-	5.5	ns
T_{TData_D}	TXCLK rising edge to TXD output delay	1.0	-	5.5	ns



SS-SMII Transmit

SS-SMII Receive Timing

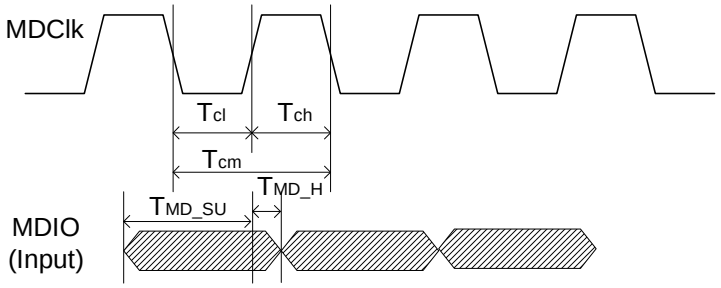
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rx_Clk}	Receive clock cycle time	-	8	-	ns
T_{RSync_SU}	RXSYNC Set up time	2.0	-	-	ns
T_{Rdata_H}	RXSYNC Hold time	0.0	-	-	ns
T_{Rdata_SU}	RXD Set up time	2.0	-	-	ns
T_{RData_H}	RXD Hold time	0.0	-	-	ns



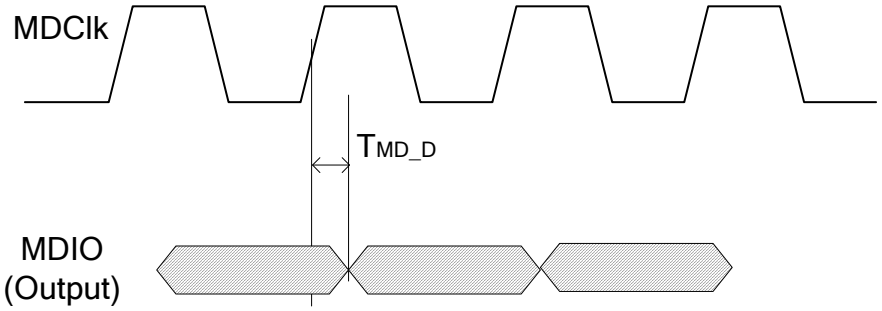
SS-SMII Receive

PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time	-	200	-	ns
T_{cl}	MDCK Low Time	-	200	-	ns
T_{cm}	MDCK cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-	-	ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns



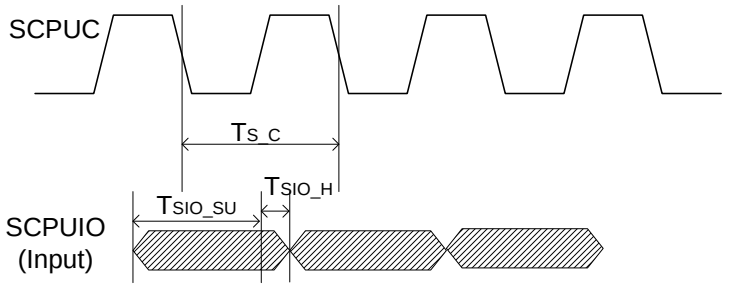
MDIO Input Cycle



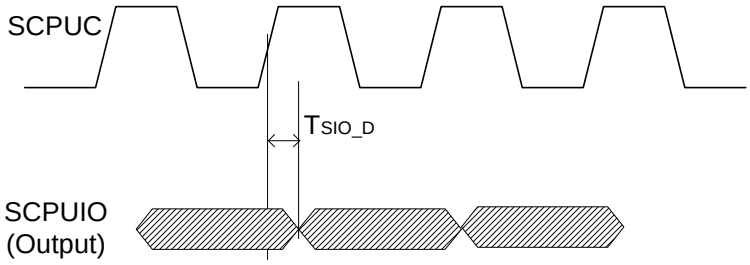
MDIO Output Cycle

CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{S_C}	SCPUC cycle time	400	-	-	ns
T_{SIO_SU}	Serial I/O set up time	10	-	-	ns
T_{SIO_H}	Serial I/O hold time	10	-	-	ns
T_{SIO_D}	Serial I/O output delay time	5	-	20	ns



Serial I/O Input Cycle

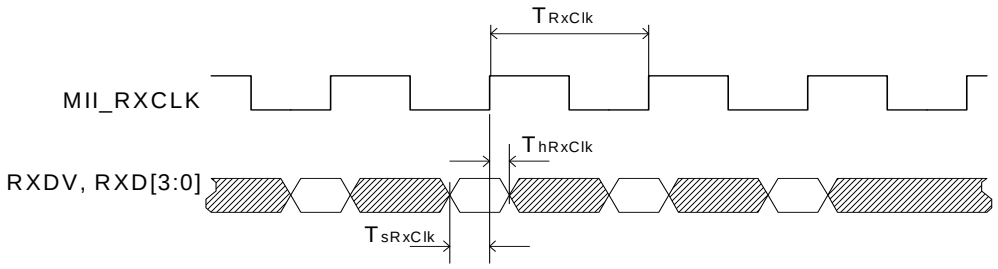


Serial I/O Output Cycle

MII Timing

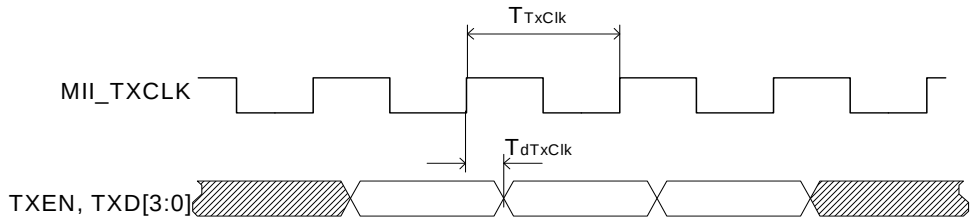
Receive Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100M MII	-	40	-	ns
T_{RxClk}	Receive clock period 10M MII	-	400	-	ns
T_{sRxClk}	RXDV, RXD to MII_RXCLK setup time	10	-	-	ns
T_{hRxClk}	RXDV, RXD to MII_RXCLK hold time	5	-	-	ns



Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100M MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10M MII	-	400	-	ns
T_{dTxClk}	MII_TXCLK rising edge to TXEN, TXD	5	-	22	ns

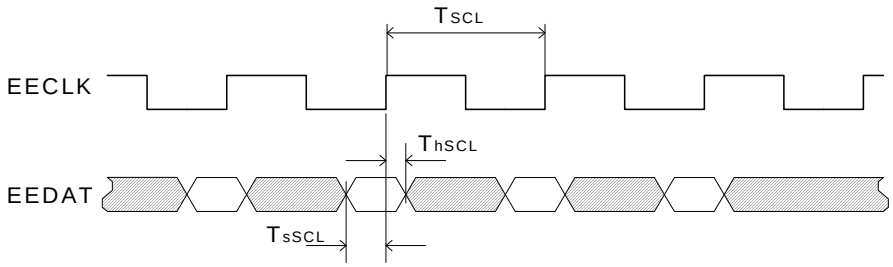


EEPROM Timing

Read data cycle
EEPROM Timing Rx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	EEDAT to EECLK setup time	20	-	-	ns
T_{hSCL}	EEDAT to EECLK hold time	20	-	-	ns

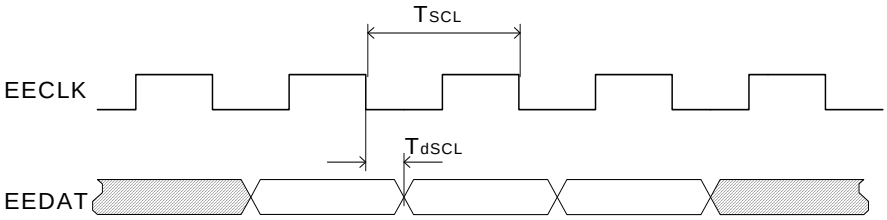
Read Data Cycle



Command cycle
EEPROM Timing Tx Parameters

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	EECLK falling edge to EEDAT	-	-	5200	ns

Command Cycle



4.3 DC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage	V_{OL}			0.4	V
Output high voltage	V_{OH}	1.80V for 1.95V I/O supply voltage. 3V for 3.3V I/O supply voltage.			V
Low level output current	I_{OL}			TBD	mA
High level output current	I_{OH}	TBD			mA
VDDIO_2 ,3 supply voltage		3.0	3.3	3.6	V
VDDIO_1 supply voltage		1.9	1.95	2.05	V
VDDC/VDDA supply voltage		1.9	1.95	2.05	V
SS-SMII Input High voltage(VDDIO_1=1.95V)	V_{T+}	1.28			V
SS-SMII Input low voltage(VDDIO_1=1.95V	V_{T-}			0.72	V
VDDIO_1 supply voltage for 3.3V		3.0	3.3	3.6	V
SS-SMII Input High voltage(VDDIO_1=3.3V)	V_{T+}	2			V
SS-SMII Input low voltage(VDDIO_1=3.3V	V_{T-}			1.4	V
Pull-down resistor	R_{PD}	51		127	KΩ
X1 Input Low Voltage	V_{IL}			0.6	V
X1 Input High Voltage	V_{IH}	1.5			V
RESETB threshold voltage	VRST	0.7*VDDI/O_1	-	0.85* VDDI/ O_1	V

Crystal specification

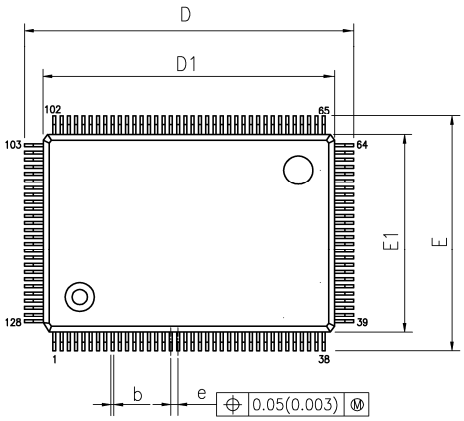
Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25℃	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10℃ ~ +70℃
6	Equivalent Series Resistance	40 ohm Max.
7	Drive Level	100 μW
8	Load Capacitance	15 pF
9	Shunt Capacitance	7 pF Max
10	Insulation Resistance	Mega ohm Min./DC 100V
11	Aging Rate A Year	+/- 5 ppm/year

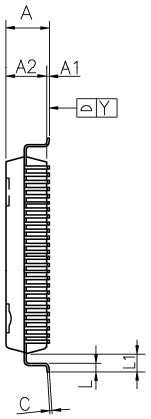
5 Order Information

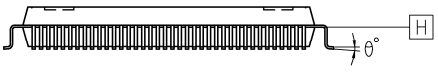
Part No.	Package	Notice
IP1717 LF	128 PIN PQFP	Lead-Free
IP1717L LF	128 PIN LQFP	EPAD Lead-Free

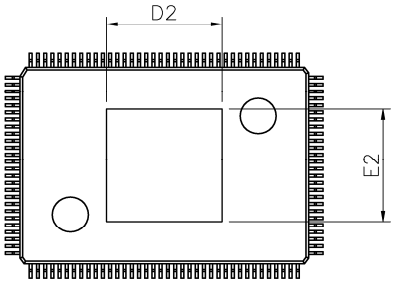
6 Package Detail

128 Pin LQFP Outline Dimensions









EPAD size:315milx315mil

(THERMALLY ENHANCED VARIATIONS ONLY)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.10	0.15	0.20
D1		20.00 BSC	
E1		14.00 BSC	
e		0.50 BSC	
D		22.00 BSC	
E		16.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
Y	–	–	0.08
θ°	0°	3.5°	7°

UNIT : mm

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
27*X27*	5.83	7.01	5.83	7.01
31*X31*	6.80	8.15	6.80	8.15

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,
實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:
1.JEDEC OUTLINE:
MS-026 BHB.
MS-026 BHB-HD(THERMALLY ENHANCED VARIATIONS ONLY).
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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