24-Port 10/100 + 5-Port 10/100/1000Mb Ethernet Switch (with 24 10/100M PHYs and Embedded 32bit CPU)

Features List

- **24-Port 10/100Mb + 5-Port 10/100/1000Mb Ethernet Switch**
  - Embedded 32-bit CPU
  - Built-in 24 10/100Mb PHYs
  - Built-in 2 Fiber port / SGMII PHYs
  - 2 RGMII
  - 1 GMII/RGMII/MII interfaces for external CPU (optional)
  - IEEE802.3az supported
  - 10/100Mb full/half duplex supported
  - 1000Mb full duplex supported
  - 100Mb TP and Fiber dual mode, selected by Signal Detection (SD) level
- **Store & Forward, Share Memory Non-blocking Architecture**
  - Built-in 4Mb SRAM for packet buffer
  - 16K Jumbo packet supported
  - Max. length 1664B if jumbo disable
- **Wire-Speed Operation On Every Port**
- **Head Of Line Blocking Prevention**
- **Flow Control Support**
  - 802.3x compliant flow control in full duplex
  - Collision/Carrier_ sense based backpressure in half duplex
- **Internal 16K MAC Address Entities**
  - CRC/Direct hashing algorithm
  - Aging timer programmable (55s~500.6hr)
  - Wire speed address learning and resolution
  - CPU accessible for security and static MAC
  - Learning enable/disable
- **IGMP/MLD Snooping Support**
  - IGMP Version 1, 2, 3 / MLD Version 1, 2
  - MLD snooping. (4 sets IP address per MLD list)
  - Snooping by Switch ASIC or CPU
- **Six Trunk Group Support**
  - Four trunk groups, trunk A~D up to 4 ports
  - Trunk E, F has 2 ports per trunk
  - Load balance based on (Port ID, DA, SA, DA/SA, IP, TCP/UTP)
  - Link fault recovery
- **Per Port 41 MIB Counters/port**
  - RMON/ Ethernet/ MIB II
- **Hardware Auto loop detection**
- **VLAN**
  - 29 Port based
  - 4K Tag based
  - Tag remove/add/modify supported
  - IVL/SVL learning mode
  - Protocol VLAN supported
  - Q-in-Q (double tag) supported
  - 64 configurable VID for Q-in-Q tag stacking
- **Class Of Service (CoS) Support**
  - Output Queue Schedule Mode support WRR/FIFS/SP/SP+WRR/WFQ/TWRR
  - Port based priority
  - 802.1Q priority tagged based
  - IP TOS based (IPv4/IPv6)
  - TCP/UDP port number based
  - Source MAC address based
  - ACL based
  - Privilege priority
  - 8 levels per port
- **Priority queuing decision Support**
  - DSCP/ TAG priority remarking
  - 802.1Qad PCP, DEN insert / modify
  - 802.1Q PCP, CFI insert/ modify
  - RX &TX Priority re-mapping
  - LLQ + latency
- **Broadcast/multicast/DLF/ARP/ICMP Storm Control**
  - 256 levels resolution for all storm control
  - All storm is enabled by per port
  - With option to drop all ARP to CPU
  - Unit time is selected for all storm
- **Sniffer Function**
  - Ingress、egress、ingress/egress methods
  - Two Sniffer destination port group configuration
  - Supports Add/ Remove Tag option for packet routing to mirroring ports
  - Supports ACL and special tag for sniffer application
- **Port Security**
  - MAC based
  - TCP/UDP port based
  - SIP based
  - 802.1x :port based & MAC based

- **Bandwidth Control**
  - From 64K bps to wire speed (resolution 64k)
  - Flow control on/off is supported
  - Queue based bandwidth control (resolution 64k/1M/2M/4M)
- **Support SMI Interface Auto-Polling**
  - Speed, Duplex, Flow control, Link
  - CPU accessible (interrupt support)
  - CPU R/W PHY register
  - MMD access support
- **Out Queue**
  - Frame buffer/ queue/ port based aging
  - Bandwidth assured/ limited
  - Latency assured
  - WRED(Weight Random Early Drop)
  - LLQ (Low latency queue) support
  - Dorm mode (WAN/LAN dual schedule mode)
- **Spanning Tree Protocol Port State Support**
  - Discard/Block/Learning/Forwarding four states support
  - Forwarding STP frame to CPU port
  - RSTP/MSTP support
- **Support 128 ACL Entities Support**
  - Ingress port
  - VLAN
  - Destination/Source MAC address
  - Destination/Source IP (specific or range)
  - TCP/UDP Destination/Source port number (specific or range)
  - IP protocol, DSCP, TCP flag
  - Action : forward, to CPU, drop, priority, Q-in-Q tag, remarking, redirect, bandwidth limited
- **Configuration**
  - Pin initial setting
  - 2-wire serial interface for configuration EEPROM
  - Advanced EEPROM program mode
  - 2-wire serial interface for low cost smart system application
  - Built in CPU I/F
- **Programmable serial LED Display Function**
  - 8 modes/ flashing speed selectable
  - Power on cable diagnosis indication
  - Loop indication
- **Support Auto Test Function For Mass-production**
  - Auto generate test frames
  - Shown the result on LED output
- **Interrupt Pin For PHY Mode/Link/SMI R/W**
  - Complete notification
- **Special TAG Supported**
- **OAM support (IEEE 802.3 ah)**
  - Auto discovery
  - Fault indication
  - Remote LoopBack test
- **IEEE1588 stamp support**
  - 16 time stamps for In/Egress per port
  - 8 time stamps for input event trigger
  - Event trigger stamp supported
  - Pulse Per Second (PPS) output supported
  - PTP trigger out supported
- **IC+ Remote Management Protocol (IRMP)**
- **Build-in SRAM Self Test (BIST)**
- **sFlow support**
- **EoC cable failure auto detection and isolation hardware**
- **Protocol forwarding to CPU or broadcast or dropped**
  - LACP,LLDP,IGMP,MLD,ICMP,BPDU,802.1x, GARP
- **IPv6 function support**
  - TCP/UDP port number and FLAG
  - Finding next header for ICMPv6, authentication, encapsulation, fragment and user define

- **Embedded 32-bit CPU**
  - Up to 450 MHz clock rate
  - Big-endian data format
  - 32K instruction cache and 32K data cache, 4-way set associative
  - 32 joint translation look aside buffers (TLB)
  - IIC bus for access to EEPROM or standard IIC slave device
  - Up to 4 interrupt inputs (programmable level or edge trigger)
  - 400MHz DDR3 SDRAM with 16 bit data bus
  - Support up to two 16MB SPI flash memory
  - 2 general-purpose timers
  - 2 watchdog timer to re-boot CPU
  - An UART with 16-byte FIFO

- **Only one 25MHz Crystal needed**
- **Adjustable IO voltage**
  - (3.3/2.5V GMII, 2.5~1.8V RGMII)
- **Built-in 1.5V and 1.8V regulator**
- **416 balls BGA (27x27 mm). Lead-free package**

General Description

IP1829 is a non-blocking, store-and-forward architecture switch controller, which builds 24-port 10/100Mbps Fast Ethernet MAC and PHY, 5-port Gigabit Ethernet MAC including 2-port SGMII/Fiber, 2-port RGMII, and one-port GMII/RGMII/MII for embedded 450MHz CPU in a single chip.

IP1829 embeds a 4Mb SRAM for the use of packet buffer. It also provides various 2-wire interfaces, such as CPU interface, SMI, and EEPROM interface, which allow the user to access the internal register, external PHY's registers and EEPROM data. The serial LED can show the status of each port (such as Link, Speed, Activity and so on) by using 74HC164 or IP403 external device through 2-wire (LEDCLK, LEDDATA) signals driving from IP1829.

For avoiding loop occur, IP1829 supports STP, RSTP and MSTP. Even a hardware loop detection mechanism is supported.

There are 16K entries in Lookup table. Hashing method can be selected either direct or CRC hashing for MAC address learning. Lookup Table aging time can be adjustable ranging from 55 seconds to 500.6 hours. IP1829 also provides the MAC learning threshold to limit the number of addresses learning.

An independent Multicast table supports 256 entries. For the Internet Group Management Protocol, IP1829 supports IGMP v1/v2/v3 for IPv4 and MLD v1/v2 for IPv6 packet snooping and aging time function. For the IGMPv3 and MLDv2 application, IP1829 provides up to 10 sets IPv4 or 4 sets IPv6 address per entry for source list table.

IP1829 has 4k entries for 802.1Q VLAN, which provides more security for VLAN member, and supports Independent VLAN Learning (IVL) and Share VLAN Learning (SVL). Further, IP1829 also has add/remove C-tag, S-tag, VLAN remarking, uplink link port and inactive VID redirect functions for the flexible VLAN application.

IP1829 has 128 entries for ACL table. The ACL (Address Control List) function provides advanced and flexible control mechanism to decide what packet should do (action) if packet matches ACL rule. ACL Rule and action:

- Rules: (Port ID, DA, SA, DA/SA, DIP, SIP, TCP/UDP Port Number (DP and SP))
- Actions: (Sniffer, Insert/remove Tag, Priority, Redirection, Trap to CPU, BW limited, DSCP, sFlow, Drop, PTP, MIB Counter)

For the Quality of Service application, IP1829 supports port-based, 802.1Q tag based, ACL based, IP CoS/DSCP based, SMAC based, IP address based, IGMP based and WAN/LAN based to decide the priority of output frame. For the Remarking application, IP1829 supports remarking for the DSCP, Crag and Stag value of transmit packet.

For the link aggregation application, IP1829 provides eight hashing methods (Port ID, DA, SA, DA/SA, DIP, SIP, DP, and SP) and support six trunk groups' sets.

For meeting the various network applications, IP1829 also supports storm control, bandwidth rate control, Output Queues functions, Sniffer, sFlow, PTP, MIB counters and eight LED display modes. Therefore, IP1829 has the best adaptability and capability for the future network conditions.

IP1829 supports the web based management interface, such as Microsoft Internet Explorer or Mozilla Firefox, Google chrome, user can more easily configure IP1829's functions by these browsers, and no extra program is needed. Besides, IP1829 also provides IRMP(IC+ remote management protocol) to let the users remotely configure the registers of IP1829.

Table of Contents

Features List 1
General Description 3
Table of Contents 4
List of Figures 7
List of Tables 8
Revision History 9
1 Pin Diagram 10
2 Block Diagram 12
3 Application Diagram 13
4 Pin Description 14
5 Function Description 30
5.1 Switch Engine and Queue Management 30
5.1.1 Packet forwarding 30
5.1.1.1 Address Learning and Hashing 30
5.1.1.2 Port Base Address Flush 30
5.1.1.3 Aging Time 31
5.1.1.4 802.1D packet forwarding 31
5.1.2 Flow Control 31
5.1.2.1 IEEE802.3x 31
5.1.2.2 Backpressure 32
5.1.2.3 Flow control auto off for high priority packet 32
5.2 Bandwidth Control 32
5.2.1 Broadcast Storm Control 33
5.2.1.1 Multicast and DLF Storm Control 33
5.2.1.2 ARP Storm Control 33
5.2.1.3 ICMP Storm Control 33
5.2.2 Interface 35
5.2.2.1 MDI (Port1~Port24) 35
5.2.2.2 SGMII/Fiber (Port25, Port26) 35
5.2.2.3 RGMII (Port27, Port28) 36
5.2.2.4 GMII (Port29) 37
5.2.3 External CPU Read / Write interface 38
5.2.4 EEPROM Interface 39
5.2.5 MIB Counter 40
5.2.6 Auto Factory Test (AFT) 40
5.2.7 LED display mode 41
5.3 VLAN 43
5.3.1 Port Based VLAN 43
5.3.2 Tag Based VLAN 43
5.3.3 Protocol Base VLAN 43
5.3.4 VLAN Function 45
5.3.4.1 Add/modify VLAN Tag 45
5.3.4.2 Remove VLAN Tag 45
5.3.4.3 VLAN up Link 46
5.3.4.4 Force the Incoming Packet Use PVID 46
5.3.4.5 VLAN Ingress Check 46
5.3.4.6 VLAN Egress Rule 47
5.3.4.7 VLAN exclusive port 47
5.3.4.8 Inactive VID redirect 47
5.4 Class Of Service (CoS) 48
5.4.1 Output Queue Schedule Mode with Priority 48

5.4.2 Port Based Priority 49
5.4.3 802.1Q VLAN Tag Based Priority 49
5.4.4 IP ToS/ DSCP CoS Based Priority 49
5.4.5 TCP/UDP Port Number Based Priority 50
5.4.6 Source MAC address Priority 51
5.4.7 VID based VLAN priority 52
5.4.8 IP address Priority 52
5.4.9 IP multicast Priority 52
5.4.10 ACL Priority 52
5.5 Capture Ethernet protocol frame & IP packet to CPU port 53
5.5.1 In Band Management Frame 53
5.5.2 Block Broadcast Frames to CPU Port 53
5.5.3 ARP and ICMP Storm Control 53
5.5.4 Block ARP to CPU Port 54
5.5.5 Ethernet L2 protocol packet capture 54
5.5.6 Ethernet L3 protocol packet capture 55
5.5.7 PPPoE Protocol Check 55
5.6 Security 56
5.6.1 MAC Address Based Security 56
5.6.2 802.1x Port Base Security 56
5.6.3 IP Address Base Security 56
5.6.4 TCP/UDP Port Number Based Security 57
5.6.5 Port Mirroring Security (Sniffer) 58
5.7 WAN/LAN Port Filtering 60
5.8 IEEE 1588 Precision Timing Protocol (PTP) 62
5.9 Hardware Loop detection 62
5.10 Trunk Channel 63
5.10.1 Trunk Channel Behavior 63
5.10.2 Load Balance 63
5.11 Spanning Tree 65
5.11.1 BPDU Packet Forwarding 65
5.11.2 Port States 65
5.12 IGMP Snooping 66
5.13 IRMP (ICPLUS remote management protocol) 67
5.14 IPv6 related functions configuration 68
5.15 ACL 69
5.16 OAM 69
5.17 Special tag 70
5.17.1 Special Tag for TX (From CPU to switch) 70
5.17.2 Special Tag for RX (From switch to CPU) 71
5.18 sFlow 73
5.19 Embedded 32-bit CPU 74
5.19.1 CPU Block Diagram 74
5.19.2 CPU Features 75
5.19.3 DDR3 Memory Controller 75
5.19.4 SPI Flash Controller 75
5.19.4.1 Direct mapping mode (D-MAP) 75
5.19.4.2 User mode 75
5.19.5 The Ethernet Gigabit MAC 75
5.19.6 Interrupt Controller 76
5.19.7 Timer and Counter 76
5.19.8 General-Purpose I/O 76
5.19.9 SPI Controller 76
5.19.10 UART 76
5.19.11 I^2C Controller 77

6 Register Description 78
6.1 PHY Register Map 78
6.1.1 MII Register 79
6.1.2 MMD Control Register 86
6.1.3 MMD Data Register 87
6.1.4 Register Page mode Control Register 90
6.1.5 WOL+ Control Register 91
6.1.6 MDI/MDIX Control Register 93
6.2 Switch Register 94
6.2.1 Switch Page Map 94
6.2.2 Switch Register Map 94
6.3 MAC Control Register 95
6.4 ARL Control Register Page 1 110
6.5 ARL Control Register Page 2 122
6.6 SMI Control Register 128
6.7 OAM Control Register 138
6.8 OAM Indirect Registers for Each Port 139
6.9 RxDMA Control Register 142
6.10 TxDMA Control Register 147
6.11 Output Queue Control Register 153
6.12 PTP Control Register 165
6.13 IRMP Control Register 173
6.14 Advance EEPROM code Register 175
6.15 45B45B45B45B45BMISC Register 176
7 Electrical Characteristics 184
7.1 Absolute Maximum Rating 184
8 AC Characteristics 185
8.1 Power On Sequence and Reset Timing 185
9 DC Characteristics 190
10 Serial Transmitter/Receiver DC characteristic 191
Order Information 192
Package Detail 193

List of Figures

Figure 1 IP1829 BGA416 ball Diagram 11
Figure 2 Block Diagram 12
Figure 3 Dumb Switch Application Diagram 13
Figure 4 Smart / Management Switch Application Diagram 13
Figure 5 SGMII / Fiber Application diagram 35
Figure 6 Waveform of RGMII 36
Figure 7 RGMII Application diagram 36
Figure 8 GMII Application diagram 37
Figure 9 MII Application diagram 37
Figure 10 External CPU Read / Write interface diagram 38
Figure 11 2 bit stream mono-color LED application diagram 42
Figure 12 Frame Format of Inserting VLAN or/and Special Tag 46
Figure 13 Frame Format of IPv4 TOS 49
Figure 14 Frame Format of IPv6 DSCP 50
Figure 15 Port Mirroring Security Block Diagram 58
Figure 16 WAN Port Filtering Block Diagram 60
Figure 17 Trunk Channel Behavior Block Diagram 63
Figure 18 Load Balance Block Diagram 64
Figure 19 BPDU Packet Forwarding Block Diagram 65
Figure 20 IGMP Snooping Block Diagram 66
Figure 21 802.3 OAM Frame Format 69
Figure 22 OAMPDU messages Frame Format 69
Figure 23 Special Tag for TX Frame Format (From CPU to switch) 70
Figure 24 Special Tag for RX Frame Format (From switch to CPU) 71
Figure 25 sFlow function diagram 73
Figure 26 Power On Sequence and Reset timing Diagram 185
Figure 27 MDIO Read / Write cycle timing Diagram 186
Figure 28 CPU Serial Bus timing Diagram 187

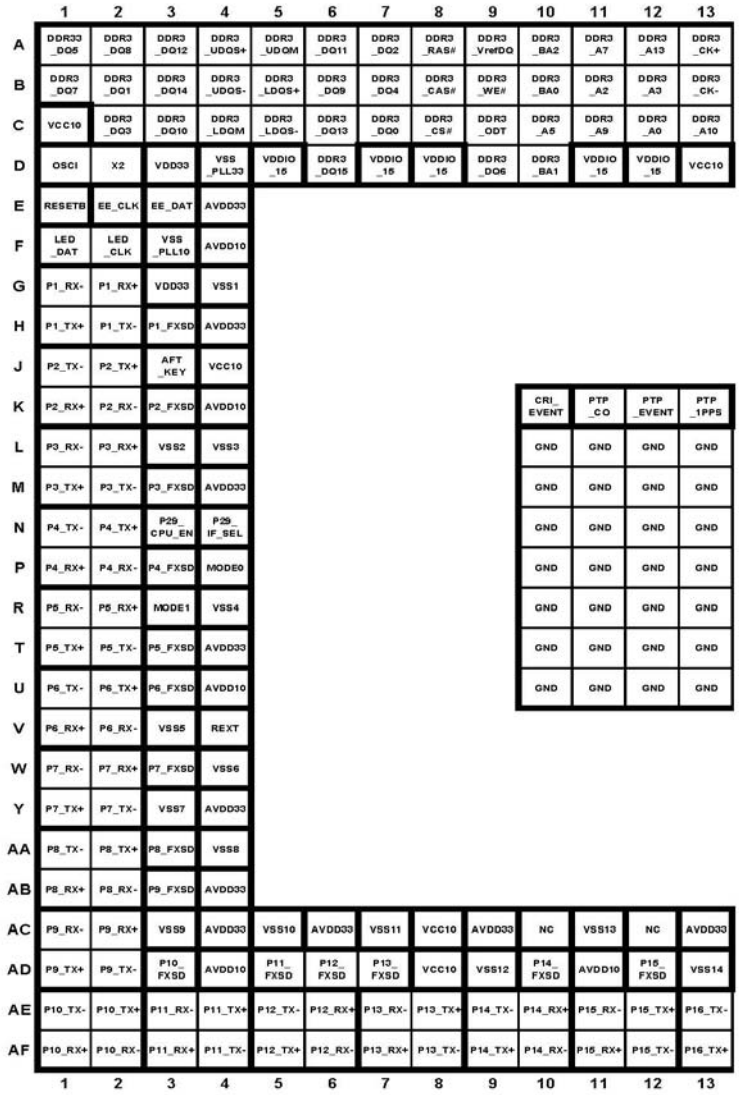
List of Tables

Table 1 Pin Symbol Abbreviations 14
Table 2 MDI Pin 14
Table 3 Gigabit port SGMII and 1000 Fiber interface Pin 17
Table 4 RGMII Pin 18
Table 5 GMII / GPIO Pin 19
Table 6 EEPROM Pin 21
Table 7 CPU R/W Interface Pin 21
Table 8 Serial LED Pin 21
Table 9 UART Pin 21
Table 10 JTAG Pin 21
Table 11 IEEE-1588 PTP Pin 22
Table 12 GPIO Pin 22
Table 13 DDR3 memory interface Pin 23
Table 14 SPI Flash memory Pin 24
Table 15 Miscellaneous Pin 25
Table 16 Power on Setting 26
Table 17 Power & Ground Pin 27
Table 18 Broadcast /ARP/ICMP Storm Counter Clear Period Selection Table 34
Table 19 Command Mode Format of EEPROM 39
Table 20 Address Format of Port MIB Counter 40
Table 21 LED display behavior vs. LED mode 41
Table 22 LED display Sequence. 41
Table 23 PVID index search VLAN table 44
Table 24 Forward the Packet with VLAN Configuration Table 45
Table 25 Output Queue Schedule Mode Description Table 48
Table 26 TCP/UDP Port Number priority Selection Table 51
Table 27 ARP and ICMP Storm Counter Clear Period Selection Table 54
Table 28 Layers Two Protocol Frames Selection Table 54
Table 29 Level Three Protocol Frames Selection Table 55
Table 30 TCP/UDP Port Number Based Security Selection Table 57
Table 31 Host / Client Forwarding WAN / LAN and Packet drop setting Condition Table 61
Table 32 Port States Selection Table 66
Table 33 ICPLUS remote management protocol format 67
Table 34 PHY Register Map 78
Table 35 Register Symbol Abbreviations 78
Table 37 MDI/MDIX Control Register 93
Table 38 MAC Control Register 95

Revision History

Revision #	History Description	Date
IP1829-DS-R01	Initial release.	2013/01/29

1 Pin Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DDR33 _DQ5	DDR3 _DQ8	DDR3 _DQ12	DDR3 _UDQS+	DDR3 _UDQM	DDR3 _DQ11	DDR3 _DQ2	DDR3 _RAS#	DDR3 _VrefDQ	DDR3 _BA2	DDR3 _A7	DDR3 _A13	DDR3 _CK+
B	DDR3 _DQ7	DDR3 _DQ1	DDR3 _DQ14	DDR3 _UDQS-	DDR3 _LDQS+	DDR3 _DQ9	DDR3 _DQ4	DDR3 _CAS#	DDR3 _WE#	DDR3 _BA0	DDR3 _A2	DDR3 _A3	DDR3 _CK-
C	VCC10	DDR3 _DQ3	DDR3 _DQ10	DDR3 _LDQM	DDR3 _LDQS-	DDR3 _DQ13	DDR3 _DQ0	DDR3 _CS#	DDR3 _ODT	DDR3 _A5	DDR3 _A9	DDR3 _A0	DDR3 _A10
D	OSCI	X2	VDD33	VSS _PLL33	VDDIO _15	DDR3 _DQ15	VDDIO _15	VDDIO _15	DDR3 _DQ6	DDR3 _BA1	VDDIO _15	VDDIO _15	VCC10
E	RESETB	EE_CLK	EE_DAT	AVDD33									
F	LED _DAT	LED _CLK	VSS _PLL10	AVDD10									
G	P1_RX-	P1_RX+	VDD33	VSS1									
H	P1_TX+	P1_TX-	P1_FXSD	AVDD33									
J	P2_TX-	P2_TX+	AFT _KEY	VCC10									
K	P2_RX+	P2_RX-	P2_FXSD	AVDD10									
L	P3_RX-	P3_RX+	VSS2	VSS3									
M	P3_TX+	P3_TX-	P3_FXSD	AVDD33									
N	P4_TX-	P4_TX+	P29_ CPU_EN	P29_ IF_SEL									
P	P4_RX+	P4_RX-	P4_FXSD	MODE0									
R	P5_RX-	P5_RX+	MODE1	VSS4									
T	P5_TX+	P5_TX-	P5_FXSD	AVDD33									
U	P6_TX-	P6_TX+	P6_FXSD	AVDD10									
V	P6_RX+	P6_RX-	VSS5	REXT									
W	P7_RX-	P7_RX+	P7_FXSD	VSS6									
Y	P7_TX+	P7_TX-	VSS7	AVDD33									
AA	P8_TX-	P8_TX+	P8_FXSD	VSS8									
AB	P8_RX+	P8_RX-	P9_FXSD	AVDD33									
AC	P9_RX-	P9_RX+	VSS9	AVDD33	VSS10	AVDD33	VSS11	VCC10	AVDD33	NC	VSS13	NC	AVDD33
AD	P9_TX+	P9_TX-	P10_ FXSD	AVDD10	P11_ FXSD	P12_ FXSD	P13_ FXSD	VCC10	VSS12	P14_ FXSD	AVDD10	P15_ FXSD	VSS14
AE	P10_TX-	P10_TX+	P11_RX-	P11_TX+	P12_TX-	P12_RX+	P13_RX-	P13_TX+	P14_TX-	P14_RX+	P15_RX-	P15_TX+	P16_TX-
AF	P10_RX+	P10_RX-	P11_RX+	P11_TX-	P12_TX+	P12_RX-	P13_RX+	P13_TX-	P14_TX+	P14_RX-	P15_RX+	P15_TX-	P16_TX+

CRI_ EVENT	PTP _CO	PTP _EVENT	PTP _1PPS
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND
GND	GND	GND	GND

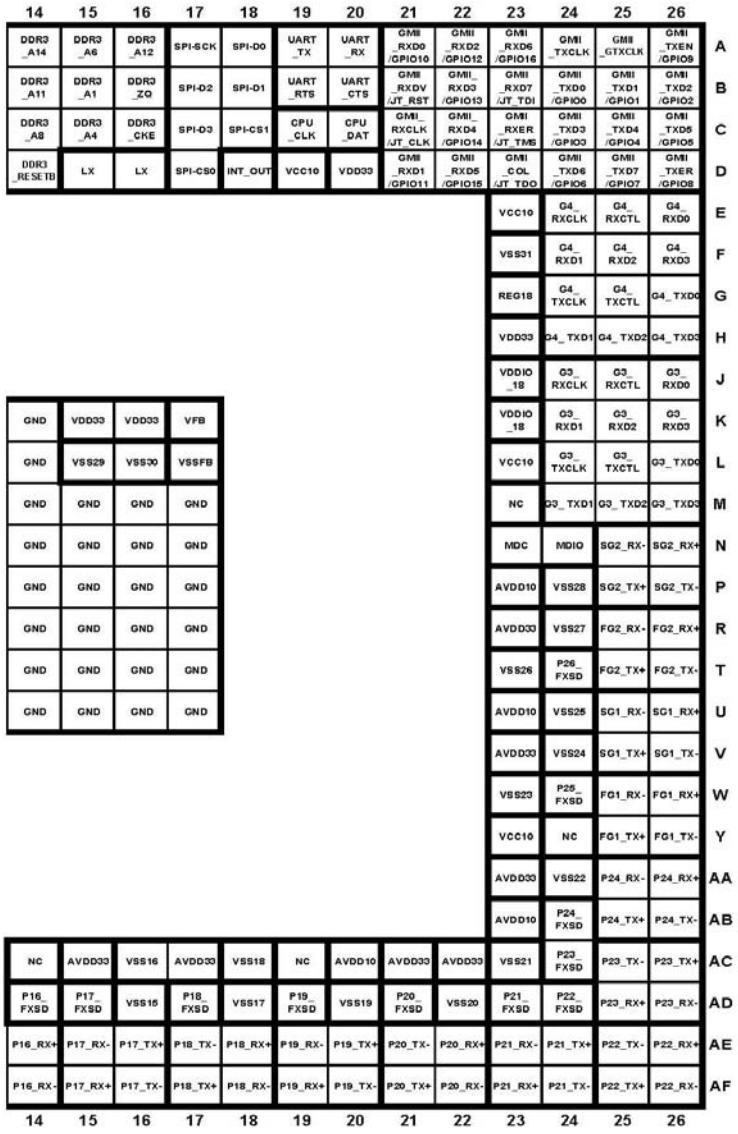


Figure 1 IP1829 BGA416 ball Diagram

2 Block Diagram

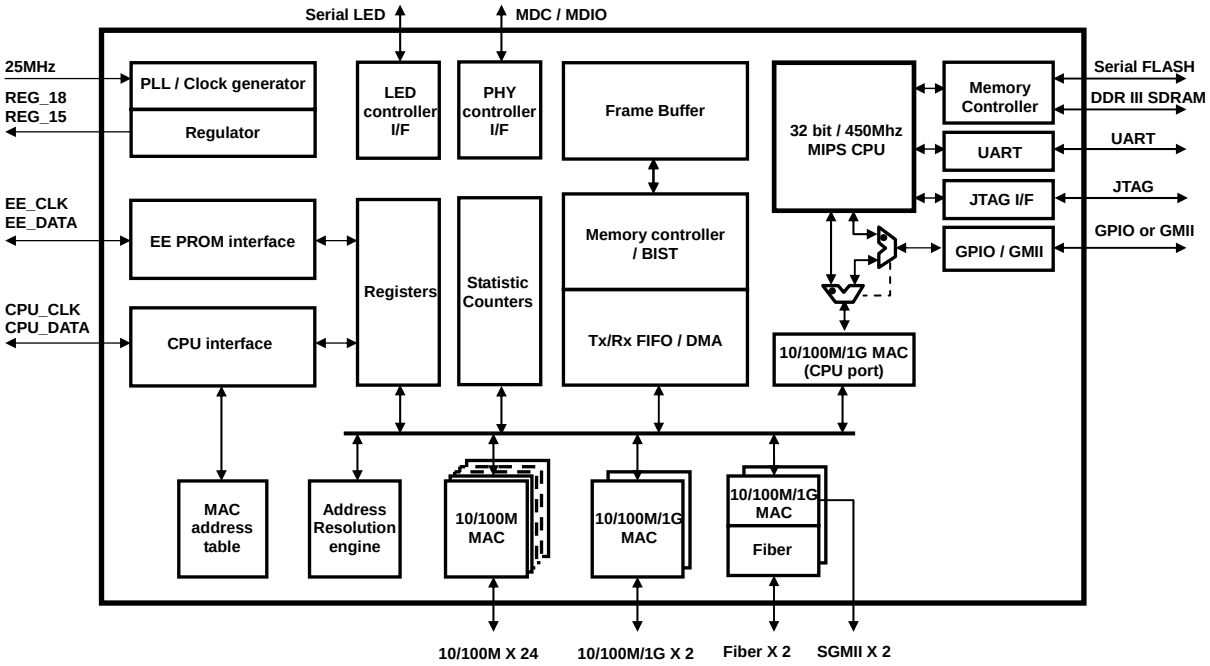


Figure 2 Block Diagram

3 Application Diagram

24 10/100M + 4G Combo Dumb Switch Application

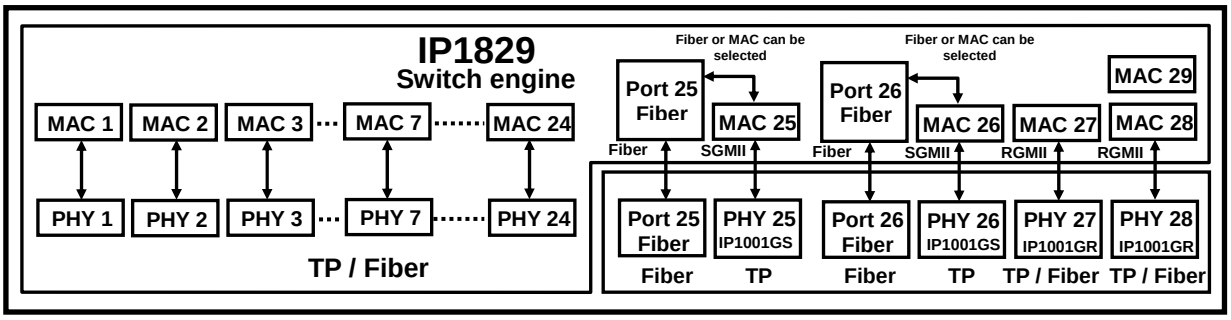


Figure 3 Dumb Switch Application Diagram

24 10/100M + 4G Combo Smart / Management Switch Application

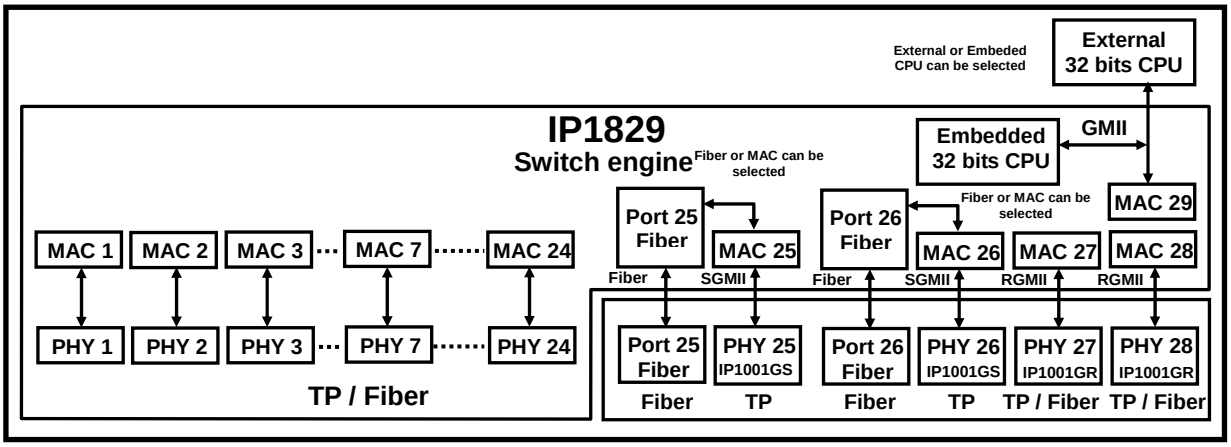


Figure 4 Smart / Management Switch Application Diagram

4 Pin Description

Table 1 Pin Symbol Abbreviations

Type	Description	Type	Description
I	Input pin	IL	Input latched upon reset
O	Output pin	PD	Pulled down with internal resistor
I/O	Bi-direction input/output	PU	Pulled up with internal resistor
P	Power or ground		

Table 2 MDI Pin

Pin No.	Label	Type	Description
Medium Dependent Interface (port 1~24,PHY address 8~31)			
H1 H2 G2 G1	P1_TX+ P1_TX- P1_RX+ P1_RX-	O O I I	**Port 01 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 01. Auto MDI/MDIX can reverse the pairs P1_TX+/P1_TX- and P1_RX+/P1_RX-.
J2 J1 K1 K2	P2_TX+ P2_TX- P2_RX+ P2_RX-	O O I I	**Port 02 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 02. Auto MDI/MDIX can reverse the pairs P2_TX+/P2_TX- and P2_RX+/P2_RX-.
M1 M2 L2 L1	P3_TX+ P3_TX- P3_RX+ P3_RX-	O O I I	**Port 03 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 03. Auto MDI/MDIX can reverse the pairs P3_TX+/P3_TX- and P3_RX+/P3_RX-.
N2 N1 P1 P2	P4_TX+ P4_TX- P4_RX+ P4_RX-	O O I I	**Port 04 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 04. Auto MDI/MDIX can reverse the pairs P4_TX+/P4_TX- and P4_RX+/P4_RX-.
T1 T2 R2 R1	P5_TX+ P5_TX- P5_RX+ P5_RX-	O O I I	**Port 05 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 05. Auto MDI/MDIX can reverse the pairs P5_TX+/P5_TX- and P5_RX+/P5_RX-.
U2 U1 V1 V2	P6_TX+ P6_TX- P6_RX+ P6_RX-	O O I I	**Port 06 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 06. Auto MDI/MDIX can reverse the pairs P6_TX+/P6_TX- and P6_RX+/P6_RX-.
Y1 Y2 W2 W1	P7_TX+ P7_TX- P7_RX+ P7_RX-	O O I I	**Port 07 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 07. Auto MDI/MDIX can reverse the pairs P7_TX+/P7_TX- and P7_RX+/P7_RX-.
AA2 AA1 AB1 AB2	P8_TX+ P8_TX- P8_RX+ P8_RX-	O O I I	**Port 08 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 08. Auto MDI/MDIX can reverse the pairs P8_TX+/P8_TX- and P8_RX+/P8_RX-.
AD1 AD2 AC2 AC1	P9_TX+ P9_TX- P9_RX+ P9_RX-	O O I I	**Port 09 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 09. Auto MDI/MDIX can reverse the pairs P9_TX+/P9_TX- and P9_RX+/P9_RX-.

Pin No.	Label	Type	Description
AE2 AE1 AF1 AF2	P10_TX+ P10_TX- P10_RX+ P10_RX-	O O I I	**Port 10 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 10. Auto MDI/MDIX can reverse the pairs P10_TX+/P10_TX- and P10_RX+/P10_RX-.
AE4 AF4 AF3 AE3	P11_TX+ P11_TX- P11_RX+ P11_RX-	O O I I	**Port 11 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 11. Auto MDI/MDIX can reverse the pairs P11_TX+/P11_TX- and P11_RX+/P11_RX-.
AF5 AE5 AE6 AF6	P12_TX+ P12_TX- P12_RX+ P12_RX-	O O I I	**Port 12 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 12. Auto MDI/MDIX can reverse the pairs P12_TX+/P12_TX- and P12_RX+/P12_RX-.
AE8 AF8 AF7 AE7	P13_TX+ P13_TX- P13_RX+ P13_RX-	O O I I	**Port 13 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 13. Auto MDI/MDIX can reverse the pairs P13_TX+/P13_TX- and P13_RX+/P13_RX-.
AF9 AE9 AE10 AF10	P14_TX+ P14_TX- P14_RX+ P14_RX-	O O I I	**Port 14 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 14. Auto MDI/MDIX can reverse the pairs P14_TX+/P14_TX- and P14_RX+/P14_RX-.
AE12 AF12 AF11 AE11	P15_TX+ P15_TX- P15_RX+ P15_RX-	O O I I	**Port 15 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 15. Auto MDI/MDIX can reverse the pairs P15_TX+/P15_TX- and P15_RX+/P15_RX-.
AF13 AE13 AE14 AF14	P16_TX+ P16_TX- P16_RX+ P16_RX-	O O I I	**Port 16 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 16. Auto MDI/MDIX can reverse the pairs P16_TX+/P16_TX- and P16_RX+/P16_RX-.
AE16 AF16 AF15 AE15	P17_TX+ P17_TX- P17_RX+ P17_RX-	O O I I	**Port 17 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 17. Auto MDI/MDIX can reverse the pairs P17_TX+/P17_TX- and P17_RX+/P17_RX-.
AF17 AE17 AE18 AF18	P18_TX+ P18_TX- P18_RX+ P18_RX-	O O I I	**Port 18 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 18. Auto MDI/MDIX can reverse the pairs P18_TX+/P18_TX- and P18_RX+/P18_RX-.
AE20 AF20 AF19 AE19	P19_TX+ P19_TX- P19_RX+ P19_RX-	O O I I	**Port 19 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 19. Auto MDI/MDIX can reverse the pairs P19_TX+/P19_TX- and P19_RX+/P19_RX-.
AF21 AE21 AE22 AF22	P20_TX+ P20_TX- P20_RX+ P20_RX-	O O I I	**Port 20 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 20. Auto MDI/MDIX can reverse the pairs P20_TX+/P20_TX- and P20_RX+/P20_RX-.
AE24 AF24 AF23 AE23	P21_TX+ P21_TX- P21_RX+ P21_RX-	O O I I	**Port 21 Media Dependent Interface** The differential data from the media is transmitted and received on two pairs for port 21. Auto MDI/MDIX can reverse the pairs P21_TX+/P21_TX- and P21_RX+/P21_RX-.

<table>
<tr><th>Pin No.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td>AF25
AE25
AE26
AF26</td><td>P22_TX+
P22_TX-
P22_RX+
P22_RX-</td><td>O
O
I
I</td><td>Port 22 Media Dependent Interface
The differential data from the media is transmitted and received on two pairs for port 22. Auto MDI/MDIX can reverse the pairs P22_TX+/P22_TX- and P22_RX+/P22_RX-.</td></tr>
<tr><td>AC26
AC25
AD25
AD26</td><td>P23_TX+
P23_TX-
P23_RX+
P23_RX-</td><td>O
O
I
I</td><td>Port 23 Media Dependent Interface
The differential data from the media is transmitted and received on two pairs for port 23. Auto MDI/MDIX can reverse the pairs P23_TX+/P23_TX- and P23_RX+/P23_RX-.</td></tr>
<tr><td>AB25
AB26
AA26
AA25</td><td>P24_TX+
P24_TX-
P24_RX+
P24_RX-</td><td>O
O
I
I</td><td>Port 24 Media Dependent Interface
The differential data from the media is transmitted and received on two pairs for port 24. Auto MDI/MDIX can reverse the pairs P24_TX+/P24_TX- and P24_RX+/P24_RX-.</td></tr>
<tr><td>H3
K3
M3
P3
T3
U3
W3
AA3
AB3
AD3
AD5
AD6
AD7
AD10
AD12
AD14
AD15
AD17
AD19
AD21
AD23
AD24
AC24
AB24</td><td>P1_FXSD
P2_FXSD
P3_FXSD
P4_FXSD
P5_FXSD
P6_FXSD
P7_FXSD
P8_FXSD
P9_FXSD
P10_FXSD
P11_FXSD
P12_FXSD
P13_FXSD
P14_FXSD
P15_FXSD
P16_FXSD
P17_FXSD
P18_FXSD
P19_FXSD
P20_FXSD
P21_FXSD
P22_FXSD
P23_FXSD
P24_FXSD</td><td>I</td><td>Port 1~ Port 24 fiber signal detect
The Fiber Signal Detect input voltage level and behavior are as below table :
<table>
<tr><th>Voltage on Pxx_FXSD</th><th>TP port</th><th>Fiber port</th><th>Fiber signal detect</th><th>Condition</th></tr>
<tr><td>< 0.4V</td><td>V</td><td>--</td><td>--</td><td>TP mode</td></tr>
<tr><td>> 1.2 V ; < 1.7 V</td><td>--</td><td>V</td><td>Off</td><td>Fiber mode / unlink</td></tr>
<tr><td>> 1.95 V ; < 3.3 V</td><td>--</td><td>V</td><td>On</td><td>Fiber mode / link</td></tr>
</table></td></tr>
</table>

Table 3 Gigabit port SGMII and 1000 Fiber interface Pin

Pin No.	Label	Type	Description
Gigabit port SGMII and 1000 Fiber interface (G1:port 25, PHY address 2 for SGMII / 6 for 1000 Fiber; G2:port 26, PHY address 3 for SGMII / 7 for 1000 Fiber)			
V26	SG1_TX-	O	Giga port 1 SGMII TXM
V25	SG1_TX+	O	Giga port 1 SGMII TXP
U26	SG1_RX+	I	Giga port 1 SGMII RXP
U25	SG1_RX-	I	Giga port 1 SGMII RXM
Y26	FXG1_TX-	O	Giga port 1 Fiber TXM. There is an internal 100 ohms resistor between FXG1_TX+ and FXG1_TX-.
Y25	FXG1_TX+	O	Giga port 1 Fiber TXP
W26	FXG1_RX+	I	Giga port 1 Fiber RXP. There is an internal 100 ohms resistor between FXG1_RX+ and FXG1_RX-
W25	FXG1_RX-	I	Giga port 1 Fiber RXM
W24	P25_FXSD	I	Giga port 1 Signal detect The input threshold voltage is around 1.6v. It is recommended to use a fiber MAU, which supports TTL level SD signal.
P26	SG2_TX-	O	Giga port 2 SGMII TXM
P25	SG2_TX+	O	Giga port 2 SGMII TXP
N26	SG2_RX+	I	Giga port 2 SGMII RXP
N25	SG2_RX-	I	Giga port 2 SGMII RXM
T26	FXG2_TX-	O	Giga port 2 Fiber TXM. There is an internal 100 ohms resistor between FXG2_TX+ and FXG2_TX-.
T25	FXG2_TX+	O	Giga port 2 Fiber TXP
R26	FXG2_RX+	I	Giga port 2 Fiber RXP. There is an internal 100 ohms resistor between FXG2_RX+ and FXG2_RX-
R25	FXG2_RX-	I	Giga port 2 Fiber RXM
T24	P26_FXSD	I	Giga port 2 Signal detect The input threshold voltage is around 1.6V. It is recommended to use a fiber MAU, which supports TTL level SD signal.

Table 4 RGMII Pin

Pin No.	Label	Type	Description
RGMII (G3:port 27, PHY address 4; G4:port 28, PHY address 5) Port 27 I/O configuration by Page C register 8 Port 28 I/O configuration by Page C register 9			
M26 M25 M24 L26 H26 H25 H24 G26	G3_TXD3, G3_TXD2, G3_TXD1, G3_TXD0, G4_TXD3, G4_TXD2, G4_TXD1, G4_TXD0	O	**RGMII Transmit Data** When it works in 10BASE-T or 100BASE-TX mode, TXD[3:0] present the transmit data at the rising edge of TXC, and when it works in 1000BASE-T mode, TXD[3:0] present the low nibble of transmit data byte at the rising edge of TXC, and present the high nibble of transmit data byte at the falling edge of TXC.
L25 G25	G3_TXCTL, G4_TXCTL	O	**RGMII Transmit Control** A GMII-like signal “TX_EN” is presented on the rising edge of TXC and a GMII-like signal “TX_ER” is derived by logical operation of the value of TXCTL at the falling edge of TXC, with the latched value of TX_EN, per RGMII specification.
L24 G24	G3_TXCLK G4_TXCLK	O	**RGMII Transmit Clock** It is a 125Mhz clock in 1000BASE-T mode, 25 MHz clock in 100BASE-TX mode, or a 2.5 MHz clock in 10BASE-T mode. IP1829 uses the clock to sample TX_CTL and TXD [3:0].
K26 K25 K24 J26 F26 F25 F24 E26	G3_RXD3, G3_RXD2, G3_RXD1, G3_RXD0, G4_RXD3, G4_RXD2, G4_RXD1, G4_RXD0	I	**RGMII Receive Data** When the PHY works in 10BASE-T or 100BASE-TX mode, RXD[3:0] latch the receive data at the rising edge of RXC, and when it works in 1000BASE-T mode, RXD[3:0] latch the low nibble of receive data byte at the rising edge of RXC, and present the high nibble of transmit data byte at the falling edge of RXC.
J25 E25	G3_RXCTL, G4_RXCTL	I	**RGMII Receive Control** A GMII-like signal “RXCTL” is presented on the rising edge of RXC and a GMII-like signal “RX_ER” is derived by logical operation of the value of RXCTL at the falling edge of RXC, with the latched value of RX_DV, per RGMII specification.
J24 E24	G3_RXCLK, G4_RXCLK	I	**RGMII Receive Clock.** It is a 125 MHz, 25MHz, or 2.5MHz reference clock from a Gigabit PHY working in 1000BASE-T, 100BASE-TX, or 10BASE-T.

Table 5 GMII / GPIO Pin

<table>
<tr><th rowspan="3">Pin no.</th><th colspan="2">Label</th><th rowspan="3">Type</th><th rowspan="3">Description</th></tr>
<tr><th colspan="2">MAC Interface</th></tr>
<tr><th>GMII</th><th>MII</th></tr>
<tr><td colspan="5">GMII (RGMII) / MII (G5: port 29, PHY address 1)</td></tr>
<tr><td>A25</td><td>GMII_
GTXCLK</td><td>--</td><td>O</td><td>GMII Transmit Clock

MDI speed: 1000Mbps — 125MHz output. IP1829 utilizes this clock to sample GMII_TXD [7:0], GMII_TXER and GMII_TXEN at the rising edge.
MDI speed: 10/100Mbps — In RGMII mode, 25MHz for 100Mb, 2.5MHz for 10Mb</td></tr>
<tr><td>A24</td><td>--</td><td>GMII_
TXCLK</td><td>I/O</td><td>MII Transmit Clock
@ PHY mode, it’s output; @ MAC mode, it’s input (default.)
MDI speed: 1000Mbps — Not used.
MDI speed: 100Mbps — 25MHz. IP1829 uses the clock to sample GMII_TXEN, GMII_TXER, and GMII_TXD [3:0].
MDI speed: 10Mbps — 2.5MHz. IP1829 uses the clock to sample GMII_TXEN, GMII_TXER, and GMII_TXD [3:0].</td></tr>
<tr><td>A26</td><td colspan="2">GMII_TXEN
(TXCTL)</td><td>O</td><td>GMII/MII Transmit Enable

MDI speed: 1000Mbps 100Mbps, 10Mbps — Indicates the valid data is present on the data bus of TXD. Synchronous to the rising edge of GMII_GTXCLK (1000M) or GMII_TXCLK (10/100M). When operating RGMII mode, this pin is TXCTL.</td></tr>
<tr><td>D25
D24
C26
C25</td><td>GMII_TXD7
GMII_TXD6
GMII_TXD5
GMII_TXD4</td><td>--</td><td>O</td><td>GMII Transmit Data (high nibble)
MDI speed: 1000Mbps — Transmit data output bus that is sent synchronously at the rising edge of GMII_GTXCLK
MDI speed: 10/100Mbps — Not used.</td></tr>
<tr><td>C24
B26
B25
B24</td><td colspan="2">GMII_TXD3
GMII_TXD2
GMII_TXD1
GMII_TXD0</td><td>O</td><td>GMII/MII Transmit Data

Transmit data output bus that is sent synchronously at the rising edge of GMII_GTXCLK(1000M) or GMII_TXCLK (10/100M).</td></tr>
<tr><td>D26</td><td colspan="2">GMII_TXER</td><td>O</td><td>GMII and MII Transmit Error

MDI speed: 1000Mbps — A “high” state present on this pin indicates transmit data error or carrier extension. It is synchronous to GMII_GTXCLK
MDI speed: 100Mbps, 10Mbps — A “high” state present on this pin indicates transmit data error. It is synchronous to TXCLK</td></tr>
</table>

<table>
<tr><th rowspan="3">Pin no.</th><th colspan="2">Label</th><th rowspan="3">Type</th><th rowspan="3">Description</th></tr>
<tr><th colspan="2">MAC Interface</th></tr>
<tr><th>GMII</th><th>MII</th></tr>
<tr><td>C21</td><td colspan="2">GMII_RXCLK</td><td>I</td><td>GMII/MII Receive Clock.

<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>1000Mbps</td><td>125MHz output.
IP1829 sends out RXD [7:0], GMII_RXDV and GMII_RXER at the rising edge of GMII_RXCLK.</td></tr>
<tr><td>100Mbps</td><td>25MHz output.
IP1829 sends out RXD [3:0], GMII_RXDV and GMII_RXER at the rising edge of GMII_RXCLK.</td></tr>
<tr><td>10Mbps</td><td>2.5MHz output.
IP1829 sends out RXD [3:0], GMII_RXDV and GMII_RXER at the rising edge of GMII_RXCLK.</td></tr>
</table></td></tr>
<tr><td>B21</td><td colspan="2">GMII_RXDV
(RXCTL)</td><td>I</td><td>GMII and MII Receive Valid

<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>1000Mbps
100Mbps
10Mbps</td><td>GMII_RXDV indicates the valid data is present on the data bus of RXD. It is synchronous to the rising edge of GMII_RXCLK
When it operation on RGMII mode, this pin is RXCTL.</td></tr>
</table></td></tr>
<tr><td>B23
A23
D22
C22</td><td>GMII_RXD7
GMII_RXD6
GMII_RXD5
GMII_RXD4</td><td>--</td><td>I</td><td>GMII Receive Data (high nibble)
<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>1000Mbps</td><td>Transmit data output bus that is sent synchronously at the rising edge of GMII_RXCLK</td></tr>
<tr><td>10/100Mbps</td><td>Not used.</td></tr>
</table></td></tr>
<tr><td>B22
A22
D21
A21</td><td colspan="2">GMII_RXD3
GMII_RXD2
GMII_RXD1
GMII_RXD0</td><td>I</td><td>GMII/RGMII/MII Receive Data

Receive data valid that is sent synchronously at the rising edge of GMII_RXCLK.</td></tr>
<tr><td>C23</td><td colspan="2">GMII_RXER</td><td>I</td><td>GMII and MII Receive Error

<table>
<tr><th>MDI speed</th><th>Description</th></tr>
<tr><td>1000Mbps</td><td>A “high” state present on this pin indicates received data error or carrier extension. It is synchronous to GMII_RXCLK</td></tr>
<tr><td>100Mbps,
10Mbps</td><td>A “high” state present on this pin indicates received data error. It is synchronous to GMII_RXCLK</td></tr>
</table></td></tr>
<tr><td>D23</td><td colspan="2">GMII_COL</td><td>I/O</td><td>GMII/MII Collision Detect
Collision detects when it operates on 10/100 half duplex mode. If transmission and reception are running. COL is always idle (logic low) if works in full duplex mode. When G5 is in PHY mode, this is an output pin.</td></tr>
<tr><td>N23</td><td colspan="2">MDC</td><td>O</td><td>Serial management bus clock output
It’s recommended to add a 30pF capacitor to ground for noise filtering.</td></tr>
<tr><td>N24</td><td colspan="2">MDIO</td><td>I/O</td><td>Serial management bus data input/output
It’s recommended to add a 1.5K ohm pull up resistor connecting to 3.3V VCC and a 30pF capacitor connecting to ground.</td></tr>
</table>

Table 6 EEPROM Pin

Pin No.	Label	Type	Description
E2	EE_CLK	O	**Serial EEPROM clock output**
E3	EE_DAT	I/O	**Serial EEPROM data input/output**

Table 7 CPU R/W Interface Pin

Pin No.	Label	Type	Description
C19	CPU_CLK	I	**Serial CPU access clock input**
C20	CPU_DAT	I/O	**Serial CPU data input/output**

Table 8 Serial LED Pin

Pin No.	Label	Type	Description
F2	LEDCLK	O	**Serial LED clock output** LED clock rate setting by Page 3 register 0x17 bit [7:6] : 00 : 781 KHz 01 : 2.5 MHz 10 : 5.2 MHz 11 : 10.4 MHz (Default)
F1	LEDDAT	O	**Serial LED data output**

Table 9 UART Pin

Pin No.	Label	Type	Description
A19	UART_TX	O	**UART serial data output.**
B19	UART_RTS	O	**UART RTS (Ready To Send)**
A20	UART_RX	I	**UART serial data input.**
B20	UART_CTS	I	**UART CTS (Clear To Send)**

Table 10 JTAG Pin

Pin No.	Label	Type	Description
C21	JTAG_CLK	I	**JTAG clock input.**
B23	JTAG_TDI	I	**Serial data input to JTAG TAP scan chain.**
D23	JTAG_TDO	O	**Serial data output JTAG TAP scan chain.**
C23	JTAG_TMS	I	**JTAG TAP test mode select.**
B21	JTAG_RST	I	**JTAG Reset input.**

Table 11 IEEE-1588 PTP Pin

Pin No.	Label	Type	Description
K11	PTP_CO	O	**PTP trigger output** Trigger output, refer to page 0x9 register 0x18
K12	PTP_EVENT	I	**PTP Event** Event trigger source input
K13	PTP_1PPS	O	**PTP 1PPS** Pulse per second reference output or clock/trigger output, refer to page 0x9 register 0x02

Table 12 GPIO Pin

Pin No.	Label	Type	Description
B24 B25 B26 C24 C25 C26 D24 D25 D26 A26 A21 D21 A22 B22 C22 D22 A23	GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16	I/O	**General Purpose Input / Output** User defined by internal CPU. The function is valid only if P29_CPU_EN is pulled up.

Table 13 DDR3 memory interface Pin

Pin No.	Label	Type	Description
DDR3 memory interface			
C12 B15 B11 B12 C15 C10 A15 A11 C14 C11 C13 B14 A16 A12 A14	DDR3_A0 DDR3_A1 DDR3_A2 DDR3_A3 DDR3_A4 DDR3_A5 DDR3_A6 DDR3_A7 DDR3_A8 DDR3_A9 DDR3_A10 DDR3_A11 DDR3_A12 DDR3_A13 DDR3_A14	O	**DDR3 address bus**
C7 B2 A7 C2 B7 A1 D9 B1 A2 B6 C3 A6 A3 C6 B3 D6	DDR3_DQ0 DDR3_DQ1 DDR3_DQ2 DDR3_DQ3 DDR3_DQ4 DDR3_DQ5 DDR3_DQ6 DDR3_DQ7 DDR3_DQ8 DDR3_DQ9 DDR3_DQ10 DDR3_DQ11 DDR3_DQ12 DDR3_DQ13 DDR3_DQ14 DDR3_DQ15	I/O	**DDR3 data bus**
B5 C5	DDR3_LDQS+ DDR3_LDQS-	O	**Lower-byte data strobe**
A4 B4	DDR3_UDQS+ DDR3_UDQS-	O	**Upper-byte data strobe**
A10 D10 B10	DDR3_BA[2] DDR3_BA[1] DDR3_BA[0]	O	**Bank address output**
A13 B13	DDR3_CK+ DDR3_CK-	O	**Differential clock outputs.**
C16	DDR3_CKE	O	**Clock enable**
C8	DDR3_CS#	O	**Chip select**
C4	DDR3_LDQM	O	**Lower-byte data mask**
A5	DDR3_UDQM	O	**Upper-byte data mask**

Pin No.	Label	Type	Description
A8 B8 B9	DDR3_RAS# DDR3_CAS# DDR3_WE#	O	**DDR3 Read / Write Command control**
C9	DDR3_ODT	O	**On-die termination:** ODT enables output to the DDR3 SDRAM. ODT is Enabled in normal operation: ODT is only applied to the following balls: DQ [7:0], DQS, DQS#, and DM for the x8; DQ [3:0], DQS, DQS#, and DM for the x4.
D14	DDR3_RESETB	O	**Reset DDR3 SDRAM output**
B16	DDR3_ZQ	I	**External reference ball for output drive calibration:** This ball is tied to external 240Ω resistor RZQ, which is tied to GND
A9	DDR3_VrefDQ	I	**Reference voltage for data:** VrefDQ must be maintained at all times (excluding self refresh) for proper device operation

Table 14 SPI Flash memory Pin

Pin No.	Label	Type	Description
A17	SPI_CLK	O	**SPI Flash memory clock output** Default operation frequency is 25MHz. Support to up maximal FLASH size 16M Bytes X 2
A18 B18 B17 C17	SPI_D0 SPI_D1 SPI_D2 SPI_D3	I/O	**SPI Flash memory data input / output** When using single I/O type SPI Flash memory, D0 is DI and D1 is DO. The D0~D3 are I/O pins when using dual or quad I/O type flash memory.
D17 C18	SPI_CS0 SPI_CS1	O	**SPI Flash memory chip select**

Table 15 Miscellaneous Pin

Pin No.	Label	Type	Description
D1	OSCI	I	**Crystal/Oscillator 25MHz input**
D2	X2	O	**Crystal output**
E1	RESETB	I	**System reset (low active)** Should be kept at “low” for at least 10 microseconds. The input voltage should be not higher than VDD33
J3	AFT_KEY	I	**Auto Factory Test enable key input**
P4 R3	MODE0 MODE1	I, PD	**Test mode select** 00: Normal (default) Reserved for test, should be “00” for normal operation
N3	P29_CPU_EN	I,PU	**Port 29 CPU enable** 0 : enable GMII/RGMII interface(for external device) 1 : enable internal CPU (default)
N4	P29_IF_SEL	I,PD	**Port 29 interface select** 0 : GMII (default) 1 : RGMII **(active when P29_CPU_EN=0)**
K10	CRI_EVENT	I	**Critical Event for OAM** Critical Event trigger input pin Critical Event triggered report to INT_OUT (Ball D18) can enable by register page C 0X05[7]
D18	INT_OUT	O	**Interrupt output. Active low** Interrupt output configuration by writing register page C 0X05 Interrupt status read from reading register page C 0X06
V4	REXT	I	**Band gap reference voltage external resistor** It must be pull down to ground by 6.19K ohm resistor.

Power on Setting

The state of these pins will be latched upon reset.

Table 16 Power on Setting

Pin No.	Label / Setting	Type	Description
A17	SPI_CLK **/effuse_DIS**	IL, PD	**eFuse disable** 0 : enable (default) 1 : disable If an external pull up resistor is used, it should be connected to VDDIO.
D17	SPI_CS0 **/Home VLAN**	IL, PD	**Home VLAN enable** 0 : disable (default) 1 : enable
C18 A19	SPI_CS1 **/LED mode [0]** UART_TX **/LED mode [1]**	IL, PD	**LED mode select** 00 : 2-bit mono-color (Giga,Link/Act) (default) (100,Link/Act) 01 : 3-bit mono-color (Giga,Link/Act,10/100 Link/Act,Full/Col) (100,Link/Act,10 Link/Act,Full/Col) 10 : 2-bit bi-color (**Giga,Link/Act**) (**100,Link/Act**) 11 : 3-bit bi-color (**Giga,Link/Act**,Full/Col) (**100,Link/Act**,Full/Col) (**bi-color**) The setting can be updated by register Page 3 0x17 bit [2:0]
B19	UART_RTS **/EEE_EN**	IL, PD	**EEE enable** 0 : enable (default) 1 : disable the pin is global setting The setting can be updated by register Page 3 0x2f,0x30
K13	PTP_1PPS **/IPG compensation**	IL, PU	**IPG compensation enable** 0 : enable 1 : disable(default) The setting can be updated by register Page 0 0x01[1]
K11	PTP_CO / **Initial cable test**	IL, PU	**Initial cable test** 0 : enable 1 : disable(default) The setting can be updated by register page 3 0x16 [13]
D18	INT_OUT / **IGMP snooping_EN**	IL, PU	**IGMP snooping enable** 0 : enable 1 : disable(default) The setting can be updated by registers page 1 0x29 [0]
F2	LED_CLK **/LUT entry over-write**	IL, PU	**LUT entry over-write** 0 : LUT entry can be write when it is empty 1 : LUT entry over-write enable (default) The function can be updated by register page 01 0x01,0x02

Pin No.	Label / Setting	Type	Description
F1	LED_DAT **/LUT hashing method**	IL, PU	**LUT hashing method** 0 : LUT direct-hashing 1 : LUT CRC-hashing (default) The function can be updated by register page 01 0x02[3]
L26 M24	G3_TXD0 **/Fiber mode[0]** G3_TXD1 **/Fiber mode[1]**	IL, PD	**Fiber mode** 00 : {P01~P24} TP (default) 01 : { P01~P08}, { P09~P16} TP ; { P17~P24} Fiber 10 : { P01~P08} TP ; { P09~P16}, { P17~P24} Fiber 11 : {P01~P24} Fiber The setting can be updated by register page 0C 0x0B, 0x0C for per port.
M25	G3_TXD2 **/GMII force link**	IL, PD	**GMII (port 29) force link** 0 : disable (default) 1 : enable The setting can be updated by registers page 3 0x12 [0]
M26 G26	G3_TXD3 **/GMII force mode[0]** G4_TXD0 **/GMII force mode[1]**	IL, PD	**GMII (port 29) force mode** 00 : Force mode disable (default) 01 : Force 100M full duplex 10 : Force 1000M full duplex 11 : Force 10M full duplex The setting can be updated by registers page 3 0x12 [3:2]
H24	G4_TXD1 **/Jumbo packet**	IL, PD	**Jumbo packet** 0 : disable (default) 1 : enable the pin is global setting The setting can be updated by registers page 0 0x02,0x03
H25 H26	G4_TXD2 **/GMII driving[0]** G4_TXD3 **/GMII driving[1]**	IL, PD	**GMII/RGMII driving** 00 : 6mA (default) 01 : 9mA 10 : 12mA 11 : 18mA The setting can be updated by register page 0C 0x08~0x0A.

Table 17 Power & Ground Pin

Pin No.	Label	Type	Description
C1, D13, D19, E23, J4, L23 Y23, AC8,AD8	VCC10	P	**1.0V power for Core circuit**
K4, U4, P23,U23, AB23,AD11, AC20,AD4	AVDD10	P	**1.0V power for analog circuit**
D15,D16	LX	P	**1.5V switching regulator output for DDR3 SDRAM**

Pin No.	Label	Type	Description
K17	VFB	P	**1.5V Switching regulator's reference feedback input**
D5, D7, D8, D11, D12	VDDIO_15	P	**1.5V power for DDR3 I/O**
G23	REG18	P	**1.8V regulator output for RGMII I/O**
J23,K23	VDDIO_18	P	**1.8V power input for RGMII I/O**
D3,D20, G3,H23, K15,K16,	VDD33	P	**3.3V power for Digital circuit**
AA23,AB4, AC4,AC6, AC9,AC13, AC15,AC17, AC21,AC22, V23,M4, H4, R23, T4,Y4	AVDD33	P	**3.3V power for Analog circuit**
K14,L10, L11,L12, L13,L14, M10~17, N10~17, P10~17, R10~17, T10~17, U10~17,	GND	P	**Digital power Ground**
E4	AVDD33_PLL	P	**3.3V power for PLL circuit**
D4	VSS_PLL33	P	**3.3V Ground for PLL circuit**
F4	AVDD10_PLL	P	**1.0V power for PLL circuit**
F3	VSS_PLL10	P	**1.0V Ground for PLL circuit**

Pin No.	Label	Type	Description
G4,F23, L3,L4, L15,L16, P24,R4, R24,T23, U24,V3, V24,W4, W23,Y3, AA4,AA24, AC3,AC5, AC7,AC16, AC18,AC23, AD9,AC11, AD13,AD16, AD18,AD20, AD22	AVSSxx	P	**Analog power Ground**

5 Function Description

5.1 Switch Engine and Queue Management

5.1.1 Packet forwarding

IP1829 utilizes the “store & forward” method to handle packet transfer. IP1829 begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

5.1.1.1 Address Learning and Hashing

Related registers	0x02[3], 0x03, 0x04	PAGE 0x01

IP1829 has 16384 entries for MAC address learning tables. It provides two hashing methods to access the MAC address table. One is the direct mapping and the other is the CRC algorithm. For the direct mapping method, if page 0x01 register 0x02[3] is set to “0”, the MAC address directly employs the least significant 13 bits of the MAC address. For the CRC algorithm method, if page 0x01 register 0x02[3] is set to “1”, IP1829 uses CRC algorithm to obtain 13bits MAC address from the 48-bits MAC.

The MAC address learning function can be either enabled or disabled for each port by programming page 0x01 register 0x03[15:0] and page 0x01 register 0x04[12:0], and MAC address with all 0s can be learned to MAC address table by programming page 0x01 register 0x02[2] if the MAC address learning function is enabled.

IP1829 provides three kinds of methods for the MAC address learning. The first method is enabled by programming page 0x01 register 0x02[1:0] to “00”, means LUT can be written even when the entry is valid. The second method is enabled by programming page 0x01 register 0x02[1:0] to “01 or 10”, means LUT can not be written before aging out. The third method is enabled by programming page 0x01 register 0x02[1:0] to “11”, means only the second layer LUT can be written before aging out,.

The packet with the following conditions will not be learned in MAC address table.

- Erroneous packet
- 802.3x pause packet(option)
- 802.1D Reserved Group packet(option)
- Multicast source MAC address

IP1829 provides the MAC address learning count threshold function to limit source MAC address number learning in MAC address table. The number of learning MAC address must not be more than threshold, the extra MAC address will not be learnt in MAC address table if learning MAC address number higher than the threshold. The threshold values can be set by programming page 0x01 register 0x07[8:0] and each port is enabled individually by programming the corresponding bits of page 0x01 register 0x05,06.

5.1.1.2 Port Base Address Flush

Related registers	0x1A, 0x1B	PAGE0x01

IP1829 can clear the MAC address that bind to specific port. The specific port can be enabled by programming the corresponding bits of page 0x01 register 0x1A ~0x1B[12:0] to “1”, and trigger the port base address flush function by programming page 0x01 register 0x1B[13] to “1”.

5.1.1.3 Aging Time

Address Aging

Related registers	0x01[15], 0x01[14:0]	PAGE 0x01

IP1829 supports programmable aging time to meet various system requirements, ranging from 55 sec to 1802295 sec ±3.8%. The user can set aging time by programming page 0x01 register 0x01[14:0]. The address aging function can be disabled by programming page 0x01 register 0x01[15] to "1".

Packet Aging

Related registers	0x66 to 0x75	PAGE 0x08

IP1829 supports packet aging (out queue aging). (If a packet stays in Queue too long, IP1829 will age out according to aging time defined in page 0x08 register 0x66[7:0]). IP1829 will drop the packet to improve the efficiency of packet buffer. The packet aging function can be enabled individually for each port by programming page 0x08 register 0x67 to 0x75

5.1.1.4 802.1D packet forwarding

Related registers	0x06, 0x07[4:0]	PAGE0x00
	0x03[0]	PAGE 0x0C

Except that the erroneous packet and the IEEE802.3x pause packet will not be forwarded, 802.1D Reserved Group packet with MAC address from 01-80-c2-00-00-00 to 01-80-c2-00-00-3F can be forwarded, dropped or "To CPU port" by programming page 0x00 register 0x06 ~0x07[3:0]. If the corresponding bits of page 0x00 register 0x06~0x07[3:0] are set to "11", the 802.1D packets for each port will be dropped. Under this situation, if page 0x00 register 0x07[4] is also set to "1", the 802.1D packet coming from CPU port can be forwarded.

Inter Frame Gap Compensation

Related registers	0x01[1:0]	PAGE 0x00

IP1829 supports an option to transmit a packet with IPG shrank 40 ppm, 80 ppm or 160 ppm to compensation the data accumulation due to TX clock frequency difference between local machine and link partner. Programming page 0x00 register 0x01[1:0] can enable this function.

5.1.2 Flow Control

IP1829 supports two kinds of flow control mechanisms, backpressure for half duplex operation and IEEE 802.3x for full duplex operation.

5.1.2.1 IEEE802.3x

Related registers	0x08 to 0x0B	PAGE 0x03
	0x0B,0x0C	PAGE 0x01

When operating in full duplex mode, IP1829 supports IEEE802.3x flow control, both symmetric pause and asymmetric pause function. Each port's flow control function can be enabled individually by programming page 0x03 register 0x08~0x0B. When the packets in buffer reach the threshold, IP1829 generates a "Xoff" pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP1829 from overrun. When the packets in buffer lower than threshold,

IP1829 generates a “Xon” pause packet to notify the link partner the receive buffer is available. Each port can be enabled individually by programming the corresponding bits of page 0x01 register 0x0Bh~0Ch for passing pause packet to specific ports.

5.1.2.2 Backpressure

Related registers	0x01[3:2]	PAGE 0x00
	0x0C to 0x0D	PAGE 0x03

When operating in half duplex mode, IP1829 supports backpressure flow control. Each port’s backpressure function can be enabled individually by programming page 0x03 register 0x0C~0D. When the packets in buffer reach the threshold, IP1829 generates a jam pattern to back off the link partner. IP1829 supports the collision based and carrier-based backpressure. When the collision based backpressure is enabled, page 0x00 register 0x01[2] set to “1”, IP1829 generates a jam pattern only when the link partner is transmitting data and the receive buffer in IP1829 is not available. When detecting a collision on line, the link partner stops transmission until a back off time expires. When the carrier based backpressure is enabled, page 0x00 register 0x01[2] set to “0”, IP1829 transmits null packets continuously to prevent link partner’s transmission when the buffer is not available.

To prevent the packet loss due to excessive collision caused by backpressure mechanism, user can program page 0x00 register 0x01[3] to “0” to disable the drop function due to 16 consecutive collisions defined in IEEE802.3.

5.1.2.3 Flow control auto off for high priority packet

Related registers	0x01[5]	PAGE 0x00

To prevent the flow control function from blocking the high priority traffic, each port of IP1829 can auto turn off flow control function for a period of time automatically when receiving a high priority packet. This function can be enabled by programming page 0x00 register 0x01[5] to “1”.

5.2 Bandwidth Control

Related registers	0x87 to 0xA3 (ingress)	PAGE0x00
	0x85 to 0xA1 (Egress), B1[6:4]	PAGE0x08

IP1829 implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP1829 provides a variety of bandwidth configurations. It limits the maximum byte counts in one second, for each port to send or receive packets. If the transmit byte counter or receive byte counter of a port reaches a pre-defined threshold, it will stop transmitting or receiving data in one second.

Each port’s Ingress/egress data rate can be programmable individually. The bandwidth rate for port 1 to port 29 is defined in page 0x00 register 0x87 to 0xA3(Ingress) and page 0x08 register 0x85 to 0xA1(Egress). The egress bandwidth parameter is defined in page 0x08 register 0xB1. Note that its bandwidth should not be more than the link speed of a port.

5.2.1 Broadcast Storm Control

Related registers	0x0D to 0x0F	PAGE0x01

To prevent the broadcast storm, the IP1829 implements a broadcast storm control mechanism. By enabling this function, a port begins to drop the incoming broadcast packets if the number of received broadcast packets reach the threshold in selected period, which is defined in page 0x01 register 0x0D [7:0] and 0x0D [9:8]. Each port's broadcast storm protection function can be enabled individually by programming page 0x01 register 0x0E and 0x0F[12:0]. IP1829 also provides four kinds of time period, which can be selected by programming page 0x01 register 0x0D [9:8] for 1G/100M/1M. The detailed configuration is shown in the following table.

5.2.1.1 Multicast and DLF Storm Control

Related registers	0x0D to 0x13	PAGE0x01

Multicast storm and DLF storm use the same threshold setting defined in page 0x01 register 0x0D [7:0]. Multicast means the bit [40] of the destination MAC address is set to "1". DLF (Destination Lookup Failure) means the MAC address doesn't exist in MAC address table is regarded as broadcast.
multicast storm is configured by programming page 0x01 register 0x10 and 0x11[12:0] and DLF storm is configured by programming page 0x01 register 0x12 and 0x13[12:0].

5.2.1.2 ARP Storm Control

Related registers	0x14 to 0x16	PAGE0x01

To prevent the ARP storm, IP1829 implements an ARP storm control mechanism. By enabling this function, a port begins to drop the incoming ARP packets if the number of received ARP packets reach the threshold in selected period, which is defined in page 0x01 register 0x14[7:0] and 0x14[9:8].

Each port's ARP storm protection function can be enabled individually by programming page 0x01 register 0x15 and 0x16[12:0]. IP1829 also provides four kinds of time period, which can be selected by programming page 0x01 register 0x14[9:8] for 1G/100M/10M. The detailed configuration is shown in the following table.

5.2.1.3 ICMP Storm Control

Related registers	0x17 to 0x19	PAGE0x01

To prevent the ICMP storm, IP1829 implements an ICMP storm control mechanism. By enabling this function, a port begins to drop the incoming ICMP packets if the number of received ICMP packets reach the threshold in selected period, which is defined in page 0x01 register 0x17[7:0] and 0x17[9:8].

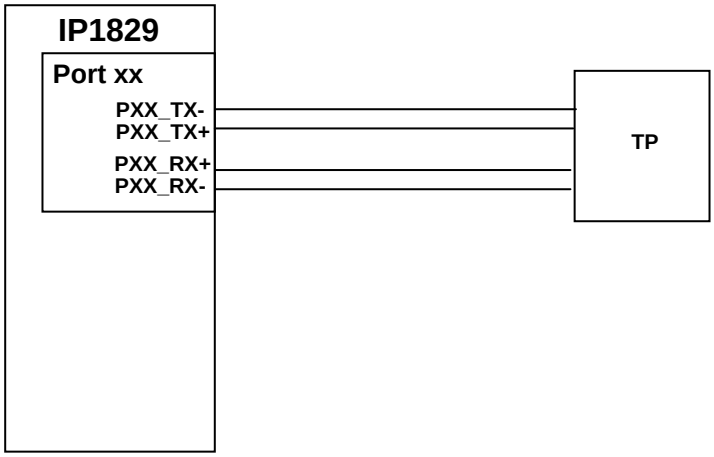
Each port's ICMP storm protection function can be enabled individually by programming page 0x01 register 0x18 and 0x19[12:0]. IP1829 also provides four kinds of time period, which can be selected by programming page 0x01 register 0x17[9:8] for 1G/100M/10M. The detailed configuration is shown in the following table.

Table 18 Broadcast /ARP/ICMP Storm Counter Clear Period Selection Table

0x0D[9:8] 0x14[9:8] 0x17[9:8]	1000Mbps	100Mbps	10Mbps
00	200us	2ms	20ms
01	1ms	10ms	100ms
10	10ms	10ms	10ms
11	100ms	100ms	100ms

5.2.2 Interface

5.2.2.1 MDI (Port1~Port24)



5.2.2.2 SGMII/Fiber (Port25, Port26)

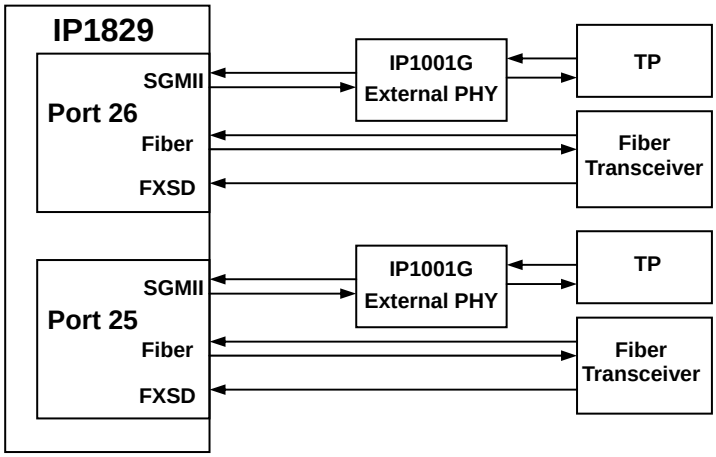


Figure 5 SGMII / Fiber Application diagram

5.2.2.3 RGMII (Port27, Port28)

IP1829 sends out data TXD [3:0] and control signal TX_CTL at the rising and falling edge of TXC. Two GMII like signals TX_EN and TXER are embedded in the TX_CTL. GMII like information TXD [7:0] is embedded in the TXD [3:0]. By recognizing the decoded TX_EN, TXD [7:0] and TXER, a PHY can capture the correct data stream.

A PHY sends out data RXD [3:0] and control signal RX_CTL at the rising and falling edge of RXC. Two GMII like signals RX_DV and RXER are embedded in the RX_CTL. GMII like information RXD [7:0] is embedded in the RXD [3:0]. By recognizing the decoded RX_DV, RXD [7:0] and RXER, IP1829 can capture the correct data stream. IP1829 samples the correct data at the rising edge of RXCLK.

To fit the timing requirement, the delay on TXC and RXC can be adjusted by programming page 0x0C register 0x08~0x0A. The driving current can be adjusted by pin G4_TXD2, G4_TXD3: GMII_DRIVR [1:0] and page 0x0C register 0x08~0x0A.

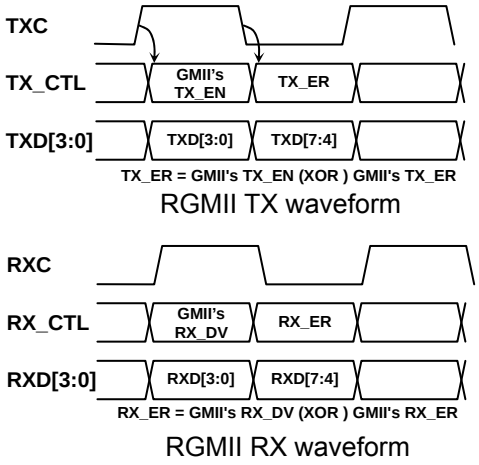


Figure 6 Waveform of RGMII

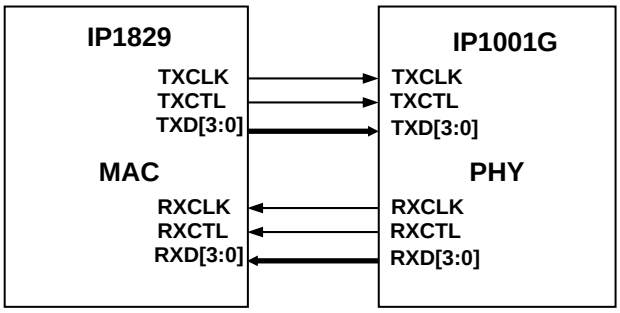


Figure 7 RGMII Application diagram

5.2.2.4 GMII (Port29)

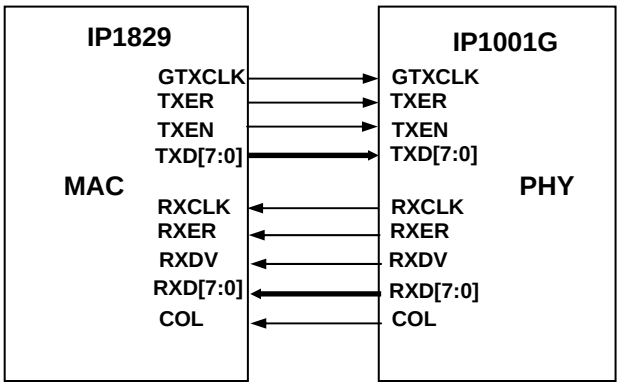


Figure 8 GMII Application diagram

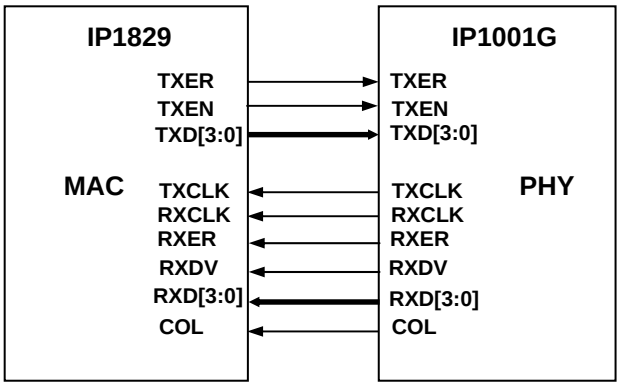


Figure 9 MII Application diagram

IP1829's port29 can select GMII or RGMII interface to connect with the external device or CPU. If pin P29_CPU_EN is set to "0" and pin P29_IF_SEL is set to "0", indicates that port29 use GMII interface to connect with external device or CPU, if P29_IF_SEL is changed to "1", indicates that port29 use RGMII interface to connect with external device or CPU. If pin P29_CPU_EN is set to "1" and pin P29_IF_SEL is set to "0", indicates that port29 use GMII interface to connect with embedded CPU. Note that embedded CPU only uses GMII interface.

5.2.3 External CPU Read / Write interface

There is no need to program the register of the IP1829 for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP1829 and the external CPU is a serial bus, which comprises a clock and an I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the switch ID, the read/write command, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.

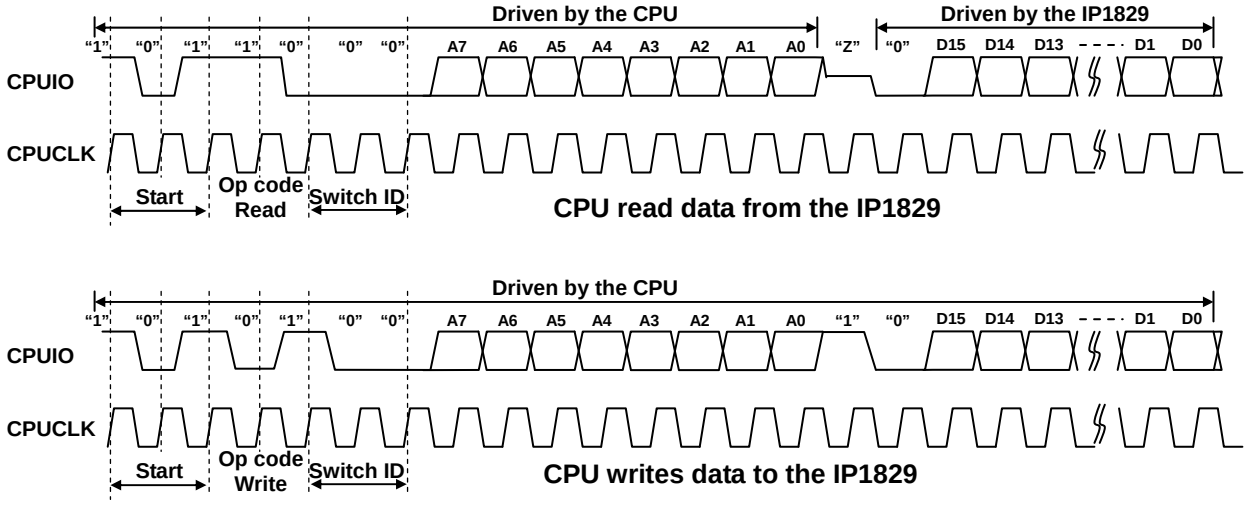


Figure 10 External CPU Read / Write interface diagram

5.2.4 EEPROM Interface

Related registers	0x01 to 0x0F	PAGE0x0B

IP1829 supports EEPROM I/F to access 24C01 to 24C4096. After detecting the rising edge of a reset input, IP1829 will start to read the content of EEPROM (acting like an EEPROM master). Being an EEPROM master, IP1829 provides command mode to download the content of EEPROM. The content of the first byte should be “00h” to be identified as IP1829 EEPROM. If the content of the second byte is “0x0B” for 24C01 to 24C16 or “0x0D” for 24C32 to 24C4096 EEPROM capacity, it runs with command mode.

In the command mode, one command occupies 4 EEPROM bytes. The content includes 1 bytes command and 1 bytes register address and 2 bytes data. If command byte < 0x40, it stands the register page address. If command byte >=0x40, it stands for the advance commands. (The detail explanation for advance commands please refer to appendix application notes)

The following is a normal EEPROM example for IP1829.

Table 19 Command Mode Format of EEPROM

Command mode		
EEPROM address	**EEPROM content**	**Description**
0x00	0x00	EEPROM start
0x01	0x0B or 0x0D	(EEPROM capacity at Command Mode)
0x02	0x00	Don’t care
0x03	0x00	Don’t care
0x04	0x03	Page address or advance Command In this case, page address is 0x03
0x05	0x0A	Register address In this case, register address is 0x0A
0x06	0x34	Bit [15:8] Register data In this case, write 0x34 to register 0x0A[15:8]
0x07	0x12	Bit [7:0] Register data In this case, write 0x12 to register 0x0A[7:0]
0x08	0xXX	Page address or advance Command
0x09	0xXX	Register address
0x0a	0xXX	Bit [15:8] Register data
0x0b	0xXX	Bit [7:0] Register data
0x0c	0xXX	Page address or advance Command
0x0d	0xXX	Register address
0x0e	0xXX	Bit [15:8] Register data
0x0f	0xXX	Bit [7:0] Register data
⋮		
XX	0xFF (or 0x00)	Page address or advance Command
XX	0xFF (or 0x00)	Register address
XX	(Do not care)	Stop Initial Reading (Follow by the command byte and register address are both 0xFF)
⋮	(Do not care)	

5.2.5 MIB Counter

Related registers	0x01[9], 0x64 to 0x66	PAGE0x00

IP1829 provides a set of RX and TX counters for statistic, IP1829 can monitor a variety of packets , including different length packet, illegal packet(over size, symbol error), unicast packet, multicast packet broadcast packet, and even byte count for packet, etc. To enable the counter, page 0x00 register 0x01[9] must set to "1". The user can read the content of the counter through page 0x00 register 0x64~0x66. The detailed description is shown in the following table.

Table 20 Address Format of Port MIB Counter

address	RX counter	TX counter
00	RX_64B	TX_64B
01	RX_65_127B	TX_65_127B
02	RX_128_255B	TX_128_255B
03	RX_256_511B	TX_256_511B
04	RX_512_1023B	TX_512_1023B
05	RX_1024_1518	TX_1024_1518
06	RX_Oversize	TX_Oversize
07	RX_Bcst	TX_Bcst
08	RX_Mcst	TX_Mcst
09	RX_Ucst	TX_Ucst
0A	RX_Pause	TX_Pause
0B	PKTs	TX_Pkt
0C	Byte_L	Bytes_L
0D	Byte_H	Bytes_H
0E	RX_Drop (buff)	TX_Drop (buff)
0F	RX_DROP others	Single Col
10	RX_CRC	Multiple Col
11	RX_Alignment	Late Col
12	RX_Runt	Defered TX
13	RX_Frag	Excessive Col
14	RX_Jabber	
15	Symbol Error	
16	ACL	
17	ACL	

5.2.6 Auto Factory Test (AFT)

IP1829 implements an AFT mechanism, which is very useful for switch pre-test. When this function is triggered by hardware pin G3 AFT_KEY, IP1829's physical ports are connected either port-pairs LoopBack or self-LoopBack and then IP1829 will generator frames for TX of all ports .

In the AFT mode, the light-on period is within 1 second, then show the test result on the LED. The status of test result will keep the LED status while this hardware pin AFT is still triggered.

For example, port1 and port2 are connected to each other (LoopBack). Check the LED of port1 and port2 is light-on, and then trigger this AFT function. If the test result is passed (no CRC or packet loss), show LED of port1 and port2 light-on. Otherwise, show LED light-off when CRC or packet loss is happened.

5.2.7 LED display mode

Related registers	0X17 to 0X1F	PAGE0x03

The bit stream is output sequentially through LED_DAT and LED_CLK and its sequence starts from port 29 to port 0. In the other word, Port 0 LED status is present on the latest LED bit, as shown in the table. To store the serial LED stream, a serial-to-parallel shift register should be used.

Table 21 LED display behavior vs. LED mode

Pin Setting	0x17 bit [2:0]	LED mode	LED display behavior	
			Giga port	10/100M port
-	000	3-bit B	**Giga, 100**, L/A	The same (switch @10M)
10	001	3-bit M	Giga-L/A, 10/100-L/A, F/C	100-L/A, 10-L/A, F/C
-	010	3-bit M	Giga-L/A, 10/100-L/A, FC/ flash	100-L/A, 10-L/A, FC/ flash
11	011	2-bit M	Giga, L/A	100, L/A
-	100	3-bit M	TX, RX, Giga-Spd [Giga light, 100 flash, 10 dark]	
00	101	3-bit B	**Giga, L/A**, F/C	**100, L/A**, F/C
-	110	3-bit B	**Giga, L/A**, FC/ flash	**100, L/A**, FC/ flash
01	111	2-bit B	**Giga, L/A**	**100, L/A**

(B: **bi-color** ; M : mono-color)

Table 22 LED display Sequence.

0x17 bit [2:0]	LED mode	LED Display Sequence. (1), (2)..... indicate the bit stream sequence shifted from LED_DAT.
000	3-bit B	**(1) (2)** Port 29 Speed **(3)** Port 29 L/A ····· **(Last one)** Port 0 L/A
001	3-bit M	**(1)** Port 29 Hi_Speed-L/A, **(2)** port 29 Lo_Speed-L/A, **(3)** port 29 F/C ····· **(Last one)** Port 0 F/C
010	3-bit M	**(1)** Port 29 Hi_Speed-L/A, **(2)** port 29 Lo_Speed-L/A, **(3)** port 29 F/C flash ····· **(Last one)** Port 0 F/C flash
011	2-bit M	**(1)** Port 29 Speed, **(2)** port 29 L/A ····· **(Last one)** Port 0 L/A
100	3-bit M	**(1)**Port 29 TX, **(2)** port 29 RX **(3)** Port 29 Speed ····· **(Last one)** Port 0 Speed
101	3-bit B	**(1) (2)** Port 29 Speed-L/A, **(3)** port 29 F/C ····· **(Last one)** Port 0 F/C
110	3-bit B	**(1) (2)** Port 29 Speed-L/A, **(3)** port 29 F/C flash····· **(Last one)** Port 0 F/C flash
111	2-bit B	**(1) (2)** Port 29 Speed-L/A, **(3) (4)** port 28 Speed-L/A ····· **(Last two)** Port 0 Speed-L/A

If page 0x03 register 0x19[13] is asserted, there will be 5-bit Fiber port indicator for P25-P29 at the head of LED sequence.
IP1829 also provides CPU control LED mode, if page 0x03 register 0x17[15] is asserted, then LED will show results according to the settings of page 0x03 register 0x1A to 0x1F.
More detail description; please refer to the LED application note.

An example for port 28/29 using 2-bit stream mono-color LED display mode with IP403 is shown below.

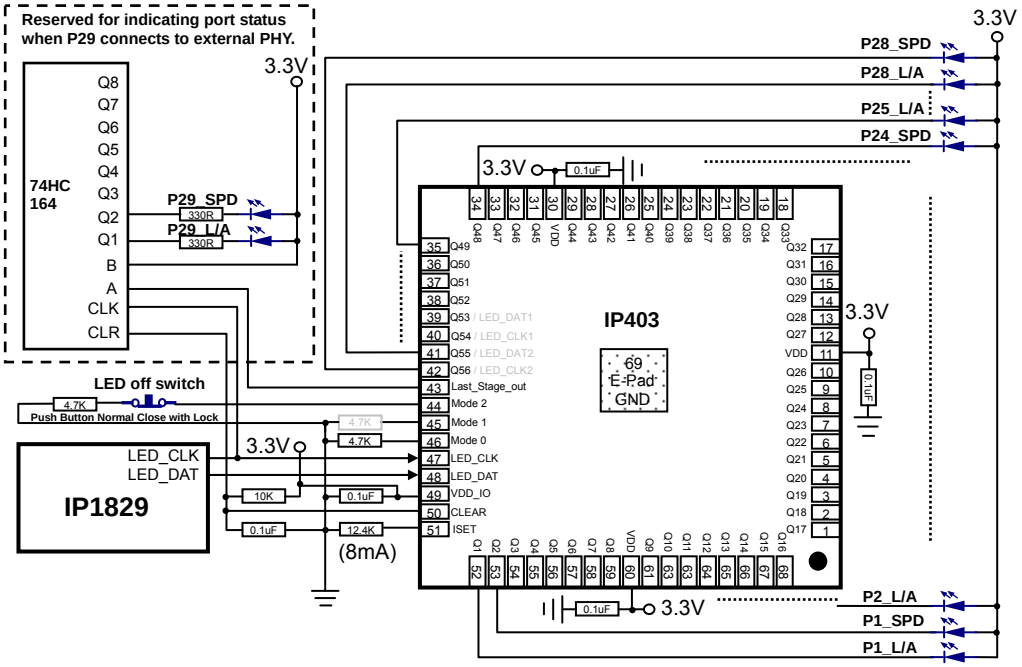


Figure 11 2-bit stream mono-color LED application diagram

5.3 VLAN

IP1829 supports port based VLAN, tag based VLAN and protocol based VLAN to implement flexible VLAN function, the detailed description is as follows.

5.3.1 Port Based VLAN

Related registers	0x30 to 0x69	PAGE0x02

IP1829 provides port-based VLAN configurations. For each port, there are two registers to describe its port-based VLAN configuration. The VLAN group can be defined in page 0x02 registers from 0x30 to 0x69.

Take the following example for the detail description. The data incoming from port 1 can be forwarded to the corresponding port defined in page 0x02 register 0x30 and 0x31. For example, if page 0x02 register 0x30 and 0x31 are written with 16'h000F and 16'h000F, the packet from port 1 can be forwarded to port 2/3/4 and port 17/18/19/20 only. Similarly, the forwarding rule for the data incoming from port 2 will refer to page 0x02 register 0x32 and 0x33. The forwarding rule for the data incoming from port 29 will refer to page 0x02 register 0x68 and 0x69.

5.3.2 Tag Based VLAN

Related registers	0x06, 0xD2 to 0xD8	PAGE0x02

IP1829 provides 4096 VLAN entries in VLAN table; the user can configure the VLAN table by programming page 0x02 register 0xD2 to 0xD8. If tag VLAN function is enabled and IP1829 receive a tagged packet, IP1829 will use the VID to lookup the VLAN entry in the VLAN table. If it is invalid, IP1829 drops the packet. If it is valid, IP1829 will forward the packet to destination port which belongs to the members of the VLAN, if this destination port is not a VLAN members, the packet will be dropped. Besides, If the source port is not a member of the VLAN, the packet can be either forwarded or dropped by programming page 0x02 register 0x09 to 0x0A.

When an un-tagged packet is received, IP1829 uses the PVID of the source port to look up the VLAN entry from VLAN table, the default PVID of the ports are defined in page 0x02 register 0x13 to 0x2F. IP1829 forwards the packet in the same way as mentioned above. For example, if port 1 receives a un-tag packet, IP1829 adopts the PVID of port 1 defined in bit [11:0] of page 0x02 register 0x13 to search the VLAN table, if the VLAN entry is valid, the packet will be forwarded to destination port which belongs to the members of the VLAN, the behavior of priority tag packet (VID equals to "000h") is the same as an un-tagged packet.

5.3.3 Protocol Base VLAN

Related registers	0x06[0], 0x6A to 0x71	PAGE0x02

IP1829 can configure a list of protocol types (Ether type, LLC,RFC1042) mapping to VLAN membership by programming page 0x02 register 0x06[0] and page 0x02 register 0x6A to 0x71. IP1829 provides 4 entries for the protocol base VLAN to use, each entry primarily consists of "type for protocol" and "protocol selection" settings.

IP1829 will check whether an incoming packet matches in "protocol selection" and "type for protocol" settings in corresponding register. For example, if the incoming packet format matches page 0x02 register 0x6A~0x6B (entry 01), the VLAN membership refers to the VID of specific protocol type. (Note that the

VID won't be added to output port, IP1829 only use to the VID to look up the VLAN member for the packets forwarding.

When protocol selection is invalid, the default VLAN membership refers to PVID index.

Table 23 PVID index search VLAN table

Protocol selection	Ingress packet	According to VID index	According to PVID index
Invalid	Ether type	---	By PVID
	LLC	---	By PVID
	RFC1042	---	By PVID
Ether Type	Ether type	By VID	---
	LLC	---	By PVID
	RFC1042	---	By PVID
LLC	Ether type	---	By PVID
	LLC	By VID	---
	RFC1042	---	By PVID
RFC1042	Ether type	---	By PVID
	LLC	---	By PVID
	RFC1042	By VID	---

5.3.4 VLAN Function

Related registers	**0x06, 0x13 to 0x2F, 0xCC to 0xCD , 0xD2 to 0xD8**	**PAGE0x02**
	0x07 to 0x08	**PAGE0x07**
	0x03	**PAGE0x0C**

5.3.4.1 Add/modify VLAN Tag

IP1829 provides two methods for adding VLAN tag. One is port-based tagging, and the other is VID-based tagging. For port-based tagging, if the corresponding bits of page 0x02 register 0xCC ~0xCD are set to "1" and page 0x02 register 0x06[1] is set to "1", the packet will be added tag. For VID-based tagging, if the corresponding bits of "add tag field" of the VLAN entry are set to "1" and page 0x02 register 0x6[3] is set to "1" and page 0x02 register 0x06[1] is set to "1", the packet will be added tag

5.3.4.2 Remove VLAN Tag

IP1829 also provides two methods for removing VLAN tag. One is port-based, and the other is VID-based. For port-based, if the corresponding bits of page 0x02 register 0XCE~CF are set to "1" and page 0x02 register 0x06[1] is set to "1", the packet will be stripped tag. For VID-based , if the corresponding bits of "remove tag filed" of the VLAN entry are set to "1" and page 0x02 register 0x6[3] is set to "1" and page 0x02 register 0x06[1] is set to "1" ,the packet will be stripped tag" .

Besides, if page 0x02 register 0x06[4] is set to "0" and page 0x0C register 0x03[0] is set to "1", the packets that send to CPU Port will not add or remove tag. The operation is illustrated as follows. It is note that the VID-based tagging defined in the VLAN entry table is also used for 802.1Q tag-based VLAN.

Table 24 Forward the Packet with VLAN Configuration Table

Frame type of the received packet	**The operation on a switch with VLAN configuration**	
	Forward to a untagged filed	**Forward to a tagged field**
Untagged	Forward the packet without modification	1. Insert a tag using the default VLAN tag value of the source or output port 2. Calculate new CRC 3. The default VLAN tag value will be added to output port by writing register 0xCC~0xCD.
Priority-tagged (VLAN ID=0)	1. Strip tag 2. Calculate new CRC	1. Keep priority field. 2. Replace the tag with the default VLAN tag value of the source or output port 3. Calculate new CRC 4. The default VLAN tag value is defined in the registers bit [11:0] in the 0x13 to 0x2F.
VLAN-tagged	1. Strip tag 2. Calculate new CRC	Forward the packet without modification

A packet without tag

DA	SA	Data	CRC

A packet with VLAN tag

DA	SA	8100	VID	Data	CRC

A packet with special and VLAN tag

DA	SA	9126	Port info.	8100	VID	Data	CRC

Figure 12 Frame Format of Inserting VLAN or/and Special Tag

5.3.4.3 VLAN up Link

Related registers	0xD0, 0xD1	PAGE0x02

When source port forwards packet to destination port in different VLAN group, for example, source port is in VLAN1, destination port is in VLAN2, the packet will be sent to “uplink port” in VLAN1 if uplink port function is enabled, When source port forwards packet to destination port in different VLAN group, the packet will be dropped if uplink port function is disabled. uplink port function is enabled by programming page 0x02 register 0xD1[13] to “1”, uplink port is configured by programming the corresponding bits of page 0x02 register 0xD0, 0xD1.

5.3.4.4 Force the Incoming Packet Use PVID

Related registers	Bit15 of 0x13 to 2F	PAGE0x02

IP1829 provides a kind of the mechanism for VLAN packets forwarding. If the corresponding bit [15] of page 0x02 register 0x13 to 0x2F. is set to “1” for each port, IP1829 will use PVID for VLAN checking instead of VID for VLAN checking, that is, IP1829 will use PVID to lookup VLAN member for the packets forwarding. The function can be enabled individually for each port by programming each bit[15] form page 0x02 register 0x13~0x2F.

5.3.4.5 VLAN Ingress Check

Related registers	0x09 to 0x0E	PAGE0x02

For packets forwarding, IP1829 provides two kinds of mechanism for the VLAN ingress check.

1. By port, IP1829 will check whether the source port of incoming packet belong to the same VLAN group by setting page 0x02 register 0x09 ~ 0x0A to 1. If the ingress port is not in VLAN membership, IP1829 will drop it.

2. By frame type, IP1829 will decide which type of the incoming packets should be forwarded by programming the corresponding bits of page 0x02 register 0x0B to 0x0E, 2bits for each port, 00 means all packet are forwarded”, 01 means “only tag packet is forwarded”, 10 means “priority and non-tag packet are forwarded”, 11 means “priority and tag packet are forwarded”,

5.3.4.6 VLAN Egress Rule

Related registers	0x0F to 0x10	PAGE0x02

For egress rule, IP1829 implements a set of VLAN egress rules, which defined port based, unicast, multicast and ARP. If an incoming packet matches specific rule. For example, if page 0x02 register10 [15] is set to “1”, the ARP packet will use the default group setting for forwarding.

5.3.4.7 VLAN exclusive port

Related registers	0xCA to 0xCB	PAGE0x02

In order to provide flexible network management, IP1829 provides the VLAN exclusive port function which can block any packet for each exclusive port. However, exclusive port can communicate with non exclusive port. For example, if page 0x02 register 0xCA is set to 0x03, port1 and port2 can not receive packet for each other, but port3 can receive packet from both port1 and port2.

5.3.4.8 Inactive VID redirect

Related registers	0x6[1] & [14:10] & [15]	PAGE0x02

The inactive VID means the specific VLAN field in the VLAN entry is set to 1’b0. If a packet refers to inactive VID, the packet will be dropped. However, IP1829 can also redirect the packet to specific port, broadcast or drop it. For example, if bit[15] and bit [14:10] of page 0x02 register 0x06. are separately set “1” and “00000”, IP1829 will force the packet to port1.

5.4 Class Of Service (CoS)

5.4.1 Output Queue Schedule Mode with Priority

Related registers	0x01 to 0x4D, 0x76 to 0x84	PAGE0x08
	0x01	PAGE0x00

IP1829 implements eight levels of priority queues (priority queue 0 to 7). The priority for each packet is based on the following schemes:

1. Port base
2. 802.1Q tag
3. IP TOS/DSCP
4. TCP Flag
5. TCP/UDP port number
6. Supreme priority (including ACL, IP address, source MAC address)

When CoS function is enabled, the following seven scheduling modes can be selectable, If CoS function is not enabled, the first-in/first-out (FIFO) forwarding method will be only used. The detailed configuration is shown in the following table, For the WRR scheduling mode, which is defined in page 0x08 register 0x01, the order of transmitting packet sent out is from high to low priority queue, Q7 is the highest queue, Q0 is the lowest queue.

Out queue schedule function also can be set for port group A and port group B. The default is group A. If bit[9] of page 0x08 register 0x76 is set to “1”, out queue schedule mode for group B also is enabled. In this condition, group A and Group B can individually run their own out queue schedule mode simultaneously.

Table 25 Output Queue Schedule Mode Description Table

Reg 0x01[2:0]	Schedule Mode	Function description
00	Fist In Fist Out Schedule	All output packets are queued to queue 0, first comes first outs.
01	WRR/Bwassure/Bwlimit/TWRR	Queue method is selected by setting **0x01[6:5]**
02	SPx1+WRR/Bwassure/Bwlimit/TWRRx7	Mixed mode, Q7 is SP , queue6~0 are WRR/Bwassure/Bwlimit/TWRR
03	SPx2+WRR/Bwassure/Bwlimit/TWRRx6	Mixed mode, Q7 and Q6 are SP , queue5~0 are WRR/Bwassure/Bwlimit/TWRR
04	SPx4+WRR/Bwassure/Bwlimit/TWRRx4	Mixed mode, Q7~Q4 are SP , queue3~0 are WRR/Bwassure/Bwlimit/TWRR
05	SPx8	unless the high priority queue is empty, otherwise, low priority cannot transmit packets ,
06	LLQx1+WRR/Bwassure/Bwlimit/TWRRx7	Mixed mode, Q7 is LLQ , queue6~0 are WRR/Bwassure/Bwlimit/TWRR
07	LLQx2+WRR/Bwassure/Bwlimit/TWRRx6	Mixed mode, Q7 and Q6 are LLQ , queue5~0 are WRR/Bwassure/Bwlimit/TWRR

Note: WRR (Weighted Round Robin), Bwassure (Bandwidth assure), Bwlimit (Bandwidth limit), TWRR (Time Weighted Rate Return), SP (Strict Priority), LLQ (Low Latency Queue).

IP1829 provides privilege priority to decide which priority of packet should be used. When these priority is set to the packet of certain port, the order of the privilege priority is ACL > MPCP/PTP>IGMP>IP address>MAC (LUT)>VID priority>TCP/UDP port number base priority > TCP flag>IP CoS base priority > VLAN tag base priority > port base priority,

IP1829 provides an option to suspend flow control function avoiding the extra delay for a high priority packet. A port's flow control function will be suspended for 1.5sec automatically when IP1829 receives a high priority packet. This function can be enabled by programming page 0x00 register 0x01[5] to "1". Besides, IP1829 also supports SBM(static bandwidth management) and DBM(dynamic bandwidth management) mechanism to facilitate the use of out queue buffer, SBM and DBM is set for per port, means some port can be configured as either SBM or DBM.

5.4.2 Port Based Priority

Related registers	0x3A to 0x3F	PAGE0x00

The port-based priority only concerns the physical port location corresponding to switch. A packet received is regarded as the high priority packet from the high priority port. Each port of IP1829 can be configured as a high priority port individually by programming page 0x00 register 0x3A~0x3F. For example, page 0x00 register 0x3A[2:0] is corresponding to port 1

5.4.3 802.1Q VLAN Tag Based Priority

Related registers	0x40 to 0x41	PAGE0x00

When the 802.1Q VLAN tag-base priority is enabled, the 802.1Q tag priority edition can be selected by programming page 0x00 register 0x41[14]. It will examine 3 bits of the priority field carried by a VLAN tag and map it to the corresponding priority. The priority mapping is shown in the following table. The 802.1Q tag-base priority function for each port can be enabled individually by programming page 0x00 register 0x40 and 0x41.

Priority field	Queue0	Queue1	Queue2	Queue3	Queue4	Queue5	Queue6	Queue7
First Ver.	2	0	1	3	4	5	6	7
Second Ver.	1	0	2	3	4	5	6	7

5.4.4 IP ToS/ DSCP CoS Based Priority

Related registers	0x42 to 0x49	PAGE0x00

IP1829 provides the IP layer CoS function by recognizing the priority octet and mapping it to the corresponding priority. For an IPv4 packet, it is embedded in the ToS (Type of Service) Octet. For an IPv6 data packet, the Traffic Class Octet is used to differentiate the Class of Service. When this function is enabled, IP1829 will automatically recognize the IP version and capture either the TOS field (IPv4) or the Differentiated Services field (IPv6).

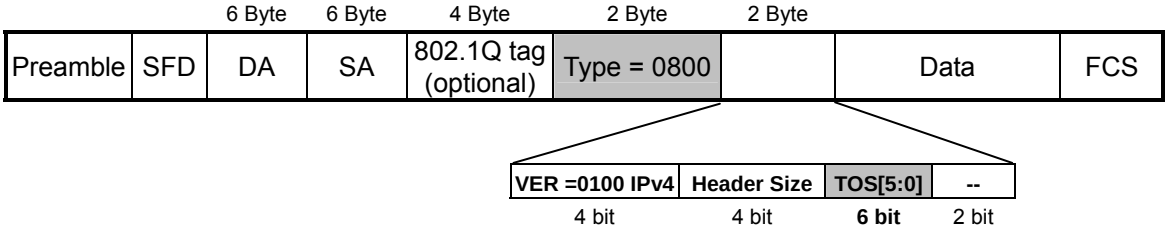


Figure 13 Frame Format of IPv4 TOS

The eight bits were allocated to a TOS field in the IP header. They can be divided into 5 sub fields:

0	1	2	3	4	5	6	7

Precedence	D	T	R	Unused

0=Most Significant Bit: 7 = Least Significant Bit.

The value of the 3 precedence bits are from 0 to 7 and are used to indicate the importance of a datagram (default is 000, higher is better).

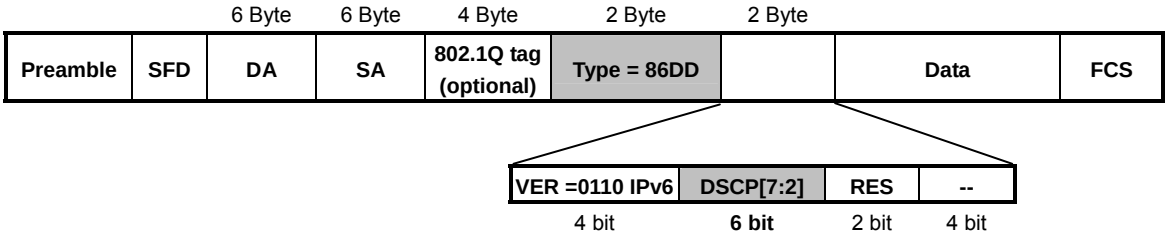


Figure 14 Frame Format of IPv6 DSCP

The IP TOS/DS priority function can be enabled individually for each port by programming page 0x00 register 0x42 and 0x43, and user can define IP TOS/DS priority setting for seven kinds of code point. If IP1829 receives a packet with IP TOS/DS code point, which is not defined in corresponding register, IP1829 provides two kinds of methods to handle undefined code point for the packet. One is the zero priority method, the packet will be treated as a lowest priority packet by programming page 0x00 register 0x45[9] to "0". The other is the Tag/Port based method, and the packet will be assigned a priority according to its priority setting on tag/port by programming page 0x00 register 0x45[9] to "1".

5.4.5 TCP/UDP Port Number Based Priority

Related registers	0x0A to 0x1C	PAGE0x00

When the TCP/UDP port number function is enabled, IP1829 will examine the TCP/UDP destination port number of the packet to decide its priority.

The user can define the priority for TCP/UDP packets by programming the corresponding bits of page 0x00 register 0x12~0x16. For example, that a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a highest priority packet if page 0x00 register 0x12[3:0] is set as 4b'0111(Q7). That a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a lowest priority packet if page 0x00 register 0x12[3:0] is set as 4b'000.(Q0)

A packet with TCP/UDP port number matches the user-defined port number, which is defined in page 0x00 register 0x0C to 0x11, the packet will be treated as a priority packet depending on the setting in page 0x00 register 0x15 to 0x16. IP1829 provides three groups for user-define port number range. For example, if port number group C is set to "highest priority" by programming page 0x00 register 0x16 [7:4], and the range of port number is set from 100 to 1 by programming page 0x00 register 0x0C~0x0D, the incoming packet(port number=10) will be forwarded to highest priority queue. The TCP/UDP port number based priority function of each port can be enabled individually by programming page 0x00 register 0x1B and 0x1C.

For the setting of TCP/UDP port number, user-defined range setting will override the setting of page 0x00 register 0x12 to 0x15. For example, if the priority of FTP (20, 21) is set to low and the priority of the port number (1~21) is set to high for user-defined range setting, the priority of port number (20, 21) will be treated as high priority rather than low priority.

Table 26 TCP/UDP Port Number priority Selection Table

Register (PAGE 0)		Port number	Definition
FTP	0x12[3:0]	20,21	0000: Queue 0 0001: Queue 1 0010: Queue 2 0011: Queue 3 0100: Queue 4 0101: Queue 5 0110: Queue 6 0111: Queue 7
SSH	0x12[7:4]	22	
TELNET	0x12[11:8]	23	
SMTP	0x12[15:12]	25	
DNS	0x13[3:0]	53	
BOOTP/DHCP	0x13[7:4]	67,68	
TFTP	0x13[11:8]	69	
HTTP_0,1	0x13[15:12]	80	
POP3	0x14[3:0]	110	
NEWS	0x14[7:4]	119	
SNTP	0x14[11:8]	123	
NETBIOS0,1,2	0x14[15:12]	137~139	
IMAP _0,1	0x15[3:0]	143,220	
SNMP_0,1	0x15[7:4]	161,162	
HTTPS	0x15[11:8]	443	
USR A	0x15[15:12]	User define A	
USR B	0x16[3:0]	User define B	
USR C	0x16[7:4]	User define C	
USR D	0x16[11:8]	User define D	
USR E	0x16[15:12]	User define E	

5.4.6 Source MAC address Priority

Related registers	0x02[3] & 0xE0 to 0xE5	PAGE0x01
	0x4A to 0x4B	PAGE 0x00

IP1829 has an option to support the Source MAC Address base Priority. IP1829 will check the corresponding bits of the LUT entry to decide the priority of the packet if source MAC address priority function is enabled, the LUT table can be configured by programming page 0x01 register 0xE0~E5. the MAC address priority function can be enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4A~4B.

5.4.7 VID based VLAN priority

Related registers	0x4C to 0x4D	PAGE0x00
	0x06[1], 0xD2 to 0xD8	PAGE0x02

IP1829 has an option to support VID based priority. This function can be enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4C to 0x4D. IP1829 will recognize the VID of incoming packets, and then check VLAN Table to find out corresponding priority setting. Each VID priority field of VLAN Table can be configured individually by programming page 0x02 register 0xD2 and 0xD8. If priority Field in VLAN entry is set to “111”, means highest queue, If priority Field in VLAN entry is set to “000”, means lowest queue.

5.4.8 IP address Priority

Related registers	0x4E to 0x4F	PAGE0x00
	0x2F to 0x3A	PAGE0x01
	0x02[15]	PAGE0x02

IP1829 has an option to support the source IP address priority. If the function is enabled, IP1829 will look up the IP entry from IP table to decide its priority. IP table can be configured by programming page 0x01 register 0x2F~0x3A. For example, if the PRI field of IP entry is set to “1111”, the IP packet will be forward to highest priority queue. If the PRI field of IP entry is set to “1000”, the IP packet will be forward to lowest priority queue. IP address priority function is enabled individually for each port by programming the corresponding bits of page 0x00 register 0x4E~0x4F to “1”. The Hashing algorithm for IP address can be set either CRC or direct method by programming page 0x02 register 0x02[15]

5.4.9 IP multicast Priority

Related registers	0x2F to 0x39	PAGE0x01
	0x50 to 0x51	PAGE 0x00

IP1829 has an option to support IP multicast priority. IP multicast priority function can be enable individually for each port by programming the corresponding bits of page 0x00 register 0x50~0x51.The user can set the priority for the IP multicast entry by programming page 0x01 0x2F ~0x39, the packet will be forward to out queue by programming PRI field of IP multicast table.

5.4.10 ACL Priority

Related registers	0x52 to 0x53	PAGE 0x00

The ACL function also has an action for priority assignment. User can set the priority for the ACL rule. The ACL priority function can be enable individually for each port by programming the corresponding bits of page 0x00 register 0x52~0x53, the packet will be forward to out queue by ACL action if it matches ACL rule.

5.5 Capture Ethernet protocol frame & IP packet to CPU port

5.5.1 In Band Management Frame

Related registers	**0x01[6], 0x5C, 0x5D,0x5E, 0x21,0x22**	**PAGE 0x00**
	0x03[0]	**PAGE 0x0C**

IP1829's default MAC address is 00-90-c3-00-00-03. If the DA of an incoming packet matches IP1829's MAC address, it will be sent to the CPU port if page 0x00 register 0x01[6] is set to "1" and page 0x0C register 0x03[0] is set to "1". IP1829's MAC address can be changed by programming page 0x00 register 0x5C~0x5E

IP1829 also provides in-band management restriction function. By checking the content of the related packet to decide the packet should be forwarded or dropped. For example, If page 0x00 register 0x01[6] is set to "1" and page 0x00 register 0x22[15] is set to "1", and the DA of the packet meets to the switch MAC address, IP1829 will forward or drop the packet, according to the corresponding bits of page 0x00 register 0x21[15:0] and page 0x00 register 0x22[14:0] , if the corresponding bit is set to "1" ,the packet will be forwarded, otherwise, the packet will be dropped

5.5.2 Block Broadcast Frames to CPU Port

Related registers	**0x0D[11:10]**	**PAGE 0x01**
	0x03[0]	**PAGE 0x0C**

In order to prevent broadcast packets to impact the performance of CPU port, IP1829 can drop broadcast and multicast frames to CPU port if page 0x01 register 0x0D[10] is set to "1" and page 0x0C 0x03[0] is set to "1", IP1829 also can only forward IPv4 /IPv6 broadcast and multicast frames to CPU port if page 0x01 register 0x0D[11] is set to "1" for specific application for CPU.

5.5.3 ARP and ICMP Storm Control

Related registers	**0x14 to 0x19**	**PAGE0x01**

In order to prevent the ARP and ICMP storm to affect the performance of IP1829, IP1829 implements ARP and ICMP storm control mechanism to drop excessive ARP/ICMP packets in specific period, ARP storm is enabled for each port by programming the corresponding bits of page 0x01 register 0x15 and 0x16[12:0] to "1", ICMP storm is enabled for each port by programming the corresponding bits of page 0x01 register 0x18 and 0x19[12:0] to "1".

A port begins to drop incoming ARP packets if the received ARP packet reaches the threshold defined in page 0x01 register 0x14[7:0], a port begins to drop the incoming ICMP packets if the received ICMP packet reaches the threshold in page 0x01 register 0x17[7:0]. Besides, IP1829 provides four kinds of periods to be selected by programming page 0x01 register 0x14[9:8] for ARP storm control and 0x17[9:8] for ICMP storm control to "00~11".

Table 27 ARP and ICMP Storm Counter Clear Period Selection Table

0x14[9:8] & 0x17[9:8]	1000Mbps	100Mbps	10Mbps
00	200us	2ms	20ms
01	1ms	10ms	100ms
10	10ms	10ms	10ms
11	100ms	100ms	100ms

5.5.4 Block ARP to CPU Port

Related registers	0x14[10]	PAGE 0x01
	0x03[0]	PAGE 0x0C

In order to prevent ARP storm to reduce the performance of CPU port, IP1829 can drop ARP frames to CPU port If page 0x01 register 0x14[10] is set to “1” and page 0x0C register 0x03[0] is set to “1”. The default setting is ARP packets to be forwarded to CPU port.

5.5.5 Ethernet L2 protocol packet capture

Related registers	0x06 to 0x07	PAGE 0x00

IP1829 recognizes layers 2 protocol frames (BPDU, 802.1x, LLDP,MPCP, Slow Protocol, GxRP, ARP, and PPPoE) to decide packet should be forwarded, dropped or “To CPU” by programming page 0x00 register 0x06~0x07 and page 0x0C register 0x03[0],the detailed description is shown in the following table ,IP1829 also provides L2 protocols for user-defined by programming page 0x00 register 0x07[14] and page 0x00 register 0x23.

Table 28 Layers Two Protocol Frames Selection Table

L2 Protocol	DA	Register (PAGE 0)	Definition
BPDU	(01-80-C2-00-00-00)	0x06[1:0]	00: forward 01: reserved 10: To CPU port only. 11: drop
Slow Protocol	(01-80-C2-00-00-02)	0x06[3:2]	
802.1x	(01-80-C2-00-00-03)	0x06[5:4]	
LLDP	(01-80-C2-00-00-0E)	0x06[7:6]	
Group 0	(01-80-C2-00-00-04~0D,0F)	0x06[9:8]	
All Bridge address	(01-80-C2-00-00-10)	0x06[11:10]	
Group 1	(01-80-C2-00-00-11~1F)	0x06[13:12]	
GARP	(01-80-C2-00-00-20, 21)	0x06[15:14]	
Group 2	(01-80-C2-00-00-22~2F)	0x07[1:0]	
Group 3	(01-80-C2-00-00-30~3F)	0x07[3:2]	
MPCP	(01-80-C2-00-00-01)	0x07[6:5]	00: drop 10: forward. x1: To CPU port only
ARP ether type = 0806		0x07[7]	0 : Forward depend on DA 1 : To DA and CPU port
IPv6 ether type = 86DD		0x07[10]	0 : Forward depend on DA 1 : To CPU port

5.5.6 Ethernet L3 protocol packet capture

Related registers	0x08 to 0x09	PAGE0x00

IP1829 recognizes layer 3 protocol frame (ICMP, TCP, UDP, OSPF ,and ICMP) to decide the packet should be forwarded, dropped or “To CPU” by programming page 0x00 register 0x08 and page 0x0C register 0x03[0]. The detailed configuration is shown in the following table.IP1829 also provides two L3 protocols for user -defined through page 0x00 register 0x08[9:8], [11:10] and 0x09

Table 29 Level Three Protocol Frames Selection Table

L3 Protocol	Register (PAGE 0)	Definition
ICMP	0x08 [1:0]	00: forward 01: reserved 10: To CPU port only. 11: drop
TCP	0x08 [3:2]	
UDP	0x08 [5:4]	
OSPF	0x08 [7:6]	
User define 1	0x08 [9:8]	
User define 2	0x08 [11:10]	
Ipv4 Other protocol	0x08 [13:12]	

5.5.7 PPPoE Protocol Check

Related registers	0x07[9:8], 0x56 to 0x59	PAGE0x00

IP1829 will check session ID of the PPPoE packets if page 0x00 register 0x07[9:8] are set to “11”, if it matches, the header of the PPPoE packet will be removed ,if it doesn’t match, the PPPoE header won’t be removed. The PPPoE session ID can be configure by programming the corresponding bits of page 0x00 register 0x56~59

5.6 Security

5.6.1 MAC Address Based Security

Related registers	0x02 to 0x04	PAGE0x01

In order to drop illegal MAC packets, IP1829 supports the MAC address based security function. When this function is enabled, IP1829 has an option to drop the packet with the SA that does not find in the MAC table. This function is valid only if the MAC learning process is disabled by programming page 0x01 register 0x03 and 0x04

For an unknown SA packet, If page 0x01 register 0x02[5] is set to “1”, the unknown SA packet will be forwarded. If page 0x01 register 0x02[5:4] is set to “01”, the unknown SA packet will be dropped. If page 0x01 register 0x02[5:4] is set to “00”, the unknown SA packet will be forwarded to CPU port.

IP1829 also supports SA associated with source port if page 0x01 register 0x02[6] is set to “1”. For example, if a packet with specific SA is learnt by port 1 in LUT, when the same SA of the packet on port 2 want to be sent to other port, the packet will not be forwarded. The packet with specific SA can send from any port if page 0x01 register 0x02[6] is set to “0”.

5.6.2 802.1x Port Base Security

Related registers	0x01[6], 0x06[5:4], 0x54 to 0x55	PAGE0x00

IP1829 supports 802.1x port base security function. If this function is enabled, IP1829 only forwards 802.1x EAPOL packets (DA=01 80 C2 00 00 03 and packet type=88 8E or DA= switch’s MAC address, packet type=88 8E and 0x01[6]=1) to CPU port and drops other types of packets. However, the ARP packets are not affected by this function and are forwarded according to their destination address.

The User can enable the 802.1x security function through programming page 0x00 register 0x06[5:4] to “10”. If the page 0x00 register 0x06 [5:4] is set to “11”, all the EAPOL packets will be dropped. This function can be enabled individually for each port by programming page 0x00 register 0x54 and 0x55.

5.6.3 IP Address Base Security

Related registers	0x01 to 0x02	PAGE0x02

IP1829 supports IPv4/IPv6 address base security function by examining the SIP address of an incoming packet. User can set each port of IP1829 to check source IP address by programming page 0x02 register 0x01 and page 0x02 register 0x02[12:0] and select one of the 2 filter modes by programming page 0x02 register 0x02[13] as shown in the following table.

To perform IP security, user has to fulfill the IP entries, if bit[183:181] in IP table are set to “111”, IP1829 will check IP address, MAC address, and source port of incoming packet whether matches the setting of IP table or not, if it matches, the packet will based on filter rule by programming page 0x02 register 0x2[13] to decide packet should be forwarded or dropped, There are two hashing methods to decide the location of an IP entry, hashing methods can support direct and CRC by programming page 0x02 register 0x02[15].

5.6.4 TCP/UDP Port Number Based Security

Related registers	0x12 to 0x20	PAGE0x00

IP1829 supports TCP/UDP port number based security function by checking the port number in an incoming packet. User can enable the function by programming register 0x1B and 0x1C. For instance, port 1 is corresponding to bit 0 of page 0x00 register 0x1B and port 17 is corresponding to bit 0 of page 0x00 register 0x1C

When this function is enabled, a packet will have one of three behaviors : 1. to CPU 2. ”to CPU and ports “ 3. Drop it, if the TCP/UDP port number matches the conditions, which defined in page 0x00 register 0x12~0x16. For example, a packet with TCP/UDP port number (FTP: 20 or 21) will be dropped if page 0x00 register 0x12[3:0] is set to “1010”. A packet with TCP/UDP port number (SMTP: 25) will be forwarded to CPU if page 0x00 register 0x12[15:12] is set to “1001”.

IP1829 provides two user-define port number setting and three user-define port number range setting to let user define port number he wants.(reg. 0x0A~0x11).

The well known TCP/UDP port is shown in following Table (defined in page 0x00 register. 0x12~0x15[11:8]), user-defined port number range setting of the TCP/UDP will override the well known TCP/UDP setting if the TCP/UDP port number is the same. For example, if FTP (20, 21) is set to drop and the port number (1~21) is set to forward to CPU port for user-defined range setting, a packet with port number (20, 21) will be forwarded to CPU port rather than dropped. There is a privilege for User-define range port number.

Table 30 TCP/UDP Port Number Based Security Selection Table

Register (PAGE 0)		Port number	Definition
FTP	0x12 [3:0]	20,21	1001: To CPU 1010: drop 1011: To CPU and ports
SSH	0x12 [7:4]	22	
TELNET	0x12 [11:8]	23	
SMTP	0x12 [15:12]	25	
DNS	0x13 [3:0]	53	
BOOTP/DHCP	0x13 [7:4]	67,68	
TFTP	0x13 [11:8]	69	
HTTP_0,1	0x13 [15:12]	80	
POP3	0x14 [3:0]	110	
NEWS	0x14 [7:4]	119	
SNTP	0x14 [11:8]	123	
NETBIOS0,1,2	0x14 [15:12]	137~139	
IMAP _0,1	0x15 [3:0]	143,220	
SNMP_0,1	0x15 [7:4]	161,162	
HTTPS	0x15 [11:8]	443	
USR A	0x15 [15:12]	User define A	
USR B	0x16 [3:0]	User define B	
USR C	0x16 [7:4]	User define C	
USR D	0x16 [11:8]	User define D	
USR E	0x16 [15:12]	User define E	

5.6.5 Port Mirroring Security (Sniffer)

Related registers	0x1E to 0x1F , 0x22 to 0x23	PAGE0x01

In some circumstances, the network administrator requires to monitor the network traffic. The port mirroring function will help the network administrator to diagnose the content of network traffic.

IP1829 provides sniffer function to meet different actual requirement. It provide two destination port group configuration and several trigger criteria. These Sniffer function are illustrated as follows.

First Sniffer destination port group configuration function:

A port mirroring function is accomplished by assigning monitored ports (source ports), snooping ports (destination ports) and snooping method. IP1829 will copy the monitored packets to all snooping ports. The IP1829 supports three kinds of snooping methods: the ingress, egress and ingress + egress, which is defined in page 0x01 register 0x1F[14:13], the ports to be monitored (mirroring source),which is defined in register 0x22 and 0x23[12:0] , the ports to snoop (mirroring destination), which is defined in page 0x01 register 0x1E and page 0x01 register 0x1F [12:0].

For example, if user wants to monitor the output traffic of port 16 and port 17 from port 1 as shown in the following figure. He has to write “01” to page 0x01 register 0x1F[14:13] to choose monitor method to be egress traffic, write 0x8000 and 0x0001 to page 0x01 register 0x22 and page 0x01 register 0x23[12:0] to select port 16 and port 17 to be monitored ports, write 0x0001 and 0x0000 to page 0x01 register 0x1E and page 0x01 register 0x1F [12:0]to select port 1 as a monitoring port. IP1829 will copy the egress traffic port 16 and port 17 to port 1.

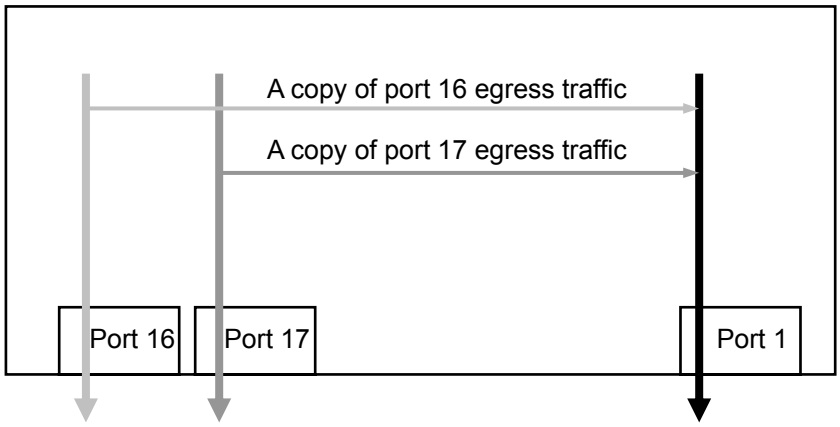


Figure 15 Port Mirroring Security Block Diagram

IP1829 also has options to keep the mirrored packet with the original tagging. The source of the mirrored packets can be separated into three groups. Their tagging status can be controlled through page 0x01 register 0x1F[15] and 0x24[7:5].

The above description is summarized as follows.

Sniffer Add/Rem Tag option for ACL routing

Original packet	Action(add/remove tag) by register CC~CF(page 0x02)	behavior	
		Reg1f[15]=1, Reg24[6]=0(page 0x01)	Reg1f[15]=1, Reg24[6]=1(page 0x01)
		Destination port	Destination port
Untag	Add tag	untag	tag
tag	Remove tag	tag	untag

Destination port must be assigned in the field of mode entry of ACL

Sniffer Add/Rem Tag option for CPU special tag routing

Original packet	Action(add/remove tag) by register CC~CF(page 0x02)	behavior	
		Reg1f[15]=1, Reg24[5]=0(page 0x01)	Reg1f[15]=1, Reg24[5]=1(page 0x01)
		Destination port (only for CPU port)	Destination port (only for CPU port)
Untag	Add tag	untag	tag
tag	Remove tag	tag	untag

Sniffer Add/Rem Tag option for other packet

Original packet (monitored port)	Action (add/remove tag) by register CC~CF (page 0x02)	behavior	
		Reg1f[15]=1, Reg24[7]=0(page 0x01)	Reg1f[15]=1, Reg24[7]=1(page 0x01)
		Destination port	Destination port
Untag	Add tag	untag	tag
tag	Remove tag	tag	untag

Destination port must be assigned in the field of special tag.

Second Sniffer destination port group configuration function

IP1829 also provides second sniffer destination port group configuration function for MAC/IGMP/IP/ACL sniffering . IP1829 will forward packets to destination port for either first sniffer group or second sniffer group, according to MAC/IGMP/IP/ACL sniffering, Besides, DA or SA trigger can be selected for MAC address table by programming page 0x01 register 0x21[14:13], which can individually support first sniffer destination group configuration and second sniffer destination group configuration.

5.7 WAN/LAN Port Filtering

Related registers	0x0A to 0x11, 0x17 to 0x1A	PAGE0x00
	0x0D to 0x16	PAGE0x06

IP1829 supports TCP/UDP port number based filter function by checking both the port number in an incoming packet and an outgoing packet. User can enable the function by programming page 0x00 register 0x17~ 0x1A. IP1829 also supports positive and negative filter. User can select either positive or negative filter to use. In positive filter, if a packet with TCP/UDP port number doesn't match the corresponding bit of TCP/UDP port number setting, the packet should be dropped according to WAN/LAN port filtering by programming page 0x06 register 0x0D~0x16. In negative mode, if a packet with TCP/UDP port number matches the corresponding bits of TCP/UDP port number setting, the packet should be dropped according to WAN/LAN port filtering by programming page 0x06 register 0x0D~0x16. WAN/LAN port filtering can be configured as "disable filter", RX drop, TX drop, or TX/RX drop. For example, if "disable filter" is set, means that packet will be forwarded, if "RX drop" is set, means that packet will be dropped at host port.

IP1829 can choose either WAN port or LAN port by programming page 0x06 register 0x11 ~12. For example, if the host port(port1) is set to "forward to LAN port only" by programming page 0x06 register 0x0D[1:0] to "10" and client port(port2) is set to LAN port by programming page 0x06 register 0x11[1] to "0" , the drop on ACT filtering only work at client port, and then the packet will be forwarded or dropped by programming page 0x06 register 0x0D[3:2] to "01" and programming page 0x06 register 0x13[3:2] to "00~1X", if client port is WAN port, the packet is always dropped. If the host port is set to "forward to WAN port only" and client port is set to WAN port, the filtering only work at client port, if client port is LAN port, the packet is always dropped.

If host port(port1) is set to "drop on ACT filtering" by programming page 0x06 register 0x0D[1:0] to "01" and programming page 0x06 register 0x13[1:0] to "00"(RX drop) , the packet will be dropped at host port(port1), If client port(port2) is set to "drop on ACT filtering" by programming "page 0x06 register 0x0D[3:2] to "01" and programming page 0x06 register 0x13[3:2] to "01"(TX drop) the packet will be dropped at client port(port2). If host port and client port are set to "Disable Forwarding WAN/LAN& Packet drop", the packet is always forwarded.

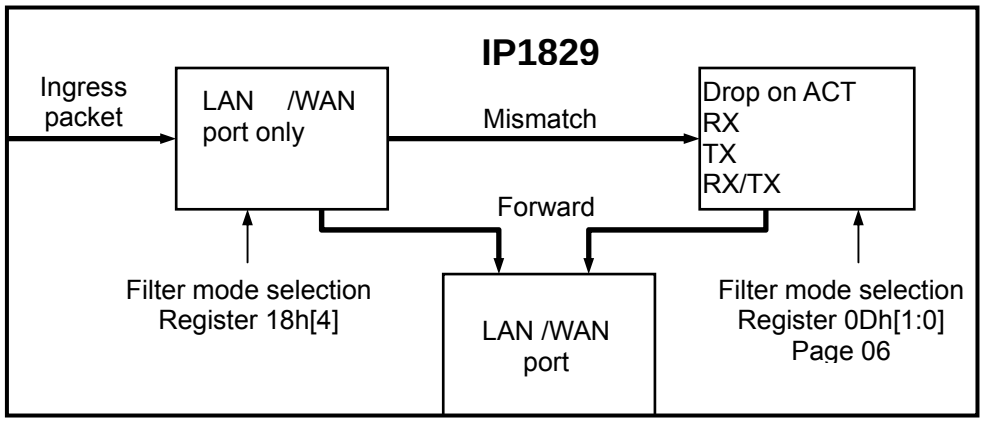


Figure 16 WAN Port Filtering Block Diagram

IP1829's TCP/UDP port number filter mode (positive or negative) and the filter method conditions (disable, drop on act, Forwarding to WAN port only ,forward to LAN port only) is summarized as follows, please refer to the following table:

Table 31 Host / Client Forwarding WAN / LAN and Packet drop setting Condition Table

Host / Client Forwarding WAN / LAN and Packet drop setting Condition														(1) **V : PASS** (2) **X : Drop** (3) Host port Switch Port to receive packet (4) Client port Switch Port to transmit packet
Host / Client			Client Port setting											
			Client is LAN Port						Client is WAN Port					
			00 Disable	01 Drop			10 LAN	11 WAN	00 Disable	01 Drop			10 LAN	11 WAN
				RX	RX+TX	TX				RX	RX+TX	TX		
Host port setting	00 Disable		V	V	X	X	V	V	V	V	X	X	V	V
	01 Drop	Act on RX	X						X					
		Act on TX+RX												
		Act on TX	V	V	X	X	V	V	V	V	X	X	V	V
	10 FWD LAN		V	V	X	X	V	V	X	X	X	X	X	X
	11 FWD WAN		X	X	X	X	X	X	V	V	X	X	V	V

5.8 IEEE 1588 Precision Timing Protocol (PTP)

Related registers	**0x0A4**	**PAGE0x00**
	0x00 to 0x36	**PAGE0x09**

IP1829 implements the precision timing protocol (including IEEE1588/IEEE802.1as) function. For the PTP application, IP1829 uses the PTP dedicated hardware to capture the timestamp of PTP frame and store them into internal buffer. The software processes the various protocol message and co-work with PTP dedicated hardware.

To synchronous the master clock, IP1829 offers the adjustable real time clock (RTC), which could increases, decreases the clock frequency and set the specific time-value into RTC. If the PTP packet is detected, the PTP dedicated hardware will capture the time-value of SFD position for PTP or event signal. After the PTP synchronization process, the CPU uses the ingress/egress time-stamp to obtain the compensation parameter. Then, the CPU will pass the relating compensation value into PTP dedicated hardware. After the long duration, the PTP dedicated RTC is synchronous with the remote master clock.

For each port, IP1829 supports 32 depth timestamp FIFO (16 for ingress, 16 for egress) to record PTP time-stamp. When all time stamps are occupied, user also set overwrite bit enable to over write time stamps cyclically. Another, IP1829 also supports 8 time stamps for incoming event trigger signal.

For the monitor system application, IP1829 support three different output synchronous signals. These output signals are pulse-per second, the programming clock duration signal and trigger-out signal. Further, please refer to PTP application note in detail.

5.9 Hardware Loop detection

Related registers	**0x6B to 0x73,**	**PAGE0x00**
	0xA5 to 0xA6	**PAGE0x00**
	0x24[3]	**PAGE0x01**

IP1829 support hardware loop detection ,Each port can configure loop detection by programming page 0x00 register 0x6B and 0x6C[12:0]. IP1829 will send loop detect packet to detect whether or not loop happen, IP1829 can check loop status of each port by reading the corresponding bits of page 0x00 register 0xA5~0xA6., if loop occur, IP1829 will block redundant until loop release. For blocking redundant path, page 0x01 register 0x24[3] must be set to “1”.

5.10 Trunk Channel

Related registers	0x1C to 0x1D	PAGE0x01

5.10.1 Trunk Channel Behavior

IP1829 provides two kinds of trunk methods to configure trunk group by programming page 0x01 register 0x1C~ 0x1D. one is the single trunk group and the other is the double trunk group, IP1829 supports 6 single trunk groups and 3 double trunk groups by programming page 0x01 register 0x1C[7:5]. The single trunk group0~3 consist of 2 to 4 ports and trunk group4~5 consist of 2 ports. The two single trunk groups can merge into one trunk group, for example, trunk0~1 can be combined as a large trunk group, the members of double trunk group can be set as port1~8(at least 2 ports), and so on. User can configure either the members of single trunk group or double trunk group individually by writing “1” to the corresponding bits of the port for each trunk in page 0x01 register 0x1C[15:8] ~0x1D. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP1829 forwards the packet to the other port of the trunk (auto recovery).

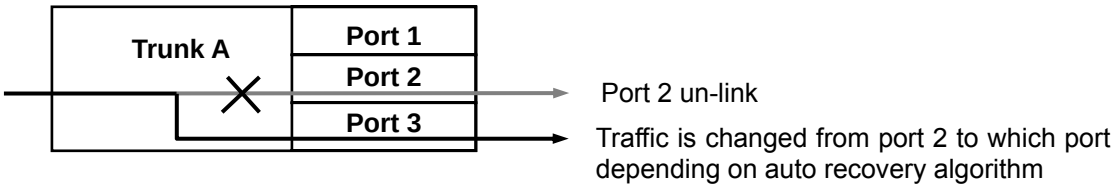


Figure 17 Trunk Channel Behavior Block Diagram

5.10.2 Load Balance

To fully utilize the bandwidth in a trunk channel, IP1829 supports load balance function. A physical port of a trunk forwards a packet only if the trunk ID of the packet matches the ID setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk ID.

IP1829 provides 8 kinds of hashing methods to support trunk function, user can select one of hashing methods to generate hashing ID by programming page 0x01 register 0x1C[2:0], the hashing ID0 means to select first port of the trunk group, hashing ID1 means to select second port of the trunk group, etc.

The sequence of the hashing methods can be set by programming page 0x01register 0x1C[3], the behavior is illustrated as follows.

Case1: disable sequence option: if incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/SP, the hashing method will change to use DA/SA. If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/DP, the hashing method will change to use DA.

Case2: enable sequence option: If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/SP, and then the hashing method will change depending on the type of packet. If the packet is IP packet, the hashing method will change to use SIP. If the packet is not IP packet, the hashing method will change to use DA/SA. If incoming packet is not TCP/UDP packet and hashing method of the trunk group is set to TCP/UDP/DP, if the packet is IP packet, the hashing method will change to use DIP. If the packet is not IP packet, the hashing method will change to use DA

Each hashing method is described as follows

Hashing method	Port	SA	DA	SA/DA	SIP	DIP	TCP/UDP DP	TCP/UDP DP
Single trunk	By port	Bit[1:0]	Bit[1:0]	Bit[1:0] XOR Bit[1:0]	Bit[3 XOR 2] Bit[1 XOR 0]			
Double trunk	By port	Bit[2:0]	Bit[2:0]	Bit[2:0] XOR Bit[2:0]	Bit[2 XOR 1];Bit[3 XOR 2]; Bit[1 XOR 0]			

If the destination port of a trunk is un-link, the packet will be forward the port shifted by -1. If the port is un-link, too, the packet will be forward the port shifted by +2. For example, if port 4 is un-link, its packet will be forwarded to port 3. If port 3 is un-link, too, the packet will be forwarded to port 1.

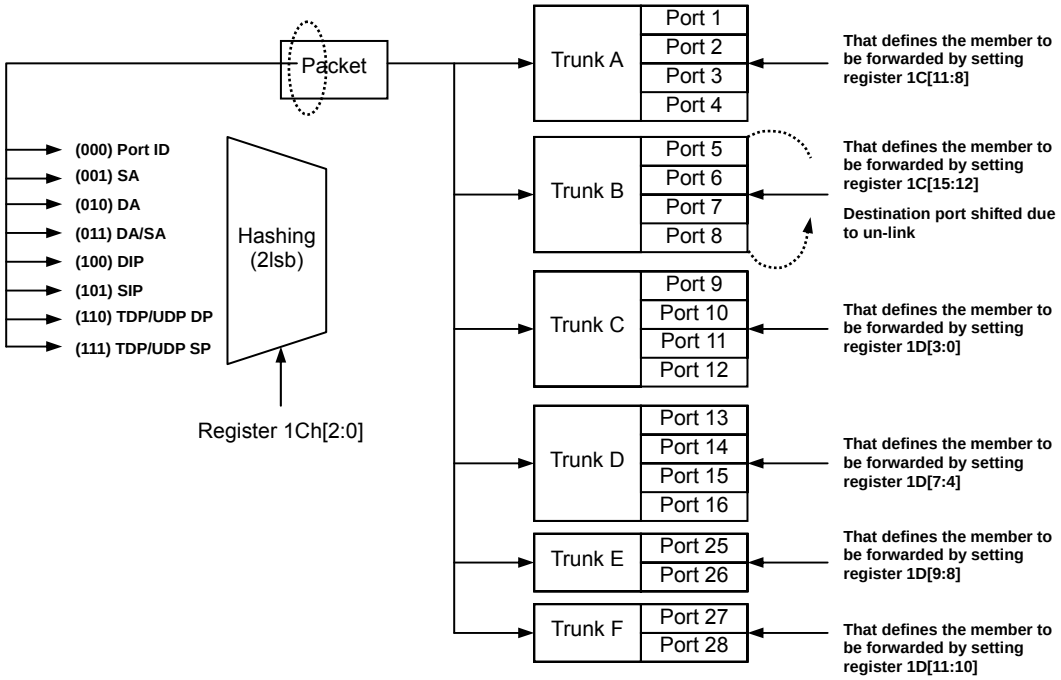


Figure 18 Load Balance Block Diagram

If the double trunk group is selected, the trunk hashing algorithm is changed from 2bit to 3 bit, single trunk group uses 2 bits hashing algorithm to generate Hashing ID, ranging from 0 to 3, double trunk group use 3 bits hashing algorithm to generate Hashing ID, ranging from 0 to 7.

5.11 Spanning Tree

Related registers	**0x06 [1:0]**	**PAGE0x00**
	0x57 to 0x96	**PAGE0x01**
	0x03[0] , [1], 0x04[15:0]	**PAGE0x0C**

5.11.1 BPDU Packet Forwarding

IP1829 support spanning tree function with the following steps:

1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU and add special tag with port information.
3. Special tag type is defined in page 0x0C register 04[15:0] and the special tag enable by writing "1" to page 0x0C register 0x03[1]. The BPDU packets is forwarded to CPU port by writing "01" to page 0x00 register 0x06[1:0] and CPU port is enabled by writing "1" to page 0x0C register 0x03[0].

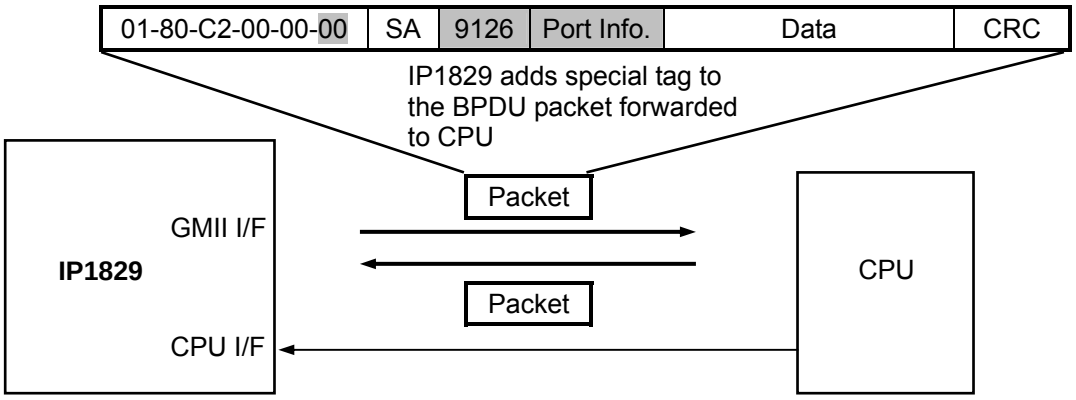


Figure 19 BPDU Packet Forwarding Block Diagram

5.11.2 Port States

Related registers	**0x57 to 0x96**	**PAGE0x01**
	0x06[6], 0xD2 to 0xD8	**PAGE0x02**

To support IEEE802.1D spanning tree protocol, each port of IP1829 supports four states (discard state, blocking state, learning state, forwarding state), is shown in the following table. Each port of IP1829 can be set in one of the four spanning tree states individually by programming page 0x01 register 0x57 to 0x5A for STP and page 0x01 register 0x57 to 0x96 for MSTP.

IP1829 also supports multiple STP. IP1829 will use MSTP registers to set up state for each port, IP1829 use FID filed of VLAN table to mapping to corresponding register. IP1829 provides 16 set of VLAN settings for MSTP.

Table 32 Port States Selection Table

Status in 802.1D	Corresponding function (register)			
	BPDU packets		Normal packets	
	Port_RX(to CPU)	Port_TX(from CPU)	Port_RX (to CPU)	Port_TX(from CPU)
Discard(00)	X	X	X	X
Blocking(01)	O	X	X	X
Learning(10)	O	O	learning	X
Forwarding(11)	O	O	O	O

5.12 IGMP Snooping

Related registers	0x29 to 0x56	PAGE0x01
	0x03[0]	PAGE0x0C

IP1829 supports IGMP v1, v2 and v3 snooping specified in RFC1112, 2236 and 3376 respectively. Because IGMP is used between hosts and multicast routers, IP1829 listens the IGMP messages that communicate between router and host to establish multicast group membership. Based on the group membership information, IP1829 forwards IP multicast data to its members which is registered in group table. IGMP snooping function can be configured by page 0x01 register 0x29~0x56. For hardware IGMP snooping, IP1829 receives query, report and leave packets to build multicast table. IP1829 also has an option to support timeout mechanism, If a host port is time expired in this group, the host port will leave the multicast group.

Except for hardware IGMP snooping, IP1829 also supports software IGMP snooping and IGMP snooping with CPU assistance. Software IGMP snooping implies that CPU must handle IP multicast traffic which includes IGMP packet and IP multicast data packet, and then forwards them to multicast group member after processing done. For the IGMP snooping with CPU assistance, the switch directly forwards the report and leave packets into CPU port, and then CPU will build multicast table according to report and leave packets. Besides, multicast data packet will be forwarded according to multicast table by IP1829.

IP1829 supports not only IGMP snooping for IPv4 but also MLD snooping for IPv6. MLDv1 is similar to IGMPv2 and MLDv2 is similar to IGMPv3. When the IGMPv3 or MLDv2 multicast packets are coming, it will be forwarded depending on multicast table and source list table.

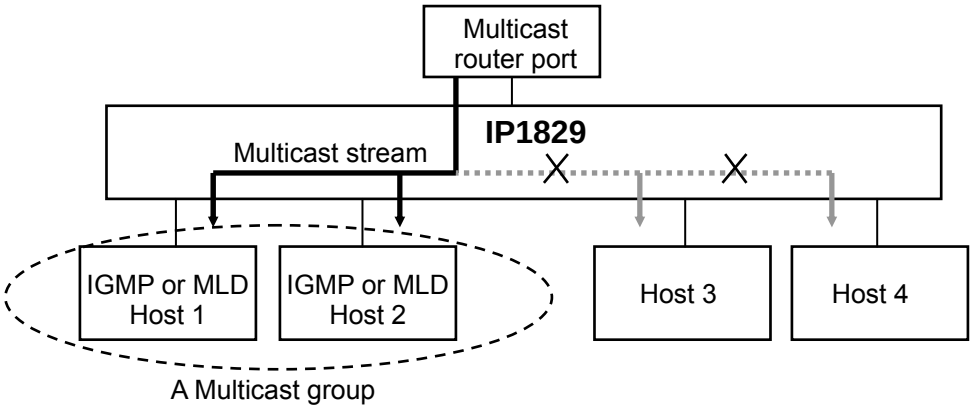


Figure 20 IGMP Snooping Block Diagram

5.13 IRMP (ICPLUS remote management protocol)

Related registers	0x01 to 0x0B	PAGE0x0A

IP1829 implements IRMP for accessing register in remote condition, IRMP is ICPLUS remote management protocol, all IP1829 registers can be easily accessed via running the IRMP protocol. All configurations of the IRMP protocol can be set by writing page 0x0A register 0x01 to 0x0B. In order to accomplish remote control, IRMP uses handshaking mechanism to complete the all IRMP actions, such as hello request /acknowledge action, login request /acknowledge, etc. The IRMPPDU frame structure is illustrated as follows (detail description, please refer to application note.)

Table 33 ICPLUS remote management protocol format

DA (6B) = Destination MAC address			SA (6B) = Source MAC address			Service tag (4B) (optional) **[0x88a8_xxxx]**	
Customer tag (4B) (optional)**[0x8100_xxxx]**	EtherType (2B) **[0x8931]**	SubType (2B) **[0xFFFF]**	Flag (1B)	Op (1B)	Vender ID (4B) **[0x0090_C300]**		Device ID(2B) **[0x8290]**
Password (4B) or Port information	Conn. ID(2B)	Reg Add 0(2B)	Reg Data 0(2B)		Reg Add 1(2B)	Reg Data 1(2B)	Reg Add 2(2B)
Reg Data 2(2B)	Reg Add 3(2B)	Reg Data 3(2B)	PAD [0x00]			CRC (4B)	

5.14 IPv6 related functions configuration

Related registers	0xA7 to 0xA9	PAGE0x00

IP1829 also supports IPv6 protocol, IP1829 examines IPv6 header to support specific purpose for IPv6 protocol. IP1829 will check next header in IPv6 header, if it matches, IPv6 packet will be forwarded, dropped, “To CPU and DA”, or To CPU by programming page 0x00 register 0xA8~0xAC, IP1829 supports the following header table

Order	Header type	Next header code
1	Fragment Header	44
2	Encapsulation header	50
3	Authentication Header	51
4	ICMPv6	58
5	User define header	xx

NDP (neighbor discovery protocol) is defined in RFC 2461. It uses ICMPv6 to exchange the messages necessary for its functions

Order	Type	Next header code
1	Router solicitation	133
2	Router Advertisement	134
3	Neighbor solicitation	135
4	Neighbor Advertisement	136
5	redirect	137

MLD (Multicast Listener Discovery) the protocol is embedded in ICMPv6 instead of using a separate protocol. MLDv1 is similar to IGMPv2 and MLDv2 is similar to IGMPv3. The protocol is described in RFC 3810

Order	Type	Next header code
1	MLDv1 query	130
2	MLDv1 listener report	131
3	MLDv1 listener done	132
4	MLDv2 listener report	143

5.15 ACL

Related registers	**0x52 to 0x53**	**PAGE0x00**
	0x24 & 0x99	**PAGE0x01**
	0x8A to 0xED	**PAGE0x02**
	0x01 to 0x6F	**PAGE0x07**

IP1829 supports 128-entries for ACL rule. The ACL function is enabled if page 0x01 register 0x24[0] is set to "1" , When a packet is received, IP1829 will examine whether the incoming packet meet in specific ACL rule entries in mode table, each mode comprises of some rules, such as SIP,DIP, TCP/UDP, SMAC,DMAC,VLAN, and physical port , and so on. If it matches, the packet will act according to corresponding ACT entry.

5.16 OAM

Related registers	**0x01 to 0x08**	**PAGE0x04**

IEEE802.3ah OAM (Operations, Administration and Maintenance) is a point to point slow protocol and is used to maintain the health of the link. The main functions provided are:

- Auto Discovery
- Fault Indication
- Remote LoopBack Test

6 bytes	6 bytes	2 bytes	1 bytes	2 bytes	1 bytes		
DA(01-80-C2-00-00-02)	SA	8809	03	flags	code	Data	FCS

Figure 21 802.3 OAM Frame Format

IP1829 supports OAM functions, including Auto Discovery/Fault Indication/Remove LoopBack Test/Remote R/W registers.

IP1829 OAM functions and controls are set via accessing the indirect register per port. Detail information please reference to the OAM application note.

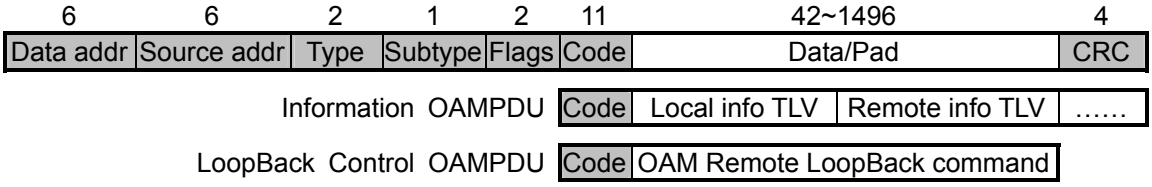


Figure 22 OAMPDU messages Frame Format

5.17 Special tag

Related registers	0x41[13]	PAGE0x00
	0x03 [1:0] , 0x04	PAGE0x0C

The purpose of special tag is:

- To allow a frame (switch to CPU) to carry ingress port number ,Queue ID ,PTP and sFlow information carriers in special tag header
- To allow a frame (CPU to switch) to indicate the output port mask and output queue number carriers in special tag header

5.17.1 Special Tag for TX (From CPU to switch)

Frame direction is from CPU to switch. IP1829 enables special tag function by programming register 0x03[1] page C. This function provides for dedicated forwarding port decision and priority assignment. These parameters are embedded in special tag header, which can be set by CPU. the special data will be remove by switch itself when the dedicated port have received packet, if DFP is set to 0 , the frame will be based on it's DA to be forwarded.

Figure 23 Special Tag for TX Frame Format (From CPU to switch)

DA	SA	Special tag	Special data
		0x9126	(1) 4 Bytes

Special data (1)						
Special tag data (4bytes)						
31	30	29	28	27	26-1	0
Dedicated priority queue (DPQ)			**DFP enable**	Dedicated forwarding port map (DFP)		

DPQ Enable bit: 0x41[13] page0 (0:Q0, 1:Q1 , …. , 7: Q7)

5.17.2 Special Tag for RX (From switch to CPU)

Frame direction is from switch to CPU. IP1829 enables special tag function by programming page 0x0C register 0x03[1] .The special tag information consists of source port number and QID , if the incoming packet with OAM information is forwarded to CPU , CPU will showed off OAM packet Flag field and code , these information carrier in special tag header 0x9126 (Page 0x0C.Reg 0x04).

Figure 24 Special Tag for RX Frame Format (From switch to CPU)

DA	SA	Special tag	Special data		
		0x9126	(1) 4 Bytes		
		0x9127(+1)	(1) 4 Bytes	(3) 8 bytes PTP stamp info	
		0x9128(+2)	(1) 4 Bytes	(2) 28 bytes sFlow info	
		0x9129(+3)	(1) 4 Bytes	(2) 28 bytes sFlow info	(3) 8 bytes PTP stamp info

Special data (1)

Special tag data (4bytes)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PTP/ normal (0)			Stamp	U/M	ACL redirect	Snif	U-SA	CCPU	DLF	PTP	SEQ3	SEQ2	SEQ1	SEQ0	0
CFM opcode (6,5,4,3,2,1)			U/M							MD_Level			--		
OAM (7)			OAMPDU Flag field							OAMPDU code					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								Queue ID			Source port				

CFM opcode&OAM &others	7: OAM	6: others CFM opcode
	5: LTM	4: LTR
	3: LBM	2: LBR
	1: CCM	0: PTP or normal packet (not include CFM,OAM)
OAMPDU Flag & code	OAMPDU Flag	OAMPDU code
	Bit[6]:remote stable	6.7 : others
	Bit[5]:remote evaluating	5: organization specific
	Bit[4]:local stable	4: LoopBack control
	Bit[3]:local evaluating	3: variable request
	Bit[2]:critical event	2: variable response
	Bit[1]:dying gasp	1: Event notification
	Bit[0]:link fault	0: information
U/M	Uni port / Multi port output	
ACL redirect	ACL action redirect	
Snif	Sniffer packet	
U-SA	Unknown SA	
CCPU	Capture to CPU	
DLF	Destination lookup Fail	
STAMP	PTP packet is stamped	
PTP	PTP packet [31:29] =0 , PTP packet [21]=1	
SEQ0,1,2,3	PTP RX stamp sequence	
QID	Out Queue from which Queue ID	
SP	Source port	

If PTP information for special tag is enabled by programming ”1” to page 0x07 register 0x7A[5] ,the PTP information will be added to incoming packet ,and then the packet will be forwarded to CPU, the special tag is 0x9127. If sFlow information for special tag is enabled by programming “1” to page 0x07 register 0x7A[4], the sFlow information will be added to incoming packet ,and then the packet will be forwarded to CPU, the special is 0x9128 . If PTP and sFlow information for special tag are enabled by programming “11” to page 0x07 register 0x7A[5:4], the both PTP and sFlow information will be add to incoming packet ,and then the packet will be forwarded to CPU, the special tag is 0x9129.

Special data (2)

Special tag data (28bytes)															
223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208
VLAN tag Remove/Add [57:42]															
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
VLAN tag Remove/Add [41:26]															
191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176
VLAN tag Remove/Add [25:10]															
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
VLAN tag Remove/Add [9:0]										arl_route_result [28:23]					
159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
arl_route_result [22:7]															
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
arl_route_result [6:0]							PRI [2:0]			Mac rx count [14:9]					
127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Mac rx count [8:0]									VID[11:5]						
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
VID [4:0]					ACL SF	Egress SF	Ingress SF	SF_Rate [15:8]							
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
SF_Rate [7:0]								0							
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
0						Service tag Remove/Add [57:48]									
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Service tag Remove/Add [47:32]															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Service tag Remove/Add [31:16]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Service tag Remove/Add [15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												PPPoE remove	QID		

Special data (3)

Special tag data (8bytes)															
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Time stamp second [31:16]															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Time stamp second [15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
full	0	Time stamp nano second [29:16]													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp nano second [15:0]															

5.18 sFlow

Related registers	0x97 to 0xD8	PAGE0x01
	0x7A[3:0]	PAGE0x07

IP1829 supports sFlow function, which can monitor the content of the packet, IP1829 provides various methods to sample sFlow packet to CPU port , such as inbound , outbound , VID, ACL and MAC Lookup table, which can be set by programming page 0x01 register 0x99 to 0x9E. sFlow can be configured individually for each port, such as sampling rate, etc. IP1829 also provides global counter or independent counter, which can be set by programming page 0x01 register 0x9E[12]. For example, if global counter is set by programming page 0x01 register 0x9E[12] to "1" and inbound method is set by programming the corresponding bits of page 0x01 register 0x99~9Eh to "000", packets start to accumulate for all ports during incoming packet is received, when accumulated packets reach threshold value, then one sampled packet will be forwarded to CPU port.

Besides, IP1829 also supports length cutoff for sFlow packet. According to the setting of the cutoff in page 0x07 register 0x7A[3:0]. If the sFlow packet length is less than the setting of the length cutoff, the sFlow packet length will not modify by CPU port.

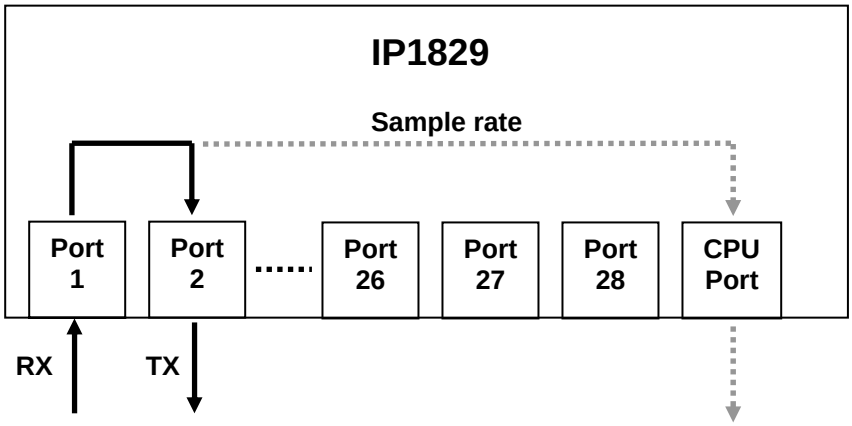
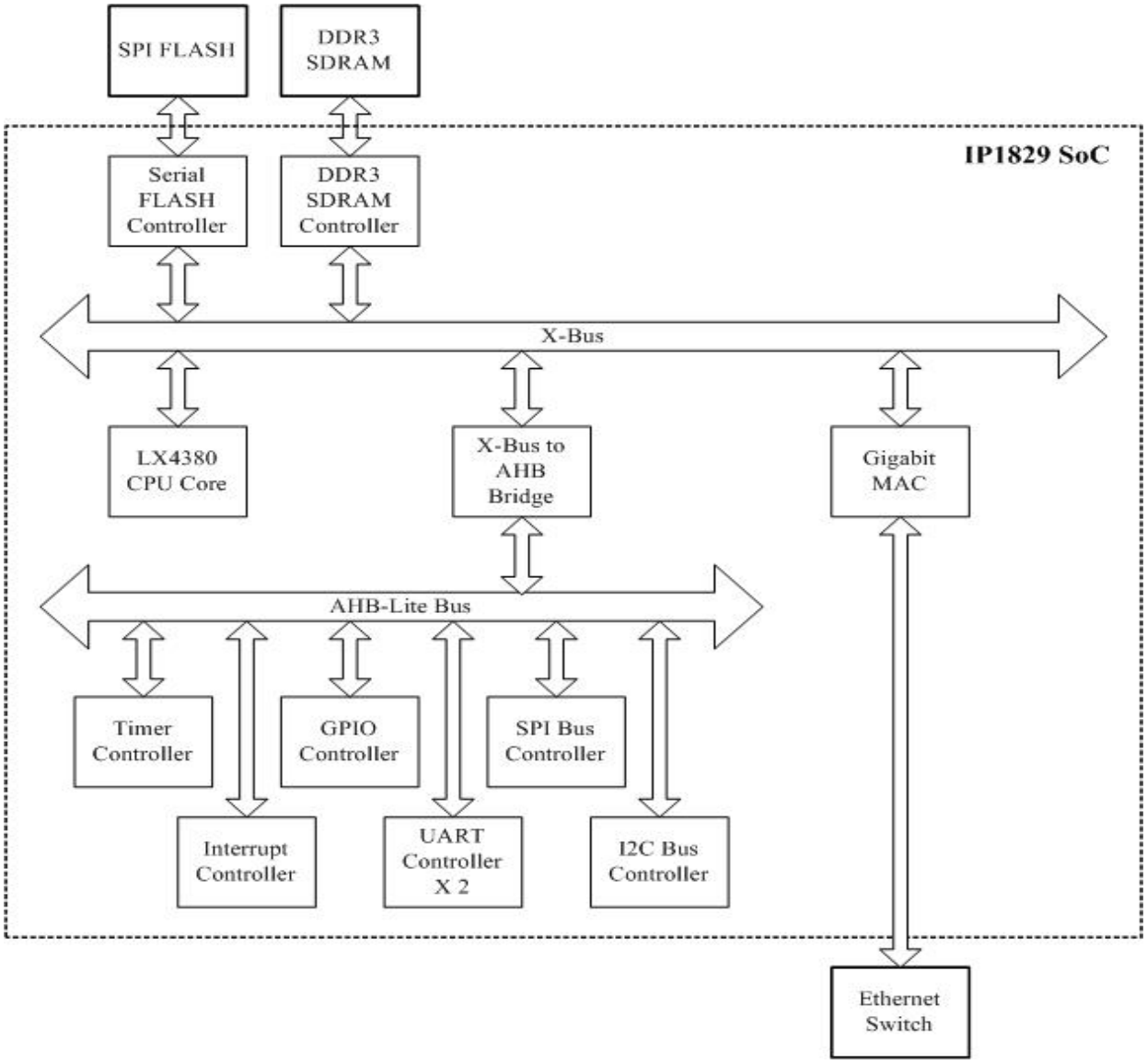


Figure 25 sFlow function diagram

5.19 Embedded 32-bit CPU

5.19.1 CPU Block Diagram



IP1829 SoC Block Diagram

The 32bit embedded CPU built in SDRAM Memory Controller, SPI Flash Controller, Gigabit MAC, Interrupt Controller, Timer and Counter, General-Purpose I/O, SPI Controller, UART, and I^2C Controller .The features and functions of 32bit embedded CPU are illustrated as follows.

5.19.2 CPU Features

- MIPS24Kef Core runs at either 500MHz or 250MHz. The clock speed is programmable (Refer to the timer controller).
- The cache supports 4-way set associative 32 KB instruction cache and 4-way set associative 32 KB data cache.
- Support MMU functions with 32 joint TLB entries.
- Use big-endian data representation.

5.19.3 DDR3 Memory Controller

The memory controller supports DDR3 memory and the data bus width can be either 8 or 16. Supported DDR3 memory size up to 256Mbytes

5.19.4 SPI Flash Controller

5.19.4.1 Direct mapping mode (D-MAP)

The purpose of direct mapping mode is to support system boot from the SPI flash device. After power on or system reset, the SPIFC will, by default, enter the direct mapping mode, in which a bus master can read boot codes from the SPI flash without the needs to issue command sequences in order to access the SPI flash. In other words, direct mapping mode supports only read access to the SPI flash.

5.19.4.2 User mode

Support two SPI-flash devices (channels). Using SPI flashes of the same memory size is recommended. The controller supports Flash up to 16 Mbytes each. (In other words, there is only 24bits address for SPI-flash in user mode).

5.19.5 The Ethernet Gigabit MAC

The Ethernet gigabit MAC is internally connected to the CPU port of the 3-port switch, so it does not implement a full 802.3 CS/CDMA MAC. Instead it only implements a gigabit MAC that always operates at gigabit full duplex mode. And the link status is always on.

A MDC/MDIO management interface is also implemented to access external Ethernet devices such as Ethernet PHY or Ethernet switch.

5.19.6 Interrupt Controller

- The interrupt controller supports the compatibility mode of the MIPS24Ke interrupt model by implementing the IP[7:2] of the STATUS register of CP0 (co-processor 0).
- The interrupt controller accepts interrupts from peripheral devices either internal of or external to the chip. These interrupts are routed to the CPU's status register (IP[7:2] of CP0 Status register) according to their assigned route number.
- Mask bits for individual peripheral interrupts can be set to mask out unwanted interrupts.
- There are a total of 4 external interrupts, coming from the 4 external interrupt pins INTR[3:0]. These external interrupt pins are multiplexed with the general-purpose I/O pins. The external interrupts can be individually configured as level high trigger, level low trigger, rising edge trigger, or falling edge trigger. These external interrupt pins are enabled only when the corresponding bits of the External Interrupt Select register is set to 1. Please see the description about general-purpose I/O for details.

5.19.7 Timer and Counter

The general timer, when enabled, will start counting down on a pre-scaled time unit. When the timer reaches zero, the timer status is set and if the interrupt is enabled, a timer interrupt is issued, at which time, the timer is loaded a value from the general value register and keeps counting down.

The watchdog timer also works similarly to the timer, except that when it reaches zero, no interrupt will be issued; instead a system reset will be issued to reset the chip.

5.19.8 General-Purpose I/O

There are up to 48 General-purpose I/Os, which can be configured as LCD I/F, SPI I/F, I2C I/F, external interrupts, or used as plain GPIO pins (However, each project may choose which GPIO pins are actually implemented by connecting/dis-connecting these 48 GPIO pins).

5.19.9 SPI Controller

The SPI controller supports 4 chip select signals that can interface with up to 4 external SPI devices, depending on the bonding of the chip.

5.19.10 UART

The UART is a 16550-compatible UART with TX and RX FIFO of 16 bytes each.

5.19.11 I²C Controller

- The I²C controller acts as an I²C master and an optional I²C slave.
- Standard Mode (S-mode), Fast Mode (F-mode), and High-speed Mode (HS-mode) are all supported. Besides, the heavy-load condition of HS-mode is also supported.
- 10-bit address is supported.
- For slave mode, general call 04, general call 06, and hardware general call are supported.
- Auto-retry when losing arbitration is supported. This feature is configurable.
- "START" code is supported in slave mode to trigger interrupts only.

6 Register Description

6.1 PHY Register Map

Read / Write PHY register by page 3 register 0x13,0x14

Table 34 PHY Register Map

Page	PHY address	Register	Description	Default
0	PHY 08~31	0	Control Register	
0	PHY 08~31	1	Status Register	
0	SHARE X 1	2	PHY Identifier 1 Register	
0	SHARE X 1	3	PHY Identifier 2 Register	
0	PHY 08~31	4	Auto-Negotiation Advertisement Register	
0	PHY 08~31	5	Auto-Negotiation Link Partner Ability Register	
0	PHY 08~31	6	Auto-Negotiation Expansion Register	
0	PHY 08~31	7	Auto-Negotiation Next Page Transmit Register	
0	PHY 08~31	8	Auto-Negotiation Link Partner Next Page Register	
0	PHY 08~31	13	MMD Access Control Register	
0	PHY 08~31	14	MMD Access Address Data Register	
0	PHY 08~31	3.0	PCS control 1 register	
0	PHY 08~31	3.1	PCS status 1 register	
0	PHY 08~31	3.20	EEE capability	
0	PHY 08~31	3.22	EEE wake error count	
0	PHY 08~31	7.60	EEE advertisement register	
0	PHY 08~31	7.61	EEE link partner ability	
0	SHARE X 3	16	Special Control Register (APS)	
0	PHY 08~31	18	Special Status Register	
X	SHARE X 3	20	Page Control Register	
4	SHARE X 3	16	WOL+ Control Register	
0	PHY 08~31	23	MDI/MDIX Control Register	

Share x 1: 24 ports share the register
Share x 3: Every 8 ports share the register
X24: Each port has its individual register
X: indicate do not care.

Table 35 Register Symbol Abbreviations

Type	Description
R	Read
W	Write
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High

6.1.1 MII Register

MII register 0 of PHY08~31 (Each PHY has its own MII register 0 with different PHY address)

PHY	MII	R/W	Description	Default
Control Register				
08~31	0.15	RW/ SC	Reset The PHY is reset if user writes “1” to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP829.	0
08~31	0.14	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, IP1829 will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN.	0
08~31	0.13	RW	Speed Selection 1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
08~31	0.12	RW	Auto-Negotiation(AN) Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
08~31	0.11	R/W	Power Down 1: power down mode 0: normal operation	0
08~31	0.10	-	Isolate IP1829 doesn’t support this function.	0
08~31	0.9	RW/ SC	Restart Auto-Negotiation 1 = re-starting Auto-Negotiation 0 = Auto-Negotiation re-start complete	0
08~31	0.8	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	1
08~31	0.7	R/W	Collision test	0
08~31	0.6	RO	Reserved	0
08~31	0.5	R/W	Unidirectional enable When bit 0.12 is one or bit 0.8 is zero or bit 0.13 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one and bit 0.13 is one： 1 = Enable transmit from MII regardless of whether the PHY has determined that a valid link has been established. 0 = Enable transmit from MII only when the PHY has determined that a valid link has been established.	0
08~31	0[4:0]	RO	Reserved	0

MII register 1 of PHY08~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	R/W	Description	Default
Status Register				
08~31	1.15	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable IP1829 does not support 100Base-T4. This bit is fixed to be 0.	0
08~31	1.14	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
08~31	1.13	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1
08~31	1.12	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
08~31	1.11	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
08~31	1.10	RO	100Base-T2 full duplex Capable 1 = 100Base-T2 full duplex capable 0 = not 100Base-T2 full duplex capable	0
08~31	1.9	RO	100Base-T2 half duplex Capable 1 = 100Base-T2 half duplex capable 0 = not 100Base-T2 half duplex capable	0
08~31	1.8	RO	Extended Status	0
08~31	1.7	RO	Unidirectional ability 1 = PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established. 0 = PHY able to transmit from MII only when the PHY has determined that a valid link has been established.	1
08~31	1.6	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
08~31	1.5	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0

MII register 1 of PHY08~31 (Each PHY has its own MII register 1 with different PHY address)

PHY	MII	R/W	Description	Default
Status Register				
08~31	1.4	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that IP1829 has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP1829 reset.	0
08~31	1.3	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that IP1829 has the ability to perform Auto-Negotiation.	1
08~31	1.2	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that IP1829 has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
08~31	1.1	RO LH	Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that IP1829 has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP1829 reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
08~31	1.0	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities IP1829 has extended register capabilities.	1

MII register 2 of PHY08~31 (24 PHYs share the MII register)

PHY	MII	R/W	Description	Default
PHY Identifier 1 Register				
08~31	2	RO	IP1829 OUI (Organizationally Unique Identifier) ID, the MSB is 3rd bit of IP829 OUI ID, and the LSB is 18th bit of IP1829 OUI ID. IP1829 OUI is 0090C3.	16'h0243

MII register 3 of PHY08~31 (24 PHYs share the MII register)

PHY	MII	R/W	Description	Default
PHY Identifier 2 Register				

MII register 3 of PHY08~31 (24 PHYs share the MII register)

PHY	MII	R/W	Description	Default
08~31	3[15:10]	RO	PHY identifier IP1829 OUI ID, the MSB is 19th bit of IP1829 OUI ID, and LSB is 24th bit of IP1829 OUI ID.	6'h03
08~31	3[9:4]	RO	Manufacture's Model Number IP1829 model number	6'h01
08~31	3[3:0]	RO	Revision Number IP1829 revision number	0

MII register 4 of PHY08~31 (Each PHY has its own MII register 4 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Advertisement Register				
08~31	4.15	R/W	1 = Next pages are supported 0 = Next pages are not supported	0
08~31	4.14	RO	Reserved by IEEE, write as 0, ignore on read	0
08~31	4.13	R/W	Remote Fault 1 = Advertises that this port has detected a remote fault. 0 = There is no remote fault.	0
08~31	4.12	RO	Reserved for future IEEE use, write as 0, ignore on read	0
08~31	4.11	RW	Asymmetric PAUSE 1 = Asymmetric flow control is supported 0 = Asymmetric flow control is not supported	1
08~31	4.10	RW	PAUSE 1 = Symmetric flow control is supported 0 = Symmetric flow control is not supported	1
08~31	4.9	RO	100BASE-T4 Not supported	0
08~31	4.8	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	1
08~31	4.7	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	1
08~31	4.6	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	1
08~31	4.5	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1
08~31	4[4:0]	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	5'b00001

MII register 5 of PHY08~31 (Each PHY has its own MII register 5 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Ability Register				
08~31	5.15	RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
08~31	5.14	RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
08~31	5.13	RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
08~31	5.12	RO	Reserved by IEEE for future use, write as 0, and read as 0.	0
08~31	5.11	RO	Asymmetric PAUSE 1 = Link partner support Asymmetric PAUSE 0 = Link partner does not support Asymmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4[11:10].	0
08~31	5.10	RO	PAUSE 1 = Link partner support Symmetric PAUSE 0 = Link partner does not support Symmetric PAUSE When local or link partner is Auto-negotiation disabled, this bit is read as 1. The pause resolution is determined by MII Reg4[11:10].	0
08~31	5.9	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
08~31	5.8	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
08~31	5.7	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX	0
08~31	5.6	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
08~31	5.5	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T	0
08~31	5[4:0]	RO	Selector Field Protocol selector of the link partner	5'b00000

MII register 6 of PHY08~31 (Each PHY has its own MII register 6 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Expansion Register				
08~31	6[15:5]	RO	Reserved	0
08~31	6.4	RO/ LH	Parallel Detection Fault 1 = a fault has been detected via parallel detection function. 0 = a fault has not been detected via parallel detection function.	0
08~31	6.3	RO	Link Partner Next Page Able 1 = Link partner is next page able. 0 = Link partner is not next page able. In 100FX or AN disabled, then this bit is always equal to 0.	0
08~31	6.2	RO	Next Page Able 1 = IP1829 next page able. 0 = IP1829 is not next page able.	1
08~31	6.1	RO/ LH	Page Received 1 = A new page has been received. 0 = A new page has not been received.	0
08~31	6.0	RO	If AN is enabled, this bit means: 1 = Link partner is Auto-Negotiation able. 0 = Link partner is not Auto-Negotiation able. In 100FX or AN disabled, then this bit is always equal to 0.	0

MII register 7 of PHY08~31 (Each PHY has its own MII register 7 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Next Page Transmit Register				
08~31	7.15	RW	Next Page Transmit Code Word Bit 15	0
08~31	7.14	RO	Reserved Transmit Code Word Bit 14	0
08~31	7.13	RW	Message Page Transmit Code Word Bit 13	1
08~31	7.12	RW	Acknowledge 2 Transmit Code Word Bit 12	0
08~31	7.11	RO	Toggle Transmit Code Word Bit 11	0
08~31	7[10:0]	RW	Message/Unformatted Field Transmit Code Word Bit 10:0	1

MII register 8 of PHY08~31 (Each PHY has its own MII register 8 with different PHY address)

PHY	MII	R/W	Description	Default
Auto-Negotiation Link Partner Next Page Register				
08~31	8.15	RO	Next Page Received Code Word Bit 15	0
08~31	8.14	RO	Acknowledge Received Code Word Bit 14	0
08~31	8.13	RO	Message Page Received Code Word Bit 13	0
08~31	8.12	RO	Acknowledge 2 Received Code Word Bit 12	0
08~31	8.11	RO	Toggle Received Code Word Bit 11	0
08~31	8[10:0]	RO	Message/Unformatted Field Received Code Word Bit 10:0	0

MII register 16 of PHY08~31 (Every 8 PHYs share the MII register)

PHY	MII	R/W	Description	Default
Special Control Register				
08~31	16.7	RW	Advance power saving mode 1 = Enable APS mode (Default) 0 = Disable APS mode Please refer to the Power Saving application note for more detail description.	1
08~31	16.4	RW	Far end fault function 1 = Far end fault function disable 0 = Far end fault function enable (Default) This bit is only used for fiber mode.	0

MII register 18 of PHY08~31 (Each PHY has its own MII register 18 with different PHY address)

PHY	MII	R/W	Description	Default
Special Status Register				
08~31	18.14	RO	Linkup 1 = linkup 0 = unlink	0
08~31	18.11	RO	Speed Mode 1 = 100 Mbps 0 = 10 Mbps	0
08~31	18.10	RO	Duplex Mode 1 = Full Duplex 0 = Half Duplex	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6.1.2 MMD Control Register

MII register 13 of PHY08~31 (Each PHY has its own MII register 13 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Control Register				
08~31	13[15:14]	R/W	Function 00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	0
08~31	13[13:5]	R/W	Reserved Write as 0, ignore on read	0
08~31	13[4:0]	R/W	DEVAD Device Address	0

MII register 14 of PHY08~31 (Each PHY has its own MII register 14 with different PHY address)

PHY	MII	R/W	Description	Default
MMD Access Address Data Register				
08~31	14[15:0]	R/W	Address Data If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	0

Example 1, Read 0.3.20 (Read Data from MMD register 3.20 of PHY address 0):

1. Write 0.13 = 0x0003 //MMD DEVAD 3
2. Write 0.14 = 0x0014 //MMD Address 20
3. Write 0.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 0.14 //Read MMD Data from 0.3.20

Example 2, Write 1.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 1):

1. Write 1.13 = 0x0007 //MMD DEVAD 7
2. Write 1.14 = 0x003C //MMD Address 60
3. Write 1.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 1.14 = 0x3210 //Write MMD Data 0x3210 to 1.7.60

6.1.3 MMD Data Register

MMD register 3.0 of PHY08~31 (Each PHY has its own MMD register 3.0 with different PHY address)

PHY	MII	R/W	Description	Default
PCS control 1 Register				
08~31	3.0[15:11]	RO	Reserved Ignore when read	0
08~31	3.0.10	R/W	Clock stop enable 1 = PHY may stop xMII Rx clock during LPI 0 = Clock not stoppable	0
08~31	3.0[9:0]	RO	Reserved Ignore when read	0

MMD register 3.1 of PHY08~31 (Each PHY has its own MMD register 3.1 with different PHY address)

PHY	MII	R/W	Description	Default
PCS status 1 Register				
08~31	3.1[15:12]	RO	Reserved Ignore when read	0
08~31	3.1.11	RO/LH	Tx LPI received 1 = Tx PCS has received LPI 0 = LPI not received	0
08~31	3.1.10	RO/LH	Rx LPI received 1 = Rx PCS has received LPI 0 = LPI not received	0
08~31	3.1.9	RO	Tx LPI indication 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
08~31	3.1.8	RO	Rx LPI indication 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
08~31	3.1.7	RO	Reserved Ignore on read	0
08~31	3.1.6	RO	Clock stop capable 1 = The MAC may stop the xMII Tx clock during LPI 0 = Clock not stoppable	0
08~31	3.1[5:0]	RO	Reserved Ignore when read	0

MMD register 3.20 of PHY08~31 (Each PHY has its own MMD register 3.20 with different PHY address)

PHY	MII	R/W	Description	Default
EEE capability Register				
08~31	3.20[15:7]	RO	Reserved Ignore when read	0

MMD register 3.20 of PHY08~31 (Each PHY has its own MMD register 3.20 with different PHY address)

PHY	MII	R/W	Description	Default
08~31	3.20.6	RO	10GBASE-KR EEE 1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	0
08~31	3.20.5	RO	10GBASE-KX4 EEE 1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	0
08~31	3.20.4	RO	1000BASE-KX EEE 1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	0
08~31	3.20.3	RO	10GBASE-T EEE 1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	0
08~31	3.20.2	RO	1000BASE-T EEE 1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	0
08~31	3.20.1	RO	100BASE-TX EEE 1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	1
08~31	3.20.0	RO	Reserved Ignore when read	0

MMD register 3.22 of PHY08~31 (Each PHY has its own MMD register 3.22 with different PHY address)

PHY	MII	R/W	Description	Default
EEE wake error count				
08~31	3.22[15:0]	RO	EEE wake error count Count wake time faults where IP1829 fails to complete its normal wake sequence within the time required for the specific PHY type. This register keeps the value before reading the contents of the register.	0x0000

MMD register 7.60 of PHY08~31 (Each PHY has its own MMD register 7.60 with different PHY address)

PHY	MII	R/W	Description	Default
EEE advertisement Register				
08~31	7.60[15:7]	RO	Reserved Ignore when read	0
08~31	7.60.6	RO	10GBASE-KR EEE 1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	0
08~31	7.60.5	RO	10GBASE-KX4 EEE 1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	0
08~31	7.60.4	RO	1000BASE-KX EEE 1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	0

MMD register 7.60 of PHY08~31 (Each PHY has its own MMD register 7.60 with different PHY address)

PHY	MII	R/W	Description	Default
08~31	7.60.3	RO	10GBASE-T EEE 1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	0
08~31	7.60.2	RO	1000BASE-T EEE 1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	0
08~31	7.60.1	R/W	100BASE-TX EEE 1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	1
08~31	7.60.0	RO	Reserved Ignore when read	0

MMD register 7.61 of PHY08~31 (Each PHY has its own MMD register 7.61 with different PHY address)

PHY	MII	R/W	Description	Default
EEE link partner ability				
08~31	7.61[15:7]	RO	Reserved Ignore when read	0
08~31	7.61.6	RO	10GBASE-KR EEE 1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	0
08~31	7.61.5	RO	10GBASE-KX4 EEE 1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for	0
08~31	7.61.4	RO	1000BASE-KX EEE 1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	0
08~31	7.61.3	RO	10GBASE-T EEE 1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	0
08~31	7.61.2	RO	1000BASE-T EEE 1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	0
08~31	7.61.1	RO	100BASE-TX EEE 1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	0
08~31	7.61.0	RO	Reserved Ignore when read	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6.1.4 Register Page mode Control Register

MII register 20 of PHY08~31 (Every 8 PHYs share the MII register)

PHY	MII	R/W	Description	Default
Page Control Register				
08~31	20[4:0]	RW	Reg16~31_Page_Sel[4:0]	00000

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce unexpected function to write these registers.

6.1.5 WOL+ Control Register

MII page4 register16 of PHY08~31 (Every 8 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ Control Register				
4	16.[15]	RW	WOL+ Interrupt Enable Set high to enable WOL+ interrupt 1=Enable 0=Disable Each PHY address can access the register of the corresponding port.	0
	16.[14]	RW	WOL+ Level Trigger This bit is used to select the output mode of WOL+ interrupt. 1=Level trigger (Low goes high or high goes low when WOL+ interrupt) 0=Edge trigger (Positive pulse or negative pulse when WOL+ interrupt)	1
	16.[13]	RW	WOL+ Positive Trigger This bit is used to select the polarity of WOL+ interrupt. 1=Low goes high or positive pulse 0=High goes low or negative pulse	0
	16.[12]	RW	Sense Link Change Set high to enable WOL+ interrupt when link change is sensing. 1=Enable 0=Disable	1
	16.[11]	RW	Sense Magic Packet Set high to enable WOL+ interrupt when magic packet is receiving. 1=Enable 0=Disable	1
	16.[10]	RW	Sense Any Packet Set high to enable WOL+ interrupt when any packet is receiving. 1=Enable 0=Disable	1
	16.[9]	RW	Sense DUT Set high to enable WOL+ interrupt when DUT is sensing WOL+ event. 1=Enable 0=Disable Each PHY address can access the register of the corresponding port.	1
	16.[8]	RW	WOL+ Down Speed Enable Set high to enable WOL+ down speed function 1=Enable 0=Disable	1
	16.[7:1]	RO	Reserved	0x00

MII page4 register16 of PHY08~31 (Every 8 PHYs share the MII register)

page	MII	R/W	Description	Default
	16.[0]	RO	PHY WOL+ Interrupt Status The status of PHY WOL+ interrupt is based on the setting of Reg16 Page4 Bit14 and Bit13. Each PHY address can access the register of the corresponding port.	1

MII page5 register16 of PHY08~31 (Every 8 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 0				
5	16[15:0]	R/W	WOL+ MAC Address 0 (the most significant word) WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

MII page5 register16 of PHY08~31 (Every 8 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 1				
5	16[15:0]	R/W	WOL+ MAC Address 1 WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

MII page5 register16 of PHY08~31 (Every 8 PHYs share the MII register)

page	MII	R/W	Description	Default
PHY WOL+ MAC Address Register 2				
5	16[15:0]	R/W	WOL+ MAC Address 2 (the least significant word) WOL+ MAC Address = {WOL+_MAC_Address_0, WOL+_MAC_Address_1, WOL+_MAC_Address_2}	0x0000

Above three definitions are in the same register. Continuously write/read this register 3 times to set/obtain WOL Magic packet MAC address.

The first write/read：WOL+ MAC Address 0.
The second write/read：WOL+ MAC Address 1.
The third write/read：WOL+ MAC Address 2.

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Example 1, Read page3 register16 (Read Data from page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Read 0.16 //Read Data from page3 register16
3. Write 0.20 = 0x0000 //restore to page0

Example 2, Write page3 register16 = 0x3400 (Write Data 0x3400 to page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Write 0.16 = 0x3400 //Write Data 0x3400 to page3 register16
3. Write 0.20 = 0x0000 //restore to page0

6.1.6 MDI/MDIX Control Register

Table 37 MDI/MDIX Control Register

MII register 23 of PHY08~31 (Each PHY has its own MII register 23 with different PHY address)

PHY	MII	R/W	Description	Default
08~31	23[1]	RW	Auto_MDIX 1 : Enable auto crossover function 0 : Disable auto crossover function	1
08~31	23[0]	RW	MDI/MDIX channel selection 1 : Select MDIX channel 0 : Select MDI channel	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

6.2 Switch Register

6.2.1 Switch Page Map

Page	Description
0x00	MAC control registers
0x01	ARL registers 1
0x02	ARL registers 2
0x03	SMI registers
0x04	OAM control registers
0x05	Reserved
0x06	RxDMA registers
0x07	TxDMA registers
0x08	Output Queue registers
0x09	PTP registers
0x0A	IRMP registers
0x0B	Advanced EEPROM code registers
0x0C	Misc/System registers
0x0D	Reserved page

6.2.2 Switch Register Map

Type	Description
R	Read
W	Write
R/W	Read/Write
SC	Self-Clearing
RO	Read Only
LL	Latching Low
LH	Latching High

6.3 MAC Control Register

Table 38 MAC Control Register

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x00	Switch ID/version register Bit[3:0] : IP1829 IC version Bit[15:4] : IP1829 ID	RO	0x8290
0x01	General MAC operation behavior register 1 Bit[1:0] : Enable IPG compensation 00 : Disable 01 : compensation 160 ppm 10 : compensation 80 ppm 11 : compensation 40 ppm (default) Bit[2] : Back pressure method 0 : Carrier Sense base 1 : Collision base Bit[3] : Collision 16 times drop enable Bit[4] : Collision back off enable bit[5] : Auto turn off flow control function if priority queue enable bit[6] : In-band management (Destination MAC address = switch MAC address) 1: to CPU port 0: Drop (switch MAC address define in offset address x5C,0x5D,0x5E) bit[7] : Disable Tx packet CRC recalculation bit[8] : Bypass Rx packets CRC error bit[9] : Enable for MIBs counters bit[10:13] : Reserved bit[10] : Reserved bit[11] : Reserved bit[12] : P27 interface select 0 : GMII 1 : RGMII bit[13] : P28 interface select 0 : GMII 1 : RGMII bit[14] : P29 interface select 1 : RGMII 0 : GMII (default) (This bit value base on pin **N4**)	R/W	0x0C17
0x02	Jumbo Packets enable for port 16 ~ 1, 1 bit per port bit[15:0] : enable jumbo 0 : Disable 1 : Enable	R/W	0x0000
0x03	Jumbo Packets enable for port 29 ~ 17, 1 bit per port bit[12:0] : enable jumbo 0 : Disable 1 : Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x04	MAC LoopBack enable (GMII/MII TX to RX) for port 16 ~ 1 bit[15:0] : LoopBack enable 0 : Disable 1 : Enable	R/W	0x0000
0x05	MAC LoopBack enable (GMII/MII TX to RX) for port 29 ~ 17 bit[12:0] : LoopBack enable 0 : Disable 1 : Enable	R/W	0x0000
0x06	Ethernet L2 protocol frames capture (if 0x33 bit[8] is 1'b1, the BPDU capture should follow the 0x30 ~ 0x33 setting) bit[1:0] : for BPDU (01-80-C2-00-00-00) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[3:2] : for Slow Protocol (01-80-C2-00-00-02) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[5:4] : for 802.1X (01-80-C2-00-00-03) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[7:6] : for LLDP (01-80-C2-00-00-0E) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[9:8] : for Group 0 (01-80-C2-00-00-04 ~ 0D, 0F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[11:10] : for All Bridge address (01-80-C2-00-00-10) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[13:12] : for Group 1 (01-80-C2-00-00-11 ~ 1F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[15:14] : for GARP (01-80-C2-00-00-20, 21) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop	R/W	0x030C
0x07	Ethernet L2 protocol frames capture bit[1:0] : for Group 2 (01-80-C2-00-00-22 ~ 2F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[3:2] : for Group 3 (01-80-C2-00-00-30 ~ 3F) 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop bit[4] : CPU does not act for drop setting for reserved group address as defined above. 0 : enable drop setting 1 : Disable drop setting bit[5] : MPCP protocol enable 0 : drop 1 : Send to CPU port only bit[6] : MPCP drop disable when MPCP protocol is not enable	R/W	0x0040

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	0 : drop 1 : Don't drop bit[7] : ARP 0: Forward depend on DA 1: To DA and CPU bit[8] : PPPoE protocol check enable 0 : Don't check PPPoE type 1 : Check PPPoE type bit[9] : PPPoE header remove 0 : Don't remove 1 : Remove bit[10] : IPv6 0 : Forward depend on DA 1 : To CPU port bit[11] : Pass Pause frame with DA not belong to Switch Address and 01-80-C2-00-00-01 0 : drop 1 : pass bit[12] : set (BPDU, 802.1x, Slow protocol, MPCP, LLDP, GxRP) Packets to highest priority if the corresponding protocol enable. 0 : Disable 1 : Enable bit[13] : Capture CFM packet to CPU 0 : Disable 1 : Enable bit[14] : Capture User define Ether Type (define in 0x23) 0 : Disable 1 : to DA and CPU Bit[15] : Check if OAM frame DA equals to 0x01_80_C2_00_00_02 0 : can be unicast 1 : DA must be 0x01_80_C2_00_00_02		
0x08	Ethernet L3 protocol packet capture bit[1:0] : ICMP bit[3:2] : TCP bit[5:4] : UDP bit[7:6] : OSPF bit[9:8] : USR1 (0x09 low byte) bit[11:10] : USR2 (0x09 high byte) bit[13:12] : Ipv4 Other protocol, 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x0000
0x09	User define IP protocol field bit[7:0] : IP protocol USR1 bit[15:8] : IP protocol USR2	R/W	0x0000
0x0A	User define TCP/UDP port number A	R/W	0x0000
0x0B	User define TCP/UDP port number B	R/W	0x0000
0x0C	User define TCP/UDP port number C upper range setting	R/W	0x0000
0x0D	User define TCP/UDP port number C lower range setting IP1829 will check if the port number C is in the following range lower range <= port number C <= upper range	R/W	0x0000
0x0E	User define TCP/UDP port number D upper range setting	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x0F	User define TCP/UDP port number D lower range setting IP1829 will check if the port number D is in the following range lower range <= port number D <= upper range	R/W	0x0000
0x10	User define TCP/UDP port number E upper range setting	R/W	0x0000
0x11	User define TCP/UDP port number E lower range setting IP1829 will check if the port number E is in the following range lower range <= port number E <= upper range	R/W	0x0000
0x12	TCP/UDP port number based priority setting: bit[3:0]: FTP (20,21) bit[7:4]: SSH (22) bit[11:8]: TELNET (23) bit[15:12]: SMTP (25) 0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x13	TCP/UDP port number based priority setting: bit[3:0]: DNS (53) bit[7:4]: BOOTP/DHCP (67, 68) bit[11:8]: TFTP (69) bit[15:12]: HTTP_0,1 (80) 0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x14	TCP/UDP port number based priority setting: bit[3:0]: POP3 (110) bit[7:4]: NEWS (119) bit[11:8]: SNTP 123) bit[15:12]: NETBIOS0,1,2 (137 ~ 139) 0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x15	TCP/UDP port number based priority setting: bit[3:0]: IMAP_0,1 (143,220) bit[7:4]: SNMP_0,1 (161,162) bit[11:8]: HTTPS (443) bit[15:12]: USR define A 0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x16	TCP/UDP port number based priority setting: bit[3:0]: USR define B bit[7:4]: USR define C bit[11:8]: USR define D bit[15:12]: USR define E 0000 to queue 0(Disable) 0001 ~ 0111: to queue 1 ~ queue 7 1001: to CPU only 1011 : to CPU and ports 1010: drop	R/W	0x0000
0x17	TCP/UDP port number based filter to WAN port select: bit[0]: FTP 0: Don't care 1: select bit[1]: SSH 0: Don't care 1: select bit[2]: TELNET 0: Don't care 1: select bit[3]: SMTP 0: Don't care 1: select bit[4]: DNS 0: Don't care 1: select bit[5]: BOOP/DHCP 0: Don't care 1: select bit[6]: TFTP 0: Don't care 1: select	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[7]: HTTP_0,1 0: Don't care 1: select bit[8]: POP3 0: Don't care 1: select bit[9]: NEWS 0: Don't care 1: select bit[10]: SNTP 0: Don't care 1: select bit[11]: NETBIOS0,1,2 0: Don't care 1: select bit[12]: IMAP_0,1 0: Don't care 1: select bit[13]: SNMP_0,1, 0: Don't care 1: select bit[14]: HTTPS 0: Don't care 1: select bit[15]: USR define A 0: Don't care 1: select (corresponding to offset address 0x0E, 0x12)		
0x18	TCP/UDP port number based filter to WAN port select: bit[0]: USR define B 0: Don't care 1: select bit[1]: USR define C 0: Don't care 1: select bit[2]: USR define D 0: Don't care 1: select bit[3]: USR define E 0: Don't care 1: select (corresponding to offset address 0x0E ~ 0x12) bit[4]: filter_md (0: negative list 1: positive list) 0 : negative list, the setting "1"s above which routed to wan will be filtered 1 : positive list, the setting "1"s above which routed to wan port can be passed, otherwise be filtered (bit[4] : Detail ref to offset address **0x0D~0x10** (page6))	R/W	0x0000
0x19	TCP/UDP Port Number function enable for port 16 ~ 1, 1 bit per port bit[15:0] : function enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x1A	TCP/UDP Port Number function enable for port 29 ~ 17, 1 bit per port bit[12:0] : function enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x1B	TCP/UDP Port Number priority enable for port 16 ~ 1,1 bit per port bit[15:0] : priority enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x1C	TCP/UDP Port Number priority enable for port 29 ~ 17, 1-bit /port bit[12:0] : priority enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x1D	TCP/UDP Port Number check for "TCP protocol" enable bit[15:0] : enable the TCP/UDP Port Number Function for "TCP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x17	R/W	0xFFFF
0x1E	TCP/UDP Port Number check for "TCP protocol" enable bit[3:0] : enable the TCP/UDP Port Number Function for "TCP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x18	R/W	0xF
0x1F	TCP/UDP Port Number check for "UDP protocol" enable bit[15:0] : enable the TCP/UDP Port Number Function for "UDP protocol" 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x17	R/W	0xFFFF

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x20	TCP/UDP Port Number check for “UDP protocol” enable bit[3:0] : enable the TCP/UDP Port Number Function for “UDP protocol” 0 : Disable 1 : Enable The Port Number Mapping is the same as define in 0x18	R/W	0xF
0x21	In-band management restriction configuration 1 When the register 0x01 bit[6] and 0x22 bit[15] are both 1’b1, the in-band Management packets will forward as the register 0x21 and 0x22 settings. bit[0] : ARP bit[1] : Ipv4 bit[2] : IPv6 bit[3] : PPPoE bit[4] : ICMP bit[5] : TCP bit[6] : UDP bit[7] : User define Ether Type bit[8] : User define IP Protocol 1 bit[9] : User define IP Protocol 2 bit[10] : ICMPv6 bit[11] : FTP bit[12] : SSH bit[13] : Telnet bit[14] : SMTP bit[15] : DNS 0 : drop 1 : forward to CPU	R/W	0x0000
0x22	In-band management restriction configuration 2 bit[0] : BOOTP/DHCP bit[1] : TFTP bit[2] : HTTP bit[3] : POP3 bit[4] : NEWS bit[5] : SNTP bit[6] : NETBIOS bit[7] : IMAP bit[8] : SNMP bit[9] : HTTPS bit[10] : user define TCP/UDP Port Number A bit[11] : user define TCP/UDP Port Number B bit[12] : user define TCP/UDP Port Number C bit[13] : user define TCP/UDP Port Number D bit[14] : user define TCP/UDP Port Number E 0 : drop 1 : forward to CPU bit[15] : in-band management restriction enable (0x01 bit[6] need to be 1’b1) 0 : Disable 1 : Enable	R/W	0x0000
0x23	User define Ether Type bit[15:0] : user define Ether Type Value	R/W	0x0000
0x24 ~ 0x2F	Reserved		
0x30	BPDU per Port Capture configuration for Port 8 ~ port 1 bit[1:0] : Port 1 BPDU setting	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[3:2] : Port 2 BPDU setting bit[5:4] : Port 3 BPDU setting bit[7:6] : Port 4 BPDU setting bit[9:8] : Port 5 BPDU setting bit[11:10] : Port 6 BPDU setting bit[13:12] : Port 7 BPDU setting bit[15:14] : Port 8 BPDU setting 00 : Forward 01 : Reserved 10 : to CPU 11 : Drop		
0x31	BPDU per Port Capture configuration for Port 16 ~ port 9	R/W	0x0000
0x32	BPDU per Port Capture configuration for Port 24 ~ port 17	R/W	0x0000
0x33	BPDU per Port Capture configuration for Port 28 ~ port 25 bit[7:0] : BPDU setting for Port 28 ~ Port 25 Bit[8] : BPDU per Port setting enable	R/W	0x0000
0x34 ~ 0x39	Reserved		
0x3A	Port base priority enable for port5~port1, 3 bit per port bit[2:0] : port base priority setting for port 1 000 – to queue 0 (lowest priority) 001 – to queue 1 … 111 – to queue 7 (highest priority) bit[5:3] : port 2 bit[8:6] : port 3 bit[11:9] : port 4 bit[14:12] : port 5	R/W	0x0000
0x3B	Port base priority enable for port10~port6, 3 bit per port	R/W	0x0000
0x3C	Port base priority enable for port15~port11, 3 bit per port	R/W	0x0000
0x3D	Port base priority enable for port20~port16, 3 bit per port	R/W	0x0000
0x3E	Port base priority enable for port25~port21, 3 bit per port	R/W	0x0000
0x3F	Port base priority enable for port29~port26, 3 bit per port	R/W	0x0000
0x40	Tag base priority settings bit[15:0] : enable 802.1Q tag priority for port16~port1, 1 bit per port	R/W	0x0000
0x41	Tag base priority settings bit[12:0] : enable 802.1Q tag priority for port29~port17, 1 bit per port bit[13] : enable special tag priority for CPU Port (Port 29) bit[14] : 802.1Q tag priority Edition select 0 : 2005 Edition 1 : earlier Edition bit[15] : exchange the priority of 3'b000 and 3'b001 for 2005 Edition	R/W	0x0000
0x42	IP CoS base priority enable for port16~port1, 1 bit per port	R/W	0x0000
0x43	IP CoS base priority enable for port29~port17, 1 bit per port	R/W	0x0000
0x44	Differentiated Services (DS) priority setting bit [2:0]: priority setting for DSCP 0 bit [5:3]: priority setting for DSCP 1 bit [8:6]: priority setting for DSCP 2 bit [11:9]: priority setting for DSCP 3	R/W	0x7FFF

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit [14:12]: priority setting for DSCP 4		
0x45	Differentiated Services (DS) priority setting bit [2:0]: priority setting for DSCP 5 bit [5:3]: priority setting for DSCP 6 bit [8:7]: priority setting for DSCP 7 bit[9] : priority for DSCP not match 0 : regard as low priority (priority 0) 1 : ignore IP priority (priority will according to tag/port)	R/W	0x03FF
0x46	DSCP configuration for DSCP_0 and DSCP_1 bit [5:0]: DSCP 0 configuration bit [11:6]: DSCP 1 configuration	R/W	0x0280
0x47	DSCP configuration for DSCP_2 and DSCP_3 bit [5:0]: DSCP 2 configuration bit [11:6]: DSCP 3 configuration	R/W	0x0692
0x48	DSCP configuration for DSCP_4 and DSCP_5 bit [5:0]: DSCP 4 configuration bit [11:6]: DSCP 5 configuration	R/W	0x0BA2
0x49	DSCP configuration for DSCP_6 and DSCP_7 bit [5:0]: DSCP 6 configuration bit [11:6]: DSCP 7 configuration	R/W	0x0E30
0x4A	Source MAC address based priority setting bit[15:0] : SMAC priority enable for port 16 ~ port 1	R/W	0x0000
0x4B	Source MAC address based priority setting bit[12:0] : SMAC priority enable for port 29 ~ port 17	R/W	0x0000
0x4C	VID based priority enable setting bit[15:0] : VID priority enable for port 16 ~ port 1	R/W	0x0000
0x4D	VID based priority enable setting bit[12:0] : VID priority enable for port 29 ~ port 17	R/W	0x0000
0x4E	IP based priority setting bit[15:0] : IP priority enable for port 16 ~ port 1 (ref Page 0x02, reg 0x01, 0x02)	R/W	0x0000
0x4F	IP based priority setting bit[12:0] : IP priority enable for port 29 ~ port 17 (ref Page 0x02, reg 0x01, 0x02)	R/W	0x0000
0x50	IGMP Multicast Group based priority enable setting bit[15:0] : IGMP Multicast Group priority enable for port 16 ~ port 1	R/W	0x0000
0x51	IGMP Multicast Group based priority enable setting bit[12:0] : IGMP Multicast Group priority enable for port 29 ~ port 17	R/W	0x0000
0x52	ACL based priority enable setting bit[15:0] : ACL priority enable for port 16 ~ port 1	R/W	0x0000
0x53	ACL based priority enable setting bit[12:0] : ACL priority enable for port 29 ~ port 17	R/W	0x0000
0x54	802.1x Port Lock Enable (port 16 ~ port 1) bit[15:0]: 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x55	802.1x Port Lock Enable (port 28 ~ port 17) bit[11:0]: 0 : normal operation 1 : drop all frames except ARP & 802.1x EAPOL packet	R/W	0x0000
0x56	PPPoE session ID A	R/W	0x0000
0x57	PPPoE session ID B	R/W	0x0000
0x58	PPPoE session ID C	R/W	0x0000
0x59	PPPoE session ID D	R/W	0x0000
0x5A	MAC reset for port16~port1, 1 bit per port bit[15:0] : 0: reset 1: normal	R/W	0xFFFF
0x5B	MAC reset for port29~port17, 1 bit per port bit[12:0] : 0: reset 1: normal	R/W	0x1FFF
0x5C	Switch's MAC address[15:0]	R/W	0x0003
0x5D	Switch's MAC address[31:16]	R/W	0xC300
0x5E	Switch's MAC address[47:32]	R/W	0x0090
0x5F	Configuration for Low Power Idle bit[4:0] : threshold of IDLE period for entering LPI bit[7:5] : the interval selection for IDLE counter 0 ~ 7 – 1us/10us/100us/ 1ms/ 10ms/ 100ms/ 1s/ 10s bit[8] : Switch enter PSS when IDLE period hit the threshold 0 : Disable 1 : Enable bit[9] : use default Tw as the resolved Tw 0 : Disable 1 : Enable bit[10] : use LinkPartner's Tw as the resolved Tw (note : bit[9] has higher priority than this bit) 0 : Disable 1 : Enable bit[11] : reserved bit[12] : select the large one between default Tw and Link Partner's Tw as the resolved Tw 0 : Disable 1 : Enable bit[13] : force to enable PSS support 0 : Disable 1 : Enable bit[14] : pre_idle period disable 0 : Enable pre_idle period 1 : Disable pre_idle period	R/W	0x0000
0x60	Configuration of the LPI State for Port 16 ~ Port 1, per port 1 bit bit[15:0] : LPI state for each port 0 : normal state 1 : in Power Saving State	R/W	0x0000
0x61	Configuration of the LPI State for Port 29 ~ Port 17, per port 1 bit bit[12:0] : LPI state for each port 0 : normal state 1 : in Power Saving State	R/W	0x0000
0x62	Configuration for LPI default Tw bit[15:0] : default Tw setting in us	R/W	0x0023
0x63	Configuration for EEE bit[7:0] : the sub type of the EEE bit[11:8] : the position of the receive Tw in the EEE header	R/W	0x0305

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x64	CPU Read statistic counter command bit[4:0]: statistic counter read address (R : ~0x17, T : ~0x13) bit[9:5]: statistic counter Port select (Port 1 ~ Port 29 : 0 ~ 28) bit[10] : statistic counter RX/TX selection 0 : RX 1 : TX bit[11] : statistic counter sequential read enable 0 : Disable 1 : Enable bit[12] : reserved bit[14] : statistic counter read clear enable 0 : Disable 1 : Enable bit[15] : statistic counter command trig/Ack	R/W	0x0000
0x65	CPU Read low 16 bits statistic counter data	R/W	0x0000
0x66	CPU Read high 16 bits statistic counter data	R/W	0x0000
0x67	MAC self test packets control setting bit[15:0] : send self test packet for Port 16 ~ Port 1, per port 1 bit 0 : do not send 1 : send	R/W	0x0000
0x68	MAC self test packets control setting bit[12:0] : send self test packet for Port 29 ~ Port 17, per port 1 bit 0 : do not send 1 : send bit[14:13] : setting for self test packets number 00 : 32768 01 : 4096 10 : 256 11 : 16	R/W	0x4000
0x69	MAC self test result bit[15:0] : self test result for Port 16 ~ Port 1, per port 1 bit 0 : fail 1 : pass	RO	0x0000
0x6A	MAC self test result bit[12:0] : self test result for Port 29 ~ Port 17, per port 1 bit 0 : fail 1 : pass	RO	0x0000
0x6B	LoopDetect config register bit[15:0] : loop detect enable for Port 16 ~ Port 1, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0x6C	LoopDetect config register bit[12:0] : loop detect enable for Port 29 ~ Port 17, per port 1 bit 0 : Disable 1 : Enable bit[13] : loop detect time unit select 0 : 500ms 1 : 10s bit[14] : setting LoopDetect SA[40] value bit[15] : setting for LoopDetect re-random 0 : Disable 1 : Enable PS. To block loop port, Page 0x01, register 0x24 bit[3] need to be 1'b1	R/W	0x0000
0x6D	LoopDetect timer bit [7:0] : LPD packet sending timer, the time interval is timer x time unit bit[15:8] : Block release timer, the time interval is timer x time unit	R/W	0x0000
0x6E	LoopDetect frame DA[15:0] setting bit[15:0] : setting for LPD frame DA[15:0]	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x6F	LoopDetect frame DA[31:16] setting bit[15:0] : setting for LPD frame DA[31:16]	R/W	0xC300
0x70	LoopDetect frame DA[47:32] setting bit[15:0] : setting for LPD frame DA[47:32]	R/W	0x0190
0x71	LoopDetect frame EtherType setting bit[15:0] : setting for LPD frame EtherType	R/W	0x8931
0x72	LoopDetect frame sub type setting bit[15:0] : setting for LPD frame sub type	R/W	0xFFFF
0x73	LoopDetect frame Device ID setting bit[7:0] : setting for LPD frame device ID	R/W	0x0005
0x74	TCP flag global configuration bit[0] : Drop null flag 0 : Disable 1 : Enable bit[1] : Drop ALL-Set flag 0 : Disable 1 : Enable bit[3:2] : Period selection for Flag storm control counter 00 : 1000 / 100 / 10 Mbps -> 200us / 2ms / 20ms 01 : 1000 / 100 / 10 Mbps -> 1ms / 10ms / 100ms 10 : 1000 / 100 / 10 Mbps -> 10ms / 10ms / 10ms 11 : 1000 / 100 / 10 Mbps -> 100ms / 100ms / 100ms	R/W	0x0000
0x75	TCP flag 0 configuration bit[7:0] : The TCP flag 0 configuration bit[10:8] : Priority setting for TCP flag 0 bit[11] : Priority setting enable for TCP flag 0 0 : Disable 1 Enable bit[13:12] : action for TCP flag 0 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : packet length checking for TCP flag 0 Priority setting 0 : Don't check packet length 1 : only packet length less than 128 bytes will be enable for the priority setting	R/W	0x0000
0x76	TCP flag 1 configuration bit[7:0] : The TCP flag 1 configuration bit[10:8] : Priority setting for TCP flag 1 bit[11] : Priority setting enable for TCP flag 1 0 : Disable 1 Enable bit[13:12] : action for TCP flag 1 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : packet length checking for TCP flag 1 Priority setting 0 : Don't check packet length 1 : only packet length less than 128 bytes will be enable for the priority setting	R/W	0x0000
0x77	TCP flag 2 configuration bit[7:0] : The TCP flag 2 configuration bit[10:8] : Priority setting for TCP flag 2 bit[11] : Priority setting enable for TCP flag 2 0 : Disable 1 Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[13:12] : action for TCP flag 2 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : packet length checking for TCP flag 2 Priority setting 0 : Don't check packet length 1 : Only packet length less than 128 bytes will be enable for the priority setting		
0x78	TCP flag 3 configuration bit[7:0] : The TCP flag 3 configuration bit[10:8] : Priority setting for TCP flag 3 bit[11] : Priority setting enable for TCP flag 3 0 : Disable 1 Enable bit[13:12] : action for TCP flag 3 00 : none 01 : storm control 10 : to CPU only 11 : drop bit[14] : packet length checking for TCP flag 3 Priority setting 0 : Don't check packet length 1 : only packet length less than 128 bytes will be enable for the priority setting	R/W	0x0000
0x79	TCP flag0 and flag1 storm control threshold setting bit[7:0] : threshold setting for TCP flag 0 bit[15:8] : threshold setting for TCP flag 1	R/W	0x0000
0x7A	TCP flag2 and flag3 storm control threshold setting bit[7:0] : threshold setting for TCP flag 2 bit[15:8] : threshold setting for TCP flag 3	R/W	0x0000
0x7B	TCP flag 0 related function enable for Port 16 ~ Port 1 bit[15:0] : enable for TCP flag 0 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7C	TCP flag 0 related function enable for Port 29 ~ Port 17 bit[12:0] : enable for TCP flag 0 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7D	TCP flag 1 related function enable for Port 16 ~ Port 1 bit[15:0] : enable for TCP flag 1 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7E	TCP flag 1 related function enable for Port 29 ~ Port 17 bit[12:0] : enable for TCP flag 1 related function 0 : Disable 1 : Enable	R/W	0x0000
0x7F	TCP flag 2 related function enable for Port 16 ~ Port 1 bit[15:0] : enable for TCP flag 2 related function 0 : Disable 1 : Enable	R/W	0x0000
0x80	TCP flag 2 related function enable for Port 29 ~ Port 17 bit[12:0] : enable for TCP flag 2 related function 0 : Disable 1 : Enable	R/W	0x0000
0x81	TCP flag 3 related function enable for Port 16 ~ Port 1 bit[15:0] : enable for TCP flag 3 related function 0 : Disable 1 : Enable	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x82	TCP flag 3 related function enable for Port 29 ~ Port 17 bit[12:0] : enable for TCP flag 3 related function 0 : Disable 1 : Enable	R/W	0x0000
0x83	EoC configuration 1 bit[15:0] : EoC function enable for Port 16 ~ Port 1	R/W	0x0000
0x84	EoC configuration 2 bit[12:0] : EoC function enable for Port 29 ~ Port 17 bit[13] : Clear EoC block when receive a good packet bit[14]: EoC release time selection 0 : 1 Minute 1 : 10 Minutes bit[15] : Force to clear all EoC block (this bit will be self clear) PS. To block loop port, Page 0x01, register 0x24 bit[3] need to be 1'b1	R/W	0x0000
0x85	EoC block status for Port 16 ~ Port 1 Bit[15:0] : block status check for Port 16 ~ Port 1 0 : normal 1 : loop detected	RO	0x0000
0x86	EoC block status for Port 29 ~ Port 17 Bit[12:0] : block status check for Port 29 ~ Port 17 0 : normal 1 : loop detected	RO	0x0000
0x87	Ingress Rate control for port 1 bit[13:0] : Input Rate control The bandwidth = Rate control configure value x 64k bps	R/W	0x0000
0x88 ~ 0xA3	Ingress Rate control for port 2 ~ port 29 bit[13:0] : Input Rate control	R/W	0x0000
0xA4	Configuration for PTP bit[0] : PTP protocol enable (packets will to CPU only) bit[1] : PTP config for DA = 01-1B-19-00-00-00 0 : Enable 1 : not regard as PTP bit[2] : PTP config for DA = 01-80-C2-00-00-0E 0 : Enable 1 : not regard as PTP bit[3] : PTP config for UDP Destination Port 0 : Enable 1 : not check for PTP bit[4] : PTP config for UDP Source Port 0 : Enable 1 : not check as PTP bit[5] : Disable PTP packet send to CPU only 0 : to CPU only 1 : forward as DA specific bit[6] : Also check NTP packet 0 : Disable 1 : Enable bit[7] : PTP packets regard as high priority 0 : Disable 1 : Enable bit[8] : Allow PTP packets with unicast DA 0 : Disable 1 : Enable Bit[9] : Check if Destination IP equal to 224.0.1.129 or 224.0.0.107 (if enable, the UDP port number must also match) 0 : Disable 1 : Enable	R/W	0x0000
0xA5	LoopDetect Port 16 ~ Port 1 status	R	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[15:0] : port status for Port 16 ~ Port 1 0 : normal 1 : loop detected		
0xA6	LoopDetect Port 29 ~ Port 17 status bit[12:0] : port status for Port 29 ~ Port 17 0 : normal 1 : loop detected	R	0x0000
0xA7	IPv6 related functions configuration bit[0] : Enable TCP/UDP Port Number related functions for IPv6 0 : Disable 1 : Enable bit[1] : Enable TCP/UDP flag related functions for IPv6 (bit[0] need 1'b1) 0 : Disable 1 : Enable bit[2]: Reserved, should be 1'b0. Bit[3] : stop finding next header at Auth header bit[4] : stop finding next header at Encapsulation header bit[5] : stop finding next header at Fragment header bit[6] : stop finding next header at user define next header 1 bit[7] : stop finding next header at user define next header 2 0 : Enable 1 : Disable Bit[8] : forwarding action "Send to CPU and ports" has higher priority than "Drop" 0 : Disable 1 : Enable Bit[9] : forwarding action "Send to CPU only" has higher priority than "Drop" 0 : Disable 1 : Enable	R/W	0x0003
0xA8	IPv6 related header forwarding bit[1:0] : Fragment header bit[3:2] : Encapsulation header bit[5:4] : Authentication header bit[7:6] : ICMPv6 header bit[9:8] : ICMPv6 MLD bit[11:10] : ICMPv6 NDP bit[13:12] : user define next header 1 bit[15:14] : user define next header 2 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x00
0xA9	IPv6 related header forwarding bit[1:0] : ICMPv6 user define type 1 bit[3:2] : ICMPv6 user define type 2 00 : Send to ports only 01 : Send to CPU and ports 10 : Send to CPU only 11 : Drop	R/W	0x0000
0xAA	IPv6 user define next header configuration bit[7:0] : user define next header 1 bit[15:8] : user define next header 2	R/W	0x0000

MAC Control Registers : Page 0x00			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0xAB	ICMPv6 user define type 1 setting bit[7:0] : lower range setting bit[15:8] : upper range setting	R/W	0x0000
0xAC	ICMPv6 user define type 2 setting bit[7:0] : lower range setting bit[15:8] : upper range setting	R/W	0x0000
0xAD	WOL+ Enable for TX enter saving mode bit[15:0] : WOL+ Enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0xAE	WOL+ enable for TX enter saving mode bit[12:0] : WOL+ enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0xAF	WOL+ configuration bit[4:0] : threshold of idle period for entering WOL+ saving mode (if giga port is enable for this function, the threshold should be greater than 30s) bit[6:5] : the interval selection for WOL+ idle counter 00 : Disable 01 : 10 s 10 : 1min 11 : 10 min bit[7] : if TX any packet, leave WOL+ mode or not 0 : leave 1 : Don't care bit[8] : if RX any packet, leave WOL+ mode or not 0 : leave 1 : Don't care bit[9] : WOL+ mode select 0 : slave 1 : master bit[10] : leave WOL+ mode if match ACL action : also to CPU 0 : Disable 1 : Enable bit[11] : Enable Interrupt to CPU 0 : Disable 1 : Enable	R/W	0x0000
0xB0	WOL+ mode control for Port 16 ~ Port 1 bit[15:0] : WOL+ active for Port 16 ~ Port 1 0 : normal 1 : enter WOL+ mode	R/W	0x0000
0xB1	WOL+ mode control for Port 29 ~ Port 17 bit[12:0] : WOL+ active for Port 29 ~ Port 17 0 : normal 1 : enter WOL+ mode	R/W	0x0000
0xB2	WOL+ event for Port 16 ~ Port 1 bit[15:0] : Indicate the port had entered WOL+ mode, read clear 0 : normal 1 : had entered WOL+ mode	RO	0x0000
0xB3	WOL+ event for Port 29 ~ Port 17 bit[12:10] : Indicate the port had entered WOL+ mode, read clear 0 : normal 1 : had entered WOL+ mode	RO	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.4 ARL Control Register Page 1

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	LUT Aging timer setting bit[14:0] : Aging timer, the aging time is about : (mg_aging_time + 1) x 55.3 sec. ±3.8% bit[15] : Aging timer disable 0 : Enable 1 : Disable	R/W	0x0005
0x02	Source MAC address learning configure bit[1:0] : LUT learning mode 00 : overwrite L1/L2 according to the aging time 01, 10 : never overwrite before aging out 11 : only L2 will overwrite before aging out bit[2]: learning for null SA. 0: Don't learn 1: learn. Bit[3] : Hashing algorithm selection 0 : Direct hashing 1 : CRC hashing bit[4] : Disable forward unknown SA frame to CPU port 0 : forward 1 : not forward bit[5] : forward unknown SA frame if source address learning function is disable 0 : drop the unknown SA frame 1 : forward the unknown SA frame bit[6] : indicates the SA of input frame should match the original learn port or not 0 : SA will not bind the port 1 : SA will bind to the original learned port bit[7] : Learning SA or not when Packet drop by VLAN ingress check 0 : Learning 1 : not Learning	R/W	0x0020
0x03	Source MAC address learning enable for Port 16 ~ Port 1 bit[15:0] : Learning enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0xFFFF
0x04	Source MAC address learning Enable for Port 29 ~ Port 17 bit[12:0] : Learning Enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x1FFF
0x05	Source MAC address learning count control enable for Port 16 ~ Port 1 bit[15:0] : learning count control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x06	Source MAC address learning count control enable for Port 29 ~ Port 17 bit[12:0] : learning count control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x07	Source MAC address learning count control threshold setting bit[8:0] : learning count control threshold	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x08 ~ 0x0A	Reserved		
0x0B	Pass Pause packet to specific ports configuration bit [15:0] : Pause packets destination setting for Port 16 ~ Port 1 0 : Don't send to this port 1 : Send to this port	R/W	0x0000
0x0C	Pass Pause packet to specific ports configuration bit [12:0] : Pause packets destination setting for Port 29 ~ Port 17 0 : Don't send to this port 1 : Send to this port bit [13] : Enable Pass Pause packet function 0 : Disable 1 : Enable	R/W	0x0000
0x0D	Broadcast storm control configuration bit[7:0] : Broadcast storm control threshold bit[9:8] : Broadcast storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10) bit[10] : Block Broadcast/Multicast to CPU Enable 0 : Disable 1 : Enable bit[11] : Don't block bcst/Mcst Ipv4/IPv6 packets when bit[10] is enable 0 : block 1 : Don't block bit[12] : ignore 01:00:5E:xx:xx:xx for Mcst storm 0: Don't ignore 1 : Ignore	R/W	0x01FF
0x0E	Broadcast storm control enable for Port 16 ~ Port 1 bit[15:0] : Broadcast storm control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x0F	Broadcast storm control enable for Port 29 ~ Port 17 bit[12:0] : Broadcast storm control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x10	Multicast storm control enable for Port 16 ~ Port 1 (share the same threshold with broadcast storm control) bit[15:0] : Multicast storm control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x11	Multicast storm control enable for Port 29 ~ Port 17 (share the same threshold with broadcast storm control) bit[12:0] : Multicast storm control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x12	DLF storm control enable for Port 16 ~ Port 1 (share the same threshold with broadcast storm control) bit[15:0] : DLF storm control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x13	DLF storm control enable for Port 29 ~ Port 17 (share the same threshold with broadcast storm control) bit[12:0] : DLF storm control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x14	ARP storm control configuration bit [7:0] : ARP storm control threshold bit[9:8] : ARP storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10) bit[10] : Blocked ARP frame forward to CPU 0 : Disable 1 : Enable bit[11] : ARP storm drop interrupt enable	R/W	0x0000
0x15	ARP storm control enable for Port 16 ~ Port 1 bit[15:0] : ARP storm control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x16	ARP storm control enable for Port 29 ~ Port 17 bit[12:0] : ARP storm control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x17	ICMP storm control configuration bit [7:0] : ICMP storm control threshold bit[9:8] : ICMP storm counter clear period selection 00 : 200 us / 2ms / 20ms for (Giga/100/10) 01 : 1 ms / 10ms / 100ms for (Giga/100/10) 10 : 10 ms / 10ms / 10ms for (Giga/100/10) 11 : 100 ms / 100ms / 100ms for (Giga/100/10) bit[10] : ICMP storm drop interrupt enable	R/W	0x0000
0x18	ICMP storm control enable for Port 16 ~ Port 1 bit[15:0] : ICMP storm control enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x19	ICMP storm control enable for Port 29 ~ Port 17 bit[12:0] : ICMP storm control enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x1A	Port base address flush configuration bit [15:0] : indicates that these addresses learnt by selected port should be flushed for Port 16 ~ Port 1 0 : Don't flush 1 : flush	R/W	0x0000
0x1B	Port base address flush configuration bit [12:0] : indicates that these addresses learnt by selected port should be flushed for Port 29 ~ Port 17 0 : Don't flush 1 : flush bit[13] : flush command trig	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x1C	Trunk operation / Group configuration bit[2:0] : Trunk load balance hashing method selection 000 : Port ID 100 : DIP 001 : SA 101 : SIP 010 : DA 110 : TCP/UDP DP 011 : DA/SA 111 : TCP/UDP SP bit[3] : Trunk hashing method sequence enable 0 : Disable 1 : Enable bit[4] : CPU route function Don't care Trunk and VLAN result bit[5] : combine Trunk Group A and Group B into one Trunk bit[6] : combine Trunk Group C and Group D into one Trunk bit[7] : combine Trunk Group E and Group F into one Trunk 0 : Disable 1 : combine bit[11:8] : Trunk Group A configuration (Port 4 ~ Port 1) 0 : not in trunk 1 : in trunk bit[15:12] : Trunk Group B configuration (Port 8 ~ Port 5) 0 : not in trunk 1 : in trunk	R/W	0x0000
0x1D	Trunk group configuration bit[3:0] : Trunk Group C configuration (Port 12 ~ Port 9) 0 : not in trunk 1 : in trunk bit[7:4] : Trunk Group D configuration (Port 16 ~ Port 13) 0 : not in trunk 1 : in trunk bit[9:8] : Trunk Group E configuration (Port 26 ~ Port 25) 0 : not in trunk 1 : in trunk bit[11:10] : Trunk Group F configuration (Port 28 ~ Port 27) 0 : not in trunk 1 : in trunk	R/W	0x0000
0x1E	First Sniffer destination port group configuration bit[15:0] : select destination configuration for Port 16 ~ Port 1 0 : none 1 : selected	R/W	0x0000
0x1F	First Sniffer destination port group configuration bit[12:0] : select destination configuration for Port 29 ~ Port 17 0 : none 1 : selected bit[14:13] : sniffer method 00: Disable 01 : egress 10: ingress 11 : ingress+egress bit[15] : Tag/Untag setting for sniffered packet 0 : according to other criteria 1 : keep the original packet	R/W	0x0000
0x20	Second Sniffer destination port group configuration (only work for LUT/ARL/IGMP) bit[15:0] : select destination configuration for Port 16 ~ Port 1 0 : none 1 : selected	R/W	0x0000
0x21	Second Sniffer destination port group configuration (only work for LUT/ARL/IGMP) bit[12:0] : select destination configuration for Port 29 ~ Port 17 0 : none 1 : selected bit[13] : LUT trigger target for sniffer destination port group 1 0 : DA 1 : SA	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[14] : LUT trigger target for sniffer destination port group 2 0 : DA 1 : SA		
0x22	Sniffer source port configuration bit[15:0] : sniffer source config for Port 16 ~ Port 1 0 : no selected 1 : source	R/W	0x0000
0x23	Sniffer source port configuration bit[12:0] : sniffer source config for Port 29 ~ Port 17 0 : no selected 1 : source	R/W	0x0000
0x24	MISC configuration bit[0] : ACL function enable 0 : Disable 1 : Enable bit[1] : ACL ether type location for tag frame 0 : the location is after SA 1 : the location is after tag (ctag and/or stag) bit[2] : ACL ether type location for RFC 1042 frame 0 : the location is after SA 1 : the location is after RFC 1042 header bit[3] : LoopDetect block enable 0 : Disable 1 : Enable bit[5] : Sniffer Add/Rem Tag option for CPU special tag routing (reg 0x1C, bit[4] must be 1'b1) 0 : keep the original data 1 : according to other criteria bit[6] : Sniffer Add/Rem Tag option for ACL redirect/to_cpu action 0 : keep the original data 1 : according to other criteria bit[7] : Sniffer Add/Rem Tag option for other packets (include CPU special tag counting with Reg 0x1C, bit[4] is 1'b0) 0 : keep the original data 1 : according to other criteria Note : bit[7:5] only work when 0x1F bit[15] is 1'b1	R/W	0x0000
0x25	802.3 OAM LoopBack configuration bit[15:0] : LoopBack enable for port 16 ~ port 1 0 : Disable 1 : Enable	R/W	0x0000
0x26	802.3 OAM LoopBack configuration bit[12:0] : LoopBack enable for port 29 ~ port 17 0 : Disable 1 : Enable	R/W	0x0000
0x27	802.3 OAM LoopBack configuration bit[15:0] : LoopBack mode select for Port 16 ~ Port 1 0 : passive mode 1 : active mode	R/W	0x0000
0x28	802.3 OAM LoopBack configuration bit[11:0] : LoopBack mode select for Port 28 ~ Port 17 0 : passive mode 1 : active mode	R/W	0x0000
0x29	IGMP snooping function configuration bit[0] : enable IGMP snooping function bit[1] : multicast table make by CPU bit[2] : Disable IP address 224.0.0.X broadcast (except IGMP packet) bit[3] : Disable ***"Leave"*** function	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	(work in hardware-based IGMP-snooping) bit[4] : Reserved bit[5] : enable IGMP group member aging 0 : Disable 1 : Enable bit[12:6] : group member aging time setting (mg_mcst_thr + 1) x 70.4 sec. ±9.1% bit[13] : router list make by CPU only 0 : Disable 1 : make by CPU bit[15:14] : router port list aging setting for geometry change detect 00 : aging Disable 01 : about 320s 10 : about 500s 11 : about 640s		
0x2A	IGMP packets forwarding configuration bit[3:0] : Query setting bit[7:4] : Leave setting bit[11:8] : unregister mcst data setting bit[15:12] : undefined IGMP type the 4-bit setting for each kind of packet is {drop, router, CPU, bcst} 0 : Disable 1 : Enable	R/W	0x1141
0x2B	IGMP packets forwarding configuration bit[4:0] : Report setting bit[9:5] : Group Specific Query setting bit[14:10] : registered mcst data setting the 5-bit setting is {group member, drop, router, CPU, bcst} 0 : Disable 1 : Enable bit[15] : the Hashing method for IGMP 0 : CRC 1 : Direct	R/W	0x5294
0x2C	IGMP Router List configuration bit[15:0] : Router List setting for Port 16 ~ Port 1 0 : normal port 1 : router port	R/W	0x0000
0x2D	IGMP Router List configuration bit[12:0] : Router List setting for Port 29 ~ Port 17 0 : normal port 1 : router port	R/W	0x0000
0x2E	Memory access command for Mcst table and Source List table Source List command (bit[8] is 1'b0) bit[5:0] : memory address bit[7:6] : reserved bit[9:8] : should be 2'b00 bit[13:10] : reserved bit[14] : read/write control 0 : read 1 : write bit[15] : command trig/ack Mcst table command bit[7:0] : memory address bit[9:8] : should be 2'b01 bit[13:10] : reserved bit[14] : read/write control 0 : read 1 : write	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[15] : command trig/ack IP table command bit[6:0] : memory address bit[7] : reserved bit[9:8] : should be 2'b10 bit[13:10] : reserved bit[14] : read/write control 0 : read 1 : write bit[15] : command trig/ack		
0x2F	Read/Write data bit[15:0] for Mcst table/Source List table/IP table	R/W	0x0000
0x30	Read/Write data bit[31:16] for Mcst table/Source List table/IP table	R/W	0x0000
0x31	Read/Write data bit[47:32] for Mcst table/Source List table/IP table	R/W	0x0000
0x32	Read/Write data bit[63:48] for Mcst table/Source List table/IP table	R/W	0x0000
0x33	Read/Write data bit[79:64] for Mcst table/Source List table/IP table	R/W	0x0000
0x34	Read/Write data bit[95:80] for Mcst table/Source List table/IP table	R/W	0x0000
0x35	Read/Write data bit[111:96] for Mcst table/Source List table/IP table	R/W	0x0000
0x36	Read/Write data bit[127:112] for Mcst table/Source List table/IP table	R/W	0x0000
0x37	Read/Write data bit[143:128] Mcst table/Source List table/IP table	R/W	0x0000
0x38	Read/Write data bit[159:144] for Mcst table/Source List table/IP table	R/W	0x0000
0x39	Read/Write data bit[4:0] : for Mcst table bit[164:160] bit[15:0] : for Source List table/IP table bit[175:160]	R/W	0x0000
0x3A	Read/Write data bit[11:0] : for IP table bit[187:176] bit[15:0] : for Source List table bit[191:176]	R/W	0x0000
0x3B ~ 0x56	Read/Write data bit[207:192] for Source List table ~ Read/Write data bit[627:624] for Source List table	R/W	0x0000
0x57	Spanning Tree Protocol port state register 1_0 bit[15:0] : port state setting for port 8 ~ port 1, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF
0x58	Spanning Tree Protocol port state register 1_1 bit[15:0] : port state setting for port 16 ~ port 9, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x59	Spanning Tree Protocol port state register 1_2 bit[15:0] : port state setting for port 24 ~ port 17, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0xFFFF
0x5A	Spanning Tree Protocol port state register 1_3 bit[9:0] : port state setting for port 29 ~ port 25, two bit per port. 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state note : this register for both STP and MSTP	R/W	0x03FF
0x5B ~ 0x5E	Multiple Spanning Tree Protocol port state register 2 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x5F ~ 0x62	Multiple Spanning Tree Protocol port state register 3 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x63 ~ 0x66	Multiple Spanning Tree Protocol port state register 4 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x67 ~ 0x6A	Multiple Spanning Tree Protocol port state register 5 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x6B ~ 0x6E	Multiple Spanning Tree Protocol port state register 6 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x6F ~ 0x72	Multiple Spanning Tree Protocol port state register 7 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x73 ~ 0x76	Multiple Spanning Tree Protocol port state register 8 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x77 ~ 0x7A	Multiple Spanning Tree Protocol port state register 9 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x7B ~ 0x7E	Multiple Spanning Tree Protocol port state register 10 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x7F ~ 0x82	Multiple Spanning Tree Protocol port state register 11 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x83 ~ 0x86	Multiple Spanning Tree Protocol port state register 12 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x87 ~ 0x8A	Multiple Spanning Tree Protocol port state register 13 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x8B ~ 0x8E	Multiple Spanning Tree Protocol port state register 14 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x8F ~ 0x92	Multiple Spanning Tree Protocol port state register 15 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000
0x93 ~ 0x96	Multiple Spanning Tree Protocol port state register 16 00 : discard state 01 : blocking state 10 : learning state 11 : forwarding state	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x97	sFlow enable configuration for Port 16 ~ Port 1 bit[15:0] : enable for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x98	sFlow Enable configuration for Port 29 ~ Port 17 bit[12:0] : enable for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x99	sFlow sample method, 3 bits per port bit[14:0] : sample method for Port 5 ~ Port 1 000 : inbound 001 : VID 010 : ACL 011 : outbound 100 : Reserved 101 : LUT_MAC	R/W	0x0000
0x9A	sFlow sample method, 3 bits per port bit[14:0] : sample method for Port 10 ~ Port 6	R/W	0x0000
0x9B	sFlow sample method, 3 bits per port bit[14:0] : sample method for Port 15 ~ Port 11	R/W	0x0000
0x9C	sFlow sample method, 3 bits per port bit[14:0] : sample method for Port 20 ~ Port 16	R/W	0x0000
0x9D	sFlow sample method, 3 bits per port bit[14:0] : sample method for Port 25 ~ Port 21	R/W	0x0000
0x9E	sFlow sample method, 3 bits per port bit[11:0] : sample method for Port 29 ~ Port 26 bit[12] : each port use the same sample counter	R/W	0x0000
0x9F	sFlow sample rate configure for Port 1 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0000
0xA0 ~ 0xBB	sFlow sample rate configure for Port 2 ~ Port 29 bit[15:0] : rate configure. (rate = total packets / sampled packet)	R/W	0x0000
0xBC	sFlow sample VID configure for Port 1 bit[11:0] : VID that want to sampled for sFlow	R/W	0x0000
0xBD ~ 0xD8	sFlow sample VID configure for Port 2 ~ Port 29 bit[11:0] : VID that want to sampled for sFlow	R/W	0x0000
0xD9	VLAN mask function configuration bit[11:0] : 12 bits VID mask 0 : mask 1 : not mask	R/W	0x0FFF
0xDA	VLAN mask function enable for Port 16 ~ Port 1 bit[15:0] : function enable setting, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0xDB	VLAN mask function enable for Port 29 ~ Port 17 bit[12:0] : function enable setting, per port 1 bit 0 : Disable 1 : Enable	R/W	0x0000
0xDC ~ 0xDF	Reserved		
0xE0	CPU read/write address table configuration	R/W	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[12:0] : LUT address bit[13] : LUT block select 0 : first block 1 : second block bit[14] : Read/Write configuration 0 : Read 1 : Write bit[15] : Command trig/ack		
0xE1	CPU read/write address table data bit[15:0] : LUT data[15:0] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE2	CPU read/write address table data bit[15:0] : LUT data[31:16] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE3	CPU read/write address table data bit[15:0] : LUT data[47:32] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE4	CPU read/write address table data bit[15:0] : LUT data[63:48] if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE5	CPU read/write address table data bit[4:0] : LUT data[68:64] bit[5] : Table address access method 0 : address calculated by CPU 1 : address calculated by HW for normal MAC entry if the command is read, store the read back data if the command is write, write this data to address table	R/W	0x0000
0xE6	IGMP join / leave enable for each port bit[15:0] : enable join / leave for port 16 ~ port 1 0 : Disable 1 : Enable	R/W	0xFFFF
0xE7	IGMP join / leave enable for each port bit[12:0] : enable join / leave for port 29 ~ port 17 0 : Disable 1 : Enable	R/W	0x1FFF
0xE8	ARP storm drop event for Port 16 ~ Port 01 bit[15:0] : indicate the ARP storm drop event for Port 16 ~ Port 1	R/C	0x0000
0xE9	ARP storm drop event for Port 29 ~ Port 17 bit[12:0] : indicate the ARP storm drop event for Port 29 ~ Port 17	R/C	0x0000
0xEA	ICMP storm drop event for Port 16 ~ Port 01 bit[15:0] : indicate the ICMP storm drop event for Port 16 ~ Port 1	R/C	0x0000
0xEB	ICMP storm drop event for Port 29 ~ Port 17 bit[12:0] : indicate the ICMP storm drop event for Port 29 ~ Port 17	R/C	0x0000

ARL Registers : Page 0x01			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0xEC ~ 0xEF	Reserved		
0xF0	Multicast VLAN Group 1 setting bit[15:0] : VLAN member setting for P16 ~ P01	R/W	0x0000
0xF1	Multicast VLAN Group 1 setting bit[12:0] : VLAN member setting for P29 ~ P17	R/W	0x0000
0xF2 ~ 0xFD	Multicast VLAN Group 2 ~ 7 setting	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.5 ARL Control Register Page 2

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	Configuration for IP filter function bit[15:0] : IP filter function enable for Port 16 ~ Port 1	R/W	0x0000
0x02	Configuration for IP filter function bit[12:0] : IP filter function enable for Port 29 ~ Port 17 bit[13] : filter mode selection 0 : drop if IP mis-match 1 : drop if IP match bit[14] : enable pass for IP equal 0.0.0.0 0 : Disable 1 : Enable bit[15] : Hashing method selection 0 : CRC hashing 1 : direct hashing	R/W	0x0000
0x03~ 05	Reserved		0x0000
0x06	VLAN configuration bit[0] : protocol base VLAN enable 0 : Disable 1 : Enable bit[1] : tag base VLAN enable 0 : Disable 1 : Enable bit[2] : SVL/IVL select 0 : SVL 1 : IVL bit[3] : select the tag/untag method 0 : based on ports 1 : based on VIDs bit[4] : Modify tag in VID tag mode for CPU port 0 : Don't modify 1 : modify tag according to settings bit[5] : CTAG Remove/Modify enable 0 : Don't change CTAG 1 : remove/modify CTAG enable bit[6] : MSTP enable 0 : Disable 1 : Enable bit[7] : always use CTAG VID 0 : use CTAG / STAG (when STAG exist) 1 : use CTAG (even with STAG) bit[8] : Multicast Group specify VLAN Group 0 : Disable 1 : Enable bit[9] : VID priority works with the priority bits remark function 0 : Disable 1 : Enable Bit[14:10] : inactive VID redirect 0 ~ 28 : redirect to Port 1 ~ Port 29 30 : broadcast others : drop bit[15] : inactive VID redirect enable 0 : Disable 1 : Enable	R/W	0x0000
0x07	Insert PVID to the output port	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[15:0] : insert PVID to the output frame for port 16 ~ port 1 0 : Disable 1 : insert PVID to the current port will replace the VID of tag frame to PVID		
0x08	Insert PVID to the output port bit[12:0] : insert PVID to the output frame for port 29 ~ port 17 0 : Disable 1 : insert PVID to the current port will replace the VID of tag frame to PVID	R/W	0x0000
0x09	VLAN ingress check configuration (802.1Q 8.6.2) bit[15:0] : check if the port is the VLAN member for Port 16 ~ Port 1 0 : Don't check if the ingress port is in the VLAN group 1 : check if the ingress port is in the VLAN group	R/W	0x0000
0x0A	VLAN ingress check configuration (802.1Q 8.6.2) bit[12:0] : check if the port is the VLAN member for Port 29 ~ Port 17 0 : Don't check if the ingress port is in the VLAN group 1 : check if the ingress port is in the VLAN group	R/W	0x0000
0x0B	VLAN ingress check for Frame Type bit[15:0] : the ingress frame type check for port 8 ~ port 1, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0C	VLAN ingress check for Frame Type bit[15:0] : the ingress frame type check for port 16 ~ port 9, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0D	VLAN ingress check for Frame Type bit[15:0] : the ingress frame type check for port 24 ~ port 17, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0E	VLAN ingress check for Frame Type bit[9:0] : the ingress frame type check for port 29 ~ port 25, 2-bit/port 00 : admit all 01 : admit tag frame only 10 : admit priority tag and non-tag frame 11 : admit priority tag and tag frame	R/W	0x0000
0x0F	VLAN egress configuration. Set the criteria for the output to use default group setting. Bit[15:0] : by port. One bit per port, for port 16 ~ port 1 0 : Don't use default group setting 1 : use default group setting	R/W	0x0000
0x10	VLAN egress configuration. Set the criteria for the output to	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	use default group setting. Bit[12:0] : by port. One bit per port, for port 29 ~ port 17 0 : Don't use default group setting 1 : use default group setting bit[13] : unicast frame 0 : Don't use default group setting 1 : use default group setting bit[14] : multicast frame (DA equal to 01:00:5E:xx:xx:xx and IGMP need to be enabled) 0 : Don't use default group setting 1 : use default group setting bit[15] : ARP frame 0 : Don't use default group setting 1 : use default group setting		
0x11	Allow for local traffic bit[15:0] : enable local traffic forwarding for Port 16 ~ Port 1 0 : Disable 1 : Enable	R/W	0x0000
0x12	Allow for local traffic bit[12:0] : enable local traffic forwarding for Port 29 ~ Port 17 0 : Disable 1 : Enable	R/W	0x0000
0x13	Port 1 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x14 ~ 0x2F	Port 2 ~ Port 29 PVID configuration bit[11:0] : PVID setting bit[14:12] : PVID priority bits setting bit[15] : Force use PVID as VID for VLAN checking 0 : Disable 1 : Enable	R/W	0x0001
0x30	Port 1 Port base VLAN configuration bit[15:0] : Port base VLAN group (P16 ~ P1) setting	R/W	0xFFFF
0x31	Port 1 Port base VLAN configuration bit[12:0] : Port base VLAN group (P29 ~ P17) setting bit[13] : Force Port 1 use Port Base VLAN	R/W	0x1FFF
0x32 ~ 0x69	Port 2 ~ Port 29 Port base VLAN configuration	R/W	0xFFFF 0x1FFF
0x6A	Protocol Based VLAN entry 01 configuration bit[15:0] : TYPE for protocol define in entry 01	R/W	0x0000
0x6B	Protocol Based VLAN entry 01 configuration bit[11:0] : VID for protocol define in entry 01 bit[13:12] : Entry A protocol selection 00 : invalid 01 : EtherType	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	10 : LLC 11 : RFC 1042		
0x6C ~ 0x89	0x6C ~ 0x71 for Protocol Based VLAN entry 02 ~ 04 configuration Note: 0x6A ~ 0x89 also used for ACL VID remarking.	R/W	0x0000 0x0000
0x8A	ACL Assigned VLAN Group 01 bit[15:0] : VLAN Group 01 member setting for Port 16 ~ Port 1 0 : not member 1 : member	R/W	0x0000
0x8B	ACL Assigned VLAN Group 01 bit[12:0] : VLAN Group 01 member setting for Port 29 ~ Port 17 0 : not member 1 : member	R/W	0x0000
0x8C ~ 0xC9	ACL Assigned VLAN Group 02 ~ 32 configuration	R/W	0x0000 0x0000
0xCA	VLAN exclusive setting for Port 16 ~ Port 1 bit[15:0] : 0: this port is normal port 1: this port is protected port	R/W	0x0000
0xCB	VLAN exclusive setting for Port 29 ~ Port 17 bit[12:0] : 0: this port is normal port 1: this port is protected port	R/W	0x0000
0xCC	VLAN output port add tag setting for Port 16 ~ Port 1 bit[15:0] : output port add tag setting 0 : Don't add 1 : add	R/W	0x0000
0xCD	VLAN output port add tag setting for Port 29 ~ Port 17 bit[12:0] : output port add tag setting 0 : Don't add 1 : add	R/W	0x0000
0xCE	VLAN output port remove tag setting for Port 16 ~ Port 1 bit[15:0] : output port remove tag setting 0 : Don't remove 1 : remove	R/W	0x0000
0xCF	VLAN output port remove tag setting for Port 29 ~ Port 17 bit[12:0] : output port remove tag setting 0 : Don't remove 1 : remove	R/W	0x0000
0xD0	VLAN uplink function configuration bit[15:0] : uplink port configuration for Port 16 ~ Port 1 0 : normal port 1 : uplink port	R/W	0x0000
0xD1	VLAN uplink function configuration bit[12:0] : uplink port configuration for Port 29 ~ Port 17 0 : normal port 1 : uplink port bit[13] : uplink port function enable 0 : Disable 1 : Enable	R/W	0x0000
0xD2	VLAN Table Access command register bit[11:0] : VID bit[12] : sequential Read bit[13] : Reserved bit[14] : Read/Write 0 : Read 1 : Write bit[15] : command trig/ack	R/W	0x0000
0xD3	VLAN Table Access data register	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[15:0] : Read/Write VLAN table data[15:0]		
0xD4	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[31:16]	R/W	0x0000
0xD5	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[47:32]	R/W	0x0000
0xD6	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[63:48]	R/W	0x0000
0xD7	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[79:64]	R/W	0x0000
0xD8	VLAN Table Access data register bit[15:0] : Read/Write VLAN table data[95:80]	R/W	0x0000
0xD9	ACL Bandwidth threshold setting 0 ~ 1 bit[6:0] : ACL bw0 threshold bit[7] : unit selection 0 : 128Kbps, 1 : 2Mbps bit[14:8] : ACL bw1 threshold bit[15] : unit selection 0 : 128Kbps, 1 : 2Mbps	R/W	0x0000
0xDA ~ 0xDF	ACL Bandwidth threshold setting 2 ~ 13	R/W	0x0000
0xE0	ACL Bandwidth threshold setting 14 bit[6:0] : ACL bw14 threshold bit[7] : unit selection 0 : 128Kbps, 1 : 2Mbps	RW	0x0000
0xE1	ACL user define pattern location setting bit[4:0] : pattern 1 location setting bit[9:5] : pattern 2 location setting	R/W	0x0000
0xE2	ACL user define pattern location setting bit[4:0] : pattern 3 location setting bit[9:5] : pattern 4 location setting	R/W	0x0000
0xE3	ACL Table Access command register bit[6:0] : entries select bit[7] : sequential read bit[8] : table select 0 : rule 1 : action bit[14] : Read/ Write 0 : Read 1 : Write bit[15] : command trig	R/W	0x0000
0xE4	ACL entries access data register bit[15:0] : read/write ACL entry data[15:0]	R/W	0x0000
0xE5	ACL entries access data register bit[15:0] : read/write ACL entry data[31:16]	R/W	0x0000
0xE6	ACL entries access data register bit[15:0] : read/write ACL entry data[47:32]	R/W	0x0000
0xE7	ACL entries access data register bit[15:0] : read/write ACL entry data[63:48]	R/W	0x0000
0xE8	ACL entries access data register	R/W	0x0000

ARL Registers : Page 0x02			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[15:0] : read/write ACL entry data[79:64]		
0xE9	ACL entries access data register bit[15:0] : read/write ACL entry data[95:80]	R/W	0x0000
0xEA	ACL entries access data register bit[15:0] : read/write ACL entry data[111:96]	R/W	0x0000
0xEB	ACL entries access data register bit[15:0] : read/write ACL entry data[127:112]	R/W	0x0000
0xEC	ACL entries access data register bit[15:0] : read/write ACL entry data[143:128]	R/W	0x0000
0xED	ACL entries access data register bit[6:0] : read/write ACL entry data[150:144]	R/W	0x0000
0xEE	Configuration for VID/PVID match behavior setting bit0 for P16 ~ P01 (not affect non_tag/priority_tag) bit[15:0] : bit0 setting for Port 16 ~ P01	R/W	0x0000
0xEF	Configuration for VID/PVID match behavior setting bit0 for P29 ~ P17 bit[12:0] : bit0 setting for Port 29 ~ P17	R/W	0x0000
0xF0	Configuration for VID/PVID match behavior setting bit1 for P16 ~ P01 bit[15:0] : bit1 setting for Port 16 ~ P01	R/W	0x0000
0xF1	Configuration for VID/PVID match behavior setting bit1 for P29 ~ P17 bit[12:0] : bit1 setting for Port 29 ~ P17 The behavior for {bit1, bit0} is : 00 : Disable 01 : drop if VID equals to PVID 10 : drop if VID does not equal to PVID 11 : act with Multicast SRC function, to pass VID equal to PVID	R/W	0x0000
0xF2	Configuration Source Ports for Multicast SRC function bit[15:0] : source port setting for P16 ~ P01	R/W	0x0000
0xF3	Configuration Source Ports for Multicast SRC function bit[12:0] : source port setting for P29 ~ P17	R/W	0x0000
0xF4	LUT memory repair control bit[0] : disable the repair entry 0 0 : enable, 1 : disable bit[1] : disable the repair entry 1 bit[2] : disable the repair entry 2 bit[3] : disable the repair entry 3 bit[5:4] : repair entry read back selection	R/W	0x0000
0xF5	LUT memory repair status bit[12:0] : the failed memory address bit[13] : the failed memory block 0 : low bits block, 1 : high bits block bit[14] : Valid bit 0 :invalid, 1 : valid	RO	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.6 SMI Control Register

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	Auto negotiation configuration for port 1 – port 16 bit [15:0] : 0 : Disable auto negotiation 1 : Enable auto negotiation	R/W	0xFFFF
0x02	Auto negotiation configuration for port 17 – port 29 bit [12:0] : 0 : Disable auto negotiation 1 : Enable auto negotiation	R/W	0x1FFF
0x03	Speed setting for 1000 Mbps for port 25 – port 29 bit[4:0] : 0 : 1000 Mbps ability disable 1 : 1000 Mbps ability enable	R/W	0x001F
0x04	Speed setting for 10/100 Mbps for port 1 – port 16 Bit[15:0] : 0 : 10 Mbps 1 : 100 Mbps	R/W	0xFFFF
0x05	Speed setting for 10/100 Mbps for port 17 – port 29 Bit[12:0] : 0 : 10 Mbps 1 : 100 Mbps	R/W	0x1FFF
0x06	Duplex setting for port 1 – port 16 bit [15:0] : 0 : half duplex 1 : full duplex	R/W	0xFFFF
0x07	Duplex setting for port 17 – port 29 bit [12:0] : 0 : half duplex 1 : full duplex	R/W	0x1FFF
0x08	Pause setting for port 1 – port 16 bit [15:0] : 0 : Disable pause 1 : Enable pause	R/W	0xFFFF
0x09	Pause setting for port 17 – port 29 bit [12:0] : 0 : Disable pause 1 : Enable pause	R/W	0x1FFF
0x0A	Asymmetric pause setting for port 1 – port 16 bit [15:0] : 0 : Disable asymmetric pause 1 : Enable asymmetric pause	R/W	0xFFFF
0x0B	Asymmetric pause setting for port 16 – port 29 bit [12:0] : 0 : Disable asymmetric pause 1 : Enable asymmetric pause	R/W	0x1FFF
0x0C	Backpressure setting for port 1 – port 16 bit [15:0] : 0 : backpressure function disable 1 : backpressure function enable	R/W	0xFFFF
0x0D	Backpressure setting for port 17 – port 29 bit [12:0] : 0 : backpressure function disable 1 : backpressure function enable	R/W	0x1FFF
0x0E	Power down setting for port 1 – port 16 Bit [15:0] : 0 : power down disable 1 : power down enable	R/W	0x0000
0x0F	Power down setting for port 17 – port 29 Bit [12:0] : 0 : power down disable 1 : power down enable	R/W	0x0000

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x10	WOL function enable for port 25 – port 28 bit [3:0] : 0 : WOL disable 1 : WOL enable bit [4] : port 25 WOL sense ANY packet to wake up bit [5] : port 25 WOL sense MAGIC packet to wake up bit [6] : port 26 WOL sense ANY packet to wake up bit [7] : port 26 WOL sense MAGIC packet to wake up bit [8] : port 27 WOL sense ANY packet to wake up bit [9] : port 27 WOL sense MAGIC packet to wake up bit [10] : port 28 WOL sense ANY packet to wake up bit [11] : port 28 WOL sense MAGIC packet to wake up	R/W	0x0FFF
0x11	PHY address setting for port 25/26/27/28/29 bit [2:0] : port 25 PHY address, default 3'd6 bit [5:3] : port 26 PHY address, default 3'd7 bit [8:6] : port 27 PHY address, default 3'd4 bit [11:9] : port 28 PHY address, default 3'd5 bit [14:12] :port 29 PHY address, default 3'd1	R/W	0x1B3E
0x12	SMI MISC setting bit [0] : port 29 force link set 0 : force link Disable 1 : force link Enable bit [1] : port 29 force duplex pin setting (RO) 0 : half duplex 1 : full duplex bit [3:2] :port 29 force speed pin setting (RO) 00 : 10 Mbps 01 : 100 Mbps 10 : 1000 Mbps 11 : reserved bit [4] : port 25 SGMII set (RO) 0 : non SGMII mode 1 : SGMII mode bit [5] : port 26 SGMII set (RO) 0 : non SGMII mode 1 : SGMII mode bit [6] : port 25 LED off @TP mode 0 : Disable 1 : Enable bit [7] : port 26 LED off @TP mode 0 : Disable 1 : Enable bit [8] : port 29 force status (according to 0x03/0x05/0x07/0x09/0x0B) 0 : Disable 1 : Enable bit [9] : port 25 force PAUSE 0 : Disable 1 : Enable bit [10] : port 26 force PAUSE	R/W	0x0100

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	0 : Disable 1 : Enable bit [11] : reserved bit [12] : port 25 SGMII force polling PHY 0 : Disable 1 : Enable bit [13] : port 25 SGMII force polling PHY selection 0 : internal PHY 1 : external PHY bit [14] : port 26 SGMII force polling PHY 0 : Disable 1 : Enable bit [15] : port 26 SGMII force polling PHY selection 0 : internal PHY 1 : external PHY		
0x13	CPU read/write PHY register command bit [4:0] : PHY address bit [9:5] : MII register address bit [10] : write all TP (port1-port24) bit [13:11] : Reserved bit [14] : 0 : read operation 1 : write operation bit [15] : the read/write PHY register command trigger 0 : idle or command complete 1 : start command(for write)/command complete(for read)	R/W	0x0000
0x14	CPU read/write PHY register command data bit [15:0] : in read command – the read back data in write command – data want to write	R/W	0x0000
0x15	SCA startup status for port 1 – port 16 (fiber port not support) bit [15:0] : 0 : cable test fail 1 : cable test good	RO	0x0000
0x16	SCA startup status for port 17 – port 29 (fiber port not support) bit [12:0] : 0 : cable test fail 1 : cable test good bit [13] : SCA period setting 0 : run 5 seconds show 3 seconds 1 : run 10 seconds show 5 seconds bit [14] : SCA enable 0 : Disable 1 : Enable bit [15] : SCA trig (only work when bit[14] is asserted) 0 : no action 1 : trig SCA and do it once	R/W	0x2000

SMI Registers : Page 0x03

<table>
<tr><th>Reg Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>0x17</td><td>
LED SETTING
bit [2:0] : LED mode (B : <u>bi-color</u> ; M : mono-color)
<table>
<tr><th rowspan="2">0x17 bit [2:0]</th><th rowspan="2">LED mode</th><th colspan="2">LED display behavior</th></tr>
<tr><th>Giga port</th><th>10/100M port</th></tr>
<tr><td>000</td><td>3-bit B</td><td><u>Giga, 100</u>, L/A</td><td></td></tr>
<tr><td>001</td><td>3-bit M</td><td>Giga-L/A, 10/100-L/A, F/C</td><td>100-L/A, 10-L/A, F/C</td></tr>
<tr><td>010</td><td>3-bit M</td><td>Giga-L/A, 10/100-L/A, FC/ flash</td><td>100-L/A, 10-L/A, FC/ flash</td></tr>
<tr><td>011</td><td>2-bit M</td><td>Giga, L/A</td><td>100, L/A</td></tr>
<tr><td>100</td><td>3-bit M</td><td>TX, RX, Giga-Spd
[Giga light, 100 flash, 10 dark]</td><td></td></tr>
<tr><td>101</td><td>3-bit B</td><td><u>Giga, L/A</u>, F/C</td><td><u>100, L/A,</u> F/C</td></tr>
<tr><td>110</td><td>3-bit B</td><td><u>Giga, L/A</u>, FC/ flash</td><td><u>100, L/A</u>, FC/ flash</td></tr>
<tr><td>111</td><td>2-bit B</td><td><u>Giga, L/A</u></td><td><u>100, L/A</u></td></tr>
</table>
bit [3] : LED AZ sleeping indication
(When enter the sleeping state, LED will light 1second and dark 1 second)
0 : Disable
1 : Enable
bit [5:4] : LED blink rate
00 : 40 ms
01 : 80 ms
10 : 120 ms
11 : 160 ms
bit [7:6] : LED clock rate
00 : 781 KHz
01 : 2.5 MHz
10 : 5.2 MHz
11 : 10.4 MHz
bit [8] : LED collision blink disable
0 : blink when collision
1 : no blink when collision
bit [9] : LED act (tx/rx) blink disable
0 : blink when act
1 : no blink when act
bit [10] : LED loop-detect indication
0 : Disable
1 : Enable
bit [11] : LED loop-detect indication time
0 : short pattern
1 : long pattern
bit [12] : LED power-saving set.
0 : Disable
1 : Enable
bit [13] : LED power-saving trig, and this bit will work when bit [12] is asserted.
0 : non action
1 : trig
bit [14] : LED power-saving time
0 : LED trig show time is 10s
1 : LED trig show time is 30s
bit [15] : reserved
</td><td>R/W</td><td>0x00C3</td></tr>
</table>

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x18	LED port selection for port 1 – port 16 bit [15:0] : LED port selection	R/W	0xFFFF
0x19	LED port selection for port 17 – port 29 bit [12:0] : LED port selection bit [13] : LED FX indication enable bit [14] : port 29 LED CPU control enable 0 : Disable 1 : Enable (The corresponding signals for led_0/led_1/led_2, reference to register 0x1B[12]/0x1D[12]/0x1F[12])	R/W	0x3FFF
0x1A	CPU control serial-LED setting for port 1 – port 16 bit [15:0] : serial-LED(led_0) setting	R/W	0xFFFF
0x1B	CPU control serial-LED setting for port 17 – port 29 bit [12:0] : serial-LED(led_0) setting	R/W	0x1FFF
0x1C	CPU control serial-LED setting for port 1 – port 16 bit [15:0] : serial-LED(led_1) setting	R/W	0xFFFF
0x1D	CPU control serial-LED setting for port 17 – port 29 bit [12:0] : serial-LED(led_1) setting	R/W	0x1FFF
0x1E	CPU control serial-LED setting for port 1 – port 16 bit [15:0] : serial-LED(led_2) setting	R/W	0xFFFF
0x1F	CPU control serial-LED setting for port 17 – port 29 bit [12:0] : serial-LED(led_2) setting	R/W	0x1FFF
0x20	SMI port status for port 1 and port 2 (7bit / port) bit [6:0] : port 1 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 2 status flow_ctrl: include backpressure in half duplex speed definition: 1x: 1000 Mbps 01: 100 Mbps 00: 10 Mbps	RO	0x0000
0x21	SMI port status for port 3 and port 4 (7bit / port) bit [6:0] : port 3 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 4 status	RO	0x0000
0x22	SMI port status for port 5 and port 6 (7bit / port) bit [6:0] : port 5 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 6 status	RO	0x0000
0x23	SMI port status for port 7 and port 8 (7bit / port) bit [6:0] : port 7 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 8 status	RO	0x0000

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x24	SMI port status for port 9 and port 10 (7bit / port) bit [6:0] : port 9 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 10 status	RO	0x0000
0x25	SMI port status for port 11 and port 12 (7bit / port) bit [6:0] : port 11 status { AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 12 status	RO	0x0000
0x26	SMI port status for port 13 and port 14 (7bit / port) bit [6:0] : port 13 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 14 status	RO	0x0000
0x27	SMI port status for port 15 and port 16 (7bit / port) bit [6:0] : port 15 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 16 status	RO	0x0000
0x28	SMI port status for port 17 and port 18 (7bit / port) bit [6:0] : port 17 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 18 status	RO	0x0000
0x29	SMI port status for port 19 and port 20 (7bit / port) bit [6:0] : port 19 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 20 status	RO	0x0000
0x2A	SMI port status for port 21 and port 22 (7bit / port) bit [6:0] : port 21 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 22 status	RO	0x0000
0x2B	SMI port status for port 23 and port 24 (7bit / port) bit [6:0] : port 23 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 24 status	RO	0x0000
0x2C	SMI port status for port 25 and port 26 (7bit / port) bit [6:0] : port 25 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 26 status	RO	0x0000
0x2D	SMI port status for port 27 and port 28 (7bit / port)	RO	0x0000

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit [6:0] : port 27 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link} bit [7] : reserved bit [14:8] : port 28 status		
0x2E	SMI port status for port 29 (7bit / port) bit [6:0] : port 29 status {AN enable, asymmetric pause, flow_ctrl, duplex,speed[1:0], link}	RO	0x0000
0x2F	EEE enable for port 1 – port 16 bit [15:0] : EEE port enable	R/W	0xFFFF
0x30	EEE enable for port 17 – port 29 bit [12:0] : EEE port enable 0 : Disable 1 : Enable bit [13] : MMD register read/write enable 0 : Disable 1 : Enable bit [14] : EEE local Tw (wake-up time) read enable 0 : Disable 1 : Enable	R/W	0x1FFF
0x31	MMD read/write command bit [4:0] : PHY address bit [9:5] : DEVICE address bit [13:10] : Reserved bit [14] : 0 : read operation 1 : write operation bit [15] : the read/write PHY register command trigger 0 : idle 1 : start command(for write)/ command complete(for read)	R/W	0x0000
0x32	MMD read/write ADDRESS bit [15:0] : ADDRESS	R/W	0x0000
0x33	MMD write DATA bit [15:0] : write data	R/W	0x0000
0x34	MMD read DATA bit [15:0] : read data	R/W	0x0000
0x35	EEE auto-negotiation ability for port 1 – port 16 bit [15:0] : 0 : AN EEE enable 1 : AN EEE disable	RO	0x0000
0x36	EEE auto-negotiation ability for port 17 – port 29 bit [12:0] : 0 : AN EEE enable 1 : AN EEE disable	RO	0x0000
0x37	EEE Tw for port 1 bit [8:0] : port 1 EEE Tw	RO	0x0000
0x38	EEE Tw for port 2 bit [8:0] : port 2 EEE Tw	RO	0x0000
0x39	EEE Tw for port 3 bit [8:0] : port 3 EEE Tw	RO	0x0000

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x3A	EEE Tw for port 4 bit [8:0] : port 4 EEE Tw	RO	0x0000
0x3B	EEE Tw for port 5 bit [8:0] : port 5 EEE Tw	RO	0x0000
0x3C	EEE Tw for port 6 bit [8:0] : port 6 EEE Tw	RO	0x0000
0x3D	EEE Tw for port 7 bit [8:0] : port 7 EEE Tw	RO	0x0000
0x3E	EEE Tw for port 8 bit [8:0] : port 8 EEE Tw	RO	0x0000
0x3F	EEE Tw for port 9 bit [8:0] : port 9 EEE Tw	RO	0x0000
0x40	EEE Tw for port 10 bit [8:0] : port 10 EEE Tw	RO	0x0000
0x41	EEE Tw for port 11 bit [8:0] : port 11 EEE Tw	RO	0x0000
0x42	EEE Tw for port 12 bit [8:0] : port 12 EEE Tw	RO	0x0000
0x43	EEE Tw for port 13 bit [8:0] : port 13 EEE Tw	RO	0x0000
0x44	EEE Tw for port 14 bit [8:0] : port 14 EEE Tw	RO	0x0000
0x45	EEE Tw for port 15 bit [8:0] : port 15 EEE Tw	RO	0x0000
0x46	EEE Tw for port 16 bit [8:0] : port 16 EEE Tw	RO	0x0000
0x47	EEE Tw for port 17 bit [8:0] : port 17 EEE Tw	RO	0x0000
0x48	EEE Tw for port 18 bit [8:0] : port 18 EEE Tw	RO	0x0000
0x48	EEE Tw for port 19 bit [8:0] : port 19 EEE Tw	RO	0x0000
0x4A	EEE Tw for port 20 bit [8:0] : port 20 EEE Tw	RO	0x0000
0x4B	EEE Tw for port 21 bit [8:0] : port 21 EEE Tw	RO	0x0000
0x4C	EEE Tw for port 22 bit [8:0] : port 22 EEE Tw	RO	0x0000
0x4D	EEE Tw for port 23 bit [8:0] : port 23 EEE Tw	RO	0x0000
0x4E	EEE Tw for port 24 bit [8:0] : port 24 EEE Tw	RO	0x0000
0x4F	EEE Tw for port 25 bit [8:0] : port 25 EEE Tw	RO	0x0000
0x50	EEE Tw for port 26	RO	0x0000

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit [8:0] : port 26 EEE Tw		
0x51	EEE Tw for port 27 bit [8:0] : port 27 EEE Tw	RO	0x0000
0x52	EEE Tw for port 28 bit [8:0] : port 28 EEE Tw	RO	0x0000
0x53	EEE Tw for port 29 bit [8:0] : port 29 EEE Tw	RO	0x0000
0x54	For PHY status register, register address and page setting bit [4:0] : PHY status register address (default 5'd17) bit [9:5] : PHY status page selection (default 5'd15)	R/W	0x01F1
0x55	For PHY status register, bit selection (select 2 bits) bit [15:0] : bit selection for PHY status register (default 16'h14)	R/W	0x0014
0x56	For PHY status register, read enable for port 1 – port 16 bit [15:0] : PHY status register address	R/W	0x0000
0x57	For PHY status register, read enable for port 17 – port 29 bit [12:0] : PHY status register address	R/W	0x0000
0x58	For PHY status register, 100 fiber status for port 1 – port 16 bit [15:0] : running on 100 fiber	RO	0x0000
0x59	For PHY status register, 100 fiber status for port 17 – port 29 bit [12:0] : running on 100 fiber	RO	0x0000
0x5A	For PHY status register, 1000 fiber status for port 1 – port 16 bit [15:0] : running on 1000 fiber	RO	0x0000
0x5B	For PHY status register, 1000 fiber status for port 17 – port 29 bit [12:0] : running on 1000 fiber	RO	0x0000
0x5C	Force link setting for port 1 – port 16 bit [15:0] : force link enable	R/W	0x0000
0x5D	Force link setting for port 17 – port 28 bit [11:0] : force link enable bit [13:12] : reserved bit [14] : Test mode polling PHY enable 0 : Disable (default) 1 : Enable bit [15] : Bypass PHY enable 0 : Disable (default) 1 : Enable	R/W	0x0000
0x5E	Reserved	R/W	0x0000
0x5F	SCA setting bit [4 :0] : SCA enable for port 25 – port 29 0 : Disable 1 : Enable (default) bit [9 :5] : SCA mode for port 25 – port 29 0 : running as IP1001G (default)	R/W	0x001F

SMI Registers : Page 0x03			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	1 : running as IP101G bit [15:10] : Reserved		
0x60	EEE local Tw register address of MMD at 1000Mbps bit [15:0] : MMD register address (0x60, 0x61 and 0x62 a set)	R/W	0x0004
0x61	EEE local Tw device address of MMD at 1000Mbps bit [4:0] : MMD device address	R/W	0x001E
0x62	EEE local Tw bit number of MMD at 1000Mbps bit [15:0] : MMD bit number of the selected register (select 9-bit of 16-bit, ex 0x01FF select the lowest 9 bits)	R/W	0x01FF
0x63	EEE local Tw register address of MMD at 100Mbps bit [15:0] : MMD register address (0x63, 0x64 and 0x65 a set)	R/W	0x0003
0x64	EEE local Tw device address of MMD at 100Mbps bit [4:0] : MMD device address	R/W	0x001E
0x65	EEE local Tw bit number of MMD at 100Mbps bit [15:0] : MMD bit number of the selected register (select 9-bit of 16-bit, ex 0x01FF select the lowest 9 bits)	R/W	0x01FF
0x66	Uni-direction enable for port 1 – port 16 bit [15:0] : 0 : uni-direction disable 1 : uni-direction enable	R/W	0x0000
0x67	Uni-direction enable for port 17 – port 29 bit [12:0] : 0 : uni-direction disable 1 : uni-direction enable	R/W	0x0000
0x68~ 0xFE	(reserved)		
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.7 OAM Control Register

OAM Registers 1 : Page 0x04			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	OAM Information OAMPDU OUI setting bit [15:0] : Information OUI[15:0]	R/W	0x90C3
0x02	OAM Information OAMPDU OUI setting bit [7:0] : Information OUI[23:16]	R/W	0x0000
0x03	OAM Information OAMPDU VENDOR setting bit [15:0] : Information VENDOR[15:0]	R/W	0x0000
0x04	OAM Information OAMPDU VENDOR setting bit [15:0] : Information VENDOR[31:16]	R/W	0x0000
0x05	OAM indirect register command bit [4:0] : port selection bit [9:5] : register selection bit [13:10] : reserved bit [14] : read/write 0 : read command 1 : write command bit [15] : the read/write OAM indirect register command trigger 0 : idle 1 : start command(for write)/command complete(for read) (reference the OAM indirect registers)	R/W	0x0000
0x06	OAM indirect register data bit [15:0] : in read command – the read back data in write command – data want to write (reference the OAM indirect registers)	R/W	0x0000
0x07	OAM Dying Gasp Independent enable for Port 01- Port 16 bit [15:0] : OAM Dying Gasp Independent enable (Using this function, do not enable OAM by asserting indirect register 0x00 bit[0] OAM enable)	R/W	0x0000
0x08	OAM Dying Gasp Independent enable for Port 17- Port 29 bit [12:0] : OAM Dying Gasp Independent enable (Using this function, do not enable OAM by asserting indirect register 0x00 bit[0] OAM enable)	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.8 OAM Indirect Registers for Each Port

OAM Indirect Registers Page 0x05			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x00	OAM configuration bit [0] : OAM enable 0 : Disable 1 : Enable bit [1] : OAM configuration trig bit [2] : OAM remote LoopBack trig bit [3] : OAM reset bit [4] : Information OAMPDU configuration Mode (When setting Mode, bit [1] should be set as “1.”) 0 : passive mode 1 : active mode bit [5] : Information OAMPDU configuration Remote LoopBack support (When setting Remote LoopBack ability, bit [1] should be set as “1.”) 0 : Disable 1 : Enable bit [6] : OAM remote read/write enable 0 : Disable 1 : Enable bit [7] : OAM remote read/write check OUI 0 : Disable 1 : Enable bit [8] : OAM LoopBack timeout enable (timeout time is 5 seconds) 0 : Disable 1 : Enable bit [9] : OAM LoopBack test result Read Clear enable, please refer to indirect register 0x08 bit[6] and bit[7]. 0 : Disable 1 : Enable bit [10] : OAM critical event register setting (Should check setting with bit [11]) 0 : no critical event 1 : critical event occur bit [11] : OAM internal critical event disable (OAM critical event according to register setting; reference to bit [10]) 0 : Enable 1 : Disable bit [12] : OAM external critical event disable (OAM critical event according to PIN) 0 : Enable 1 : Disable bit [13] : OAM critical event indication once per second enable 0 : Disable 1 : Enable bit [14] : OAM Discovery check Unidirectional field	R/W	0x0000

OAM Indirect Registers Page 0x05			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	0 : Disable 1 : Enable bit [15] : OAM Discovery check Remote LoopBack field 0 : Disable 1 : Enable		
0x01	OAM remote read/write command	R/W	0x0000
0x02	OAM remote read/write data	R/W	0x0000
0x03~ 0x07	(reserved)		
0x08	OAM Status bit [0] : link status 0 : unlink 1 : link bit [1] : OAM mode 0 : passive mode 1 : active mode bit [2] : local fault (refer to 0x17 for detail) 0 : local OAM no faults 1 : local OAM fault occurred bit [3] : remote fault (refer to 0x17 for detail) 0 : remote OAM no faults 1 : remote OAM fault occurred bit [5:4] : reserved bit [6] : active LoopBack test packets send out 0 : test packets not send out 1 : test packets send out bit [7] : active LoopBack test result 0 : fail 1 : ok bit [9:8] : reserved bit [10] : OAM remote read/write OUI check result (if 0x00 bit[6] and bit [7] are enable) 0 : mismatch 1 : match bit [13:11] : OAM Discovery state bit [15:14] : OAM Transmit state	RO	0x0000
0x09	OAM local flag bit [15:0] : OAM local flag	RO	0x0000
0x0A	OAM local Information OAMPDU revision bit [15:0] : OAM local Information OAMPDU revision	RO	0x0000
0x0B	OAM local Information OAMPDU state and configuration bit [7:0] : OAM local Information OAMPDU configuration bit [15:8] : OAM local Information OAMPDU state	RO	0x0000
0x0C	OAM local Information OAMPDU OUI[15:0] bit [15:0] : OAM local Information OAMPDU OUI[15:0]	RO	0x0000

OAM Indirect Registers Page 0x05			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x0D	OAM local Information OAMPDU OUI[23:16] bit [7:0] : OAM local Information OAMPDU OUI[23:16]	RO	0x0000
0x0E	OAM local Information OAMPDU VENDOR bit [15:0] : OAM local Information OAMPDU VENDOR[15:0]	RO	0x0000
0x0F	OAM local Information OAMPDU VENDOR bit [15:0] : OAM local Information OAMPDU VENDOR[31:16]	RO	0x0000
0x10	OAM remote flag bit [15:0] : OAM remote flag	RO	0x0000
0x11	OAM remote Information OAMPDU revision bit [15:0] : OAM remote Information OAMPDU revision	RO	0x0000
0x12	OAM remote Information OAMPDU state and configuration bit [7:0] : OAM remote Information OAMPDU configuration bit [15:8] : OAM remote Information OAMPDU state	RO	0x0000
0x13	OAM remote Information OAMPDU OUI[15:0] bit [15:0] : OAM remote Information OAMPDU OUI[15:0]	RO	0x0000
0x14	OAM remote Information OAMPDU OUI[23:16] bit [7:0] : OAM remote Information OAMPDU OUI[23:16]	RO	0x0000
0x15	OAM remote Information OAMPDU VENDOR bit [15:0] : OAM remote Information OAMPDU VENDOR[15:0]	RO	0x0000
0x16	OAM remote Information OAMPDU VENDOR bit [15:0] : OAM remote Information OAMPDU VENDOR[31:16]	RO	0x0000
0x17	OAM local/remote fault record(clear by indirect register 0x00 bit[3] reset) bit [0] : OAM local link fault bit [1] : OAM local dying gasp bit [2] : OAM local critical event bit [7:3] : reserved bit [8] : OAM remote link fault bit [9] : OAM remote dying gasp bit [10] : OAM remote critical event	RO	0x0000
0x18~ 0x1F	(reserved)		

6.9 RxDMA Control Register

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01 | 0x0C	(Reserved)		
0x0D	TCP/UDP destination port filter method Bit[1:0]: Port 1 “Forwarding WAN/LAN / Packet drop” setting 00 : Disable Forwarding WAN/LAN& Packet drop 01 : Packet Drop enable (TX/RX ref 0x13 ~ 0x16) 10 : Forwarding to LAN port only (ref 0x11~0x12) 11 : Forwarding to WAN port only (ref 0x11 ~0x12) Bit[3:2] : Port 2 “Forwarding WAN/LAN / Packet drop” setting Bit[5:4] : Port 3 “Forwarding WAN/LAN / Packet drop” setting Bit[7:6] : Port 4 “Forwarding WAN/LAN / Packet drop” setting Bit[9:8] : Port 5 “Forwarding WAN/LAN / Packet drop” setting Bit[11:10]: Port 6 “Forwarding WAN/LAN / Packet drop” setting Bit[13:12]: Port 7 “Forwarding WAN/LAN / Packet drop” setting Bit[15:14]: Port 8 “Forwarding WAN/LAN / Packet drop” setting	R/W	0x0000
0x0E	TCP/UDP destination port filter method Bit[1:0] : Port 9 “Forwarding WAN/LAN / Packet drop” setting Bit[3:2] : Port 10“Forwarding WAN/LAN / Packet drop” setting Bit[5:4] : Port 11“Forwarding WAN/LAN / Packet drop” setting Bit[7:6] : Port 12“Forwarding WAN/LAN / Packet drop” setting Bit[9:8] : Port 13“Forwarding WAN/LAN / Packet drop” setting Bit[11:10]: Port 14“Forwarding WAN/LAN / Packet drop” setting Bit[13:12]: Port 15“Forwarding WAN/LAN / Packet drop” setting Bit[15:14]: Port 16“Forwarding WAN/LAN / Packet drop” setting	R/W	0x0000
0x0F	TCP/UDP destination port filter method Bit[1:0] : Port 17“Forwarding WAN/LAN / Packet drop” setting Bit[3:2] : Port 18“Forwarding WAN/LAN / Packet drop” setting Bit[5:4] : Port 19“Forwarding WAN/LAN / Packet drop” setting Bit[7:6] : Port 20“Forwarding WAN/LAN / Packet drop” setting Bit[9:8] : Port 21“Forwarding WAN/LAN / Packet drop” setting Bit[11:10]: Port 22“Forwarding WAN/LAN / Packet drop” setting Bit[13:12]: Port 23“Forwarding WAN/LAN / Packet drop” setting Bit[15:14]: Port 24“Forwarding WAN/LAN / Packet drop” setting	R/W	0x0000
0x10	TCP/UDP destination port filter method Bit[1:0] : Port 25“Forwarding WAN/LAN / Packet drop” setting Bit[3:2] : Port 26“Forwarding WAN/LAN / Packet drop” setting Bit[5:4] : Port 27“Forwarding WAN/LAN / Packet drop” setting Bit[7:6] : Port 28“Forwarding WAN/LAN / Packet drop” setting Bit[9:8] : Port 29“Forwarding WAN/LAN / Packet drop” setting ***Drop/ Filter rule**: (ref below table)*	R/W	0x0000

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	(1) "Forwarding WANLAN / Packet drop setting = 10 or 11 *This port only reference forwarding to WAN/LAN port only setting.* *(2) "Forwarding WAN/LAN / Packet drop setting = 01* *(i) this port is Drop enable and look at "drop act on" setting* *(a) if act on RX , then all packet RX at this port is dropped* *(b) if act on TX , then all packet from other port TX out this port will be dropped* *(3) "Forwarding WAN/LAN / Packet drop setting = 00* *Filter & Drop function at this port is disabled*		
0x11	WAN Port setting for TCP/UDP destination port bit[15:0] : WAN port setting (P16~P1) 0: set as LAN 1: set as WAN	R/W	0x0000
0x12	WAN Port setting for TCP/UDP destination port bit[12:0] : WAN port setting (P29~P17) 0: set as LAN 1: set as WAN	R/W	0x0000
0x13	TCP/UDP destination port filter – Drop act on TX/RX setting Bit[1:0] : Port 1 drop act 00: Rx (all matched P1 Rx packet drop) 01: Tx (all matched packet Tx to P1 drop) 1x: Rx+Tx (packet RX/TX to P1 drop) bit[3:2] : Port 2 drop act bit[5:4] : Port 3 drop act bit[7:6] : Port 4 drop act bit[9:8] : Port 5 drop act Bit[11:10] : Port 6 drop act bit[13:12] : Port 7 drop act bit[15:14] : Port 8 drop act	R/W	0x0000
0x14	TCP/UDP destination port filter – Drop act on TX/RX setting Bit[1:0] : Port 9 drop act bit[3:2] : Port 10 drop act bit[5:4] : Port 11 drop act Bit[7:6] : Port 12 drop act bit[9:8] : Port 13 drop act Bit[11:10] : Port 14 drop act bit[13:12] : Port 15 drop act bit[15:14] : Port 16 drop act	R/W	0x0000
0x15	TCP/UDP destination port filter – Drop act on TX/RX setting Bit[1:0] : Port 17 drop act bit[3:2] : Port 18 drop act bit[5:4] : Port 19 drop act Bit[7:6] : Port 20 drop act bit[9:8] : Port 21 drop act Bit[11:10] : Port 22 drop act bit[13:12] : Port 23 drop act bit[15:14] : Port 24 drop act	R/W	0x0000

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x16	TCP/UDP destination port filter – Drop act on TX/RX setting Bit[1:0] : Port 25 drop act bit[3:2] : Port 26 drop act bit[5:4] : Port 27 drop act Bit[7:6] : Port 28 drop act bit[9:8] : Port 29 drop act	R/W	0x0000

Host / Client Forwarding WAN / LAN and Packet drop setting Condition

Host / Client			Client Port setting											
			Client is LAN Port						Client is WAN Port					
			00 Disable	01 Drop			10 LAN	11 WAN	00 Disable	01 Drop			10 LAN	11 WAN
				RX	RX+TX	TX				RX	RX+TX	TX		
Host port setting	00 Disable		V	V	X	X	V	V	V	V	X	X	V	V
	01 Drop	Act on RX	X						X					
		Act on TX+RX												
		Act on TX	V	V	X	X	V	V	V	V	X	X	V	V
	10 FWD LAN		V	V	X	X	V	V	X	X	X	X	X	X
	11 FWD WAN		X	X	X	X	X	X	V	V	X	X	V	V

(1) V : PASS

(2) X : Drop

(3) Host port
Switch Port to receive packet

(4) Client port
Switch Port to transmit packet

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x17	RX Priority queuing decision setting (1 bit/ port) P16 ~ P01 Bit[15:0] : priority to Q based on ACL DSCP selected remark QID 0: Disable 1 : Enable Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x0000
0x18	RX Priority queuing decision setting (1 bit/ port) P29 ~ P17 Bit[12:0] : priority to Q based on ACL DSCP selected remark QID 0: Disable 1 : Enable	R/W	0x0000
0x19	RX Priority queuing decision setting (1 bit/ port) P16 ~ P01 Bit[15:0] : priority to Q based on VLAN-table remarked tag priority 0: Disable 1: Enable	R/W	0x0000
0x1A	RX Priority queuing decision setting (1 bit/ port) P29 ~ P17 Bit[12:0] : priority to Q based on VLAN-table remarked tag priority 0: Disable 1: Enable Bit[14] : 0 : disable 1: enable (priority to Q based on ACL/VLAN) Bit[15] : ACL DSCP pri / VLAN-table Tag pri criteria order 0 : ACL DSCP pri > VLAN-table tag pri 1 : VLAN-table tag pr > ACL DSCP pri (Note: IF DSCP pri / Tag pri remark are both enabled this reg only affect rx packet to which one queue)	R/W	0x0000
0x1B	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (P16 ~ P01) Bit[15:0] : mac_priority to DSCP auto remarking 0: Disable 1: Enable	R/W	0x0000
0x1C	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (P29 ~ P17) Bit[12:0] : mac_priority to DSCP auto remarking 0: Disable 1: Enable	R/W	0x0000
0x1D	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (P16 ~ P01) Bit[15:0] : VLAN-table remarked tag priority to DSCP auto remarking	R/W	0x0000
0x1E	(Mac priority/ VLAN-table remarked tag priority) to DSCP auto remarking (P29 ~ P17) Bit[12:0] : VLAN-table remarked tag priority to DSCP auto remarking Bit[15] : mac_pri / remarked tag pri criteria order 0 : mac pri > remarked tag pri 1 : remarked pri > tag pri (Criteria ACL DSCP pri > above description) (If QinQ VID Sel is enable , ACL DSCP remark will be disabled)	R/W	0x0000
0x1F	TCP Flag attribute priority: Bit[0]: <= 256 Bytes TCP SYN highest priority enable Bit[1]: <= 256 Bytes TCP SYN/ACK highest priority enable Bit[2]: <= 256 Bytes TCP ACK highest priority enable	R/W	0x0000

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x20	WRED Drop packet setting: Bit[0] : WRED drop act on TCP packet only (1: tcp0: all) Bit[1] : WRED drop act on TCP exclude TCP SYN <= 256 B Bit[2] : WRED drop act on TCP exclude TCP SYN/ACK <= 256 B Bit[3] : WRED drop act on TCP exclude TCP ACK <= 256 B Bit[8] : sFlow packet force TX out (0: normal drop 1: force tx, regardless any drop) Bit[9] : sFlow packet port map to CPU packet length cutoff (0: Disable 1: Enable)	R/W	0x0000
0x21	Out Queue Pause / Drop to RX setting Bit[15:0] : P16~P01 out queue **threshold** to RX pause/drop disable 0: Enable 1: Disable (1bit/port)	R/W	0x0000
0x22	Out Queue Rx Pause / Drop to RX setting Bit[12:0] : P29~P17 out queue **threshold to RX** pause/drop Disable	R/W	0x0000
0x23	(reserved for test only) Bit[15:14] = 0 mode 0 Bit[10:0] : The share frame buffer threshold for flow control ON\ Bit[15:14] = 1 mode 1 Bit[9:0] : mg_jumbo_off_pg Bit[15:14] = 2 mode 2 Bit[3:0] : threshold x 1us , on off hold on time (1000 M) Bit[7:4] : threshold x 10us , on off hold on time (100M) Bit[11:8] : threshold x 100us , on off hold on time (10M) Bit[12] : Half duplex pause on/off spacing 0 : on 1: off	R/W	0x06A7 (0x39) (0x1888)
0x24	P01 RX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x4688
0x25	P01 RX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap Bit[8:6] : Priority 7 remap Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x4688
0x26	P02 RX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x01F5

RxDMA Registers : Page 0x06			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x27	P02 RX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap Bit[8:6] : Priority 7 remap	R/W	0x4688
0x28 ~ 0x5B	P03 ~ P28 RX priority remap data	R/W	0x01F5 0x4688
0x5C	P29 RX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x01F5
0x5D	P29 RX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap Bit[8:6] : Priority 7 remap	R/W	0x4688
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.10 TxDMA Control Register

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	QinQ double tag remove service tag operation configuration Bit [15:0] : output frame remove service tag (P16 ~ P01) 0 : Disable 1 : remove service tag to output frame	R/W	0x0000
0x02	QinQ double tag remove service tag operation configuration Bit [12:0] : output frame remove service tag (P29 ~ P17) 0 : Disable 1 : remove service tag to output frame	R/W	0x0000
0x03	QinQ double tag add service tag operation configuration Bit [15:0] : output frame add service tag (P16 ~ P01) 0 : Disable 1 : add service tag to output frame	R/W	0x0000
0x04	QinQ double tag add service tag operation configuration Bit [12:0] : output frame add service tag (P29 ~ P17) 0 : Disable 1 : add service tag to output frame (QinQ detect enable set from 0x05 ~ 0x06)	R/W	0x0000
0x05	Detect RX QinQ double tag enable for port 16 ~ port 1 , Bit [15:0] : 0 : Disable 1 : Enable	R/W	0x0000

		0x05~0x06 detect enable				0x05~0x06 detect disable			
Qing (add,rmv)		00	01	10	11	00	01	10	11
Service Tag rx	0	x	x	add	x	x	x	add	x
	1	x	rmv	mdf	x	x	x	add	x

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x06	Detect RX QinQ double tag enable for port 29 ~ port 17 , Bit [12:0] : 0 : Disable 1 : Enable	R/W	0x0000
0x07	802.1Q tagged PVID use TX port enable for P16 ~ P01 Bit [15:0] : 0 : Disable 1 : Enable Criteria priority (0x75 ~ 0x78): 00: TX PVID (0x07~0x08) > ACL VID > QID register 0x70 ~0x74 > RX PVID 01: TX PVID (0x07~0x08) > ACL VID > RX PVID 10: TX PVID (0x07~0x08) > ACL VID > Vlan table pri remark > RX PVID 11: TX PVID (0x07~0x08) > ACL VID > Vlan table pri remark > QID register 0x70 ~0x74 > RX PVID (QID register 0x70 ~ 0x74 only relative to { pri, cfi } , VID index will use RXPVID)	R/W	0x0000
0x08	802.1Q tagged PVID use TX port enable for P29 ~ P17 Bit [12:0] : 0 : Disable 1 : Enable	R/W	0x0000
0x09	QinQ double tag type-length definition bit [15:0] :	R/W	0x88A8
0x0A	QinQ double tag {PCP, DEI, VID} definition0 – Data (S-Tag VID) by ACL rule / register setting Used to insert into/modify frame which should add/modify a double tag	R/W	0x0000
0x0B ~ 0x49	QinQ double tag {PCP, DEI, VID} definition1~63 – Data (S-Tag VID) by ACL rule / register setting Used to insert into frame which should add a double tag	R/W	0x0000
0x4A	QinQ double tag VID r/w address and select method P1 Bit[5:0] : Port 1 S-TAG VID r/w register select address Bit[11:8] : Port 1 S-TAG VID r/w address select method *0000 : address = mg_stag_vid_adr_p1[5:0]* *0001 : address = acl_dvid_sel[5:0], 6'd0 means no ACL act* *(if ACL entry is not hit , mg_stag_vid_adr_p1[5:0] will be used)* *0010 : address = 802.1Q-VID[11:6] (C-TAG VID[11:6])* *0011 : address = 802.1Q-VID[5:0] (C-TAG VID[5:0])* *0100 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[11:8] (C-TAG VID[11:8])* *0101 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[7:4] } (C-TAG VID[7:4])* *0110 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[3:0]} (C-TAG VID[3:0])* *(use RX 1Q-VID before TX remove/modify 1Q-VID,* *If RX packet is non-1Q-VID , then RX-PVID will be used)* *1010 : address = 802.1Q-VID[11:6] (C-TAG VID[11:6])* *1011 : address = 802.1Q-VID[5:0] (C-TAG VID[5:0])* *1100 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[11:8] (C-TAG VID[11:8])* *1101 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[7:4] (C-TAG VID[7:4])* *1110 : address = {mg_stag_vid_adr_p1[1:0], 802.1Q-VID[3:0] (C-TAG VID[3:0])* *(Insert / modify : use TX 1Q-VID , come from ARL result)*	R/W	0x0000

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	(Remove : use RX port's PVID) Bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)		
0x4B	QinQ double tag VID r/w address and select method P2 Bit[5:0] : Port 2 S-TAG VID r/w Register select address Bit[10:8] : Port 2 S-TAG VID r/w address select method Bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)	R/W	0x0000
0x4C ~ 0x66	QinQ double tag VID r/w address and select method P3~P29 Bit[5:0] : Port 3~29 S-TAG VID r/w Register select address Bit[10:8] : Port 3~29 S-TAG VID r/w address select method Bit[12] : QinQ double tag {PCP, DEI} field keep original packet During qinq tag modification. (0: modified 1: keep org)	R/W	0x0000
0x67	Ipv4/v6 DSCP/IPP TOS remarking (ACL Select 0, 1) / (QID = 0,1) bit[5:0] : ACL select 0 / Queue 0 , remarking Value Bit[6] : ACL select 0 / Queue 0 DSCP[2:0]/ IPP remarking 0 : Enable 1: Disable Bit[7] : ACL select 0 / Queue 0 DSCP[5:3]/ TOS remarking 0 : Enable 1: Disable bit[13:8] : ACL select 1 / Queue 1 , remarking Value Bit[14] : ACL select 1 / Queue 1 DSCP[2:0]/ IPP remarking 0 : Enable 1: Disable Bit[15] : ACL select 1 / Queue 1 DSCP[5:3]/ TOS remarking 0 : Enable 1: Disable	R/W	0x0000
0x68	Ipv4/v6 DSCP/IPP TOS remarking (ACL Select 2, 3) / (QID = 2,3) bit[5:0] : ACL select 2 / Queue 2 , remarking Value Bit[6] : ACL select 2 / Queue 2 DSCP[2:0]/ IPP remarking Bit[7] : ACL select 2 / Queue 2 DSCP[5:3]/ TOS remarking bit[13:8] : ACL select 3 / Queue 3 , remarking Value Bit[14] : ACL select 3 / Queue 3 DSCP[2:0]/ IPP remarking Bit[15] : ACL select 3 / Queue 3 DSCP[5:3]/ TOS remarking	R/W	0x0000
0x69	Ipv4/v6 DSCP/IPP TOS remarking (ACL Select 4, 5) / (QID = 4,5) bit[5:0] : ACL select 4 / Queue 4 , remarking Value Bit[6] : ACL select 4 / Queue 4 DSCP[2:0]/ IPP remarking Bit[7] : ACL select 4 / Queue 4 DSCP[5:3]/ TOS remarking bit[13:8] : ACL select 5 / Queue 5 , remarking Value Bit[14] : ACL select 5 / Queue 5 DSCP[2:0]/ IPP remarking Bit[15] : ACL select 5 / Queue 5 DSCP[5:3]/ TOS remarking	R/W	0x0000
0x6A	Ipv4/v6 DSCP/IPP TOS remarking (ACL Select 6, 7) / (QID = 6,7) bit[5:0] : ACL select 6 / Queue 6 , remarking Value. Bit[6] : ACL select 6 / Queue 6 DSCP[2:0]/ IPP remarking Bit[7] : ACL select 6 / Queue 6 DSCP[5:3]/ TOS remarking	R/W	0x0000

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[13:8] : ACL select 7 / Queue 7 , remarking Value Bit[14] : ACL select 7 / Queue 7 DSCP[2:0]/ IPP remarking Bit[15] : ACL select 7 / Queue 7 DSCP[5:3]/ TOS remarking		
0x6B	Ipv4/v6 DSCP/IPP TOS Setup command (0x6E/0x6F QID rule per queue setting, per queue default is disabled) bit[7:0] : queue enable for Q7 ~ Q0 bit[13:8] : Read/ Write dscp enable data From/to Pxx bit[15] : 0: Read 1: Write	R/W	0x0000
0x6C	Ipv4/v6 DSCP/IPP TOS remarking Method (from ACL table) bit[15:0] : ACL ruled Ipv4 DSCP/IPP TOS remarking (1 bit / port) (ACL has higher priority than queue ID)	R/W	0x003F
0x6D	Ipv4/v6 DSCP/IPP TOS remarking Method (from ACL table) bit[12:0] : ACL ruled Ipv4 DSCP/IPP TOS remarking (1 bit / port) (ACL has higher priority than queue ID)	R/W	0x003F
0x6E	Ipv4/v6 DSCP/IPP TOS remarking Method (from QID)(0x6B set per queue based) bit[15:0] : queue ID rules Ipv4 DSCP/IPP TOS remarking (1 bit / port) (0x6C, 0x6D ACL has higher priority than 0x6E 0x6F queue ID)	R/W	0x003F
0x6F	Ipv4/v6 DSCP/IPP TOS remarking Method (from QID) (0x6B set per queue based) bit[12:0] : queue ID rules Ipv4 DSCP/IPP TOS remarking (1 bit / port) (0x6C, 0x6D ACL has higher priority than 0x6E 0x6F queue ID)	R/W	0x003F
0x70	802.1Q TAG {PCP, CFI} remarking (Q1 , Q0) bit[0] : Queue 0 original CFI value 0 remarking bit[1] : Queue 0 original CFI value 1 remarking bit[6:4] : Queue 0 , 802.1Q priority remarking value bit[8] : Queue 1 original CFI value 0 remarking bit[9] : Queue 1 original CFI value 1 remarking bit[14:12] : Queue 1 , 802.1Q priority remarking value	R/W	0x1202
0x71	802.1Q TAG {PCP, CFI} remarking (Q3 , Q2) bit[0] : Queue 2 original CFI value 0 remarking bit[1] : Queue 2 original CFI value 1 remarking bit[6:4] : Queue 2 , 802.1Q priority remarking value bit[8] : Queue 3 original CFI value 0 remarking bit[9] : Queue 3 original CFI value 1 remarking bit[14:12] : Queue 3 , 802.1Q priority remarking value	R/W	0x3222
0x72	802.1Q TAG {PCP, CFI} remarking (Q5 , Q4) bit[0] : Queue 4 original CFI value 0 remarking bit[1] : Queue 4 original CFI value 1 remarking bit[6:4] : Queue 4 , 802.1Q priority remarking value bit[8] : Queue 5 original CFI value 0 remarking	R/W	0x5242

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	bit[9] : Queue 5 original CFI value 1 remarking bit[14:12] : Queue 5 , 802.1Q priority remarking value		
0x73	802.1Q TAG {PCP, CFI} remarking (Q7 , Q6) bit[0] : Queue 6 original CFI value 0 remarking bit[1] : Queue 6 original CFI value 1 remarking bit[6:4] : Queue 6 , 802.1Q priority remarking value bit[8] : Queue 7 original CFI value 0 remarking bit[9] : Queue 7 original CFI value 1 remarking bit[14:12] : Queue 7 , 802.1Q priority remarking value	R/W	0x7262
0x74	802.1Q TAG {PCP, CFI} remarking Setup command (qid rule) bit[7:0] : queue enable for Q7 ~ Q0 Bit[13:8] : Read/Write remarking enable data to From/to Pxx Bit[15] : 0: Read 1: Write	R/W	0x0000
0x75	802.1Q TAG {PCP, CFI} remarking criteria (P08 ~ P01 , 2bit / port) Bit[1:0] : Port 1 remarking criteria 00: TX PVID (0x07~0x08) > ACL VID > QID register 0x70 ~0x74 > RX PVID 01: TX PVID (0x07~0x08) > ACL VID > RX PVID 10: TX PVID (0x07~0x08) > ACL VID > VLAN table pri remark > RX PVID 11: TX PVID (0x07~0x08) > ACL VID > VLAN table pri remark > QID register 0x70 ~0x74 > RX PVID (QID register 0x70 ~ 0x74 only relative to { pri, cfi } , VID index will use RXPVID) Bit[15:2] : Port 8 ~ Port 2 remarking criteria	RW	0xFFFF
0x76	802.1Q TAG {PCP, CFI} remarking criteria (P16 ~ P09 , 2bit / port)	R/W	0xFFFF
0x77	802.1Q TAG {PCP, CFI} remarking criteria (P24 ~ P17 , 2bit / port)	R/W	0xFFFF
0x78	802.1Q TAG {PCP, CFI} remarking criteria (P29 ~ P25 , 2bit / port)	R/W	0x03FF
0x79	TX (802.1Q TAG) type-length field definition Bit [15:0] : CTAG T/L field (Add / MDF)	R/W	0x8100
0x7A	Port 29 Special Tag setting Bit[3:0] : sFlow packet length cutoff setting 4'd0 : 64 Bytes 4'd1 : 256 Bytes 4'd2 : 512 Bytes 4'd3 : 768 Bytes 4'd4 : 1024 Bytes 4'd5 : 1280 Bytes 4'd6 : 1536 Bytes 4'd7 : 1792 Bytes 4'd8 : 2048 Bytes 4'd9 : 2304 Bytes 4'd10 : 2560 Bytes 4'd11 : 2816 Bytes 4'd12 : 3072 Bytes 4'd13 : 3328 Bytes 4'd14/15: Disable length cutoff Note: (1) If original packet length < length cutoff setting ,packet length will	R/W	0x0030

TxDMA Registers : Page 0x07			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	not modify Bit[4] : sFlow information add to special tag (28 Bytes) 1: Enable 0 : Disable Bit[5] : PTP stamp information add to special tag (8 Bytes) 1: Enable 0 : Disable		
0x7B	**Reserved**		
0x7C	**Reserved**		
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.11 Output Queue Control Register

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	Port Group A Out queue schedule mode / weight selection Bit[2:0] : Schedule mode 0 : First come First schedule 1 : WRR/WFQ/BW/TWRR 2 : SPx1 + WRR/WFQ/BW/TWRR x7 3 : SPx2 + WRR/WFQ/BW/TWRR x6 4 : SPx4 + WRR/WFQ/BW/TWRR x4 5 : SPx8 6 : LLQx1 + WFQ/BW/TWRR x7 (LLQ in WRR will switch to SP) 7 : LLQx2 + WFQ/BW/TWRR x6 (LLQ in WRR will switch to SP) (LLQ : Low latency Queue) Bit[4:3] : BW throttle period sel / TWRR tickle unit 00 : 64 kbit/s / 51.2 ms 01: 1 Mbit/s / 3.19 ms 10 : 2 Mbit/s / 1.55 ms 11: 4 Mbit/s / 0.82 ms Bit[6:5]: Queue method(00: WRR 01: BW 10: WFQ 11: TWRR) Bit[7] : Delay Bound mode (Q7/Q6/Q5/Q4/Q3/Q2/Q1) (Q0 queue out only when Q7~Q1 is empty) must set bit[6:5] = 10/01, at the same time Bit[8] : Q0 BE(best effort) queue disable (only bit[7] = 1) (Q0 is also delay bound queue if disable BE) Bit[9] : WRED Drop enable (must also set 0x53/0x54) Bit[10] : Delay Bound/LLQ Pause-Backpressure enable (will enable if 0x01[6:5]=01/10 & 0x01[7] =1) Bit[11] : Priority remap enable (0: CPU 1: Std) Bit[14:12] : (reserved) Bit[15] : Queue schedule ratio value “0” definition BW/WFQ/TWRR (0: eq value1 1: Stop & hold packet)	R/W	0x0000
0x02	Port Group A Out queue schedule ratio 0 Bit[7:0] : Q0 weight / bandwidth allocate / Bit[15:8] : Q1 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x03	Port Group A Out queue schedule ratio 1 Bit[7:0] : Q2 weight / bandwidth allocate / Bit[15:8] : Q3 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x04	Port Group A Out queue schedule ratio 2 Bit[7:0] : Q4 weight / bandwidth allocate / Bit[15:8] : Q5 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x05	Port Group A Out queue schedule ratio 3 Bit[7:0] : Q6 weight / bandwidth allocate / Bit[15:8] : Q7 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
	Note 1: if 0x0E ~ 0x13 SRP parameter is setup with value > 0 , *Q7 BW = mg_oq_lan_ratio3[15:8]x 64 Bytes/ slot time* *Q6 BW = mg_oq_lan_ratio3[7:0] x 64 Bytes / slot time* *Note 2: The LAN port max BW (if port SRP parameter > 0)* *Q7 BW = mg_oq_lan_max_bw3[15:8]x 64 Bytes/ slot time* *Q6 BW = mg_oq_lan_max_bw3[7:0] x 64 Bytes / slot time* *Note 3: If Delay bound mode is enable , Per Queue latency limit* *= ratio x {16us, 64us, 256us, 1024us}(ref 0x69[10:9])*		
0x06	Port Group A Out queue 0 latency threshold Bit[7:0] : Q0 latency threshold Bit[15:8] : Q1 latency threshold	R/W	0x4080
0x07	Port Group A Out queue 1 latency threshold Bit[7:0] : Q2 latency threshold Bit[15:8] : Q3 latency threshold	R/W	0x1020
0x08	Port Group A Out queue 2 latency threshold Bit[7:0] : Q4 latency threshold Bit[15:8] : Q5 latency threshold	R/W	0x0408
0x09	Port Group A Out queue 3 latency threshold Bit[7:0] : Q6 latency threshold Bit[15:8] : Q7 latency threshold	R/W	0x0102
0x0A	Port Group A Out queue Max Bandwidth Bit[7:0] : Q0 max bandwidth Bit[15:8] : Q1 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0B	Port Group A Out queue Max Bandwidth Bit[7:0] : Q2 max bandwidth Bit[15:8] : Q3 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0C	Port Group A Out queue Max Bandwidth Bit[7:0] : Q4 max bandwidth Bit[15:8] : Q5 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x0D	Port Group A Out queue Max Bandwidth Bit[7:0] : Q6 max bandwidth Bit[15:8] : Q7 max bandwidth (value =0 : unlimited) *Ethernet AV setup:* *The LAN port max BW (if port 0x0E ~0x13 SRP parameter > 0)*	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Q7 BW = mg_oq_lan_max_bw3[15:8]x 64 Bytes/ slot time *Q6 BW = mg_oq_lan_max_bw3[7:0] x 64 Bytes / slot time*		
0x0E	Ethernet AV SRP BW Credit-shaper parameter setup Bit[2:0] : Port 01 Bit[5:3] : Port 02 Bit[8:6] : Port 03 Bit[11:9] : Port 04 Bit[14:12] : Port 05 SRP parameter (sche mode must : WFQ / BW /TWRR) *(250 us *n : reg0x66[13:11])* *000 : Disable* *001 : Q7.125 us* *010 : Q7.250 us * n* *011 : Q7.125 us & Q6.125 us* *100 : Q7.125 us & Q6.250 us * n* *101 : Q7.250 us *n & Q6.250 us * n* (Must set: Group A 0x0D Q7/Q6 max bandwidth → As MAX Threshold 0x09 Q7/Q6 latency threshold → As Idle Slope 0x05 Q7/Q6 bandwidth allocate → As min BW threshold Group B 0x84 Q7/Q6 max bandwidth → As MAX Threshold 0x80 Q7/Q6 latency threshold → As Idle Slope 0x7c Q7/Q6 bandwidth allocate → As min BW threshold For Credit Shaped BW control, MAX must > min BW Threshold,	R/W	0x01F5
0x0F	Ethernet AV SRP BW Credit-shaper parameter setup Bit[2:0] : Port 06 Bit[5:3] : Port 07 Bit[8:6] : Port 08 Bit[11:9] : Port 09 Bit[14:12] : Port 10	R/W	0x01F5
0x10	Ethernet AV SRP BW Credit-shaper parameter setup Bit[2:0] : Port 11 Bit[5:3] : Port 12 Bit[8:6] : Port 13 Bit[11:9] : Port 14 Bit[14:12] : Port 15	R/W	0x01F5
0x11	Ethernet AV SRP BW Credit-shaper parameter setup Bit[2:0] : Port 16 Bit[5:3] : Port 17 Bit[8:6] : Port 18 Bit[11:9] : Port 19 Bit[14:12] : Port 20	R/W	0x01F5
0x12	Ethernet AV SRP BW Credit-shaper parameter setup	R/W	0x01F5

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[2:0] : Port 21 Bit[5:3] : Port 22 Bit[8:6] : Port 23 Bit[11:9] : Port 24 Bit[14:12] : Port 25		
0x13	Ethernet AV SRP BW Credit-shaper parameter setup Bit[2:0] : Port 26 Bit[5:3] : Port 27 Bit[8:6] : Port 28 Bit[11:9] : Port 29	R/W	0x01F5
0x14	P01 TX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x4688
0x15	P01 TX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap Bit[8:6] : Priority 7 remap Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) > RX priority remapping (PG06.0x24~0x5D) > ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)	R/W	0x4688
0x16	P02 TX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x01F5
0x17	P02 TX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap Bit[8:6] : Priority 7 remap	R/W	0x4688
0x18 ~ 0x4B	P03 ~ P28 TX priority remap data	R/W	0x01F5 0x4688
0x4C	P29 TX Priority remap data Bit[2:0] : Priority 0 remap Bit[5:3] : Priority 1 remap Bit[8:6] : Priority 2 remap Bit[11:9] : Priority 3 remap Bit[14:12] : Priority 4 remap	R/W	0x01F5
0x4D	P29 TX Priority remap data Bit[2:0] : Priority 5 remap Bit[5:3] : Priority 6 remap	R/W	0x4688

<table>
<tr><th colspan="4">Output Queue Register : Page 0x08</th></tr>
<tr><th>Reg Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td></td><td>Bit[8:6] : Priority 7 remap</td><td></td><td></td></tr>
<tr><td>0x4E</td><td>Out queue Random Early Detect threshold
Bit[3:0] : WRED threshold for ACT0
Bit[7:4] : WRED threshold for ACT1
Bit[11:8] : WRED threshold for ACT2
Bit[15:12] : WRED threshold for ACT3

<table><tr><th>WRED Drop probability</th><th>Q7/Q6</th><th>Q5/Q4</th><th>Q3/Q2</th><th>Q1/Q0</th></tr><tr><td>oq_wred_cnt > ACT3</td><td>1/(0x52 thr)</td><td>1/(0x51 thr)</td><td>1/(0x50 thr)</td><td>1/(0x4F thr)</td></tr><tr><td>ACT2 <oq_wred_cnt < ACT3</td><td>x</td><td>1/(0x52 thr)</td><td>1/(0x51 thr)</td><td>1/(0x50 thr)</td></tr><tr><td>ACT1 <oq_wred_cnt < ACT2</td><td>x</td><td>x</td><td>1/(0x52 thr)</td><td>1/(0x51 thr)</td></tr><tr><td>ACT0<oq_wred_cnt < ACT1</td><td>x</td><td>x</td><td>x</td><td>1/(0x52 thr)</td></tr><tr><td>oq_wred_cnt < ACT0</td><td>x</td><td>x</td><td>x</td><td>x</td></tr></table></td><td>R/W</td><td>0xA842</td></tr>
<tr><td>0x4F</td><td>WRED markA weight threshold
Bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)</td><td>R/W</td><td>0x0002</td></tr>
<tr><td>0x50</td><td>WRED markB weight threshold
Bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)</td><td>R/W</td><td>0x0004</td></tr>
<tr><td>0x51</td><td>WRED markC weight threshold
Bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)</td><td>R/W</td><td>0x0008</td></tr>
<tr><td>0x52</td><td>WRED markD weight threshold
Bit[8:0] : mark weight threshold drop rate(1/packet) = 1/(threshold)</td><td>R/W</td><td>0x000A</td></tr>
<tr><td>0x53</td><td>Out queue WRED enable
Bit[15:0] : Port 16 ~ Port01 Out Queue WRED ability
1: Enable 0 : Disable</td><td>R/W</td><td>0x0000</td></tr>
<tr><td>0x54</td><td>Out queue WRED enable
Bit[12:0] : Port 29 ~ Port17 Out Queue WRED ability
1: Enable 0 : Disable</td><td>R/W</td><td>0x0000</td></tr>
<tr><td>0x55</td><td>P1~P2 queue based SBM (static bandwidth management /
DBM (Dynamic bandwidth management) select
Bit[7:0] : P01 Q7~Q0 SBM /DBM select (1: SBM 0: DBM)
Bit[15:8] : P02 Q7~Q0 SBM /DBM select

must set mg_oq_sche_mode[6:5] = 01
(Out queue BW-mode)
<u>(DBM must work with 0x64~0x65 BW range set)</u>
<u>(DBM will be disabled internally if 0x64 ~ 0x65 TX port BW range is not set.)</u>

ex: throttle enable:
1: traffic stop when hit bandwidth limit threshold (SBM)
0: Traffic between Bandwidth MAX , min (DBM)</td><td></td><td>0x0000</td></tr>
</table>

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Note1: Per queue bandwidth range control must set PG08.0x01[6:5] = 2'b01 if belong to Port Group A PG08.0x76[6:5] = 2'b01 if belong to Port Group B PG08.0x55~0x63 (0: enable queue bw range control 1: only bandwidth limited) For Port Group A , PG08.0x02~0x05 used as Bandwidth-min PG08.0x0A~0x0D used as Bandwidth-MAX For Port Group B , PG08.0x79~0x7C used as Bandwidth-min PG08.0x81~0x84 used as Bandwidth-MAX Note2: If MAX < min, min BW will not be assured. It only show BW limited at MAX value		
0x56 ~ 0x63	P03 ~ P29 queue based SBM (static bandwidth management / DBM (Dynamic bandwidth management) select Bit[7:0] : Pn Q7~Q0 SBM /DBM select (1: SBM 0: DBM) Bit[15:8] : Pn+1 Q7~Q0 SBM /DBM select	R/W	0x0000
0x64	Queue DBM (Dynamic Bandwidth management) enable Bit[15:0]: mg_oq_bw_range_en P16 ~ P01	R/W	0x0000
0x65	Queue DBM (Dynamic Bandwidth management) enable Bit[12:0]: mg_oq_bw_range_en P29~P17	R/W	0x0000
0x66	Out queue aging time Bit[7:0]: Out queue aging time =(1~2)* value* 100 ms Bit[8] : fast aging enable (unit = 1.638 ms) Bit[10:9] : Out queue latency timing unit (Delay Bound mode) 0: 16 us/ 64us / 1024 us (Giga/100/10) 1 : 64 us 2: 256 us 3: 1024 us Bit[13:11] : SRP macro slot period threshold (unit 250us) 000 : 250 us 001 : 500 us 010 : 1 ms 011 : 2 ms 100 : 4 ms 101/110/111 : 8 ms Bit[14]: mg_oq_latency_en (rdma pause/drop on instantly when out queue port WRED pause) Bit[15] : mg_oq_bw_min_resol (ref PG08.0x66[15]) for queue *(0: Per Queue BW control normal burst mode)* *(1 & PG08.0xB1[7]=0: Per Queue BW control min burst mode)* *(1 & PG08.0xB1[7]=1: Per Queue BW control leaky bucket mode)* *Note: Token Bucket BW control Per queue can be implemented from bandwidth range enable and set PG08.0x66[15] = 1, PG08.0xB1[7]=1 (Max bandwidth will be the token size)*	R/W	0x0000
0x67	P02~01 Out queue aging enable Bit[7:0] : P01 Q7~Q0 queue aging enable	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[15:8] : P02 Q7~Q0 queue aging enable		
0x68 ~ 0x75	P03 ~ P29 Out queue aging enable Bit[7:0] : Pxx Q7~Q0 queue aging enable Bit[15:8] : Pxy Q7~Q0 queue aging enable	R/W	0x0000
0x76	Port Group B Out queue schedule mode Bit[2:0] : Schedule mode 0 : First come First schedule 1 : WRR/WFQ/BW/TWRR 2 : SPx1 + WRR/WFQ/BW/TWRR x7 3 : SPx2 + WRR/WFQ/BW/TWRR x6 4 : SPx4 + WRR/WFQ/BW/TWRR x4 5 : SPx8 6 : LLQx1 + WFQ/BW/TWRR x7 (LLQ in WRR will switch to SP) 7 : LLQx2 + WFQ/BW/TWRR x6 (LLQ in WRR will switch to SP) Bit[4:3] : BW throttle period sel / TWRR tickle unit 00 : 64 kbit/s / 51.2 ms 01: 1 Mbit/s / 3.19 ms 10 : 2 Mbit/s / 1.55 ms 11: 4 Mbit/s / 0.82 ms Bit[6:5] : Queue method(00: WRR 01: BW 10: WFQ 11: TWRR) Bit[7] : Delay Bound mode (Q7/Q6/Q5/Q4/Q3/Q2/Q1) (Q0 queue out only when Q7~Q1 is empty) must set bit[12:11] = 10, at the same time Bit[8] : Q0 BE(best effort) queue disable (only bit[13] = 1) (Q0 is also delay bound queue if disable BE) Bit[9] : Port Group B schedule mode setting enable 0: set as Group A 1: set as Group B (PG08.0x01[8:0]) (PG08.0x76[8:0])	R/W	0x0000
0x77	Out queue Port Group A/B selection Bit[15:0] : Port 16 ~ Port01 Group A/B select 1: Group B 0 : Group A	R/W	0x4688
0x78	Out queue Port Group A/B selection Bit[12:0] : Port 29 ~ Port17 Group A/B select 1: Group B 0 : Group A	R/W	0x4688
0x79	Port Group B Out queue schedule ratio 0 Bit[7:0] : Q0 weight / bandwidth allocate / Bit[15:8] : Q1 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x7A	Port Group B Out queue schedule ratio 1 Bit[7:0] : Q2 weight / bandwidth allocate / Bit[15:8] : Q3 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit	R/W	0x0000
0x7B	Port Group B Out queue schedule ratio 2 Bit[7:0] : Q4 weight / bandwidth allocate / Bit[15:8] : Q5 weight / bandwidth allocate /	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	(value =0 : weight 128 /unlimited bandwidth / queue in prohibit		
0x7C	Port Group B Out queue schedule ratio 3 Bit[7:0] : Q6 weight / bandwidth allocate / Bit[15:8] : Q7 weight / bandwidth allocate / (value =0 : weight 128 /unlimited bandwidth / queue in prohibit *Note 1: if 0x61 SRP parameter is setup with value > 0 ,* *Q7 BW = mg_oq_wan_ratio3[15:8]x 64 Bytes/ slot time* *Q6 BW = mg_oq_wan_ratio3[7:0] x 64 Bytes / slot time* *Note 2: The WAN port max BW (if port SRP parameter > 0)* *Q7 BW = mg_oq_wan_max_bw3[15:8]x 64 Bytes/ slot time* *Q6 BW = mg_oq_wan_max_bw3[7:0] x 64 Bytes / slot time*	R/W	0x0000
0x7D	Port Group B Out queue 0 latency threshold Bit[7:0] : Q0 latency threshold Bit[15:8] : Q1 latency threshold	R/W	0x4080
0x7E	Port Group B Out queue 1 latency threshold Bit[7:0] : Q2 latency threshold Bit[15:8] : Q3 latency threshold	R/W	0x1020
0x7F	Port Group B Out queue 2 latency threshold Bit[7:0] : Q4 latency threshold Bit[15:8] : Q5 latency threshold	R/W	0x0408
0x80	Port Group B Out queue 3 latency threshold Bit[7:0] : Q6 latency threshold Bit[15:8] : Q7 latency threshold	R/W	0x0102
0x81	Port Group B Out queue Max Bandwidth Bit[7:0] : Q0 max bandwidth Bit[15:8] : Q1 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x82	Port Group B Out queue Max Bandwidth Bit[7:0] : Q2 max bandwidth Bit[15:8] : Q3 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x83	Port Group B Out queue Max Bandwidth Bit[7:0] : Q4 max bandwidth Bit[15:8] : Q5 max bandwidth (value =0 : unlimited)	R/W	0x0000
0x84	Port Group B Out queue Max Bandwidth Bit[7:0] : Q6 max bandwidth Bit[15:8] : Q7 max bandwidth (value =0 : unlimited) *Ethernet AV setup:* *The WAN port max BW (if port SRP parameter > 0)* *Q7 BW = mg_oq_wan_max_bw3[15:8]x 64 Bytes/ slot time*	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Q6 BW = mg_oq_wan_max_bw3[7:0] x 64 Bytes / slot time		
0x85	Egress Rate control for port 1 bit[13:0] : Output Rate control Bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2nd bucket token rate) (PIR : peak information rate : 1st bucket token rate)	R/W	0x0000
0x86 ~ 0xA1	Egress Rate control for port 2 ~ port 29 bit[13:0] : Output Rate control Bit[15:14] : 00 : write Both PIR/CIR 01 : write PIR 10 : read CIR 11 : read PIR (CIR : committed information rate : 2nd bucket token rate) (PIR : peak information rate : 1st bucket token rate)	R/W	0x0000
0xA2	Port 01/02 Out queue rate control setting Bit[7:0] : P01 Q7~Q0, disable egress rate calculation. Bit[15:8] : P02 Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count, then Q7 take the (100% - 75%) Bandwidth.	R/W	0x0001
0xA3 ~ 0xAF	Port 03~P28 queue rate control setting Bit[7:0] : Pxx Q7~Q0, disable egress rate calculation. Bit[15:8] : Pxy Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count, then Q7 take the (100% - 75%) Bandwidth.	R/W	0x0001
0xB0	Port29 queue rate control setting Bit[7:0] : P29 Q7~Q0, disable egress rate calculation. (ex: if WFQ mode, set Q6~Q0 has 75% bandwidth take into egress rate count, then Q7 take the (100% - 75%) Bandwidth. (ex: if BW mode, set Q3~Q0 has total 25 % bandwidth take into egress rate Count, and Q7~Q4 total can use 75 %, and per Queue can setup SBM/DBM separately.	R/W	0x0001
0xB1	Out queue parameter setup Bit[3:0]: 2nd bucket size[3:0] (leaky bucket size) 4'b0000: 4 KB 4'b0001: 8 KB 4'b0010: 16 KB 4'b0011: 32 KB 4'b0100: 64 KB 4'b0101: 128 KB 4'b0110: 256 KB 4'b0111: 512 KB 4'b1000: 1024 KB 4'b1001: 2 KB 4'b1010: 1 KB	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	4'b1011: 512 B 4'b1100: 256 B 4'b1101: 128 B 4'b1110: 64 B 4'b1111: 32 B The max. output bytes no. in one period time = Rate control configure value x 64k bps (4096 Bytes / 500 ms)(512 Bytes / 62.5 ms) Bit[6:4]: Bandwidth period 3'b000: (4096 Bytes / 500 ms) 3'b001: (2048 Bytes / 250 ms) 3'b010: (1024 Bytes / 125 ms) 3'b011: (512 Bytes / 62.5 ms) 3'b100: (256 Bytes / 31.25 ms) 3'b101: (128 Bytes / 15.625 ms) 3'b110: (64 Bytes / 7.8125 ms) 3'b111: (32 Bytes / 3.90625 ms) The max. output bytes no. in one period time = Rate control configure value x 64k bps (4096 Bytes / 500 ms)(512 Bytes / 62.5 ms) Bit[7]: Out queue rate-jitter regulator enable for egress rate ctrl (**Leaky Bucket Method** 0: dis 1:en**)** 0 : Egress rate control using periodically Burst mode 1 : Egress rate control using leaky bucket mode bit[8]: egress rate control trigger pause / drop enable (0 :shaping traffic 1: policing traffic) Bit[9]: Out queue rate-jitter regulator enable burst mode for egress rate control (**Token Bucket method** 0: dis 1:en) Bit[10]: enable per queue pause / drop for BW mode (if PG08.0xB1[11:10] =10, enable depend on PG08.0x55~0x63 if PG08.0xB1[11:10] =11, all queue is enable, regardless 0x55~63 Bit[11]: enable out queue BW / WFQ pause / drop (BW / WFQ throttle) Bit[13:12]: TWRR Tickle unit type 00 : fixed Giga (51.2ms /3.19ms /1.55ms /0.82ms) 01 : fixed 100M (512ms /31.9ms /15.5ms /8.2ms) 10 : fixed 10 M (5120ms /319ms /155ms /82ms) 11 : Bit time (51.2 /3.19 /1.55 /0.82)x10^6 bit time Bit[14] : Out queue congest condition (1: port based 0: queue based) Bit[15] : Queue bandwidth bytes cnt keep residue at Bw-assured mode (precise BW for jumbo packet)		
0xB2	TX queue mapping from TX "Port priority" Bit[15:0]: mg_oq_wlan_pri_en P16 ~ P01	R/W	0x0000
0xB3	TX queue mapping from TX "Port priority" Bit[12:0]: mg_oq_wlan_pri_en P29 ~ P17	R/W	0x0000

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Priority remapping : TX priority remapping (PG08.0xB2~0xB3 > PG08.0x14 ~ 0x4D) >> RX priority remapping (PG06.0x24~0x5D) >> ACL DSCP remark addr / VLAN Table Remark pri (PG06.0x17 ~ 0x1A)		
0xB4	Bit[2:0]: Out queue rate control rate jitter enable burst mode **burst size (1st Token Bucket size)**. 0 : 4 KB 1 : 16 KB 2 : 32 KB 3 : 64 KB 4 : 128 KB 5 : 256 KB 6 : 512 KB 7 : 1024 KB Bit[3]: WRED TAIL DROP (1:Enable 0:Disable) Bit[4]: WRED IP ECN enable WRED notify explicit congestion notification in IP header. (Rule: ip packet , hit WRED drop , ECN bit = 01/10) Bit[5]: WRED mode 1 enable (drop instantly without oq_rd_holb_cnt) Bit[6] : WRED normal en (WRED enable ignore Delay bound weighted amount setting) Bit[7] : WRED HEAD DROP (1:Enable 0:Disable) Bit[8] : Out queue aging priority 0: Normal packet > Aging out packet (send normal first , aging packet still in queue , Use more Buffer) 1: Aging out packet > normal packet (stop TX and switch to aging, affect TX rate , less buffer used)	R/W	0x00F0
0xB5	P1 ~ P24 Out queue pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0040
0xB6	P1 ~ P24 Out queue pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0080
0xB7	P25 ~ P28 Out queue pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0040
0xB8	P25 ~ P28 Out queue pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0080
0xB9	P29 Out queue pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0040
0xBA	P29 Out queue pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0080
0xBB	Out queue Q0 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xBC	Out queue Q0 pause off threshold setting	R/W	0x0040

Output Queue Register : Page 0x08			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[10:0] : out queue pause off threshold		
0xBD	Out queue Q1 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xBE	Out queue Q1 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xBF	Out queue Q2 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xC0	Out queue Q2 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xC1	Out queue Q3 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xC2	Out queue Q3 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xC3	Out queue Q4 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xC4	Out queue Q4 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xC5	Out queue Q5 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xC6	Out queue Q5 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xC7	Out queue Q6 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xC8	Out queue Q6 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xC9	Out queue Q7 pause on threshold setting Bit[10:0] : out queue pause on threshold	R/W	0x0020
0xCA	Out queue Q7 pause off threshold setting Bit[10:0] : out queue pause off threshold	R/W	0x0040
0xCB	Reserved		0x0000
0xCC	Reserved		0x0000
0xCD	Reserved		0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.12 PTP Control Register

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x00	PTP clock reset bit Bit[0] : 1: clear the PTP clock reference register configuration to default reg.0x10 reg.0x11 reg.0x12 reg.0x13 reg.0x14 reg.0x15 reg.0x16 reg.0x17 0: no action	SC	0x0000
0x01	PTP time stamps read command Bit[3:0] : time stamp address Bit[4] : ingress/egress index 1 : egress time stamps 0 : ingress time stamps Bit[9:5] : port index ,from 0x00~ 0x1D (p01~p29 and event) Bit[11:10] : do not care Bit[12] : data register (0x0B/0x0C/0x0D/0x0E) read indication 1 : read back data is the data you last written in 0 : the read back data is time stamp data or current PTP time Bit[13] : NC Bit[14] : NC Bit[15] : command trigger 1 : issue a command 0 : idle	R/W	0x0000
0x02	PTP general configuration register Bit[0] : Enable the PTP clock 1: Enable the PTP real time clock 0: Disable the PTP real time clock Bit[1] : MAC PTP stamp buffer overwrite enable 1: write buffers from 0 to 15 in circles 0: no more write when buffers full Bit[2] : Programmable output enable 1: Enable the output of programmable clock 0: Disable the output Bit[3] :EVENT input trigger positive edge detection 1: Enable positive edge detection 0: Disable positive edge detection Bit[4] :EVENT input trigger falling edge detection 1: Enable falling edge detection 0: Disable Falling edge detection Bit[5] : EVENT PTP stamp buffer overwrite enable 1: write buffers from 0 to 7 in circles 0: no more write when buffers full Bit[6]: PTP Trigger Out Function Enable 1: Enable PTP trigger out function	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	0: Disable PTP trigger out function Bit[7]: PTP Trigger Out "Type" Selection 1: Period 0: Pulse Bit[8]: PTP Trigger Out "High Duration" Setting 1: Multiple Cycles (refers to 0x18 register, bit[15:8]) 0: One Cycle Bit[10:9]: PTP Pulse Per Second Pin (ptp_pps) source selection 0: PTP Pulse Per Second (ptp_pps) 1: PTP programming output clock (reference: 0x02[2]) 2: PTP Trigger output clock 3: Reserve		
0x03	PTP port time stamp enable Bit[0] : p01 ingress time stamp enable Bit[1] : p01 egress time stamp enable Bit[2] : p02 ingress time stamp enable Bit[3] : p02 egress time stamp enable Bit[4] : p03 ingress time stamp enable Bit[5] : p03 egress time stamp enable Bit[6] : p04 ingress time stamp enable Bit[7] : p04 egress time stamp enable Bit[8] : p05 ingress time stamp enable Bit[9] : p05 egress time stamp enable Bit[10] : p06 ingress time stamp enable Bit[11] : p06 egress time stamp enable Bit[12] : p07 ingress time stamp enable Bit[13] : p07 egress time stamp enable Bit[14] : p08 ingress time stamp enable 1 : Enable,0 : Disable Bit[15] : p08 egress time stamp enable 1 : Enable,0 : Disable	R/W	0x0000
0x04	Port 16~port 9 PTP time stamp enable Bit[15:0] : (same definition with register 0x03, except port 16~ port 9)	R/W	0x0000
0x05	Port 24~port 17 PTP time stamp enable Bit[15:0] : (same definition with register 0x03, except Port 24~port 17)	R/W	0x0000
0x06	EVENT and Port 29~port 25 PTP time stamp enable Bit[9:0] : (same definition with register 0x03, except Port 29~port 25) Bit[10] : EVENT input time stamp enable	R/W	0x0000
0x07	PTP time stamp clear register Bit[0] : p01 ingress stamp counter/full notification clear Bit[1] : p01 egress stamp counter/full notification clear Bit[2] : p02 ingress stamp counter/full notification clear Bit[3] : p02 egress stamp counter/full notification clear Bit[4] : p03 ingress stamp counter/full notification clear	SC	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[5] : p03 egress stamp counter/full notification clear Bit[6] : p04 ingress stamp counter/full notification clear Bit[7] : p04 egress stamp counter/full notification clear Bit[8] : p05 ingress stamp counter/full notification clear Bit[9] : p05 egress stamp counter/full notification clear Bit[10] : p06 ingress stamp counter/full notification clear Bit[11] : p06 egress stamp counter/full notification clear Bit[12] : p07 ingress stamp counter/full notification clear Bit[13] : p07 egress stamp counter/full notification clear Bit[14] : p08 ingress stamp counter/full notification clear 1 : clear to zero,0 : no action Bit[15] : p08 egress stamp counter/full notification clear 1 : clear to zero,0 : no action		
0x08	Port 16~port 9 PTP time stamp clear register Bit[15:0] : (same definition with register 0x07, except port 16~ port 9)	SC	0x0000
0x09	Port 24~port 17 PTP time stamp clear register Bit[15:0] : (same definition with register 0x07, except port 24~ port 17)	SC	0x0000
0x0A	EVENT and Port 29~port 25 PTP time stamp clear register Bit[9:0] : (same definition with register 0x07, except Port 29~port 25) Bit[10] : EVENT input time stamp clear	SC	0x0000
0x0B	PTP time data for nano-second Bit[15:0] : nano-second[15:0]	R/W	0x0000
0x0C	PTP time data for nano-second Bit[13:0] : nano-second[29:16]	R/W	0x0000
0x0D	PTP time data for second Bit[15:0] : second[15:0]	R/W	0x0000
0x0E	PTP time data for second Bit[15:0] : second[31:16]	R/W	0x0000
0x0F	PTP clock control register Bit[0] : command trigger 1: issue a command 0: idle Bit[2:1] : 00 : read back the current PTP clock into register 0x0B~0x0E 01 : Set the PTP time date 0x0B~0x0E to current PTP clock 10 : Add the PTP time date 0x0B~0x0E to current PTP clock 11 : Sub the PTP time date 0x0B~0x0E from current PTP clock Note! The register bit 0x01[12] should be “0” for reading back the current clock from 0x0B~0x0E	R/W SC	0x0000
0x10	PTP frequency addend value configuration Set the PTP real time clock divided from source (125MHz) Bit[15:0] : addend value for the frequency compensation [15:0]	R/W	0x0000
0x11	PTP frequency addend value configuration Set the PTP real time clock divided from source (125MHz)	R/W	0x8000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[15:0] : addend value for the frequency compensation [31:16] Note : (a) This value is calculated as follows : If PTP real time clock is 62.5MHz, value = 62.5MHz/125MHz * 2^32 = 32'h8000_0000 If PTP real time clock is 20MHz, value = 20MHz/125MHz * 2^32 = 32'h28F5_C28F (b) The default value is 32'h8000_0000 (62.5MHz) modification is not recommend		
0x12	PTP clock period register The period of PTP real time clock set Bit[15:0] : 16bits clock period in nano-second Note : (a) The default clock period is 16ns, modification is not recommend (b) this register should be derived from register 0x10 and 0x11	R/W	0x0010
0x13	PTP frequency compensation configuration based on reg.0x10 and 0x11 Bit[15:0] : the frequency compensation value [15:0]	R/W	0x0000
0x14	PTP frequency compensation configuration based on reg.0x10 and 0x11 Bit[9:0] : the frequency compensation value [25:16] Example (a) If 200ppm is needed for PTP clock Then the frequency compensation bit[25:0] = 200ppm*addend value = 32'h8000_0000*200ppm = 26'h68db8 Example (b) If PTP clock should modify 150ns in 50ms duration, then you should set Then the frequency compensation bit[25:0] = 150ns/50ms * addend value = 26'h192A	R/W	0x0000
0x15	PTP frequency compensation duration in numbers of PTP clock cycles Bit[15:0] : duration in numbers of PTP clock cycles [15:0]	R/W	0x0000
0x16	PTP frequency compensation duration in numbers of PTP clock cycles Bit[9:0] : duration in numbers of PTP clock cycles [25:16] Note : This register takes actively only when reg.0x17[1]=1, and the clock cycle is based PTP period defined in reg.0x10 and 0x11	R/W	0x0000
0x17	PTP frequency compensation control register Bit[0] : command trigger	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	1: frequency correction enable 0: Disable Bit[1] : 1 : use the rate duration set in registers 0x15 and 0x16 0 : always correction Bit[2] : 1 : frequency sub 0 : frequency add		
0x18	PTP programmable output configuration Bit[7:0] : the “low” duration in numbers of PTP clock cycles Bit[15:8] : the “high” duration in numbers of PTP clock cycles Note : This register takes actively only when reg.0x02[2]=1 and the clock cycle is based PTP period defined in reg.0x10 and 0x11	R/W	0x0000
0x19	PTP interrupt indication enable when a frame has been time stamped Bit[0] : p01 ingress time stamp interrupt enable Bit[1] : p01 egress time stamp interrupt enable Bit[2] : p02 ingress time stamp interrupt enable Bit[3] : p02 egress time stamp interrupt enable Bit[4] : p03 ingress time stamp interrupt enable Bit[5] : p03 egress time stamp interrupt enable Bit[6] : p04 ingress time stamp interrupt enable Bit[7] : p04 egress time stamp interrupt enable Bit[8] : p05 ingress time stamp interrupt enable Bit[9] : p05 egress time stamp interrupt enable Bit[10] : p06 ingress time stamp interrupt enable Bit[11] : p06 egress time stamp interrupt enable Bit[12] : p07 ingress time stamp interrupt enable Bit[13] : p07 egress time stamp interrupt enable Bit[14] : port 08 ingress time stamp interrupt enable 1: Enable 0: Disable Bit[15] : port 08 egress time stamp interrupt enable 1: Enable 0: Disable	R/W	0x0000
0x1A	Port 16~port 9 PTP time stamp interrupt enable Bit[15:0] : (same definition with register 0x19, except port 16~ port 9)	R/W	0x0000
0x1B	Port 24~port 17 PTP time stamp interrupt enable Bit[15:0] : (same definition with register 0x19, except port 24~ port 17)	R/W	0x0000
0x1C	EVENT and Port 29~port 25 PTP time stamp interrupt enable Bit[9:0] : (same definition with register 0x19, except Port 29~port 25) Bit[10] : EVENT input time stamp interrupt enable	R/W	0x0000
0x1D	PTP time stamp status register Bit[0] : p01 stamp status for ingress 1: notify a time stamp has been write into buffer 0: no time stamp wrote after last buffer read Bit[1] : p01 stamp status for egress	RO	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	1: notify a time stamp has been write into buffer 0: no time stamp wrote after last buffer read Bit[2] : p02 stamp status for ingress Bit[3] : p02 stamp status for egress Bit[4] : p03 stamp status for ingress Bit[5] : p03 stamp status for egress Bit[6] : p04 stamp status for ingress Bit[7] : p04 stamp status for egress Bit[8] : p05 stamp status for ingress Bit[9] : p05 stamp status for egress Bit[10] : p06 stamp status for ingress Bit[11] : p06 stamp status for egress Bit[12] : p07 stamp status for ingress Bit[13] : p07 stamp status for egress Bit[14] : p08 stamp status for ingress Bit[15] : p08 stamp status for egress Note : the status is cleared when any of the correspond buffers has been read		
0x1E	Port 16~port 9 PTP time stamp status register Bit[15:0] : (same definition with register 0x1D, except port 16~ port 9)	RO	0x0000
0x1F	Port 24~port 17 PTP time stamp status register Bit[15:0] : (same definition with register 0x1D, except port 24~ port 17)	RO	0x0000
0x20	EVENT and Port 29~port 25 PTP time stamp status register Bit[9:0] : (same definition with register 0x1D, except Port 29~port 25) Bit[10] : EVENT input time stamp status register	RO	0x0000
0x21	P25 PTP ingress latency correction Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x22	P26 PTP ingress latency correction Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x23	P27 PTP ingress latency correction Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x24	P28 PTP ingress latency correction Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x25	P29 PTP ingress latency correction Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	R/W	0x0000
0x26	P25 PTP egress latency correction Bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x27	P26 PTP egress latency correction Bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x28	P27 PTP egress latency correction Bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x29	P28 PTP egress latency correction Bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x2A	P29 PTP egress latency correction Bit[15:0] : correct the egress time by adding the latency correction (ns)	R/W	0x0000
0x2B	10M TP ingress latency correction (embedded PHY) Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0564
0x2C	100M TP ingress latency correction (embedded PHY) Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0140
0x2D	100M Fiber ingress latency correction (embedded PHY) Bit[15:0] : correct the ingress time by subtracting the latency correction (ns)	RO	0x0128
0x2E	10M TP egress latency correction (embedded PHY) Bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0474
0x2E	100M TP egress latency correction (embedded PHY) Bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0088
0x2F	100M TP egress latency correction (embedded PHY) Bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0088
0x30	100M Fiber egress latency correction (embedded PHY) Bit[15:0] : correct the egress time by adding the latency correction (ns)	RO	0x0088
0x31	PTP Specific Time Trigger Out data for nano-second Bit [15:0]: nano-second [15:0]	R/W	0x0000
0x32	PTP Specific Time Trigger Out data for nano-second Bit [15:0]: nano-second[29:16]	R/W	0x0000
0x33	PTP Specific Time Trigger Out data for second Bit[15:0] : second[15:0]	R/W	0x0000
0x34	PTP Specific Time Trigger Out data for second Bit[15:0] : second[31:16]	R/W	0x0000
0x35	PTP Specific Time Trigger Out Period Setting Bit[15:0]: Period Value Setting[31:16]	R/W	0x0000
0x36	PTP Specific Time Trigger Out Period Setting. (Unit: RTC Rate) Bit[15:0]: Period Value Setting[15:0] [Example] : The value is calculated as follows: If PTP real time clock is 62.5MHz (where Reg0x11: 0x8000), the 125us period should be setting as : 0x1e84 = 125us / 16ns Note : ● PTP Specific Time Trigger out Period Value == 0x0000h indicates disable the period function. ● PTP Specific Time Trigger out Period Value must large than “high	R/W	0x0000

PTP Register : Page 0x09			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	duration cycles (0x18 register, bit[15:8])"; otherwise, it will be disable the period function.		
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

6.13 IRMP Control Register

IRMP Register : Page 0x0A			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	IRMP operation Bit[8:0] : The period of IRMP time out, the unit is “second” If no IRMP command is received in (bit[8:0]~bit[8:0]+1)sec., a granted port will be released and send out a goodbye frame (Default value is 0x12C, 300sec) Bit[11:9] : (Reserved) Bit[12] : password is needed 1 : The IRMP should check password (default) 0 : no password needed Bit[13] : The IRMP power abnormal indication enable 1 : when switch detects the power level is under threshold, a last gasp frame is send out by granted port (default) 0 : No power detection function Bit[14] : IRMP topology function enable 1 : Enable (default) 0 : Disable Bit[15] : Destination Address is limited to switch MAC address. 1 : IRMP check the DA of frame with the switch MAC address only 0 : IRMP check the DA of frame with switch MAC address and broadcast address (default)	R/W	0x712C
0x02	IRMP function enable for p16~p1, 1 bit per port Bit[0] : IRMP function enable for p01 1 : IRMP enable (default) 0 : IRMP disable Bit[15:1] : IRMP function enable for p16~p02 The same definition with bit[0]	R/W	0xFFFF
0x03	IRMP function enable for p29~p17, 1 bit per port Bit[12:0] : IRMP function enable for p29~p17 The same definition with register 0x01	R/W	0x1FFF
0x04	IRMP ether-type definition Bit[15:0] : The ether-type definition of IRMP (default : 16’h0806)	R/W	0x8931
0x05	IRMP sub-type definition Bit[15:0] : The sub-type definition of IRMP (default : 16’hFFFE)	R/W	0xFFFE
0x06	Vender ID [15:0] Bit[15:0] : The vender identifier [15:0] (default : 0xC300)	R/W	0xC300
0x07	Vender ID [31:16] Bit[15:0] : The vender identifier [31:16] (default : 0x0090)	R/W	0x0090
0x08	Device ID and Version Bit[3:0] : The IRMP version control (default : 4’h0) Bit[15:4] : The device identifier [11:0] (default : 12’h829)	R/W	0x8290

IRMP Register : Page 0x0A			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x09	IRMP Password [15:0] Bit[15:0] : The IRMP password [15:0] (default : 16'h0000)	R/W	0x0000
0x0A	IRMP password [31:16] Bit[15:0] : The IRMP password [31:16] (default : 16'h0000)	R/W	0x0000
0x0B	IRMP connect ID Bit[15:0] : The random ID generated for each connection	RO	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

Note : The IRMP operation flow, please refer to IRMP application note.

6.14 Advance EEPROM code Register

Advance EEPROM code Register : Page 0x0B			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x01	advance EEPROM operation Bit[0] : The advance EEPROM function enable 1 : Enable 0 : Disable (default) Bit[1] : The advance EEPROM code start point bit[16] (MSB) (refer to register 0x02) Bit[2] : action code hold 1 : hold the command for debugging 0 : normal processing command code (default) bit[3] : action code trigger again 1 : re-start the action code from start address 0 : normal (default) Bit[15:4]: (Reserved)	R/W	0x0000
0x02	The advance EEPROM code start bit[15:0] Bit[15:0] : start point Note : Four EEPROM bytes to form a command code, The code begin at EEPROM address is {start point [16:0], 2'b00} Note : MSB bit[16] is defined in 0x01[1]	R/W	0x0000
0x03	Data buffer 0 for advance EEPROM code Bit[15:0] : buffer_0	RO	0x0000
0x04 ~ 0x0A	Data buffer 1~data buffer 7 for advance EEPROM code Bit[15:0] : buffer	RO	0x0000
0x0B	operation temporary 0 for advance EEPROM code Bit[15:0] : temp_0	RO	0x0000
0x0C ~ 0x0E	operation temporary 1~3 for advance EEPROM code Bit[15:0] : temp_1~3	RO	0x0000
0x0F	Logic result of advance EEPROM code bit[3:0] : logic temporary bit[3:0] 1 : true 0 : false Bit[4] : The final result after command : result check 1 : true 0 : false	RO	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

Note : The advance EEPROM operation flow, please refer to Advance_EEPROM_code application note.

6.15 45B45B45B45B45BMISC Register

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x00	Switch software reset Bit[0] : 1: reset the switch of IP1829, all parameters are maintained 0: no action Bit[4] : 1: reset the switch of IP1829, all parameters are reset to default 0: no action	SC	0x0000
0x01	BIST Enable and reset mask set Bit[0] : Software reset mask for BIST complete Bit[1] : Software reset mask for buffer over-/under-flow Bit[2] : Software reset mask for output queue critical event Bit[3] : Software reset mask for share management Bit[4] : Software reset mask for output queue overflow Bit[5] : Frame buffer ECC enable Bit[6] :MIB memory block BIST enable 1 : Enable BIST 0 : Disable BIST Bit[7] :LUT memory block BIST enable Bit[8] :Source List memory block BIST enable Bit[9] :Multicast Table block BIST enable Bit[10] :VLAN memory block BIST enable Bit[11] :Buffer management memory block BIST enable Bit[12] : (reserved) Bit[13] :Frame buffer memory block BIST enable Bit[14] :Output queue memory block BIST enable Bit[15] :PTP memory block BIST enable Note : some memory blocks share the same BIST enable bit	R/W	0xFFE0
0x02	Build in self test information Bit[3:0] : MIBs 4 Blocks BIST result 1 : OK 0 : Fail Bit[4] : LUT BIST result Bit[5] : Source List BIST result Bit[6] : Multicast table BIST result Bit[7] : VLAN BIST result Bit[8] : Buffer management BIST result Bit[9] : Frame buffer BIST result Bit[10] : Output queue BIST result Bit[11] : PTP BIST result Bit[12] : LUT memory is under BIST 1 : BIST is going 0 : BIST finish Bit[13] : VLAN /Multicast memory is under BIST Bit[14] : Output queue memory is under BIST Bit[15] : Frame Buffer is under BIST	RO	0x3FFF

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
0x03	Switch input/output pin configuration Bit[0] : p29 is connected to CPU indication 1: connect to CPU 0: normal port Bit[1] : p29 special tag function enable when P29 is CPU port (bit[0]=1) 1 : enable 0: disable Bit[2] : RGMII pads internal LDO power output disable 1: Power down the LDO output 0: LDO power output normally Bit[3] : CPU I/F mode setting 1: serial mode 0: SPI mode Bit[4] : p25 MII PHY mode enable Bit[5] : p26 MII PHY mode enable Bit[6] : p27 MII PHY mode enable Bit[7] : p28 MII PHY mode enable Bit[8] : p29 MII PHY mode enable 1 : MII clocks is provided by IP1829 0 : MII clocks is provided by external device Bit[9] : p25 turbo MII enable Bit[10] : p26 turbo MII enable Bit[11] : p27 turbo MII enable Bit[12] : p28 turbo MII enable Bit[13] : p29 turbo MII enable 1 : enable turbo MII (MII TX/RX clock is set to 50MHz) 0 : disable turbo MII (MII TX/RX clock is 25/2.5MHz) Bit[14] : (reserved, should be “0”) Bit[15] : Direct LED mode 1 : direct LED output 0 : serial LED output	R/W	0x0108
0x04	Special TAG Type/Len setting Bit[15:0]: special tag type/length item	R/W	0x9126
0x05	Interrupt output configuration Bit[0] : interrupt enable for CPU read/write SMI done Bit[1] : interrupt enable for link status change Bit[2] : interrupt enable for link operation mode change Bit[3] : interrupt enable for CPU read/write EEPROM done Bit[4] : interrupt enable for last gasp Bit[5] : interrupt enable for PTP Bit[6] : interrupt enable for loop detection Bit[7] : interrupt enable for critical event	R/W	0x0B02

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	1: interrupt enable 0: Disable Bit[13:8] : interrupt pulse period when bit[14]=1, Pulse period = (bit[13:8]+1) x 8ns Bit[14] : interrupt trigger type 1: pulse trigger 0: level trigger (read and clear) Bit[15] : Interrupt is action high 1: high active 0: low active		
0x06	Interrupt status Bit[0] : interrupt notification for CPU read/write SMI done Bit[1] : interrupt notification for link status change Bit[2] : interrupt notification for link operation mode change Bit[3] : interrupt notification for CPU read/write EEPROM done Bit[4] : interrupt notification for last gasp Bit[5] : interrupt notification for PTP Bit[6] : interrupt notification for loop detection Bit[7] : interrupt notification for critical event 1: interrupt occurred 0: normal	RO RC	0x0000
0x07	Last gasp configuration Bit[0] : last gasp detect enable 1: Enable 0:Disable Bit[1] : last gasp detect method 1: detect high 0: detect low Bit[2] : critical event detect enable 1: Enable 0:Disable Bit[3] : critical event detect method 1: detect high 0: detect low Bit[4] : switch fast test mode enable (for test only) 1: Enable 0: Disable Bit[5] : reserved Bit[7:6] : Output pad driving current set [2:1] (EEPROM/LED/CPU) 00 : 4mA 01 : 8mA (default) 10 : 18mA 11 : 28mA Bit[9:8] : output pad slew rate set [2:1] (EEPROM/LED/CPU) 00 : default Bit[12:10] : MDC/MDIO pad driving current set 000 : 4mA 001 : 6mA 010 : 8mA 011 : 12mA (default) 100 : 18mA 101 : 22mA 110 : 28mA 111 : 34mA Bit[15:13] : MDC/MDIO pad slew rate set 000 : default		0x0C80
0x08	I/O configuration 0 Bit[2:0] : p27 Rx. path input delay set (0~7ns)	R/W	0x0C00

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Default : 000 Bit[5:3] : p27 Tx. Path output delay set (0~7ns) Default : 000 Bit[8:6] : p27 GMII/MII/RGMII output driving current set Default : 011 Bit[11:9] : p27 GMII/MII/RGMII output driving slew set Default : 000 Bit[12] : CPU watch dog reset disable 0 : enable reset from CPU (default) 1 : disable Bit[13] : CPU clock source selection bit 0 : internal PLL (default) 1 : clock source from AFE		
0x09	I/O configuration 1 Bit[2:0] : p28 Rx. path input delay set (0~7ns) Default : 000 Bit[5:3] : p28 Tx. Path output delay set (0~7ns) Default : 000 Bit[8:6] : p28 GMII/MII/RGMII output driving current set Default : 011 Bit[11:9] : p28 GMII/MII/RGMII output driving slew set Default : 000	R/W	0x0C00
0x0A	I/O configuration 2 Bit[2:0] : p29 Rx. path input delay set (0~7ns) Default : 000 Bit[5:3] : p29 Tx. Path output delay set (0~7ns) Default : 000 Bit[8:6] : p29 GMII/MII/RGMII output driving current set Default : 011 Bit[11:9] : p29 GMII/MII/RGMII output driving slew set Default : 000	R/W	0x0C00
0x0B	Port 16 ~port 1 Fiber mode set 0 Bit[14:0] : p15~p01 fiber mode enable Bit[15] : p16 fiber mode enable 1: fiber mode 0: TP mode	R/W	0x0000
0x0C	Port 24 ~port 17 Fiber mode set 0 Bit[7:0] : p24~p17 fiber mode enable 1: fiber mode 0: TP mode Bit[8] : p25's operation status 1: fiber path(Serdes) 0: TP path(SGMII) Bit[9] : p26's operation status 1: fiber path(Serdes) 0: TP path(SGMII)	R/W RO RO	0x0000
0x0D	CPU read/write EEPROM command Bit [7:0] : Byte Address Bit [10:0] : Device Address Bit[12:11] :(reserved) Bit[13] : do not care Bit[14] : read/write operation	R/W	0x0000

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	0 : read operation 1 : write operation Bit[15] : the read/write command trigger 0 : idle or command complete 1 : start command When reading bit[15] : command complete indication 0 : command not complete 1 : command complete		
0x0E	CPU read/write EEPROM command Bit [7:0] : High Byte Address Bit [11:10] : EEPROM force mode after initial read procedure 0: as initial Auto-detect 1: Force 24C32~24C4096 2: Force 24C01 ~ 24C16 3: unused Bit[14:12] : EEPROM clock period 000: 3200 ns 001: 2400 ns 01x: 1600 ns 1xx: 800 ns Bit [15] : restart EEPROM initial read procedure Note: use for **24c32 ~ 24C4096** EEPROM address {00h, 01h} = 0x290D : command mode EEPROM address {00h, 01h} = 0x290C : data mode Note: use for **24c01 ~ 24C16** EEPROM address {00h, 01h} = 0x290B : command mode EEPROM address {00h, 01h} = 0x290A : data mode	R/W	0x0000
0x0F	CPU read/write EEPROM command data Bit [7:0] : in read command – the read back data in write command – data want to write Bit[9:8] : Unused Bit[11:10]: size mode selection Bit[14:12]: EEPROM initial Read command mode area size Size_mode = 0 1xx : 1Kbit (ROM addr : 0x00000 ~ 0x0007F) 011 : 2Kbit (ROM addr : 0x00000 ~ 0x000FF) 010 : 4Kbit (ROM addr : 0x00000 ~ 0x001FF) 001 : 8Kbit (ROM addr : 0x00000 ~ 0x003FF) 000 : 16Kbit (ROM addr : 0x00000 ~ 0x007FF) Size_mode = 1 1xx : 16Kbit (ROM addr : 0x00000 ~ 0x007FF) 011 : 32Kbit (ROM addr : 0x00000 ~ 0x00FFF) 010 : 64Kbit (ROM addr : 0x00000 ~ 0x01FFF) 001 : 128Kbit (ROM addr : 0x00000 ~ 0x03FFF) 000 : 256Kbit (ROM addr : 0x00000 ~ 0x07FFF) Size_mode = 2/3 1xx : 256Kbit (ROM addr : 0x00000 ~ 0x07FFF) 011 : 512Kbit (ROM addr : 0x00000 ~ 0x0FFFF) 010 : 1024Kbit (ROM addr : 0x00000 ~ 0x1FFFF) 001 : 2048Kbit (ROM addr : 0x00000 ~ 0x3FFFF) 000 : 4096Kbit (ROM addr : 0x00000 ~ 0x7FFFF)	R/W	0x0000

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	Bit[15] : unused (EEPROM read stop criteria : (a) STOP sign or (b) Read out configured Area size)		
0x10	FX/SGMII path operation mode setting Bit[0] : p25 auto path selection 0: manual set (see bit[1]) 1: using fiber signal detect (SD) to determine data path Bit[1] : p25 data path selection 0: Fiber path (SGMII/100Base-FX/1000Base-X, see bit[2]) 1: TP path (connect external PHY with SGMII) Bit[2] : Fiber path SGMII mode enable 0: 100Base-FX/1000Base-X (refer to the Serdes PHY registers) 1: SGMII (see bit[3]) Bit[3] : PHY mode or MAC mode of SGMII I/F 0: SGMII-MAC mode 1: SGMII-PHY mode (see bit[6:4]) Bit[5:4] : SGMII-PHY speed selection 10: 1000Mbs 01: 100Mbs 00: 10Mbs Bit[6] : SGMII-PHY duplex mode 0: half duplex 1: full duplex Bit[7] : (reserved) Bit[8] : p26 auto path selection 0: manual set (see bit[9]) 1: using fiber signal detect (SD) to determine data path Bit[9] : p25 data path selection 0: Fiber path (SGMII/100Base-FX/1000Base-X, see bit[10]) 1: TP path (connect external PHY with SGMII) Bit[10] : Fiber path SGMII mode enable 0: 100Base-FX/1000Base-X 1: SGMII (see bit[11]) Bit[11] : PHY mode or MAC mode of SGMII I/F 0: SGMII-MAC mode 1: SGMII-PHY mode (see bit[13:12]) Bit[13:12] : SGMII-PHY speed selection 10: 1000Mbs 01: 100Mbs 00: 10Mbs Bit[14] : SGMII-PHY duplex mode 0: half duplex 1: full duplex	R/W	0x6161
0x11	IEEE802.3az TX clock silence enable Bit[0] : p25 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[1] : p25 MII TXC clock silence enable	R/W	0x0000

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	1 : enable clock off during LPI 0:disable Bit[2] : p26 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[3] : p26 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[4] : p27 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[5] : p27 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[6] : p28 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[7] : p28 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[8] : p29 GMII/RGMII GTXC clock silence enable 1 : enable clock off during LPI 0:disable Bit[9] : p29 MII TXC clock silence enable 1 : enable clock off during LPI 0:disable		
0x12	CPU 's PLL configuration 0 Bit[15:0] : the configuration bit [15:0] for DDR3 PLL & CPU PLL	RW	0x0000
0x13	CPU 's PLL configuration 1 Bit[15:0] : the configuration bit [31:16] for DDR3 PLL & CPU PLL	RW	0x0000
0x20	eFuse Command register Bit[6:0] : The eFuse access address Bit[9:7] : reserved Bit[10] : eFuse initial read operation trigger again (SC) 1 : read all eFuse data and set switch again (Note : all other bits should be "0") 0 : Idle (default) Bit[11] : eFuse program enable (SC) 1 : eFuse programmable 0 : eFuse can not be programmed (default) Bit[12] : When read eFuse data register (0x21) 1 : data(reg. 0x21) is the last wrote into data register 0 : data(reg. 0x21) is the read back data from eFuse (default) Bit[13] : NC Bit[14] : command operation mode (SC) 1 : write command to eFuse 0 : read command to eFuse (default) Bit[15] : eFuse read/write command issue trigger (SC)/ 1 : issue a command to eFuse 0 : No action (default) When read, command complete indication (RO) 1 : command is complete 0 : command is processing (default) ********** **Note:** Every eFuse bit can only be programmed once!!	R/W	0x0000

Misc/Syetem Register : Page 0x0C			
Reg Addr.	**Register Description**	**R/W**	**Default value**
	If the same fuse is programmed more than once, the result will become unpredictable.		
0x21	EFuse data register Bit[7:0] : The eFuse byte burn command / read back data (see 0x20[12]) 1: Burn out this fuse bit 0: Idle Bit[15:8] : reserved	R/W	0x0000
0xFF	Register Page selection [5:0] : page selection	R/W	0x0000

Note : About the eFuse data format please refer to the application note.

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	V_{DDIO}	– 0.5	+3.6V	V
	Core	V_{DDCore}	– 0.5	+2.3V	V
Input Voltage		V_I	– 0.5	$V_{DDI/O}$	V
Output Voltage		V_O	– 0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	+70	°C
IC Junction Temperature		T_J		+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

8 AC Characteristics

8.1 Power On Sequence and Reset Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{clk_lead}	X1 clock valid before reset released	10	-	-	ms
T_{rst}	Reset period	10	-	-	ms
T_{diff}	Time difference among power sources			30	ms
T_{pwr_lead}	All power source ready before reset released	11			ms

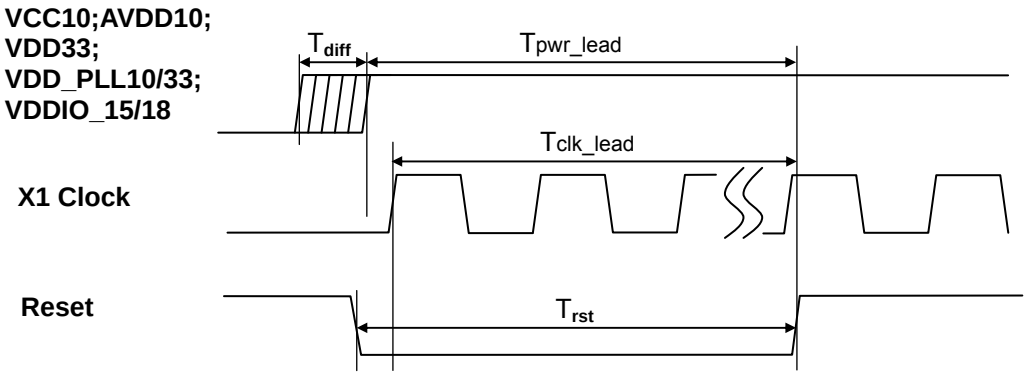
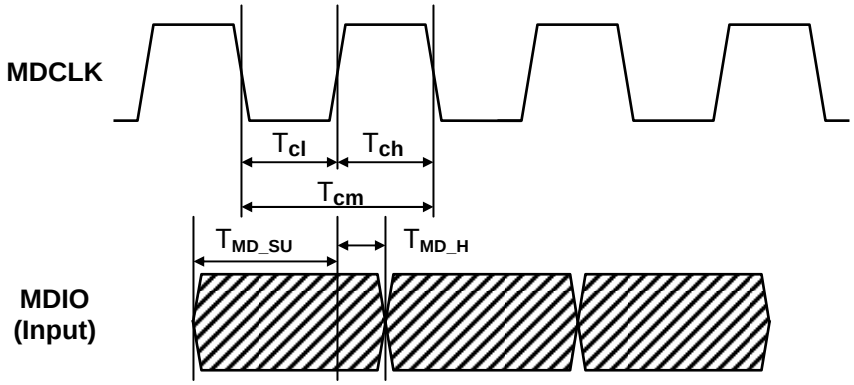


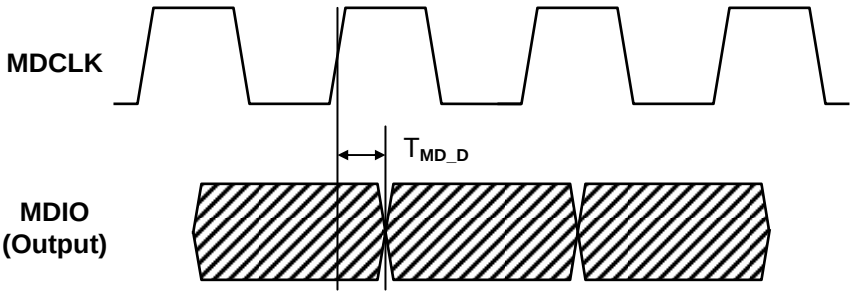
Figure 26 Power On Sequence and Reset timing Diagram

PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time	-	200	-	ns
T_{cl}	MDCK Low Time	-	200	-	ns
T_{cm}	MDCK cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-		ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns



MDIO Input Cycle

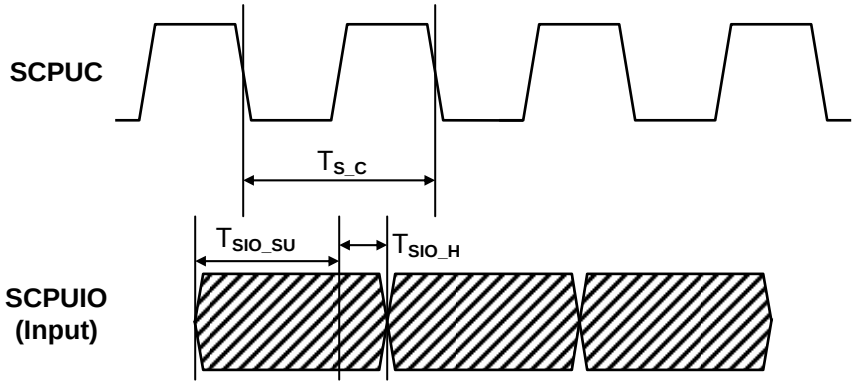


MDIO Output Cycle

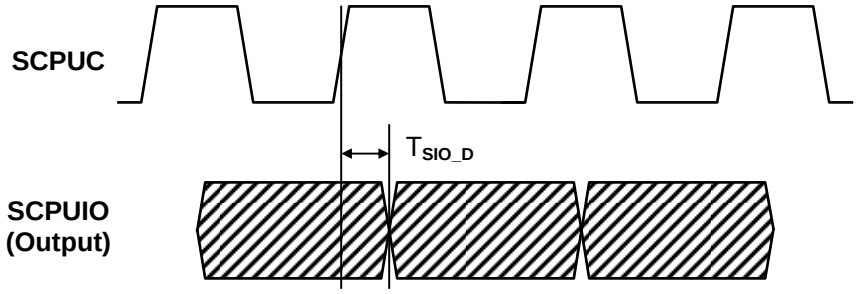
Figure 27 MDIO Read / Write cycle timing Diagram

CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{S_C}	Serial CPU Clock cycle time	400		-	ns
T_{SIO_SU}	Serial I/O set up time	10	-		ns
T_{SIO_H}	Serial I/O hold time	10	-	-	ns
T_{SIO_D}	Serial I/O output delay time		-	20	ns



Serial I/O Input Cycle

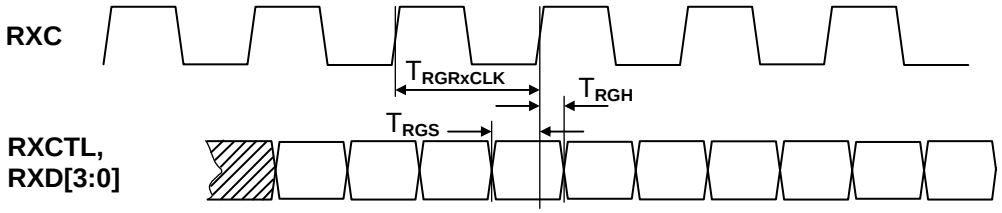


Serial I/O Output Cycle

Figure 28 CPU Serial Bus timing Diagram

RGMII Rx Part Timing

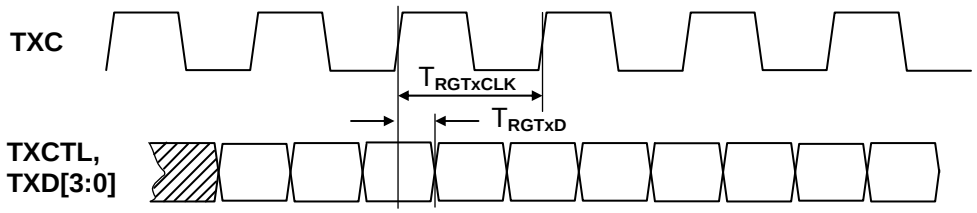
Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RGRxCLK}$	Period of receive clock in giaga mode	-	8	-	ns
	Period of transmit clock in 100M mode	-	40	-	ns
	Period of transmit clock in 10M mode	-	400	-	ns
T_{RGS}	RXCTL, RXD to RXC setup time (no clock delay added)	1			ns
	(RGMII Rx delay setting = 010)	-0.95			
T_{RGH}	RXCTL, RXD to RXC hold time (no clock delay added)	1.3			ns
	(clock delay setting = 010)	-0.95			



RGMII Receive Timing

RGMII Tx Part Timing

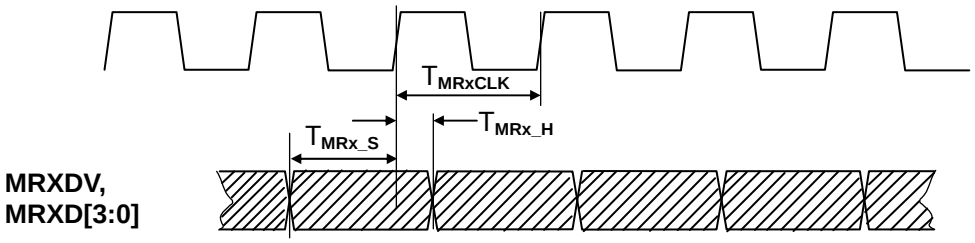
Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RGTxCLK}$	Period of transmit clock in giga mode	-	8	-	ns
	Period of transmit clock in 100M mode	-	40	-	ns
	Period of transmit clock in 10M mode	-	400	-	ns
T_{RGTxD}	TXCTL, TXD output delay from TXC edge (no clock delay added)	1.7		3.5	ns
	(clock delay setting = 111)	1.1		2.7	



RGMII Transmit Timing

MII Receive Timing

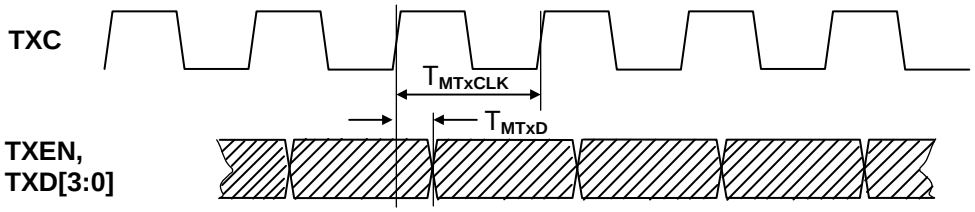
Symbol	Description	Min.	Typ.	Max.	Unit
T_{MRxCLK}	Receive clock period 100Mbps MII	-	40	-	ns
	Receive clock period 10Mbps MII	-	400	-	ns
T_{MRx_S}	RXDV, RXD to MII_RXCLK setup time	2	-	-	ns
T_{MRx_H}	RXDV, RXD to MII_RXCLK hold time	0.5	-	-	ns



MII Receive Timing

MII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{MTxCLK}	Transmit clock period 100Mbps MII	-	40	-	ns
	Transmit clock period 10Mbps MII	-	400	-	ns
T_{MTxD}	MII_TXCLK falling edge to TXEN, TXD	5	-	25	ns



MII Transmit Timing

9 DC Characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage		V_{OL}			0.1xVDD33	V
Output high voltage		V_{OH}	0.9xVDD33			V
VDD33 supply current		I_{VDD33}			0.1xVDD_IO18	mA
VCC10 supply current		I_{VCC10}	0.9xVDD_IO18			mA
AVDD10 supply current		I_{AVDD10}				mA
VDDIO_15 supply current		$I_{VDDIO15}$				mA
VDD_IO18 supply current		$I_{VDDIO18}$				mA
VDD_PLL33 supply current		$I_{VDDPLL33}$				mA
VDD_PLL10 supply current		$I_{VDDPLL10}$				mA
VDD33 supply voltage		V_{VDD33}	3.135	3.3	3.465	V
VCC10 supply voltage		V_{VCC10}	0.95	1.0	1.05	V
AVDD10 supply voltage		V_{AVDD10}	0.95	1.0	1.05	V
VDDIO_15 supply voltage		$V_{VDDVO15}$	1.425	1.5	1.575	V
VDD_IO18 supply voltage		$V_{VDDVO18}$	1.71	1.8	1.89	V
VDD_PLL33 supply voltage		$V_{VDDPLL33}$	3.135	3.3	3.465	V
VDD_PLL10 supply voltage		$V_{VDDPLL10}$	0.95	1.0	1.05	V
RESET Threshold voltage			$0.4*V_{DD33}$		$0.6*V_{DD33}$	V
X1 Input Low Voltage (3.3V operation)		V_{ILX1}			0.6	V
X1 Input High Voltage (3.3V operation)		V_{IHX1}	1.5			V
Pull-down resistor		R_{PD}	51		127	KΩ
Theremal resistor(Junction to ambient) @2 layer PCB; Air flow: 0ft/sec.		Θ_{JA}		40.5		^{O}C/W
Thermal resistor(Junction to ambient) @4 layer PCB; Air flow: 0ft/sec.		Θ_{JA}		19.3		^{O}C/W
RGMII						
Input Low to High	VDDIO =1.8V	V_{IH}	1.08		---	V
Input High to Low		V_{IL}	---		0.72	V
Input Low to High	VDDIO =2.5V	V_{IH}	1.5		---	V
Input High to Low		V_{IL}	---		1	V
MII						
Input Low to High	VDDIO =1.8V	V_{IH}	1.08		---	V
Input High to Low		V_{IL}	---		0.72	V
Input Low to High	VDDIO =2.5V	V_{IH}	1.5		---	V
Input High to Low		V_{IL}	---		1	V

Input Low to High	VDDIO =3.3V	V_{IH}	1.98		---	V
Input High to Low		V_{IL}	---		1.32	V

10 Serial Transmitter/Receiver DC characteristic

Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{OD}	Output Voltage Swing(single-ended)	200	300	400	mV **peak**
R_O	Output Impedance(single-ended)	40	50	60	Ωs

Receiver DC Characteristics

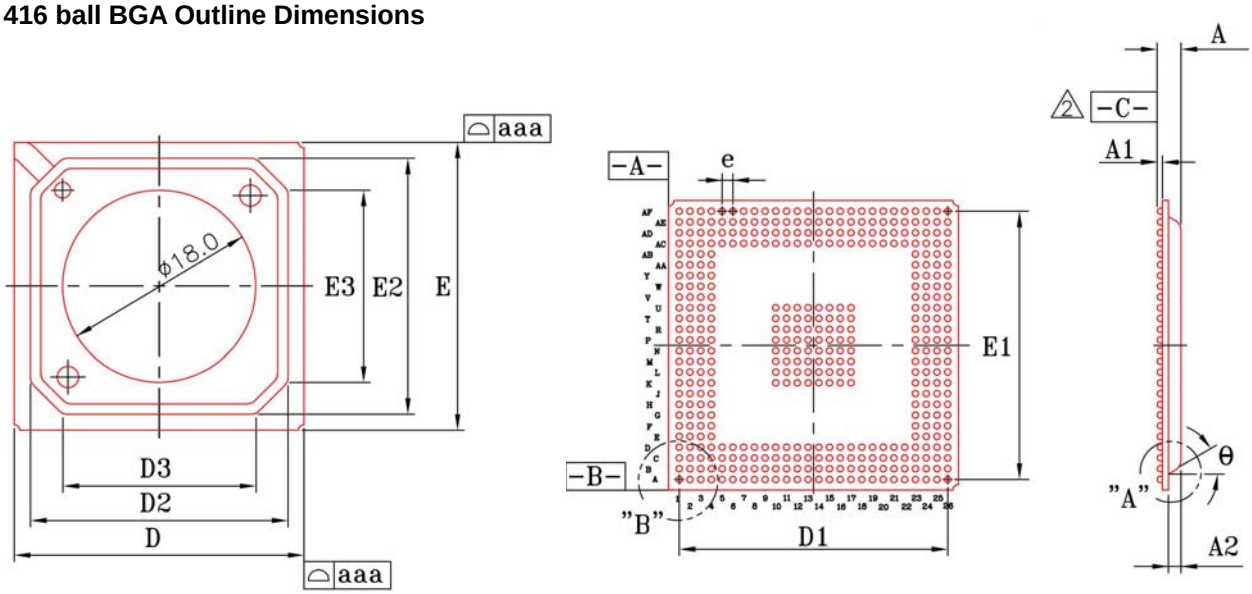
Symbol	Parameter	Min	Typ	Max	Units
V_{RCOM}	Common mode voltage(Supplied by IC itself)	0.8	1.0	1.2	V
V_{IDTH}	Input Differential Threshold	200			mV
R_{IN}	Receiver 100Ω Differential Input Impedance	80	100	120	Ω

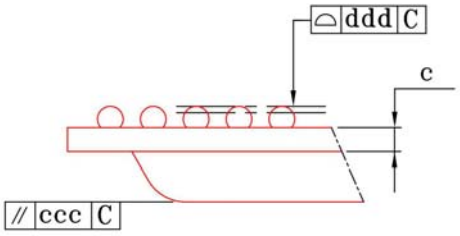
Order Information

Part No.	Package	Notice
IP1829	416-Ball BGA	-

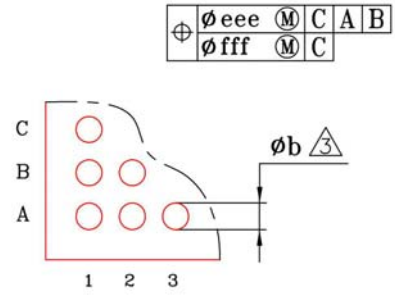
e Detail

416 ball BGA Outline Dimensions





DETAIL "A"



DETAIL "B"

Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	2.23	2.43	---	0.088	0.096
A1	0.40	0.50	0.60	0.016	0.020	0.024
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.50	0.60	0.70	0.020	0.024	0.028
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	---	25.00	---	---	0.984	---
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	---	18.00	---	---	0.709	---
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	---	25.00	---	---	0.984	---
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	---	18.00	---	---	0.709	---
e	---	1.00	---	---	0.039	---
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
θ	30° TYP			30° TYP		

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MS-034.
6. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd

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