8-Port PSE Controller for PoE Systems

Features

- IEEE 802.3AF-2003 and 802.3AT-2009 compliant
- Single DC power supply voltage input (45~57V)
- Pin Compatible with IP808
- Wide temperature range: -40℃~+85℃
- Supplies 8 independent power ports
- Built-in power FETs
- 0.1R sense embedded
- Built in Total current limit for Smart power management.
- I^2C Bus to access up to 8 x IP808AR devices
- Continuous system monitoring for every port
- Independent system parameters setting for every port
- Thermal monitoring and protection
- Built-in 3.3V regulators for external devices
- Built-in Power on Reset
- Configurations: (1) 30W x 8 ports
- Built-in LEDs control for multi-port use
- Built-in EEPROM interface for dumb application
- Low power dissipation
- Direct or Shift Overload LED
- H/W ALT_A/ALT_B mode Setting
- Package and operation temperature
  48 Pin(7mmx7mm) QFN, -40~85℃

Application

- 8 port PSE Switch
- 24 port PSE Switch

General Description

IP808AR is an 8-port PSE (Power Sourcing Equipment) controller IC for PoE (Power over Ethernet) systems. It integrates power, analog and logic circuits into a single chip, and can be used for Midspans and Endpoint PSE applications.

IP808AR meets all IEEE 802.3AF-2003 requirements, such as multi-point resistor detection, PD classification, DC Disconnect, and Back-off for Midspans. It also meets all IEEE 802.3AT-2009 requirements, such as two-event classification and supply maximum 36W per port.

IP808AR comprises internal temperature monitoring and thermal protection to protect against junction overheating. The 3.3V regulator is built-in to support external devices. Multiple IP808ARs can integrate to build an 8 x N ports PSE system, and I^2C bus uses to collect PD power status from each IP808AR to support global power managements.

Management switch host has options to communicate IP808ARs via I^2C bus for PSE management activities. Optocouplers can be implemented to provide electrical isolations between the host and IP808ARs for signal communication.

Table of Contents

List of Figures

List of Tables

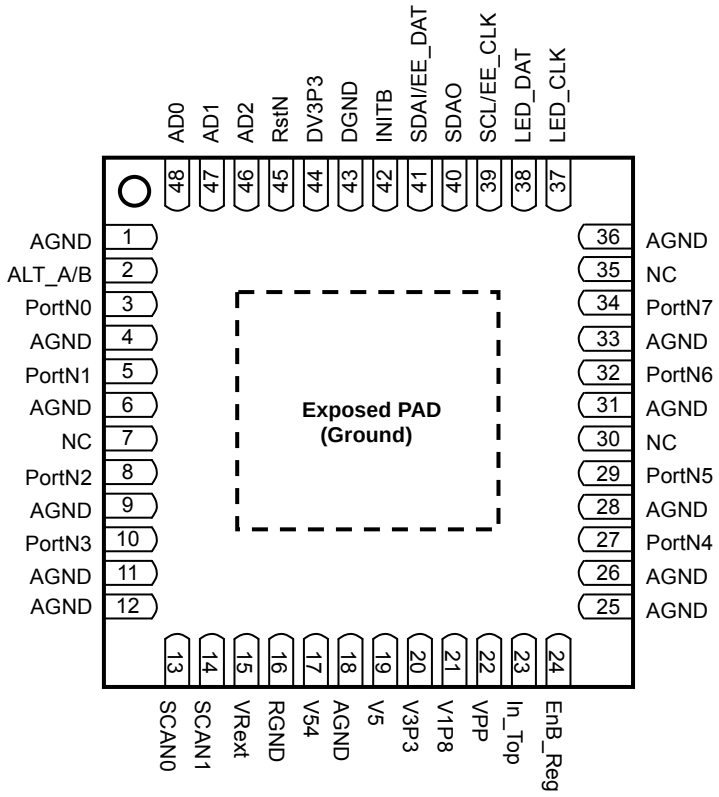
Revision History

Revision #	Date	Change Description
IP808AR-DS-Darft	2018/08/07	Initial release

1 Pin diagram

1.1 IP808AR Pin diagram (QFN48)

(7mm X 7mm Top view)



Exposed pad is system GND, must be soldered to PCB ground plane

Figure 1 IP808AR Pin Diagram

2 IP808AR application diagram

2.1 Dumb & Smart device application

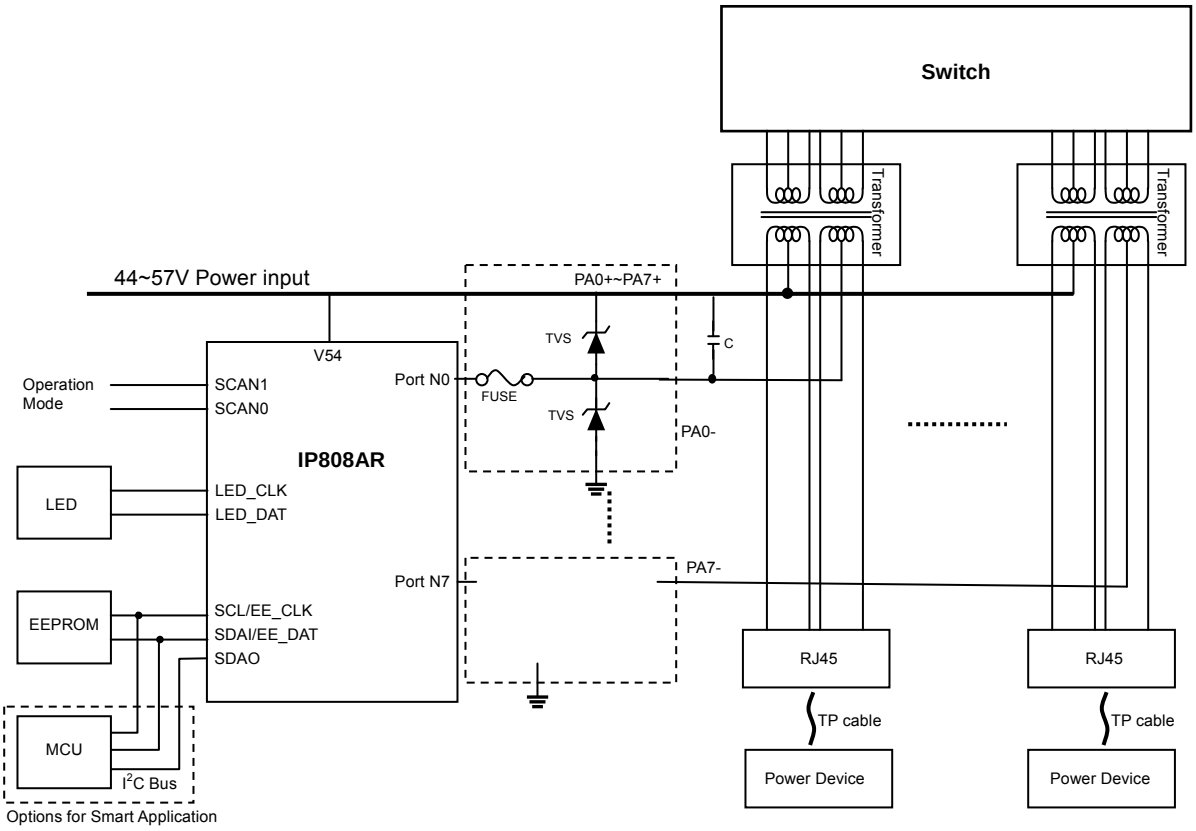


Figure 2 Application Diagram

Application	MCU	EEPROM	IP808AR Mode setting	Reference
Smart	V	X	Manual mode	Section 5.3
Dumb	X	V: update default value X: use default value	Auto mode	Section 5.4

V: necessary; X: unnecessary

3 Block diagram

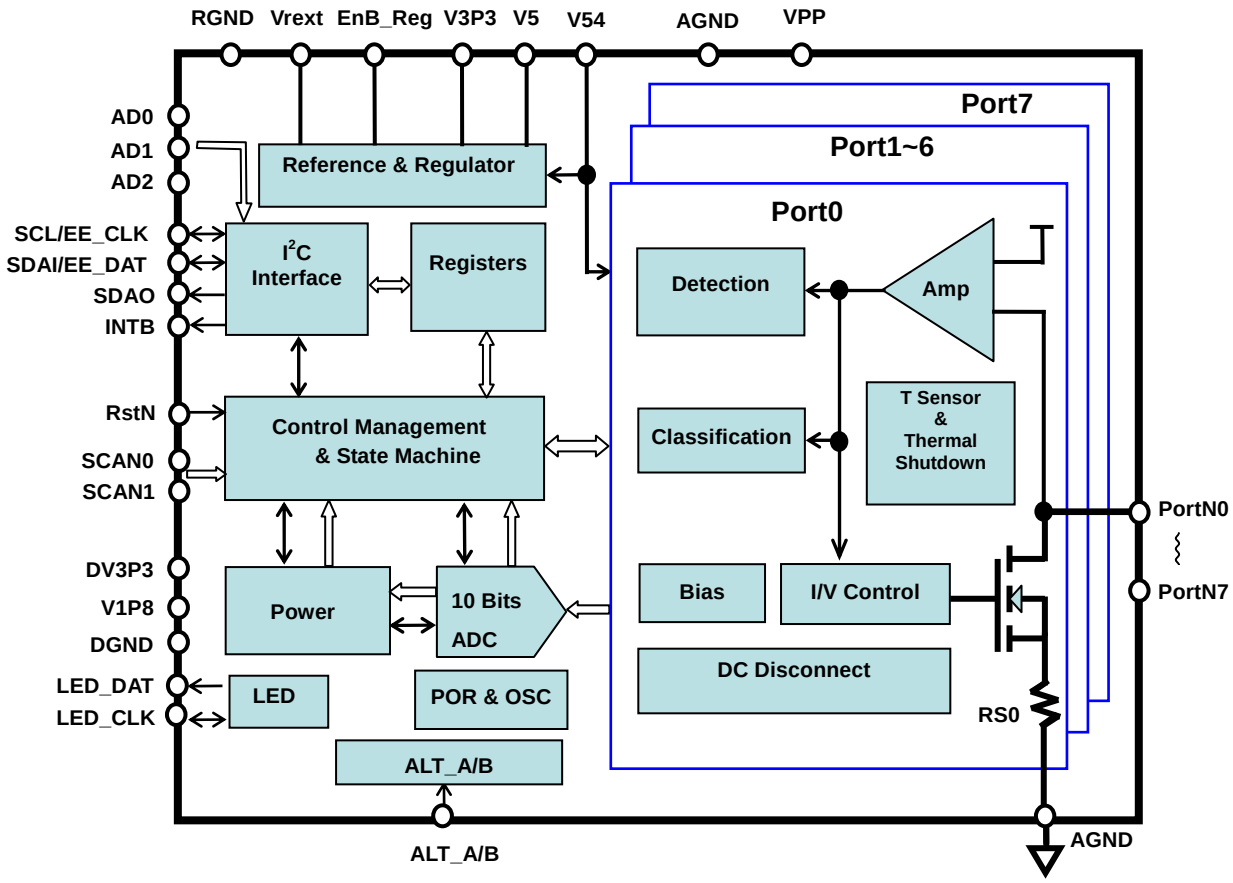


Figure 3 Block Diagram

3.1 Blocks Description

The blocks of IP808AR include global blocks for and per port blocks as below:

Global blocks for 8 ports:

- Reference & Regulator
- I²C Interface
- Registers
- Control Management & State Machine
- Power Management
- 10 Bits ADC
- POR & OSC

Per port blocks for individual port:

- Detection
- Classification
- I/V Control & Fold-back
- Amp
- DC Disconnect
- T sensor & Thermal Shutdown
- Bias
- Power MOSFET

3.1.1 Global Blocks

- **Reference & Regulator:**

The Reference & Regulator generates 1.8V, 3.3V and 5V power for internal use and 3.3V power also can supply typical 6mA current on V3P3 pin for external devices if EnB_Reg pin is connected to GND. If EnB_Reg is conncted to 3.3V, the internal 3.3V regulator is disabled and V3P3 pin should be connected to an external 3.3V power source.

It also generates 1.25V voltage on VREXT pin, which is connected to ground through an external 62KΩ resistor, to generate internal bias current.

- **Registers**:

The "Registers" provides the 8 bits data for Ilim, Icut programming registers, and all other needing registers per port

- **Control Management & State Machine:**

This block provides all the control procedures to perform PoE function. The "State Machine" implements as specified in the IEEE802.3AF/AT.

- **Power Management:**

The "Power Management" provides power management method to meet PD power requirement, or not to power PD if power is not enough.

- **10 Bits ADC:**

The 10 Bits ADC used to convert analog signals into digital bus for Control Management, State Machine, and Power Management for request.

- **POR & OSC:**

The POR generates an internal power on reset signal when V54 is power on. The POR also monitors V3P3, DV3P3, V5, & V54 voltage level. If these voltages level are below specific thresholds, a reset signal generates and resets IP808AR.

The OSC is an internal oscillator to generate 8MHz clock for IP808AR timing source.

- **I^2C Interface:**

A host (master) can communicates with multiple IP808AR (slave) via I^2C Interface (SCL/EE_CLK, SDAO, SDAI/EE_DAT) to collect PD power status to support global power managements and all control requirements.

3.1.2 Per Port Block

- **Detection:**

The IP808AR uses 4 points detection method to discover PD. It shall accepted resistance as a valid "AF/AT PD" between 19KΩand 26.5KΩ, with a paralleled capacitance small than 0.15uF.

It shall rejects resistance with paralleled capacitance as an invalid "AF/AT PD" small than 15KΩ, larger than 33KΩ, or capacitance larger than 10uF.

The specification is as specified in the IEEE802.3AF/AT.

- **Classification:**

The "Classification" is to distinguish the requested power of PD as specified in the IEEE802.3AF/AT.

In IEEE 802.3AF, classification is 1-event method.

In IEEE 802.3AT, classification is 2-event method.

- **I/V Control:**

The "I/V Control" is to control the slew rate during "detection, classification, inrush, short circuit, power off … and so on", as specified in IEEE802.3AF/AT

When short circuit event occurs, the "I/V control" will reduce the port current instantaneously to protect the power MOSFET from damages.

- **Amp:**

The "AMP" is used to convert the differential voltage between V54 and PortNx into single end voltage. This voltage will be fed into the "Detection, Classification, I/V Control" blocks to perform the IEEE8023AF/AT specifications.

- **DC Disconnect:**

The IP808AR supports DC Disconnect function according to IEEE 802.3AF-2003 & IEEE 802.3AT-2009 requirement.

This DC Disconnect continuously monitors port current after port inrush time, and disconnects port current when port current is below 7.5mA (typical) for more than 360ms (typical) .Please refer to Tmpdo in table 8 for detail information.

- **T sensor & Thermal Shutdown:**

The "T sensor" senses the temperature of each port, and will shutdown the port current as temperature beyond 150℃. When temperature goes down to 129℃, the port will start again.

- **Bias:**

The "Bias" provides the current & voltage bias for all ports according to control signals.

4 Pin description

Type	Description	Type	Description
P	Power or Ground	O	Output
I	Input	OD	Open drain
IL	Input latched upon reset	NC	No connection in internal

Table 1 Pin description

Pin no.	Label	Type	Description
	EPAD	P	Exposed pad, it should be connected to AGND.
1	AGND	P	Analog ground
2	ALT_A/B	IL	This pin is latched upon power-on reset to define the ALT_A/B Type 1: ALT_A (Default) 0 : ALT_B
3	PortN0	I	Port0 negative feeding voltage input.
4	AGND	P	Analog ground
5	PortN1	I	Port1 negative feeding voltage input.
6	AGND	P	Analog ground
7	NC	NC	No connection.
8	PortN2	I	Port2 negative feeding voltage input.
9	AGND	P	Analog ground
10	PortN3	I	Port0 negative feeding voltage input.
11	AGND	P	Analog ground
12	AGND	P	Analog ground
13	SCAN0	I	Operation mode, please refer to section 5.2 table 2 for more detail information.
14	SCAN1	I	Operation mode, please refer to section 5.2 table 2 for more detail information. It should be connected to AGND for normal operation.
15	Vrext	O	Connecting to RGND through a 62KΩ±1% resistor, it is for internal bias only.
16	RGND	P	Low noise analog reference ground, it should be connected to AGND.
17	V54	P	Main power supply input for chip The 1uF capacitor should be added between V54 and AGND.
18	AGND	P	Analog ground
19	V5	P	Internal 5V generation for internal use only. A 4.7uF capacitor should be added between V5 and AGND.
20	V3P3	P	When EnB_Reg is connected to AGND, the built-in 3.3v regulator is active, and besides IP808AR itself, V3P3 can provide 3.3v (6mA) for external device. When EnB_Reg is connected to 3.3v, V3P3 should be connected to an external power 3.3V (6mA minimum) for IP808AR. A 4.7uF capacitor should be added between V3P3 and AGND.
21	V1P8	P	Internal 1.8V for internal use only Adding an 1uF capacitor between V1P8 and AGND
22	VPP	P	Connecting to V5 for EFuse power

(Continued)

Pin no.	Label	Type	Description
23	In_Top	P	It should be connected to AGND for normal operation.
24	EnB_Reg	I	Enable/Disable the internal 3.3V regulator Please refer to pin description of V3P3.
25	AGND	P	Analog ground
26	AGND	P	Analog ground
27	PortN4	I	Port4 negative feeding voltage input.
28	AGND	P	Analog ground
29	PortN5	I	Port5 negative feeding voltage input.
30	NC	NC	No connection
31	AGND	P	Analog ground
32	PortN6	I	Port6 negative feeding voltage input.
33	AGND	P	Analog ground
34	PortN7	I	Port7 negative feeding voltage input.
35	NC	NC	No connection
36	AGND	P	Analog ground
37	LED_CLK	OD	Serial LED clock output, please refer to section 5.9 LED interface.
38	LED_DAT	OD	Serial LED data output,direct to Overload LED
39	SCL/EE_CLK	I/OD	In manual mode, this pin is I^2C clock input. In auto mode, this pin is clock out to EEPROM.
40	SDAO	OD	I^2C serial data output
41	SDAI/EE_DAT	I/OD	In manual mode, this pin is I^2C serial data input. In auto mode, this pin is data input from EEPROM.
42	INTB	OD	Interrupt output and low active
43	DGND	P	Digital ground, it should be connected to AGND.
44	DV3P3	P	Digital power 3.3V A 4.7uF capacitor should be added between DV3P3 and DGND and DV3P3 should be connected to V3P3.
45	RstN	I	It is a low active signal to reset IP808AR.
46	AD2	IL	I^2C device address bus AD2
47	AD1	IL	I^2C device address bus AD1
48	AD0	IL	I^2C device address bus AD0

5 Functional Description

5.1 System Reset

System reset occurs in either of the following conditions:

1. Reset triggered by the built-in power-on-reset circuit

IP808AR generates an internal power on reset signal when V54 is power on. It didn't leave reset state until V54 reaching V54_UVL. After reset, IP808AR still keeps on monitoring voltage level of V3P3, DV3P3, and V54. If the voltage level of V54 (V3P3) is below V54_UVL(V3P3_UVL),or over V54_OVL (V3P3_OVL), IP808AR enters reset state. Please refer to section 7.3 for detail specification of V54_UVL, and V3P3_UVL. It is note that there are two values for one parameter because of hysteresis.

2. Reset triggered by the reset pin (RstN)

3. Reset triggered by the Software

- **System Control Register @ 0x02 of Page 1**

Bit #	R/W	Default	Description
7:1	R	0	**Reserved.**
0	R/W	0	**Software Reset**. Writing 1 to this bit initiates a system reset. After system reset, this bit is automatically cleared. Writing 0 has no effects. Reading this bit always returns 0.

5.2 Operation Modes & System Configuration

IP808AR operates in four possible modes, namely the **Auto Mode**, **Manual Mode**, **Diagnostic Mode**, and **Scan Mode**. The mode in which the chip operates in is determined by the two pins **SCAN<1:0>** at system reset.

- **Auto Mode** means the chip is operating in a stand alone fashion, i.e. without the need for software intervention. The state machine does the detection, classification, power configuration, and system event monitoring automatically. The system events and status will be recorded in the corresponding registers, however, no interrupt will be generated and I^2C bus in this mode could be used.

  If there is an EEPROM, the contents of the EEPROM are loaded into the register file as initial values. Please refer to the section 5.4 for the description of the syntax of the contents of the EEPROM.

- **Manual Mode** means the chip will not be working, that is all ports are disabled, until the software has (1) enabled the port by writing 0x01 to the **Port Power Control Register**, the state machine start doing the detection, classification, power configuration, and system event monitoring as does in auto mode. The interrupt output pin will be active if the interrupt masks are turned off by software and predefined events occur. The ports can be disabled (power turned off and no further detection activity) by writing 0x00 to the **Port Power Control Register**. If the operation mode is either in manual mode or diagnostic mode, the host CPU can read register 0 (I^2C LSB Device Address Register) to make sure that IP808AR has done the system start up procedure.

- **Diagnostic Mode**, as its name suggests, is not for normal operation. It is used in field diagnosis and mass production test. In this mode, the state machine will be working in a step-by-step fashion, in which the state machine will stop at each detection, classification, and power configuration step and can be controlled by software to advance to the next step. The port current, voltage, or temperature measured by the ADC can be read in each step. Another use of diagnostic mode is to program the E-Fuse during mass production.

- **Scan Mode** is also not for normal operation. It is used to execute the scan test through the scan in, scan out, and scan enable pins. The state machine will not be working in this mode.

Mode / Pin setting	Auto Mode			Manual Mode			Diagnostic Mode	Scan Mode
	LED Master	LED Slave	LED Disable	LED Master	LED Slave	LED Disable		
SCAN0	0	0	0	1	1	1	0	1
SCAN1	0	0	0	0	0	0	1	1
AD2	1	0	X	1	0	X	X	X
LED_CLK	1	1	0	1	1	0	0	X
LED_DAT	1	1	0	1	1	0	X	X

Please refer to Section 5.10 for LED mode setting.

Table 2 Mode Setting

A summary of available functions in different modes

Function	Auto mode	Manual mode	Diagnostic mode	Reference
Auto start detection,classfiction, and power up	V	-	-	Section 5.2
Program to detection, classfiction, and power up	-	V	-	Section 5.2
Stepbystepdetection classfiction, and power up	-	-	V	Section 5.2
Access register through I^2C	-	V	V	Section 5.3
Load EEPROM	V			Section 5.4
LED master & slave	V	V	-	Section 5.10

Table 3 Available functions in Operation modes

- **System Configuration Register @ 0x01 of Page 1**

Bit #	R/W	Default	Description
7:6	R	Pin Setting	**Operation Modes**. At system reset, these bits latch the input pins **SCAN<1:0>** to determine the operation mode. 00b: Auto Mode. 01b: Manual Mode. 10b: Diagnostic Mode. 11b: Scan Mode.
5	R	0	Reserved.
4	R/W	Pin Setting	**Alternative Indicator**. At system reset, IP808AR latches the input pins **ALT_A_B** to determine the wiring alternative. However, this bit can also be set by software in manual mode or by EEPROM in auto mode. 0: Alternative A. 1: Alternative B.
3:2	R	0	Reserved.
1	R/W	0	**Suspend Power Up**. When set to 1 and the operation mode is manual mode, the state machine will be suspended before entering the power up state (thus the port will not be powered up) until the **Start Power Up** bit is set to be 1.
0	R/W	0	**Enable I^2C Checksum**. Enable I^2C checksum mechanism. Please refer to the I^2C slave interface. 0 = disable, 1 = enable.

- **Hardware Revision Registers @ 0x03~0x04 of Page 1**

Bit #	R/W	Default	Description
7:0	R	0x80	**Hardware Revision MSB.**

Bit #	R/W	Default	Description
7:0	R	0x8A	**Hardware Revision LSB.**

- **Watchdog Timer Register @ 0x05 of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Watchdog Timer Enable**. 0 = enable watchdog timer. 1 = disable watchdog timer.
6:0	R/W	0x7F	**Watchdog Timer**. When enabled, the watchdog timer starts counting down every 100mS, when the watchdog timer reaches 0, a watchdog reset will be generated to reset the whole chip.

- **Scratch Register @ 0x06 of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Scratch Register**. A scratch pad that can be written any value. The value will be reset to 0 when system reset occurs.

- **Alternative A/B Register @ 0x07 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	Pin Setting	**Alternative A/B**. At system reset, IP808AR latches the input pins **ALT_A_B** to determine the wiring alternative. However, these bits can also be set by software in manual mode or by EEPROM in auto mode. 0: Alternative A. 1: Alternative B. Bit 0 corresponds to port 0, bit 1 corresponds to port 1, and so on.

AF/AT Mode Register @ 0x25 of Page 0

Bit #	R/W	Default	Description
7:0	R/W	0xFF	**AF/AT Mode**. The 8 bits represent the AF/AT mode of the 8 ports, where bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc. 0 = AF mode. 1 = AT mode.

5.3 I²C Slave Interface

Through the I²C slave interface of IP808AR, host CPU can access the register file in IP808AR. It consists of SCL, SDAO and SDAI pins, where SCL is Clock, SDAO is Serial Data Output and SDAI is Serial Data Input. It should be note that SDAO and SDAI could be connected to implement a bidirectional data pin. This I²C interface supports the 7-bit addressing mode of the I²C standard. The clock speed can be up to 1M bit/sec.

There can be up to eight IP808AR chips on one I²C bus, the LSB 3 bits of the I²C address can be assigned with the address pin AD2~AD0. The MSB 4 bits of the I²C address are fixed at **1110b**.

The following diagram is the register read/write cycles of the I²C bus.

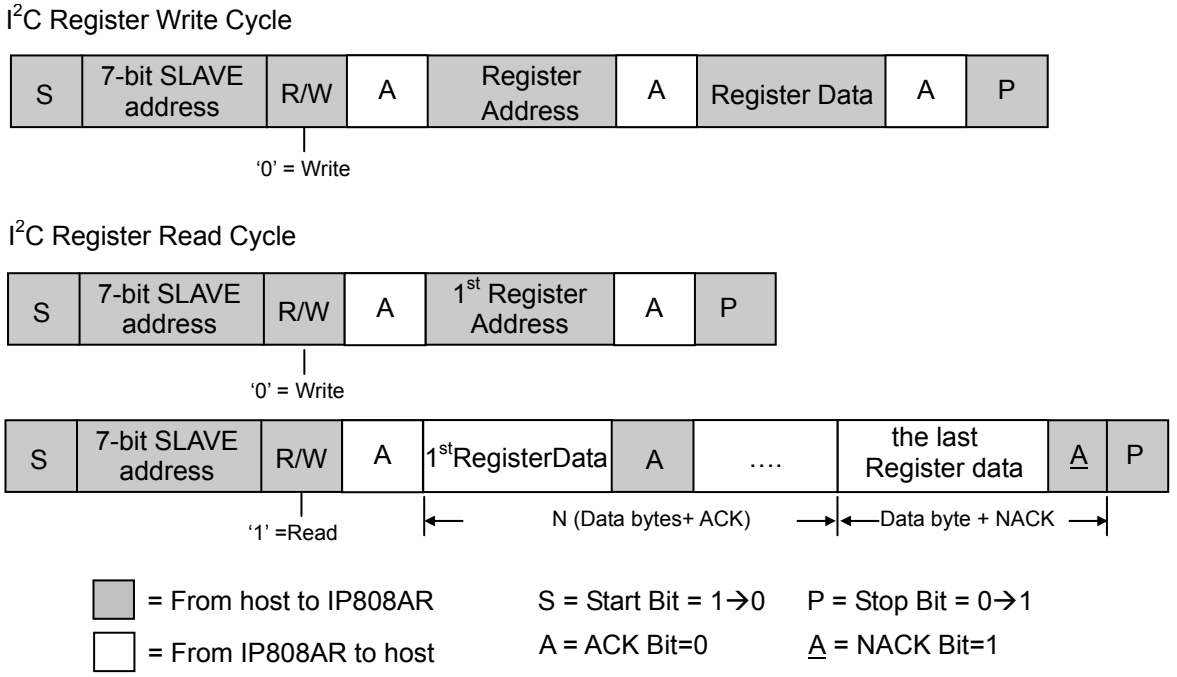


Figure 4 I²C bus read/write cycles diagram

Following the 7-bit slave address and read/write bit, the 1st data byte received by IP808AR is always interpreted as the register address to be accessed, thus named the address byte.

In a write cycle, following the address byte, there is only one byte, which contains the register data to be written. IP808AR replies an ACK to the host whenever it receives a data byte. After writing this byte, the host should terminate the write cycle by sending a STOP bit.

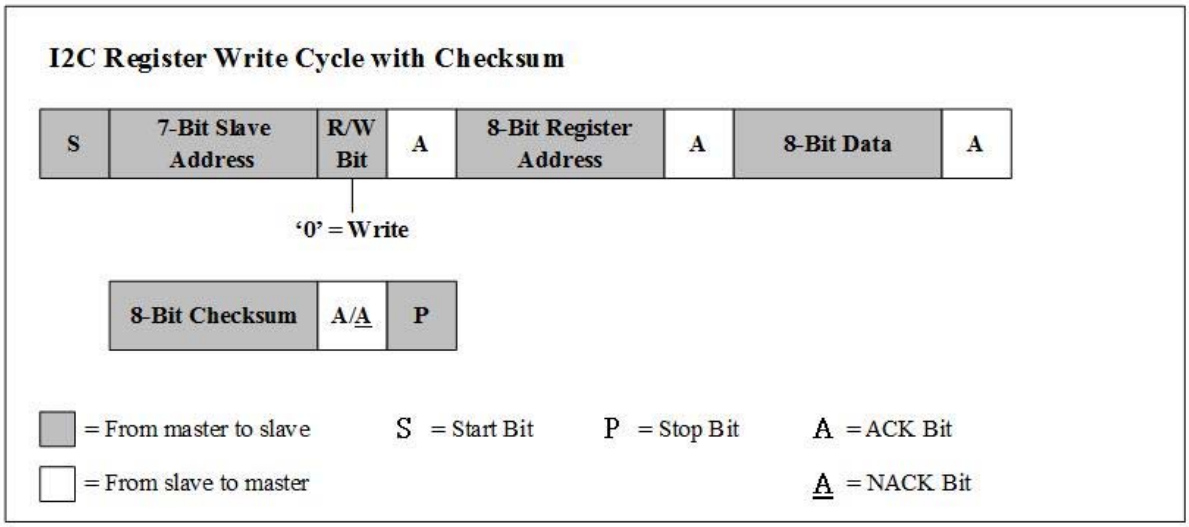
In a read cycle, the host writes only one byte, which contains the initial address of registers to be read, to the IP808AR firstly. Then the host needs to start another I²C cycle with its read/write bit set to 1. IP808AR will continue to send out the next data and increase the address by one automatically whenever the host acknowledges a data byte with an ACK, If the calculated register address is valid (within valid address range). The host can terminates a read cycle by sending a NACK following by a STOP bit. If the address of the data to be sent back falls out of valid register address range, IP808AR always returns 00h.

➢ **I²C Device Address Register @ 0x00 of Both Pages**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6	R/W	0	**Register Page**. This bit specifies the page number of the register to be accessed through the I²C interface. 0: page 0 1: page 1
5:3	R	0	Reserved.
2:0	R	000b	**I²C Device LSB Address**. Unique device address to identify this chip on the I²C bus. This address is latched in from the input pins AD2~AD0.

The highest I²C clock speed supported is 1MHz. However, in order to prevent abnormal activity on the I²C bus from hanging IP808AR, the I²C interface implements a time out mechanism. Host CPU can stop the I²C clock when it's low and resume the clock within 10ms. If the clock does not resume within 10ms, the I²C interface will abort the current I²C cycle and wait for the next START condition.

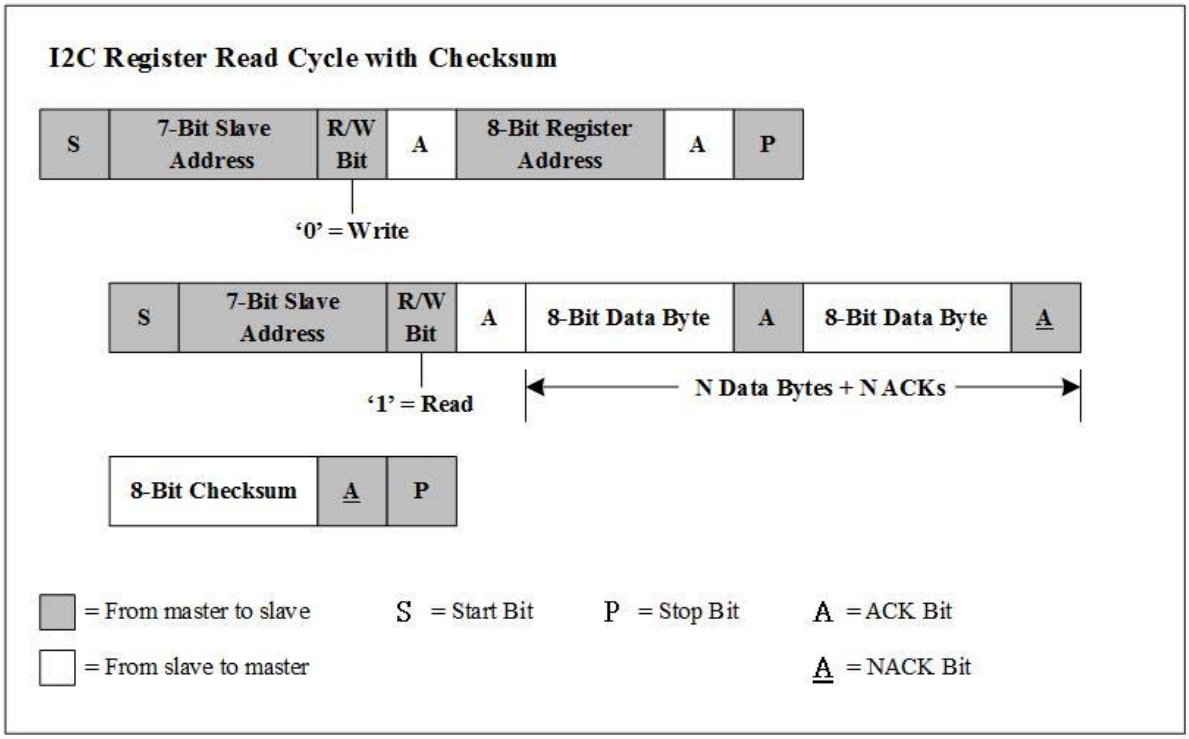
To improve reliability, the I²C slave can optionally support checksum mechanism. The I²C checksum mechanism is enabled using the **System Configuration Register**. When the checksum mechanism is enabled, checksums will be added to the I²C read/write cycles. When checksum fails in write cycle, access to the register is ignored. When checksum fails in read cycle, the data read by the I²C master should be considered corrupted. The following diagrams are the register read/write cycles of the I²C interface with checksum enabled



The 8-bit checksum for I2C write cycle is calculated as the following:

0xFF - (7-bit slave address and R/W bit + 8-bit register address + 8-bit data + carry out bits) = 8-bit checksum.

In write cycle, the IP808AR will verify the checksum bits and if the checksum fails, the data will not be written into the register and a NACK bit is sent back to the host. If the checksum succeeds, the register will be written and an ACK bit is sent back to the host.



The 8-bit checksum for I2C read cycle is calculated as the following:

0xFF - (7-bit slave address and R/W bit + 8-bit data + carry out bits) = 8-bit checksum.

When the desired data byte is read by the host, the host can send a NACK bit to IP808AR; in return, IP808AR will send out an 8-bit checksum. The host should again send a NACK bit to IP808AR and then the STOP bit. The checksum then can be used by the host to verify if the read data byte is corrupted.

5.4 EEPROM controller

When IP808AR operates in auto mode, the register file can be loaded with some initial value from external EEPROM (24xx series EEPROM, Maximum support to 24C16). IP808AR reads the EEPROM starting from address 0, parses the contents of the EEPROM command blocks, checks for integrity of the contents, and then writes the designated registers. This process continues until there is either no more data or the integrity check fails. EEPROM is necessary only if user wants to modify the default value of registers in auto mode.

The format of the EEPROM follows:

BYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Device ID (AD2~AD0)			# of Data Bytes				X
1	Starting Register Address							
2	Data Byte 1							
3	Data Byte 2							
…	…							
1 + N	Data Byte N							
2 + N	Checksum Byte							
3 + N	Next command block							

Figure 5 EEPROM Format

Where:

- **Device ID**: (AD2~AD0)=100b = Master, 000b = Slave0, 001b = Slave1, 010b = Slave2, 011b = Slave3, other values of Device ID are invalid and the EEPROM loading process will be stopped. On normal mode IP808AR doesn't check this field
- # **Of Data Bytes**: the number of data bytes in this command block. 0 = 1 byte, 1 = 2 bytes, etc.
- **Starting Register Address**: the starting register address to be loaded by the following data bytes.
- **Data Bytes**: the data bytes to be loaded in to specified registers.
- **Checksum Byte**: the checksum byte is the checksum of all previous bytes in the command block. The checksum is calculated by adding all the previous bytes with the carry bit (if any) adding back to the sum. If the checksum fails, the system start up procedure fails and the system halt.

5.5 PSE State Machine

IP808AR has eight ports and each port is mainly controlled by a state machine to perform the detection, classification, and powering up procedures. As the eight state machines run in parallel, they contend for ADC 1 in the detection and classification procedures. Thus an arbiter is needed to grant the access rights among the eight state machines.

Furthermore, to limit the chip inrush current, a maximum of two ports are allowed to start their classification procedures simultaneously. And only one port is allowed to turn on power at a time. After successful detection, classification, and power configuration, the port power is turned on.

The state machine is also designed to respond to abnormal power events, such as overload, short circuit, and overheat (thermal shutdown); basically port power will be turned off when such event happens. It takes time to cool off the device after power is turned off, so the state machine will delay a certain amount of time before starting next detection procedure for the port. The above mentioned programmable amount of time is set in the **Error Delay Register**.

- **Port 0~7 Power Control Registers @ 0x98~0x9F of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Enable Power Up Suspended Interrupt.** When the state machine is suspended before entering the power up state and this bit is 1, an interrupt will be issued.
6:2	R	0x0	**Reserved**
1:0	R/W	0x0	**PSE Enable.** **00b = PSE port disabled**. The port is disabled, port power is turned off, and the PSE state machine returns to the IDLE state. **01b = PSE port enabled**. The port is enabled, and the PSE state machine starts the detection process if the port is not in error condition and the **Start State Machine** bit in the **State Machine Control Register** is set to be 1. **10b = PSE port force power on**. The port is forced to turn power on without going through the normal detection, classification, and power configuration processes. This is used for testing purpose, not for normal operation. **11b = PSE port enabled (skip detection process)**. The port is enabled, and the PSE state machine skips the detection process and starts the classification process directly. This is only used for testing purpose and not for normal operation.

- **Port 0~7 State Machine Control Registers @ 0x90~0x97 of Page 1**

Bit #	R/W	Default	Description
7	R	0	**Power Up Suspended.** When in manual mode and when the **Suspend Power Up** bit is set, the state machine will be suspended before entering the power up state. At which time, this bit will be set to 1 by hardware. When the state machine is re-started by setting the **Start Power Up** bit, this bit will be cleared automatically by hardware.
6	R/W	0	**Step State Machine**. When in diagnostic mode, writing 1 to this bit will advance the state machine to the next state, after which this bit will be cleared by hardware. Writing 0 has no effect. Note that not every state can be stepped; Basically, only those states directly related to the detection and classification procedures can be stepped.

Bit #	R/W	Default	Description
5	R/W	0	**Start Power Up**. When in manual mode and when the **Suspend Power Up** bit is set, the state machine will be suspended before entering the power up state. Writing a 1 to this bit will re-start the state machine to enter the power up state. After entering the power up state, this bit will be cleared by hardware.
4:0	R	0	**Current State of the State Machine.** Current state of the state machine. 0 = DISABLED 1 = TEST_MODE 2 = TEST_ERROR 3 = IDLE 4 = START_DETECTION 5 = DETECT_EVAL 6 = SINATURE_INVALID 7 = BACKOFF 8 = START_CLASSIFICATION (AF Mode) 1-EVENT_CLASS (AT Mode) 9 = CLASS_EV1 (AT Mode) 10 = MARK_EV1 (AT Mode) 11 = CLASS_EV2 (AT Mode) 12 = MARK_EV2 (AT Mode) 13 = CLASSIFICATION_EVAL 14 = POWER_DENIED 15 = POWER_UP 16 = POWER_ON 19 = ERROR_DELAY 20 = PWRUP_SUSPENDED

- **Port 0~7 Detected Signature Registers @ 0x68~0x6F of Page 0**

Bit #	R/W	Default	Description
7:3	R	0x0	Reserved.
1:0	R	0	**Detected Signature**. 00b = R_{BAD}. 01b = R_{GOOD}.

- **Port 0~7 Invalid Signature Event Registers @ 0xDC of Page 1**

Bit #	R/W	Default	Description
7:0	R/W0C	0	**Invalid Signature Event** In manual or diagnostic mode, write 0 to clear the bit. Writing 1 to this bit has no effect. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

- **Port 0~3 Classification Event Number Registers @ 0xA0 of Page 1**

Bit #	R/W	Default	Description
7:6	R/W	2	**Number of Classification Events for Port 3**. Valid value range is from 0 to 2. The value 3 will be regarded as 2. If the value is 0, no classification is executed, and the PD is always deemed class 0 device. This register can be written to by host CPU. However, according to IEEE802.3 standard, if the port is in AF mode, only one classification event is executed, and in AT mode, there will be two classification events. So, this register will be automatically updated when the AF/AT Mode Register is updated.

Bit #	R/W	Default	Description
5:4	R/W	2	**Number of Classification Events for Port 2**.
3:2	R/W	2	**Number of Classification Events for Port 1**.
1:0	R/W	2	**Number of Classification Events for Port 0**.

Port 4~7 Classification Event Number Registers @ 0xA1 of Page 1

Bit #	R/W	Default	Description
7:6	R/W	2	**Number of Classification Events for Port 7**.
5:4	R/W	2	**Number of Classification Events for Port 6**.
3:2	R/W	2	**Number of Classification Events for Port 5**.
1:0	R/W	2	**Number of Classification Events for Port 4**.

PSE Skip Event 2 Register @ 0xA2 of Page 1

Bit #	R/W	Default	Description
7:0	R/W	0xFF	**Skip the Second Classification Event.** Bit 0 corresponds to port 0, bit 1 corresponds to port 1, etc. 0 = do not skip event 2 in AT mode 1 = skip event 2 in AT mode

- **Port 0~1 Detected PD Class Registers @ 0x88 of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:4	R	5	**Detected PD Class of Port 1**. 0 = Class 0 1 = Class 1 2 = Class 2 3 = Class 3 4 = Class 4 5 = Unknown
3	R	0	Reserved.
2:0	R	5	**Detected PD Class of Port 0.**

- **Port 2~3 Detected PD Class Registers @ 0x89 of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:4	R	5	**Detected PD Class of Port 3**.
3	R	0	Reserved.
2:0	R	5	**Detected PD Class of Port 2.**

- **Port 4~5 Detected PD Class Registers @ 0x8A of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:4	R	5	**Detected PD Class of Port 5**.
3	R	0	Reserved.
2:0	R	5	**Detected PD Class of Port 4.**

- **Port 6~7 Detected PD Class Registers @ 0x8B of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:4	R	5	**Detected PD Class of Port 7**.
3	R	0	Reserved.
2:0	R	5	**Detected PD Class of Port 6.**

- **Port I_{CLASS} Registers @ 0x78~0x87 of Page 0**

Bit #	R/W	Default	Description
7:6	R	0	Reserved.
5:0	R	5	**Port I_{CLASS} MSB**. The current detected in classification. The MSB 10 bits are integer and the LSB 4 bits are fractional. Unit is in mA
Bit #	**R/W**	**Default**	**Description**
7:0	R	0x00	**Port I_{CLASS} LSB.**

- **Error Delay Register @ 0xE4 Page 0**

Bit#	R/W	Default	Description
7:0	R/W	0x10	**Error Delay.** The programmable error delay in units of 0.1S. Minimum value is 9.

5.6 Power Manager

Power manager is responsible for two tasks: **power configuration** and **power monitoring**. Power configuration is the task to allocate power to the ports requesting for power. Power monitoring is the task to monitor power conditions (current, voltage, and temperature). When invalid conditions occur, proper actions will be taken to prevent hazardous consequences.

5.6.1 Power Trunks

Before doing power configuration, the total available power must be determined first. IP808AR supports two trunks of power, where each power trunk has its own set of parameters to facilitate the calculation of total available power.

- **Trunk Power Limit** is the maximum power supply capacity allocated to the power trunk.

- **Trunk 0 Power Limit Register @ 0x40~0x41 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved**.
2:0	R/W	1	**Trunk 0 Power Limit (MSB)**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x2C	**Trunk 0 Power Limit (LSB)**. Trunk Power Limit specifies the upper limit of the power supply. Default is 300 Watts.

- **Trunk 1 Power Limit Register @ 0x42~0x43 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved**. **0x42**
2:0	R/W	1	**Trunk 1 Power Limit (MSB)**. **0x42**
7:0	R/W	0x2C	**Trunk 1 Power Limit (LSB)**. **0x43** Default is 300 Watts.

- **Trunk Select Register @ 0x69 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved**.
1:0	R/W	0	**Trunk Select**. Writing to this register will switch power trunk. Note that whenever the parameters of the power trunk currently in use are updated, this Trunk Select Register must also be written to make the newly updated parameters in effect. 0 = Trunk 0, 1 = Trunk 1.

5.6.2 Power Configuration

Power manager is responsible to allocate powers to the ports that pass the detection and classification process. To do so, several parameters must be specified or be calculated in advance:

1) Maximun Trunk Power (specified in register 0x40~0x43, page1).
2) Power configuration Mode (specified in register 0x10, page1).

- **Power configuration Mode** specifies the way to determine the requested port power of the power device (**RPP** of **Power configuration Mode Register**) in the power configuration process.
- **Requested Port Power** is determined in the power configuration process according to **RPP** of power configuration mode.
- **Power configuration Mode Register @ 0x10 of Page 1**

Bit #	R/W	Default	Description
7:5	R/W	0	Reserved
4:3	R/W	1	**Requested port power (RPP)** specifies ways to determine the port power requested by the power device in the power configuration process 0 = Host Defined Power Limit (HDPL) specified in Host Defined Power Limit registers 1 = Class defined power limit (CDPL) specified in Class Defined Power Limit registers. 2 = highest possible power (set by AT/AF flag). In AF mode, the maximum power allowed is 15.5Watts; in AT mode, the maximum power allowed is 30 Watts.
2:0	R	0	Reserved.

- **PD Requested Power @ 0x90~0x97 of Page 0**

Bit #	R/W	Default	Description
7:0	R	0x00	**PD Requested Power**. The power requested by and allocated to the PD, which is calculated according to the power allocation mode and the class of the PD. The unit is Watt. The MSB 6 bits are the integer number and the LSB 2 bits are the fraction number.

- **Class 0 Defined Power Limit Registers @ 0x12 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 0 Port Power Limit (C0DPL)**. The maximum allowable port power for class 0 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W.

- **Class 1 Defined Power Limit Registers @ 0x13 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x10	**Class 1 Port Power Limit (C1DPL)**. The maximum allowable port power for class 1 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x10 = 4.0W.

- **Class 2 Defined Power Limit Registers @ 0x14 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x1c	**Class 2 Port Power Limit (C2DPL)**. The maximum allowable port power for class 2 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0

Bit #	R/W	Default	Description
			specifies the fractional part of the power limit value. Default is 0x1c = 7.0W.

- **Class 3 Defined Power Limit Registers @ 0x15 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 3 Port Power Limit (C3DPL)**. The maximum allowable port power for class 3 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W.

- **Class 4 Type 1 Power Limit Registers @ 0x16 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 4 Port Power Limit Type 1 (C4DPL_TYPE1)**. The maximum allowable port power for class 4 type 1 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W

- **Class 4 Type 2 Power Limit Registers @ 0x17 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x78	**Class 4 Port Power Limit Type 2 (C4DPL_TYPE2)**. The maximum allowable port power for type 2 class 4 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x78 = 30.0W

- **Host Defined Port 0~7 Power Limit Registers @ 0x18~0x1F of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x78	**Class 4 Port Power Limit Type 2 (C4DPL_TYPE2)**. The maximum allowable port power for type 2 class 4 devices if RPP is set to be 0. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x78 = 30.0W

5.6.3 Port Polling

Besides power configuration, power manager is also responsible for the monitoring of port current (I), port voltage (V), and port temperature (T). When either of IVT is out of its valid range, power manager will take prompt actions to prevent the system from hazardous consequences.

Power manager do the monitoring by periodically polling the IVT of each port. The poll period can be specified in the **IVT Poll Register**.

- **Force Poll Register @ 0xE2 of Page 0**

Bit #	R/W	Default	Description
7:0	R/W	0	**Force Poll**. In manual mode or diagnostic mode, writing a 1 to the bit will force an IVT polling on the corresponding port. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, and so on. When the polling completes, the bit will be cleared automatically. Note that only one port can be polled at a time. Thus, writing a value with more than one bit set to 1 will not start IVT polling and the contents of this register stay 0. Also, when auto-polling is enabled, writing to this register has no effect.

- **IVT Poll Register @ 0xE3 of Page 0**

Bit #	R/W	Default	Description
7	R	0	**Polling in Progress.** When the IVT polling is in progress, this bit will be set to 1. Otherwise, this bit stays 0.
6	R	0	Reserved
5	R/W	0	**Enable Auto Poll**. Enable automatically polling of IVT of powered ports. In auto mode, this bit will be set to 1 automatically after system reset. When a forced IVT polling is in progress, writing to the auto poll bit has no effect. So, to enable auto polling, host CPU must first make sure the force poll bits have become 0.
4:0	R/W	2	**Poll Period**. Number of 8ms between each poll to the port IVT. Minimum value is 2.

- **Port 0~7 Current Registers @ 0xA0~0xAF of Page 0**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Port Current**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port Current**. The port current. MSB 10 bits are the integer part and LSB 2 bits are the fractional part. The unit is mA. This value is updated every time the port is polled.

- **Port 0~7 Port N Voltage Registers @ 0xB0~0xBF**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Port N Voltage**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port N Voltage**. The MSB 8 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Volts. This value is updated every time the port is polled. Note that the true port voltage is (**Power Supply Voltage – Port N Voltage**). Please refer to Supply Voltage Registers.

Port 0~7 Temperature Registers @ 0xC0~0xCF of Page 0

Bit #	R/W	Default	Description
7:5	R	0	Reserved.
4:0	R	0	**Port Temperature**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port Temperature**. The MSB 9 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Celsius. This value is updated every time the port is polled.

- **Power Supply Voltage Registers @ 0xE0~0xE1 of Page 0**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Power Supply Voltage**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Power Supply Voltage**. The supply voltage in Volts. The MSB 8 bits are the integer part, where the LSB 4 bits are the fractional part. This value is updated every time the port is polled

5.6.4 Power Event Handling

After the IVTs are polled and recorded, the power manager checks the polled values against predefined valid ranges. If the polled values drop out of the predefined valid range, power events are recorded and handled. The power events triggered by IVT monitor are **Current Limit Event, Trunk Voltage Limit Event ,and Temperature Limit Event.**

When a power event occurs, if its corresponding power event handle bit is 1, the port power is turned off. If IP808AR is in manual mode or diagnostic mode, and the power event's corresponding status mask bit is 1, an interrupt will be issued to the host CPU.

- **Port Temperature Limit Event (Bit 7).** After the port is polled and if the port temperature is above the value specified in **Port Temperature Limit Register**, a **Port Temperature Limit Event** occurs.

- **Port Temperature Limit Registers @ 0x24~0x25 of Page 1**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R/W	0x9	**Port Temperature Limit MSB**
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x60	**Port Temperature Limit LSB** The 8 MSB bits are the integer part, and the 4 LSB bits are the fraction part. Default 0x960 = 150°C.

- **Trunk Voltage Limit Event (Bit 6).** After the port is polled and if the port has being turn on ,the trunk voltage is check against **Trunk Voltage Limit Register**, if the voltage drops out of the predefined range , a **trunk voltage Limit Event** occurs .The upper and lower voltage limits can be set in the **Trunk Voltage Limit Register**

- **Trunk 0 Voltage Limit Registers @ 0x4C~0x4F of Page 1**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R/W	0x3	**Trunk 0 Voltage Upper Limit MSB**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0xC0	**Trunk 0 Voltage Upper Limit LSB**. The 8 MSB bits are the integer part, and the 4LSB bits are the fraction part. Default 0x3C0 = 60 Volts
Bit #	**R/W**	**Default**	**Description**
7:4	R	0	Reserved.
3:0	R/W	0x2	**Trunk 0 Voltage Lower Limit MSB**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x80	**Trunk 0 Voltage Lower Limit LSB**. The 8 MSB bits are the integer part, and the 4LSB bits are the fraction part. Default 0x280 = 40 Volts

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- **Trunk 1 Voltage Limit Registers @ 0x50~0x53 of Page 1**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R/W	0x3	**Trunk 0 Voltage Upper Limit MSB**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0xC0	**Trunk 0 Voltage Upper Limit LSB**. The 8 MSB bits are the integer part, and the 4LSB bits are the fraction part. Default 0x3C0 = 60 Volts
Bit #	**R/W**	**Default**	**Description**
7:4	R	0	Reserved.
3:0	R/W	0x2	**Trunk 0 Voltage Lower Limit MSB**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x80	**Trunk 0 Voltage Lower Limit LSB**. The 8 MSB bits are the integer part, and the 4LSB bits are the fraction part. Default 0x280 = 40 Volts

- **Port Current Limit Event (Bit 5).** After the port is polled and if the port has being turn on ,the port current is check against **Port Current Limit Register**, if the port current exceeds the port current limit a **Port Current Limit Event** occurs

- **Port Current Limit Registers @ 0x30~0x3F of Page 1**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R/W	0xC	**Port Current Limit MSB**
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x80	**Port Current Limit LSB** The 10 MSB bits are the integer part, and the 2 LSB bits are the fraction part. Default 0xC80 = 800mA. Note: if Port current limit above 640mA , the **Overload** (I_{CUT}) **Event** occur earlier than port current limit

5.7 Real time Monitor Power Event

Power events described in previous sections are discovered only when the ports are polled. The analog monitor can continuously watch over and report time-critical power events so that the power manager can take prompt actions. Power events from analog monitor include thermal shutdown event, severe short circuit event (I > 1.4 Amp), MPS error event (DC Disconnect), overload event (I > I_{CUT}), and short circuit event (I > I_{LIM}).

- **Thermal Shutdown Event** is the event where the port temperature is over the pre-defined thermal shutdown threshold. The port power is turned off and the port is eligible for detection only after the port is cooled off (temperature drops below the threshold).
- **Severe Short Circuit Event** is the event where the port current is over 1.4 Amp. Immediate action must be taken to eliminate such event. The power manager responds to this event by temporarily turn off port power.
- **DC Disconnect Event** is the event the port cannot maintain its power signature (MPS). If the event lasts for specified period of time, this will be considered an **MPS error event** and the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Overload (I_{CUT}) Event** is the event where port current is greater than I_{CUT}. If the event lasts for specified period of time, this will be considered an **overload event**. When an overload condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Short Circuit (I_{LIM}) Event** is the event where port current is greater than I_{LIM}. This event should be sampled by the power manager to determine if a **short circuit event** has occurred either during the power up process or after the port being powered up. When a short circuit condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.

A summary of power off conditions

Condition	description	Power off moment	Reference Section
Trunk<PDRequest power	Power Trunk not enough power to port used	Power up sequence	5.6.1
Trunk Voltage > limit	Trunk Voltage Event	IVT polling	5.6.4
Port temp > limit	Port temperature Event	IVT polling	5.6.4
Port temp > thermal	Thermal Shutdown Event	Real-time monitor	5.7
Port I > 1.4A	Severe Short Circuit Event	Real-time monitor	5.7
Port unplug UTP	DC Disconnect Event	Real-time monitor	5.7
PortI > Ilim (AT =850mA)	short circuit event	Real-time monitor	5.7
PortI > Icut (AT =640mA)	Overload (I_{CUT}) Event	Real-time monitor	5.7

Table 4 Port power off conditions

5.8 Port Status and Interrupt

Port state and power events are recorded in the registers. In manual mode and diagnostic mode, these statuses can generate interrupts to host CPU for further processing.

- **Port Power Event Handle Register @ 0x81 of Page 1**

Bit #	R/W	Default	Description
7	R/W	1	**Port Temperature Limit Event Handle**. 0 = Do not turn off power when the event occurs. 1 = Turn off power when the event occurs.
6	R/W	0	**Trunk Voltage Limit Event Handle**.
5	R/W	0	**Port Current Limit Event Handle**.
4:0	R	0	Reserved

- **Port 0~7 Power Event Register @ 0x70~0x77 of Page 1**

Bit #	R/W	Default	Description
7	W1C	0	**Port Temperature Limit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
6	W1C	0	**Trunk Voltage Limit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
5	W1C	0	**Port Current Limit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
4	W1C	0	**Port Thermal Shutdown Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
3	R	0	**Reserved**
2	W1C	0	**Port MPS Error (DC Disconnect) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
1	W1C	0	**Port Short Circuit Limit (I_{LIM}) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
0	W1C	0	**Port Overload (I_{CUT}) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.

- **Port 0~7 Severe Short Circuit Event Register @ 0x87 of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Port 7 Severe Short Circuit Event**.
6	R/W	0	**Port 6 Severe Short Circuit Event**.
5	R/W	0	**Port 5 Severe Short Circuit Event**.
4	R/W	0	**Port 4 Severe Short Circuit Event**.
3	R/W	0	**Port 3 Severe Short Circuit Event**.
2	R/W	0	**Port 2 Severe Short Circuit Event**.
1	R/W	0	**Port 1 Severe Short Circuit Event**.
0	R/W	0	**Port 0 Severe Short Circuit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.

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- **Port 0~7 Power Event Mask Register @ 0x78~0x7F of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Port Temperature Limit Event Mask**. In manual mode or diagnostic mode, when mask bit is 0, no interrupt will be issued for this event.
6	R/W	0	**Port Thermal Shutdown Event Mask**.
5	R/W	0	**Port Thermal Shutdown Event Mask**.
4	R/W	0	**Port Thermal Shutdown Event Mask**.
3	R	0	**Reserved**
2	R/W	0	**Port MPS Error (DC Disconnect) Event Mask**.
1	R/W	0	**Port Short Circuit (I_{LIM}) Event Mask**.
0	R/W	0	**Port Overload (I_{CUT}) Event Mask**.

- **Port Severe Short Circuit Event Mask Register @ 0x86 of Page 1**

Bit #	R/W	Default	Description
4	R/W	0	**Port Severe Short Circuit Event Mask**

- **Port Interrupt Register @ 0x80 of Page 1**

Bit #	R/W	Default	Description
7	R	0	**Port 7 Interrupt**. Port 7 has interrupt.
6	R	0	**Port 6 Interrupt**. Port 6 has interrupt.
5	R	0	**Port 5 Interrupt**. Port 5 has interrupt.
4	R	0	**Port 4 Interrupt**. Port 4 has interrupt.
3	R	0	**Port 3 Interrupt**. Port 3 has interrupt.
2	R	0	**Port 2 Interrupt**. Port 2 has interrupt.
1	R	0	**Port 1 Interrupt**. Port 1 has interrupt.
0	R	0	**Port 0 Interrupt**. Port 0 has interrupt.

- **Port Power Status Register @ 0x82 of Page 1**

Bit #	R/W	Default	Description
7:0	R	0	**Power Status of the Ports**. 0 = power off. 1 = power on. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

5.9 Total Current Limit

When the IVT is polled, the port currents are summed up to get the total current consumption. Total current limit Register can be specified and checked against the total current consumption. When this total current limit is exceeded, the last port powered on would be turned off. The total current limit is by default disabled and can be enabled by using the Total Current Limit Control Register. The total current limit is specified in the PSE Available Current Registers.

IP808AR have Overload LED threshold register, When the PSE consumed current is more that the Overload LED Threshold, the Overload LED will be turn on. Please refer to the section 5.10 for LED interface Display setting description

- **Total Current Limit Control Registers @ 0xC0 of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Enable Total Current Limit** 0= Disable 1= Enable
6:3	R	0	Reserved.
2:0	R/W	0	**Victim Strategy**. Strategy to pick victim port. 0 = Last port powered up. 1 = First port powered up. 2 = The port with least current. 3 = The port with greatest current.

- **PSE Available Current Registers @ 0x54~0x55 of Page 1**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:0	R/W	5D	**PSE Available Current MSB**
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	C0	**PSE Available Current LSB** Total available current is the maximum current that the power supply can provide to the ports. The MSB 13 bits are the integer part and LSB 2 bits are the fractional part. The unit is mA.

- **PSE Consumed Current Registers @ 0x56~57 of Page 1**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:0	R	0	**PSE Consumed Current MSB**
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**PSE Consumed Current LSB** Total available current is the maximum current that the power supply can provide to the ports. The MSB 13 bits are the integer part and LSB 2 bits are the fractional part. The unit is mA. The total consumed current is updated when the IVT monitor performs an IVT polling.

- **Overload LED Threshold Registers @ 0xDD~0xDE of Page 1**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:0	R/W	17	**Overload LED Threshold MSB**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	70	**Overload LED Threshold LSB**. When the PSE consumed current is more that the Overload LED Threshold, the Overload LED will be turn on. The unit is in mA

5.10 LED Interface

In auto mode or manual mode, the LED interface can hook up with an IP403 (Serial-to-Parallel LED driver) to display the port status. A port status LED is lit up when IP808AR allocates power to the port

LED interface is enabled by pulling up LED_DAT pin with a resister. One IP808AR can handle 8 LEDs and up to three IP808ARs can share one IP403, where one IP808AR serves as the master to drive LED_CLK and the others are slaves. AD2 pin defines IP808AR to be a master or a slave. The index counter in all IP808ARs counts from 0 to 55 repeatly with LED_CLK after reset and the value of index counter in all IP808AR are identical. An IP808AR will send out 8-bit LED information on LED_DAT when its index counter reaches start index defined in start index register (0x0B). The detail is illustrated in the LED start index register (0x0B) and figure 6.

If there is only one IP808AR, user can replace IP403 with a 74LV164 to display port status for cost saving. IP808AR should be configured as a master.

LED Configuration Register @ 0x08 of Page 1

Bit #	R/W	Default	Description
7	R/W	0/1	**LED Interface Enable**. Enable the LED interface. 0 = disable, 1 = enable. The default value of this bit is latched from LED_DAT pin.
6	R/W	0	**Dedicate Overload LED Enable** The LED_DAT pin can act as a dedicated LED to display the overload status. 0 = disable. 1 = enable.
5	R/W	0	**Shift Overload LED Enable** Enable one shift pattern to show the overload status. 0 = disable. 1 = enable.
4	R/W	1	**LED Order**. The order in which 8-bit LED information is shifted out. 0 = Port 0, Port1, …. Port7. 1 = Port7, Port6, …. Port 0.
3	R/W	0	**LED Active Level**. 0 = light up a LED by driving logic low 1 = light up a LED by driving logic high
2	R/W	1	**LED Initial Level**. The initial level of the LED. After reset, the LED will be driven to this initial value.
1	R/W	1	**LED Clock Rate**. Clock rate of the LED clock. 0 = LED clock is 512k Hz 1 = LED clock is 1M Hz
0	R/W	0/1	**LED Master**. 0 = slave. IP808AR receives LED clock on LED_CLK pin. 1 = master. IP808AR drives LED_CLK pin. The default value of this bit is latched from AD2 pin.

➢ **LED Start Index Register @ 0x0B of Page 1**

<table>
<tr><th>Bit #</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7:6</td><td>R</td><td>0</td><td>Reserved.</td></tr>
<tr><td>5:0</td><td>R/W</td><td></td><td>LED Start Index.

There are 3 default values can be selected with I^{2}C address pin AD2 ~ AD0. It is benefit to implement a multiple (no more than 3) IP808AR LED display without software programming.
<table>
<tr><th>AD2~AD0</th><th>default value of bit [5:0]</th></tr>
<tr><td>1,0,0 (master)</td><td>0x30h (48d)</td></tr>
<tr><td>0,0,0(slave)</td><td>0x28h (40d)</td></tr>
<tr><td>0,0,1(slave)</td><td>0x20h (32d)</td></tr>
<tr><td>0,1,0(slave)</td><td>0x18h (24d)</td></tr>
<tr><td>0,1,1(slave)</td><td>0x10h (16d)</td></tr>
</table>

The following table demostrates the LED applications for 1~3 IP808AR.
<table>
<tr><th>3 x IP808AR</th><th>Master</th><th>Slave1</th><th>Slave2</th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>0x20h</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>0,0,0</td><td>0,0,1</td></tr>
<tr><th>2 x IP808AR</th><th>Master</th><th>Slave1</th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>--</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>0,0,0</td><td>--</td></tr>
<tr><th>1 x IP808AR</th><th>Master</th><th></th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>--</td><td>--</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>--</td><td>--</td></tr>
</table>

In manual mode, because AD0~AD2 is used for I^{2}C address at the same time, the default setting of LED start index may be incorrect. User has to correct the LED start index by writing this register to make sure that IP808AR can send out LED status correctly.

There is an alternative for LED implementation if there is a MCU in the system. The MCU reads the port status of IP808AR through I^{2}C and write the LED information to IP403, where IP403 works as a GPIO controller not a serial-to-parallel LED driver. Because LED is handled by MCU itself, the start index in IP808AR can be ignored.</td></tr>
</table>

➢ **Overload LED Index Registers @ 0x0C of Page 1**

Bit #	R/W	Default	Description
7:6	R	0	Reserved.
5:0	R/W	2F	**Overload LED Index**. When the LED interface and Overload LED Enable register are enabled and the index count reaches the index defined in the registers, IP808AR drives out the status of overload.

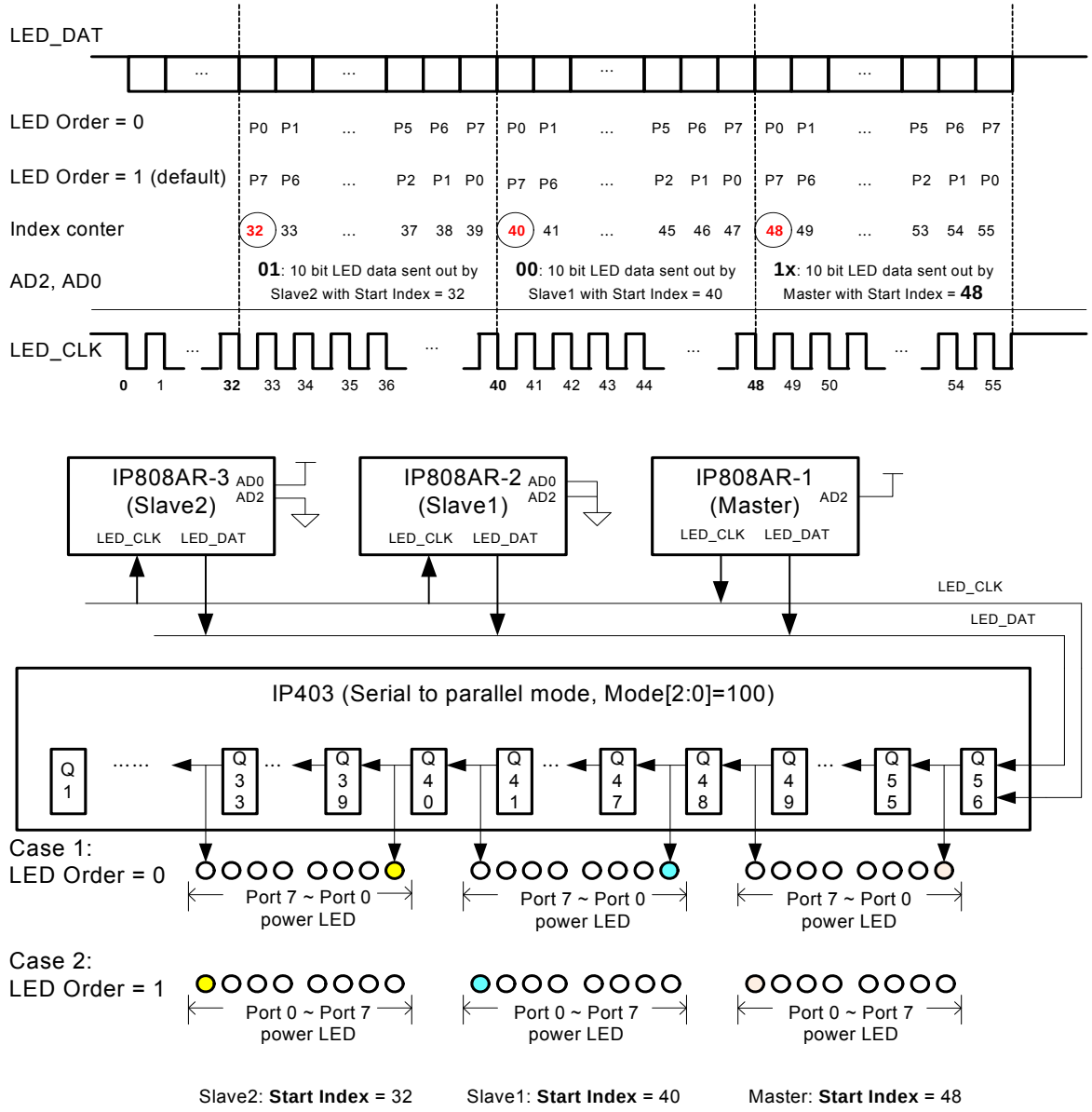


Figure 6 LED behavior and system diagram of multiple IP808AR application

6 IP808AR Register descriptions

Table 5 Register Page 0 description

Page #	Register Address and Attribute		Register Name	Default Value
I^2C Interface Registers				
0	0x00	R/W	Register Page & I^2C LSB Device Address (I^2C Addr)	(x0xx,xPPP) P: pin setting
Analog Configure and Control Registers				
0	0x01~0x24	R	Reserved (write prohibited)	-
0	0x25	R/W	AF/AT Mode	(1111,1111)
0	0x26~0x5E	R	Reserved (write prohibited)	-
0	0x5F	R/W	Inrush Time	(0111,1110)
0	0x60~0x67	R	Reserved (write prohibited)	-
Detection Result				
0	0x68	R	R_{DET} for Port 0	(xxxx,xx00)
0	0x69	R	R_{DET} for Port 1	(xxxx,xx00)
0	0x6A	R	R_{DET} for Port 2	(xxxx,xx00)
0	0x6B	R	R_{DET} for Port 3	(xxxx,xx00)
0	0x6C	R	R_{DET} for Port 4	(xxxx,xx00)
0	0x6D	R	R_{DET} for Port 5	(xxxx,xx00)
0	0x6E	R	R_{DET} for Port 6	(xxxx,xx00)
0	0x6F	R	R_{DET} for Port 7	(xxxx,xx00)
0	0x70~0x77	R	Reserved (write prohibited)	-
Classification Currents				
0	0x78	R	I_{CLASS} for Port 0 MSB	(xxx0,0000)
0	0x79	R	I_{CLASS} for Port 0 LSB	(0000,0000)
0	0x7A	R	I_{CLASS} for Port 1 MSB	(xxx0,0000)
0	0x7B	R	I_{CLASS} for Port 1 LSB	(0000,0000)
0	0x7C	R	I_{CLASS} for Port 2 MSB	(xxx0,0000)
0	0x7D	R	I_{CLASS} for Port 2 LSB	(0000,0000)
0	0x7E	R	I_{CLASS} for Port 3 MSB	(xxx0,0000)
0	0x7F	R	I_{CLASS} for Port 3 LSB	(0000,0000)
0	0x80	R	I_{CLASS} for Port 4 MSB	(xxx0,0000)
0	0x81	R	I_{CLASS} for Port 4 LSB	(0000,0000)
0	0x82	R	I_{CLASS} for Port 5 MSB	(xxx0,0000)
0	0x83	R	I_{CLASS} for Port 5 LSB	(0000,0000)
0	0x84	R	I_{CLASS} for Port 6 MSB	(xxx0,0000)
0	0x85	R	I_{CLASS} for Port 6 LSB	(0000,0000)
0	0x86	R	I_{CLASS} for Port 7 MSB	(xxx0,0000)
0	0x87	R	I_{CLASS} for Port 7 LSB	(0000,0000)
Classification Results (Detected PD Classes)				
0	0x88	R	Detected PD Class Port 1 & 0	(x101,x101)
0	0x89	R	Detected PD Class Port 3 & 2	(x101,x101)
0	0x8A	R	Detected PD Class Port 5 & 4	(x101,x101)
0	0x8B	R	Detected PD Class Port 7 & 6	(x101,x101)
0	0x8C~0x8F	R	Reserved (write prohibited)	-
PD Requested Powers				
0	0x90	R	PD 0 Requested Power	(0000,0000)
0	0x91	R	PD 1 Requested Power	(0000,0000)
0	0x92	R	PD 2 Requested Power	(0000,0000)
0	0x93	R	PD 3 Requested Power	(0000,0000)

Page #	Register Address and Attribute		Register Name	Default Value
0	0x94	R	PD 4 Requested Power	(0000,0000)
0	0x95	R	PD 5 Requested Power	(0000,0000)
0	0x96	R	PD 6 Requested Power	(0000,0000)
0	0x97	R	PD 7 Requested Power	(0000,0000)
0	0x98~0x9F	R	Reserved (write prohibited)	-
Port Currents				
0	0xA0	R	Port 0 Current MSB	(xxxx,0000)
0	0xA1	R	Port 0 Current LSB	(0000,0000)
0	0xA2	R	Port 1 Current MSB	(xxxx,0000)
0	0xA3	R	Port 1 Current LSB	(0000,0000)
0	0xA4	R	Port 2 Current MSB	(xxxx,0000)
0	0xA5	R	Port 2 Current LSB	(0000,0000)
0	0xA6	R	Port 3 Current MSB	(xxxx,0000)
0	0xA7	R	Port 3 Current LSB	(0000,0000)
0	0xA8	R	Port 4 Current MSB	(xxxx,0000)
0	0xA9	R	Port 4 Current LSB	(0000,0000)
0	0xAA	R	Port 5 Current MSB	(xxxx,0000)
0	0xAB	R	Port 5 Current LSB	(0000,0000)
0	0xAC	R	Port 6 Current MSB	(xxxx,0000)
0	0xAD	R	Port 6 Current LSB	(0000,0000)
0	0xAE	R	Port 7 Current MSB	(xxxx,0000)
0	0xAF	R	Port 7 Current LSB	(0000,0000)
Port N Voltages				
0	0xB0	R	Port 0 Voltage MSB	(xxxx,0000)
0	0xB1	R	Port 0 Voltage LSB	(0000,0000)
0	0xB2	R	Port 1 Voltage MSB	(xxxx,0000)
0	0xB3	R	Port 1 Voltage LSB	(0000,0000)
0	0xB4	R	Port 2 Voltage MSB	(xxxx,0000)
0	0xB5	R	Port 2 Voltage LSB	(0000,0000)
0	0xB6	R	Port 3 Voltage MSB	(xxxx,0000)
0	0xB7	R	Port 3 Voltage LSB	(0000,0000)
0	0xB8	R	Port 4 Voltage MSB	(xxxx,0000)
0	0xB9	R	Port 4 Voltage LSB	(0000,0000)
0	0xBA	R	Port 5 Voltage MSB	(xxxx,0000)
0	0xBB	R	Port 5 Voltage LSB	(0000,0000)
0	0xBC	R	Port 6 Voltage MSB	(xxxx,0000)
0	0xBD	R	Port 6 Voltage LSB	(0000,0000)
0	0xBE	R	Port 7 Voltage MSB	(xxxx,0000)
0	0xBF	R	Port 7 Voltage LSB	(0000,0000)
Port Temperatures				
0	0xC0	R	Port 0 Temp. MSB	(xxx0,0000)
0	0xC1	R	Port 0 Temp. LSB	(0000,0000)
0	0xC2	R	Port 1 Temp. MSB	(xxx0,0000)
0	0xC3	R	Port 1 Temp. LSB	(0000,0000)
0	0xC4	R	Port 2 Temp. MSB	(xxx0,0000)
0	0xC5	R	Port 2 Temp. LSB	(0000,0000)
0	0xC6	R	Port 3 Temp. MSB	(xxx0,0000)
0	0xC7	R	Port 3 Temp. LSB	(0000,0000)
0	0xC8	R	Port 4 Temp. MSB	(xxx0,0000)
0	0xC9	R	Port 4 Temp. LSB	(0000,0000)

Page #	Register Address and Attribute		Register Name	Default Value
0	0xCA	R	Port 5 Temp. MSB	(xxx0,0000)
0	0xCB	R	Port 5 Temp. LSB	(0000,0000)
0	0xCC	R	Port 6 Temp. MSB	(xxx0,0000)
0	0xCD	R	Port 6 Temp. LSB	(0000,0000)
0	0xCE	R	Port 7 Temp. MSB	(xxx0,0000)
0	0xCF	R	Port 7 Temp. LSB	(0000,0000)
0	0xD0~0xDF	R	Reserved (write prohibited)	-
Power Supply Voltage				
0	0xE0	R	Supply Voltage MSB	(xxxx,0000)
0	0xE1	R	Supply Voltage LSB	(0000,0000)
IVT Poll Control				
0	0xE2	R/W	Force IVT Poll	(0000,0000)
0	0xE3	R/W	IVT Poll Control	(x000,0010)
0	0xE4	R/W	Error Delay	(0001,0000)
0	0xE5 ~ 0xFF	R	Reserved (write prohibited)	-

Table 6 Register Page 1 description

Page #	Register Address and Attribute		Register Name	Default Value (Binary)
Register Page & I²C Interface Registers				
1	0x00	R/W	Register Page & I²C LSB Device Address (I²C Addr)	(x0xx,xPPP) P:pin setting
System Configuration & Control Registers				
1	0x01	R/W	Operation mode	(PPx0,xxxx) P:pin setting
1	0x02	R/W	Software Reset	(xxxx,xxx0)
1	0x03	R	Hardware Revision MSB	(1000,0000)
1	0x04	R	Hardware Revision LSB	(1000,1010)
1	0x05	R/W	Watchdog Timer	(0000,0000)
1	0x06	R/W	Scratch register	(0000,0000)
1	0x07	R/W	Alternative A or B	(PPPP,PPPP) P:PinSetting
LED Control & Configuration				
1	0x08	R/W	LED Control	(Pxx1,011P) P:PinSetting
1	0x09~0x0A	R	Reserved (write prohibited)	-
1	0x0B	R/W	LED Start Index	(PPPP,PPPP) P:PinSetting
1	0x0C	R/W	Overload LED Index	(0010,1111)
Power Configuration				
1	0x10	R/W	Power Configuration Mode (PAM)	(0000,1000)
1	0x11	R	Reserved (write prohibited)	
1	0x12	R/W	Class 0 Port Power Limit	(0011,1110)
1	0x13	R/W	Class 1 Port Power Limit	(0001,0000)
1	0x14	R/W	Class 2 Port Power Limit	(0001,1100)
1	0x15	R/W	Class 3 Port Power Limit	(0011,1110)
1	0x16	R/W	Class 4 Port Power Limit Type 1	(0011,1110)
1	0x17	R/W	Class 4 Port Power Limit Type 2	(0111,1000)
1	0x18	R/W	Host Define Port 0 Power Limit	(0111,1000)
1	0x19	R/W	Host Define Port 1 Power Limit	(0111,1000)
1	0x1A	R/W	Host Define Port 2 Power Limit	(0111,1000)
1	0x1B	R/W	Host Define Port 3 Power Limit	(0111,1000)
1	0x1C	R/W	Host Define Port 4 Power Limit	(0111,1000)
1	0x1D	R/W	Host Define Port 5 Power Limit	(0111,1000)
1	0x1E	R/W	Host Define Port 6 Power Limit	(0111,1000)
1	0x1F	R/W	Host Define Port 7 Power Limit	(0111,1000)
1	0x20~0x23	R	Reserved (write prohibited)	-
1	0x24	R/W	Port Temp. Limit MSB	(xxx0,1001)
1	0x25	R/W	Port Temp. Limit LSB	(0110,0000)
1	0x26~0x2F	R	Reserved (write prohibited)	-
1	0x30	R/W	Port 0 Current Limit MSB	(xxxx,0010)
1	0x31	R/W	Port 0 Current Limit LSB	(1101,0000)
1	0x32	R/W	Port 1 Current Limit MSB	(xxxx,0010)
1	0x33	R/W	Port 1 Current Limit LSB	(1101,0000)
1	0x34	R/W	Port 2 Current Limit MSB	(xxxx,0010)
1	0x35	R/W	Port 2 Current Limit LSB	(1101,0000)
1	0x36	R/W	Port 3 Current Limit MSB	(xxxx,0010)

Page #	Register Address and Attribute		Register Name	Default Value (Binary)
1	0x37	R/W	Port 3 Current Limit LSB	(1101,0000)
1	0x38	R/W	Port 4 Current Limit MSB	(xxxx,0010)
1	0x39	R/W	Port 4 Current Limit LSB	(1101,0000)
1	0x3A	R/W	Port 5 Current Limit MSB	(xxxx,0010)
1	0x3B	R/W	Port 5 Current Limit LSB	(1101,0000)
1	0x3C	R/W	Port 6 Current Limit MSB	(xxxx,0010)
1	0x3D	R/W	Port 6 Current Limit LSB	(1101,0000)
1	0x3E	R/W	Port 7 Current Limit MSB	(xxxx,0010)
1	0x3F	R/W	Port 7 Current Limit LSB	(1101,0000)
Power Trunk Control & Configuration				
1	0x40	R/W	Trunk 0 Power Limit MSB	(xxxx,x000)
1	0x41	R/W	Trunk 0 Power Limit LSB	(1111,1010)
1	0x42	R/W	Trunk 1 Power Limit MSB	(xxxx,x000)
1	0x43	R/W	Trunk 1 Power Limit LSB	(1111,1010)
1	0x44~0x4B	R	Reserved (write prohibited)	-
1	0x4C	R/W	Trunk 0 Supply Voltage Upper Limit MSB	(xxxx,0011)
1	0x4D	R/W	Trunk 0 Supply Voltage Upper Limit LSB	(1100,0000)
1	0x4E	R/W	Trunk 0 Supply Voltage Lower Limit MSB	(xxxx,0010)
1	0x4F	R/W	Trunk 0 Supply Voltage Lower Limit LSB	(1000,0000)
1	0x50	R/W	Trunk 1 Supply Voltage Upper Limit MSB	(xxxx,0011)
1	0x51	R/W	Trunk 1 Supply Voltage Upper Limit LSB	(1100,0000)
1	0x52	R/W	Trunk 1 Supply Voltage Lower Limit MSB	(xxxx,0010)
1	0x53	R/W	Trunk 1 Supply Voltage Lower Limit LSB	(1000,0000)
1	0x54	R/W	PSE Available Current MSB	(x101,1101)
1	0x55	R/W	PSE Available Current LSB	(1100,0000)
1	0x56	R	Total consumed Current MSB	(x000,0000)
1	0x57	R	Total consumed Current LSB	(0000,0000)
1	0x58~0x68	R	Reserved (write prohibited)	-
1	0x69	R/W	Trunk Select	(xxxx,xx00)
1	0x6A~0x6F	R	Reserved (write prohibited)	-
Port Status				
1	0x70	R/W1C	Port 0 Status	(0000,0000)
1	0x71	R/W1C	Port 1 Status	(0000,0000)
1	0x72	R/W1C	Port 2 Status	(0000,0000)
1	0x73	R/W1C	Port 3 Status	(0000,0000)
1	0x74	R/W1C	Port 4 Status	(0000,0000)
1	0x75	R/W1C	Port 5 Status	(0000,0000)
1	0x76	R/W1C	Port 6 Status	(0000,0000)
1	0x77	R/W1C	Port 7 Status	(0000,0000)
1	0x78	R/W	Port Status Mask	(1111,1111)
1	0x79~0x7F	R	Reserved (write prohibited)	-
1	0x80	R	Port Interrupt Status	(0000,0000)
1	0x81	R/W	Power Event Handle	(111x,xxxx)
1	0x82	R	Port Power Status	(0000,0000)
1	0x83	R	MPS Present Status	(0000,0000)
1	0x84~0x8F	R	Reserved (write prohibited)	-
State Machine Control & Status				
1	0x90	R/W	Port 0 State Machine State	(00x0,0000)
1	0x91	R/W	Port 1 State Machine State	(00x0,0000)
1	0x92	R/W	Port 2 State Machine State	(00x0,0000)

Page #	Register Address and Attribute		Register Name	Default Value (Binary)
1	0x93	R/W	Port 3 State Machine State	(00x0,0000)
1	0x94	R/W	Port 4 State Machine State	(00x0,0000)
1	0x95	R/W	Port 5 State Machine State	(00x0,0000)
1	0x96	R/W	Port 6 State Machine State	(00x0,0000)
1	0x97	R/W	Port 7 State Machine State	(00x0,0000)
1	0x98	R/W	Port 0 Power Control	(xxxx,xx00)
1	0x99	R/W	Port 1 Power Control	(xxxx,xx00)
1	0x9A	R/W	Port 2 Power Control	(xxxx,xx00)
1	0x9B	R/W	Port 3 Power Control	(xxxx,xx00)
1	0x9C	R/W	Port 4 Power Control	(xxxx,xx00)
1	0x9D	R/W	Port 5 Power Control	(xxxx,xx00)
1	0x9E	R/W	Port 6 Power Control	(xxxx,xx00)
1	0x9F	R/W	Port 7 Power Control	(xxxx,xx00)
1	0xA0	R/W	Port 3-0 Classification Event Number	(1010,1010)
1	0xA1	R/W	Port 7-4 Classification Event Number	(1010,1010)
1	0xA2	R/W	PSE Skip Event 2	(1111,1111)
1	0XA3~0xBF	R	Reserved (write prohibited)	-
Total Current Limit Control Registers				
1	0xC0	R/W	Total current limit control	(0xxx,x000)
1	0xC1~0xD9	R	Reserved (write prohibited)	-
1	0xDA	R/W0C	Power Denied Event Status	(0000,0000)
1	0xDB	R	Reserved (write prohibited)	-
1	0xDC	R/W0C	Invalid Signature Event Status	(0000,0000)
1	0xDD	R/W	Overload LED Threshold MSB	(0010,0111)
1	0xDE	R/W	Overload LED Threshold LSB	(0001,0000)
1	0xDF~0xFF	R	Reserved (write prohibited)	-

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

(Note: Beyond these ratings can cause damage to the device)

Table 7 Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Supply Voltage	V54 – AGND	-0.3		+75	V
PortN0~PortN7	PortNn– AGND @n=0~7	-0.3		+75	V
V5	V5 – AGND	-0.3		+5.5	V
All other Pins	All other Pin – (AGND, or DGND)	-0.3		+3.6	V
RGND, AGND	DGND – AGND	-0.3		+0.3	V
Maximum Junction Temperature				150	℃
Storage Temperature Range		-65		150	℃
Lead Temperature	30s, reflow			260	℃
ESD at all Pins	HBM	±2			KV

7.2 Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
Ta	Ambient temperature	-40		+85	℃
V54	V54 – AGND @ AF	44	48	57	V
	V54 – AGND @ AT	50	54	57	V

7.3 Electrical Characteristics for Analog I/O Pins

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V54	Power Supply voltage	45V~57V @AF	44		57	V
		51V~57V @AT	50		57	V
I54	V54 operating current	All ports on @w/o peripheral load current & port load current		8	15	mA
V3P3	V3P3 voltage	External Capacitance=4.7uF V3P3 short DV3P3	3.13	3.30	3.46	V
Iout_v3p3	EnB_Reg=low	V3P3 providing to peripheral device V3P3 short DV3P3			6	mA
Iin_v3p3	EnB_Reg=high	External 3.3V provides to V3P3 V3P3 short DV3P3	6			mA
V5	Internal use only	External Capacitance=4.7uF	4.99	5.25	5.51	V
V1P8	Internal use only	External Capacitance=1uF	1.71	1.8	1.89	V
V54_UVL	V54 under voltage lockout	Rising V54 – AGND		30		V
		Falling V54 – AGND		27		V
V54_OVL	V54 overvoltage lockout	Rising V54 – AGND		63		V
		Falling V54 – AGND		60		V
V3P3_Rise	V3P3 Rise ,Release	Rising V3P3 – AGND V3P3 short DV3P3		2.8		V
V3P3_Fall	V3P3 Fall Reset	Falling V3P3 – AGND V3P3 short DV3P3		1.9		V

7.4 IEEE802.3 AF/AT Mode Parameters

Table 8 IEEE802.3 AF/AT Mode Parameters

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
Tovlrec	Auto-recovery time	From overload shutdown to next detection			1.6		s
Tudlrec	Auto-recovery time	From Imin_off shutdown to next detection			1.6		s
Tbackoff	Back-off time	Midspan mode detection back-off time			2.5		s
Iinrush	Inrush current	For t=50ms Cload=180uF max.		400	425	450	mA
Imin_off	Port off	Must disconnect for t greater than Tmpdo		0		5	mA
Imin_onoff	Port off or on	May or may not disconnect for greater than Tmpdo		5	7.5	10	mA
Tmpdo	PD Maintenance power signature dropout time limit	AF/AT		300	310	400	ms
Tmps	PD Maintenance power signature time for validity	Port current pulse width to reset disconnect timer			6		ms
Icut	Over load current (default)	AF@Vport=44V		350	375	400	mA
		AT@Vport=50V		600	640	664	mA
	Maximum Over load current	Class 0	Vport=44V	350	375	400	mA
		Class 1		91	112	133	
		Class 2		160	206	252	
		Class 3		350	375	400	
		Class 4	Vport=50V	600	640	680	
Tcut	Over load time	Iport > Icut, AF/AT		50	62.5	75	ms
Ilim	Current limit	AF@Vport=44V		400	425	450	mA
		AT@Vport=50V		800	860	920	mA
Tlim	Current limit time	Iport = Ilim, AF/AT		50	62.5	75	ms
Toff	Turn off time	From VportN to V54-2.8V				500	ms
Ron	Port onMOS(0.15R) +Rs(0.1R)	Iport≦640mA, & Ta=25℃			0.25		Ω
Ioff_port	PortN leakage current	V54=54V , Ta=25℃, Port off				10	uA

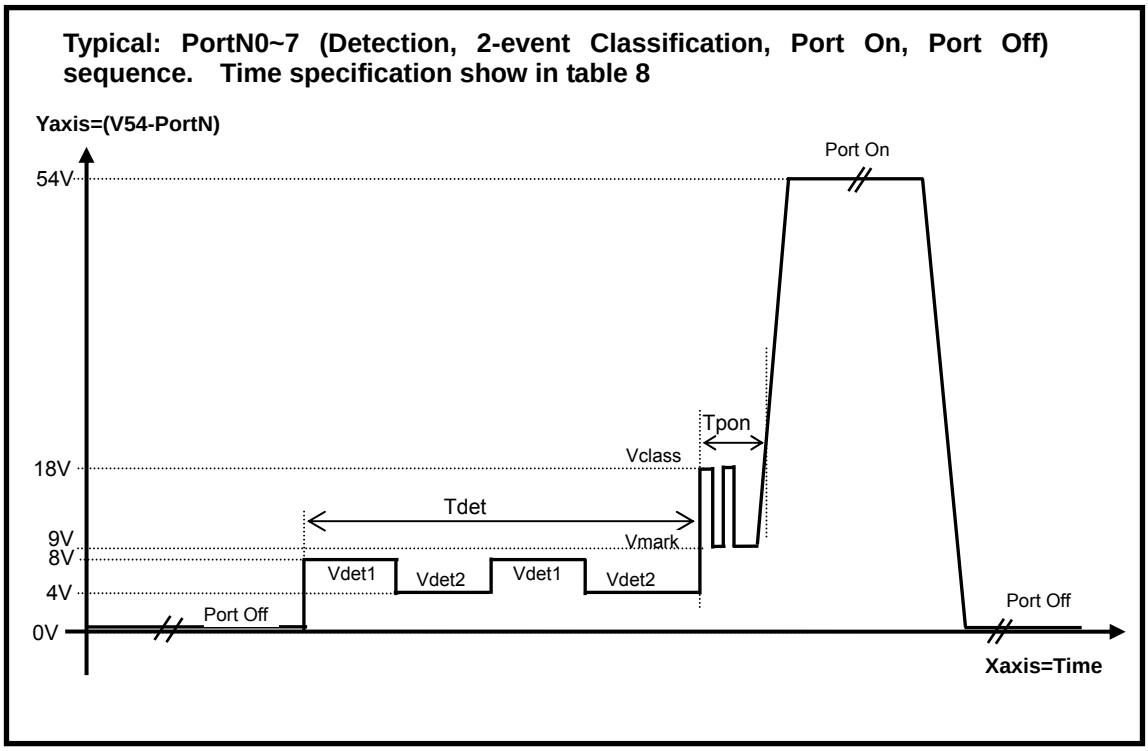


Figure 7 Typical Power up Sequence

IEEE802.3 AF/AT Mode Parameters: (continued)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Detection						
Vdet1	Detection voltage @first point	V54 – PortNn, (n=0~7) @Rdet=25KΩ	2.8	8	10	V
Vdet2	Detection voltage @second point	V54 – PortNn, (n=0~7) @Rdet=25KΩ	2.8	4	10	V
Idetlim	Detection current limit	V54=PortNn, (n=0~7)			5	mA
Tdet	Time to complete detection of a PD	AF/AT		326	500	ms
Vdet_oc	Detection port open circuit voltage	V54 – PortNn, (n=0~7) @Port open circuit			30	V
Rdet_min	Minimum Rdet detection resistance	@Cdet=0.15uF	15	17	19	KΩ
Rdet_max	Maximum Rdet detection resistance	@Cdet=0.15uF	26.5	30	33	KΩ
Rdet_open	Open circuit resistance	Rdet @Cdet=0.15uF	500			KΩ
Cdet_good	Valid Cdet detection capacitance	@Rdet=25KΩ	0		0.15	uF
Cdet_bad	Invalid Cdet detection capacitance	@Rdet=25KΩ	10			uF
Parameter	**Description**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Classification						
Vclass	Classification voltage	V54 – PortNn, (n=0~7) @0mA≦Iclass≦50mA	15.5	18.0	20.5	V
Iclasslim	Classification current	V54=PortNn, (n=0~7)	51		100	mA

	limitation					
Iclass	Classification current	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
		Invalid class	51			
Vmark	Mark voltage	V54 – PortNn, (n=0~7) @0mA≦Imark≦10mA	7	9	10	V
Imarklim	Mark current limitation	V54=PortNn, (n=0~7)	5		100	mA
Tcle	Classification event time	Width for classification event 1 or event 2	6	12	30	ms
Tme1	Mark event 1 time	Width for mark event 1	6	9	12	ms
Tme2	Mark event 2 time	Width for mark event 2	16	22		ms
Tpon	Power turn on time	From end of valid detect to application of power to port		55	400	ms
Temperature Sensor						
Tsd	Thermal shutdown	Internal temperature for thermal shutdown		150		℃
Thy	Thermal shutdown hysteresis	Internal temperature for release thermal shutdown		129		℃

7.5 Digital Electrical Characteristics

Table 9 Digital Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I^2C & EEPROM interface						
VIL	Input low voltage	SCL/EE_CLK,SDAI/EE_DAT@ I^2C mode, SCAN0, SCAN1			0.8	V
VIH	Input high voltage	SCL/EE_CLK,SDAI/EE_DAT@I^2C mode, SCAN0, SCAN1	2.2			V
VOL	Open drain output low voltage	SCL/EE_CLK,SDAI/EE_DAT@auto mode @ Isink =5mA			0.7	V
VOL	Open drain output low voltage	SDAO,INTB,LED_CLK,LED_DAT @ Isink =5mA			0.7	V
Tscl	SCL/EE_CLK input	I^2C input clock			1	MHz
Tee	SCL/EE_CLK output	Output clock for EEPROM			1	MHz
T_{SDAO}	SDAO output Delay		350			ns
T_{SDAOH}	SDAO output Hold		125			ns
T_{SDAI}	SDAI Input Setup		50			ns
T_{SDAIH}	SDAI Input Hold		50			ns
Others						
VIL	Input low voltage	AD0~AD2			0.8	V
VIH	Input high voltage	AD0~AD2	2.2			V

7.6 AC Timing

7.6.1 Power On Sequence and Reset Timing

Description	Min.	Typ.	Max.	Unit
V54_Power on time@ V54 rising time from 0v to 57v		100	-	ms
V54 stable to RstN release	200			ms
Reset to System up time	150			ms

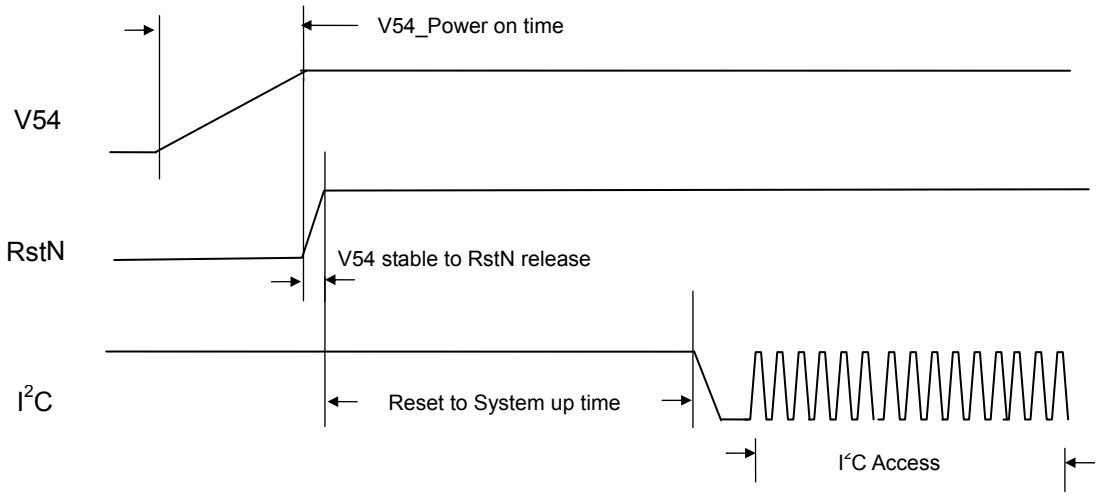


Figure 8 Power on Sequence and Reset Timing Diagram

7.6.2 EEPROM Timing

7.6.2.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns

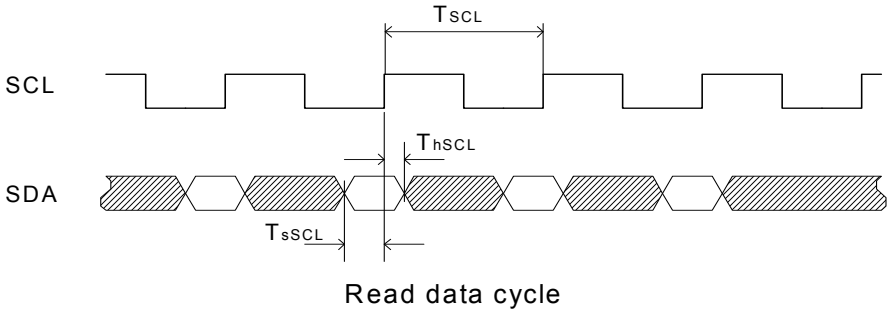


Figure 9 EEPROM Read Cycle Timing Diagram

7.6.2.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns

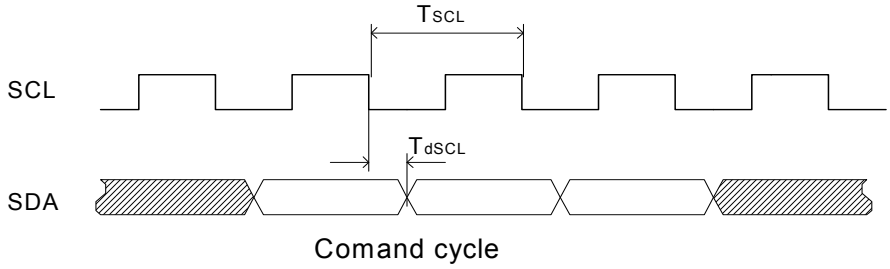


Figure 10 EEPROM Command Cycle Timing Diagram

7.6.3 I²C Timing

7.6.3.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	I²C clock period	1000	-	-	ns
T_{SDAO}	SDAO output delay	350	-		ns
T_{SDAOH}	SDAO output hold time of the last data bit	125	-	-	ns

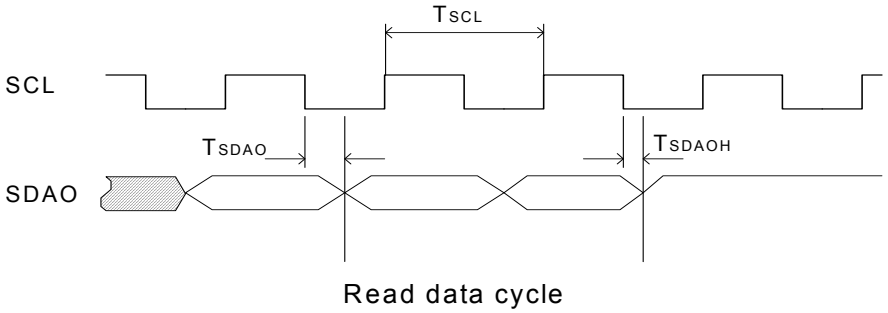


Figure 11 EEPROM Command Cycle Timing Diagram

7.6.3.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	I²C clock period	1000	-	-	ns
T_{SDAI}	SDAI setup time	50	-	-	ns
T_{SDAIH}	SDAI hold time	50	-	-	ns

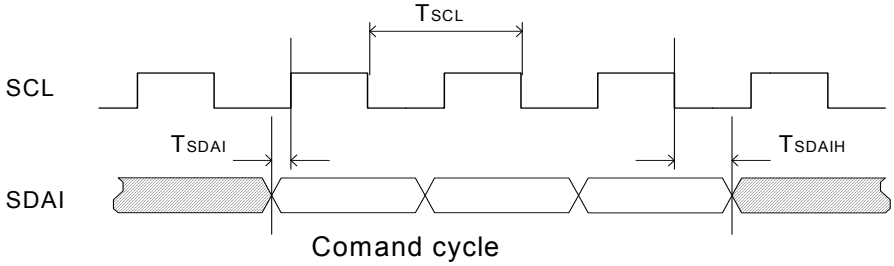


Figure 12 I²C Command Cycle Timing Diagram

7.7 Thermal Data

θ_{JA}	θ_{JC}	Ψ_{JT}	Conditions	Units
21	9.6	0.47	4 Layer PCB	°C/W

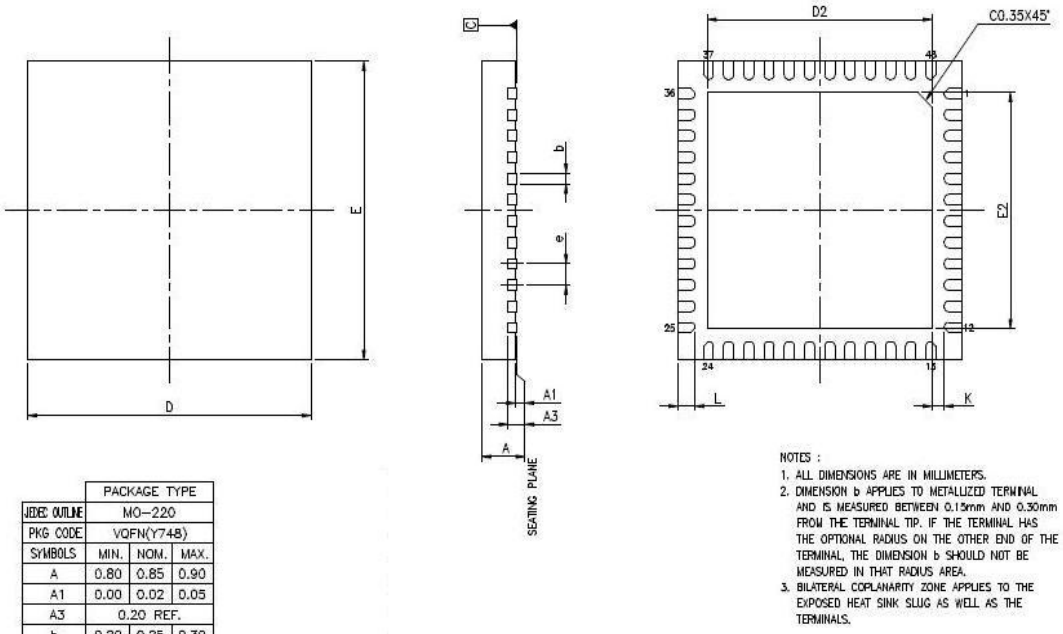
8 Order Information

Table 10 Order Information

Part No.	Package	Operating Temperature	Notice
IP808AR	48-Lead QFN	-40°C to 85°C	

9 Package Detail

9.1 48 QFN Outline Dimensions (in mm)



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y748)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
K	0.20	—	—

	D2			E2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.20	5.30	5.40	5.20	5.30	5.40	0.35	0.40	0.45	V	X	N/A

Figure 13 Package Outline Dimensions

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