Ground Fault Interrupter Earth Leakage Current Detector
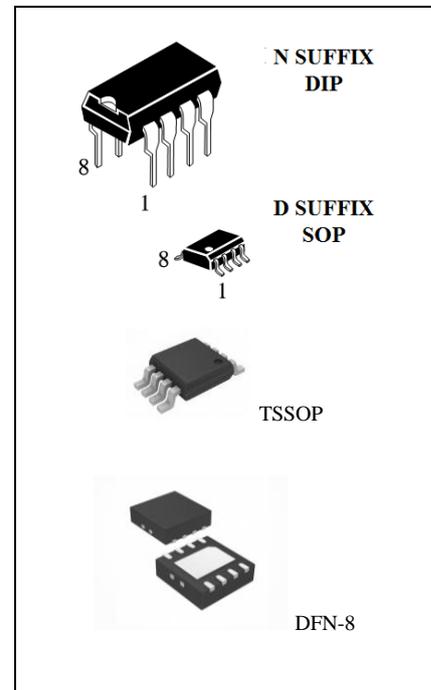
IL7101

DESCRIPTION

The IL7101 is designed for use in earth leakage circuit interrupters for operation directly off the AC Line in breakers.

It contains pre regulator, main regulator, after regulator, differential amplifier, level comparator, latch circuit. The input in the differential amp latch circuit. The input in the differential amplifier is connecting to the secondary node of zero current transformer.

The level comparator generates high level when earth leakage current is greater than some level.

FEATURE

- Low Power Consumption (P_D=5mW) 100V/200V
- 100V/200V Common Built-in Voltage Regulator
- High Gain Differential Amplifier
- High Input Sensitivity
- Minimum External Parts
- Large Surge Margin
- Wide Operating Temperature Range (T_A= -30 to 85°C)
- High Noise Immunity
- Meet U. L. 943 standards

N SUFFIX
DIP

D SUFFIX
SOP

TSSOP

DFN-8

ORDERING INFORMATION

Device	Trip Voltage (rms)	Operating Temperature Range	Package	Shipping
IL7101SN	11.5mV to 13.86mV		DIP-8	Tube
IL7101AN	13.86mV to 15.6mV			
IL7101SDT	11.5mV to 13.86mV		SOP-8	Tape& Reel
IL7101ADT	13.86mV to 15.6mV	T_A = -30° to 85° C		
IL7101STSDT	11.5mV to 13.86mV	for all packages	TSSOP-8	Tape& Reel
IL7102ATSDT	13.86mV to 15.6mV			
IL7101SDNT	TBD		DFN-8	Tape & Reel
IL7101ADNT	TBD			

## ABSOLUTE MAXIMUM RATINGS

- Supply Voltage   20V
- Supply Current   8mA
- Power Dissipation   200mW
- Operating Temperature   - 30 to 85°C
- Storage Temperature   - 55 to 125°C

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
These are stress ratings only and functional operation of the device at these or any other conditions beyond those
indicated under "recommended operating conditions" is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
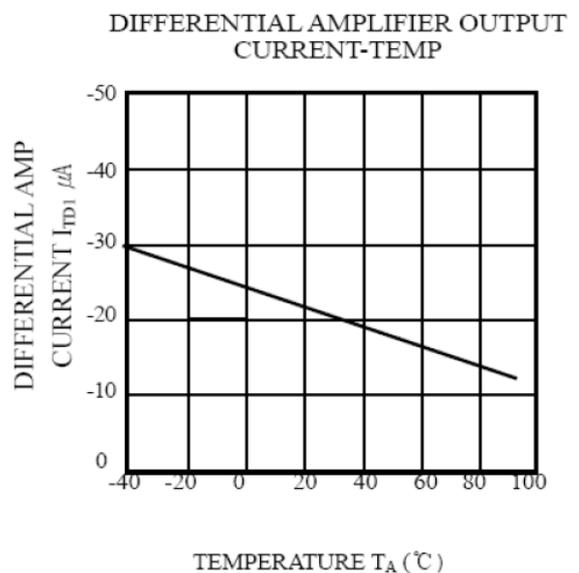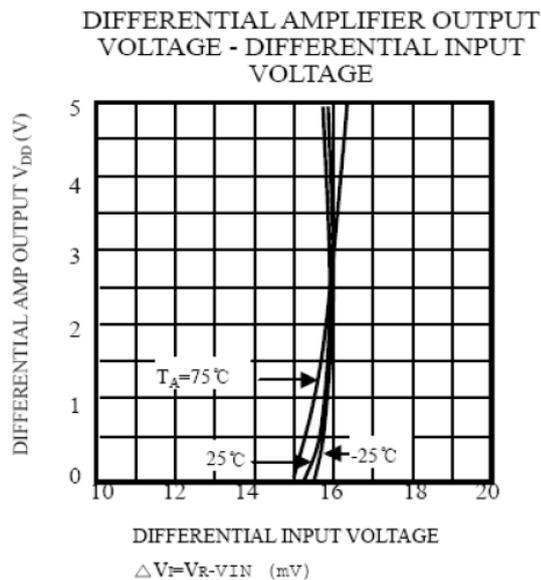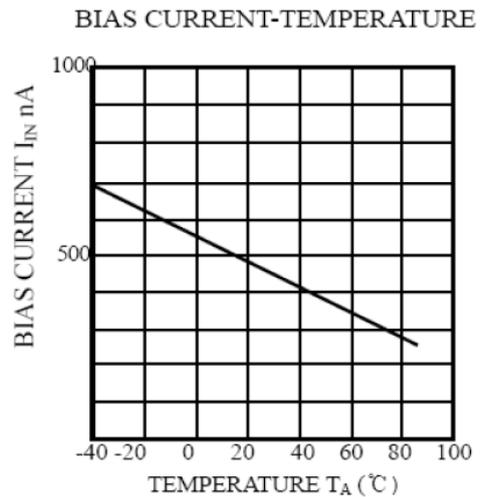
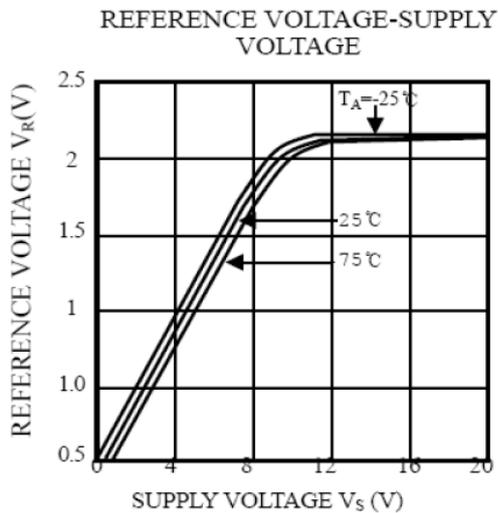### Pin Configuration

(Top View)

Block Diagram

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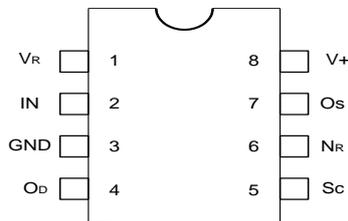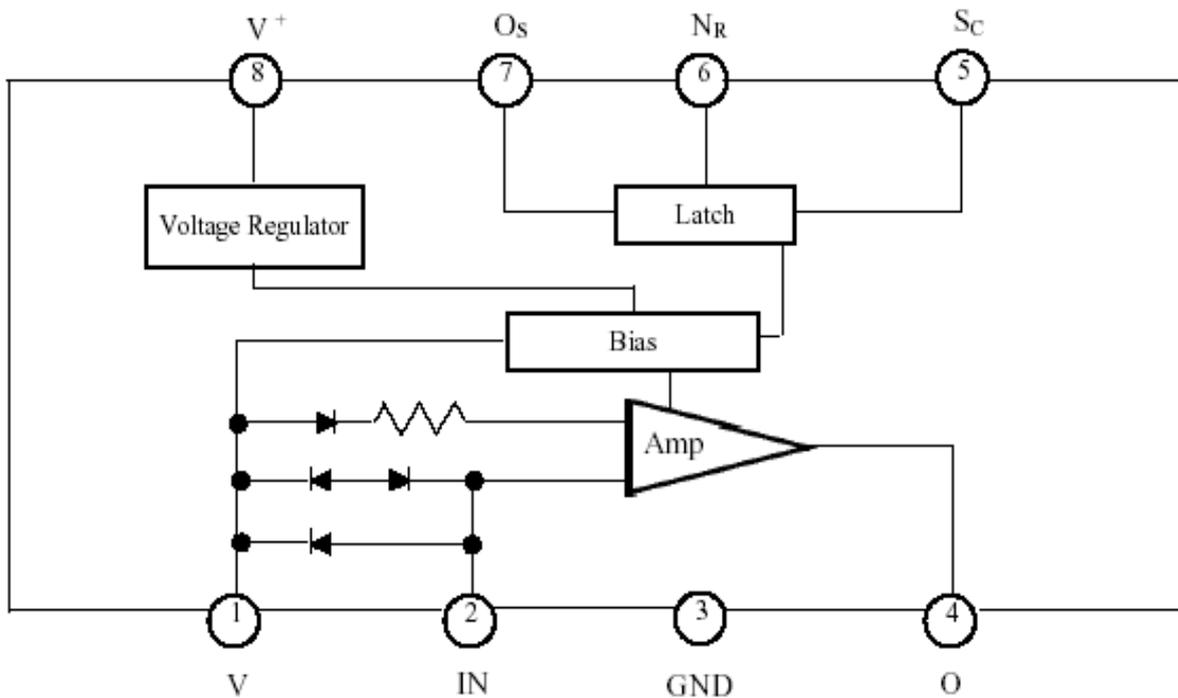
Recommended Operating Condition: T_A=-30°C to 80°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX	UNIT
Supply Voltage	V^+	12			V
Vs-GND Capacitor	Cvs	1			μF
O_S-GND Capacitor	Cos			1	μF

Electrical Characteristics

PARAMETER	SYMBOL	CONDTIONS		TEMP. (°C)	MIN.	TYP.	MAX.	UNIT	Test Circuit
Supply Current 1	I_{S1}	V^+=12V, $V_R - V_I$ = 30 mV		-30	-	-	580	μA	1
				25	-	400	530		
				85	-	-	480		
Trip Voltage	V_T	V^+ = 16V, $V_R - V_I$ = X	IL7101S	-30	11.5		13.86	mV (rms)	2
			IL7101A	85	13.86		15.6		
Differential Amplifier Output Current 1	I_{TD1}	V^+ = 16 V, $V_R - V_I$ = 30 mV V_{OD} = 1.2 V		25	-12	-	-30	μA	3
Differential Amplifier Output current 2	I_{TD2}	V^+ = 16 V, $V_R - V_I$ = short V_{OD} = 0.8 V		25	17	-	37	μA	4
Output Current	I_O	V_{SC} = 1.4 V V_{OS} = 0.8 V	I_{SI} = 580μA	-30	-200	-		μA	5
			I_{SI} = 530μA	25	-100	-			
			I_{SI} = 480μA	85	-75	-			
S_C ON Voltage	V_{SC} ON	V^+ = 16 V		25	0.7	-	1.4	V	6
S_C Input Current	I_{SC} ON	V^+ = I2V		25	-	-	5	μA	7
Output "L" Current	I_{OSL}	V^+ = 12 V, V_{OSL} = 0.2 V		-30 85	200	-	-	μA	8
Input Clamp Voltage	V_{IC}	V^+ = 12 V, I_{IC} = 20 mA		-30 85	4.3	-	6.7	V	9
Differential Input Clamp Voltage	V_{IDC}	I_{IDC} = 100mA		-30 85	0.4	-	2	V	10
Max. Current Voltage	V_{SM}	I_{SM} = 7 mA		25	20	-	28	V	11
Supply Current 2	I_{S2}	V_{OS} = 0.5 V, $V_R - V_I$ = X		-30 85	-	-	1200	μA	12
Latch Circuit Off Supply Voltage	V+ OFF			25	0.5			V	13
Response Time	T_{ON}	V^+ = 16 V, $V_R - V_I$ = 0.3 V		25	1	-	4	ms	14

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Typical Performance Curves

VOLTAE-SUPPLY VOLTAGE

SUPPLY CURRENT-SUPPLY VOLTAGE

REFERENCE VOLTAGE-SUPPLY VOLTAGE

BIAS CURRENT-TEMPERATURE

DIFFERENTIAL AMPLIFIER OUTPUT VOLTAGE - DIFFERENTIAL INPUT VOLTAGE

DIFFERENTIAL AMPLIFIER OUTPUT CURRENT-TEMP
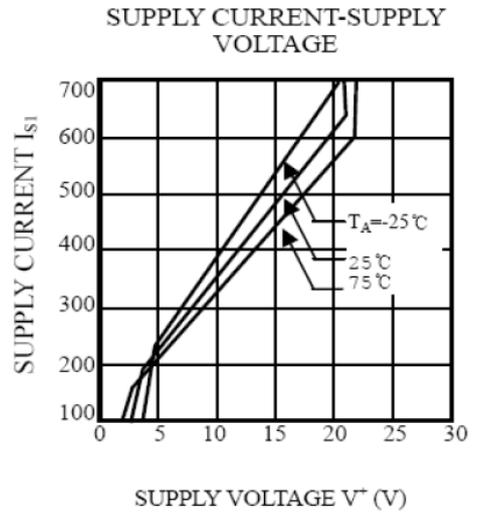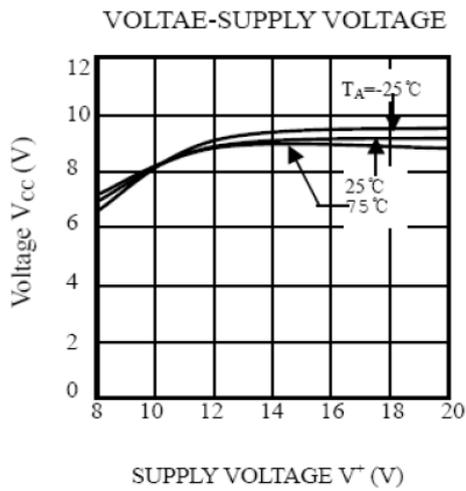
Test Circuit

1.

2.

3.

4.

5.

6.

7.

8.

9.

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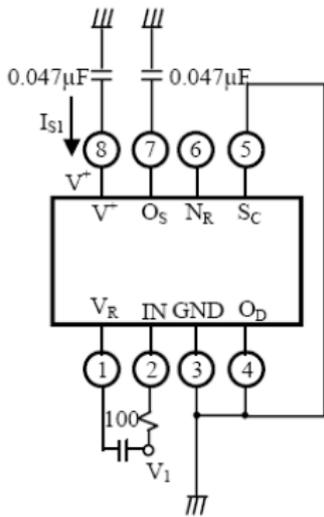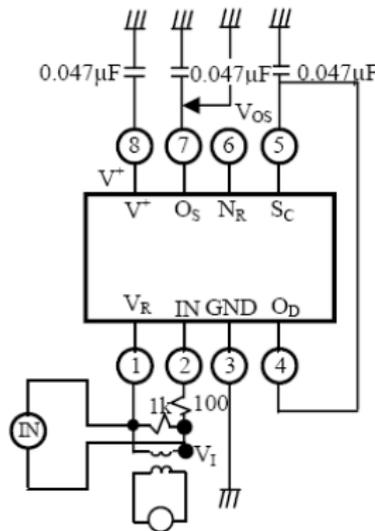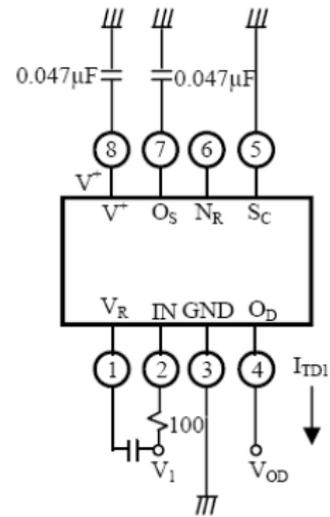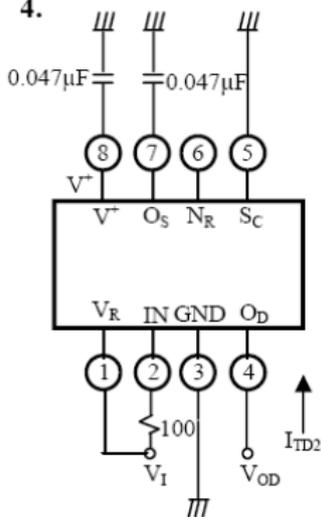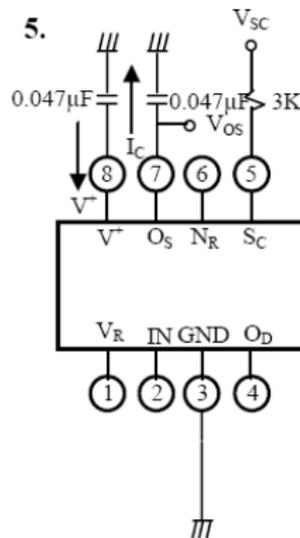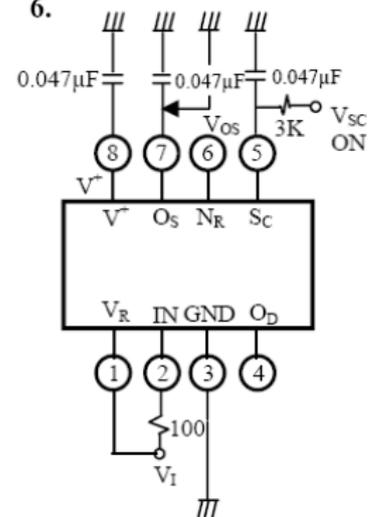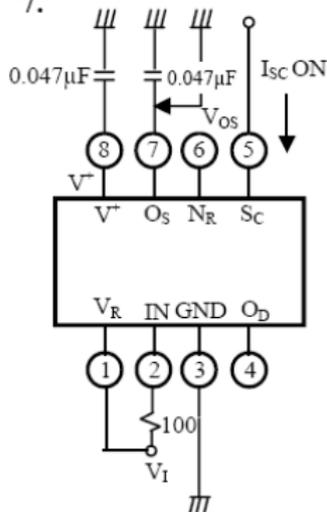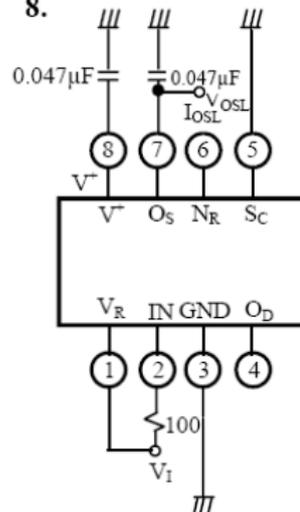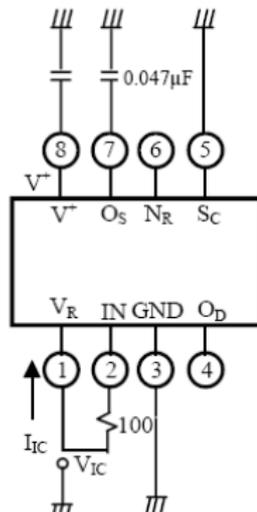
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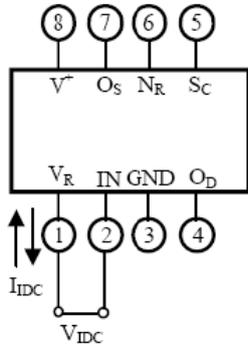
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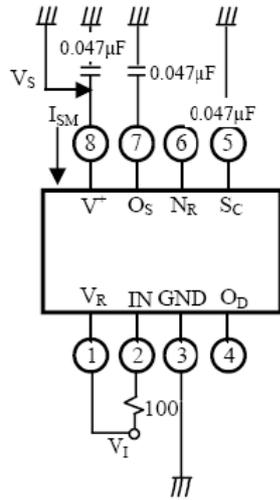
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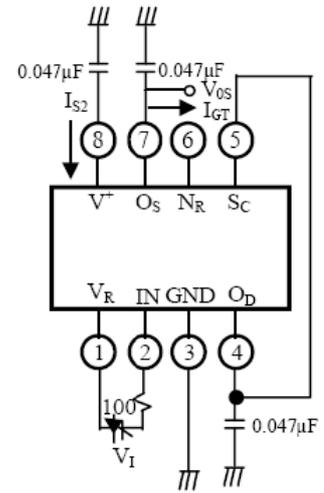
13.

14.

Typical Application

Supply voltage circuit is connected as a previous diagram. Please decide constants R1, R2, C4, and C5 of a filter in order to keep at least 12V in Vs, when normal supply current flows.

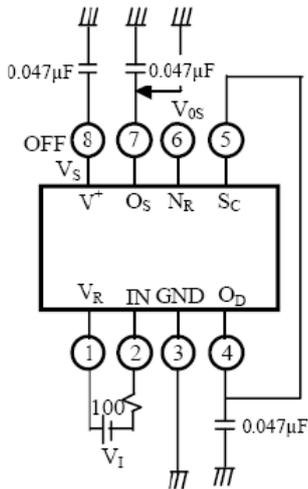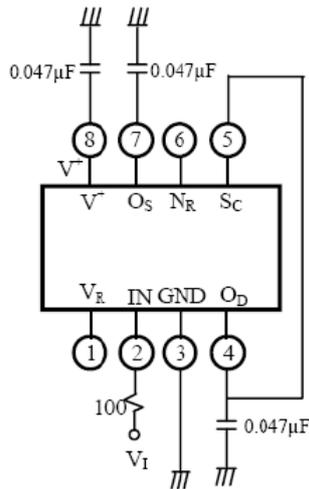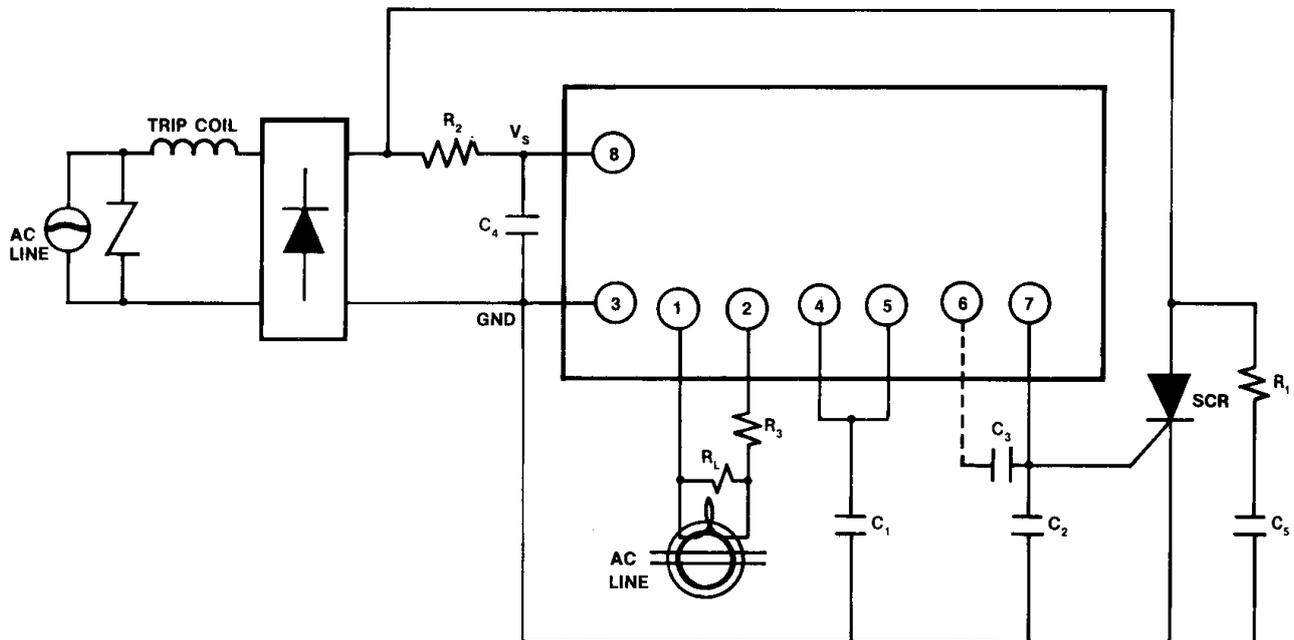In this case, please connect C4 (more than 1 μF) and C2 (less than 1 μF). ZCT and load resistance RL of ZCT are connected between input pin① and ②. In this case protective resistance (R3=100Ω) must be insulted. Sensitivity current is regulated by RL, and output of amplifier shows in pin④. External capacitor C1 between pin④ and GND is used for noise removal.

When large current is grounded in the primary side (AC line) of ZCT, the wave form in the secondary side of ZCT is distorted and some signals doesn't appear in the output of amplifier. So please connect a varistor or a diode (2pcs.) to ZCT in parallel.

Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.) latch circuit operates and supply gate current in the gate of SCR connected to the output pin⑦.

Pin⑥ can be used in the open state, but please connect capacitor (about 0.047 μF) between pin⑥ and ⑦.

Capacitor C6 between pin① and GND is used to remove noise and is about 0.047 μF.

N SUFFIX DIP
(MS – 001BA)
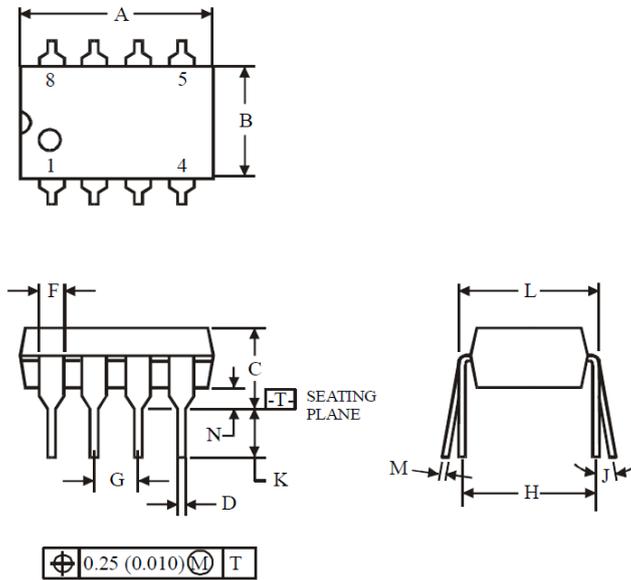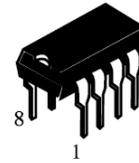
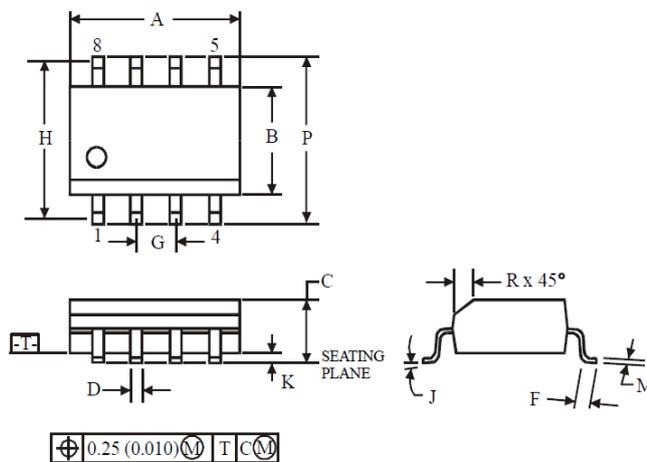| Symbol	Dimension, mm	
	MIN	**MAX**
A	8.51	10.16
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOP
(MS - 012AA)

Symbol	Dimension, mm	
	MIN	**MAX**
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.

2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B ‑ 0.25 mm (0.010) per side.

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TSSOP – 8 Package Dimension
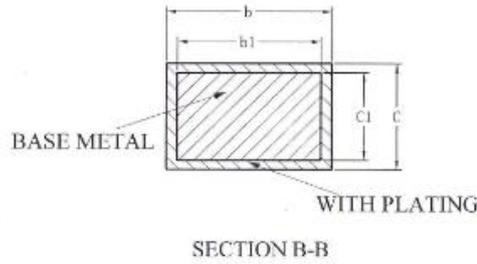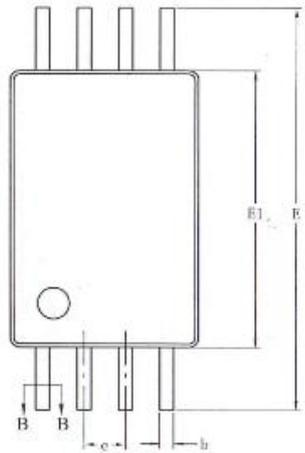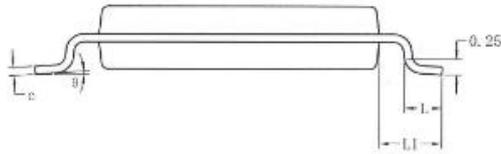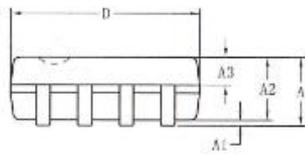
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

BASE METAL

WITH PLATING

SECTION B-B

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DFN – 8 Package Dimension
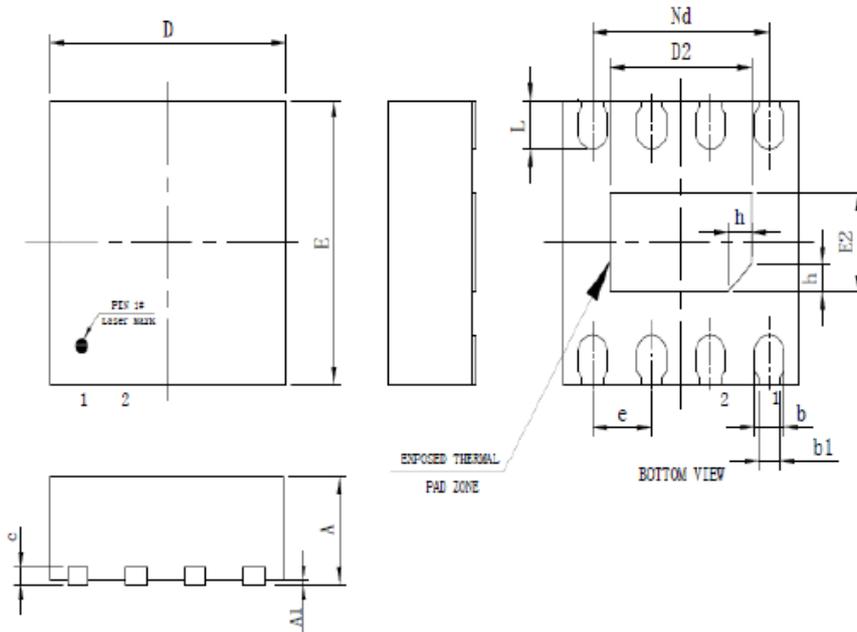
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
b1	0.18REF		
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.10	1.20	1.30
e	0.50BSC		
Nd	1.50BSC		
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
L	0.30	0.35	0.40
h	0.15	0.20	0.25

ENPOSED THERMAL
PAD ZONE

BOTTOM VIEW

Specification revisions history

Date	Rev	Changes	Remark
2018, Jun	05	Change the Trip voltage range	
2018, Oct	06	Added the TSSOP – 8 PKG	
2019. Apr	07	Added the DFN8 PKG	

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