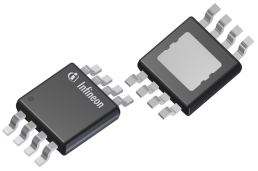
EiceDRIVER™ Power 2EP1xxR family datasheet

Full-bridge transformer driver for IGBT and SiC MOSFET gate driver supply

Technical documents

2EP100R, 2EP101R, 2EP110R, 2EP130R



Features

- Open loop full-bridge transformer driver for designing isolated gate driver supplies for a wide variety of switch technologies (IGBTs, SiC MOSFETs, GaN HEMTs, and others)
- Wide input supply range: from 4.5 V to 20 V
- Supports up to 5 W output power supplies
- Wide frequency range: from 50 kHz to 695 kHz with an internal oscillator or external clock
- Highly accurate duty-cycle adjustment: from 10% to 50%
- Adjustable overcurrent threshold
- Short circuit protection for power outputs
- Overtemperature protection
- Ready output to indicate normal operation
- Small, space-saving package

Potential applications

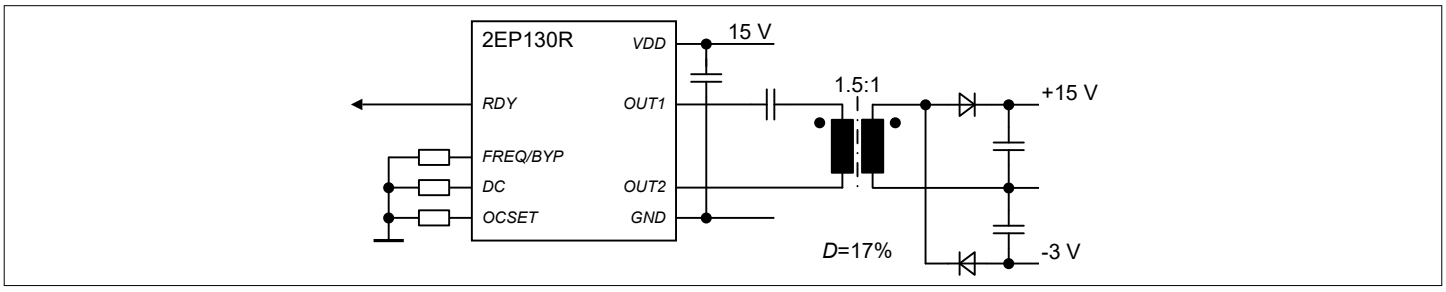
- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters
- UPS and energy storage systems
- Welding
- Commercial air-conditioning
- High-voltage DC-DC converters and DC-AC inverters
- Isolated switch-mode power supplies
- Power meters

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2EP1xxR is a full-bridge transformer driver family providing up to 13 W at its outputs for an open-loop isolated supply. It is optimized to supply gate drivers for a variety of switches such as TRENCHSTOP™ IGBTs, OptiMOS™ MOSFETs, CoolMOS™ super-junction MOSFETs, CoolGaN™ high electron mobility transistors, and CoolSiC™ MOSFETs together with EiceDRIVER™ gate driver ICs, and other similar products.



Schematic example for 2EP130R

The 2EP1xxR family offers the following product variants:

- 2EP100R and 2EP101R are optimized for low-component count designs for IGBT and SiC MOSFET gate driver supplies
- 2EP110R allows a fine duty-cycle adjustment to adapt the output voltage ratio to the application requirements of SiC and GaN power switches
- 2EP130R is optimized for highly flexible designs to adapt to different application requirements. It provides:
  - 5-step overcurrent protection

- 41 selectable switching frequencies or synchronization to external PWM for transformer adaptation
- 41 selectable duty-cycle options to adjust the output supply voltage

All 2EP1xxR family variants provide several safety functions to secure safe device operation, such as:

- UVLO monitoring
- Overtemperature protection
- Short circuit protection for the outputs
- Average overcurrent protection
- Soft start
- Ready output

The 2EP1xxR family is available in the thermally enhanced package, PG-TSSOP-8-1, with a fine pitch of 0.65 mm.

Part number	Function			Adjustment method	Marking
	Frequency	Duty cycle	Overcurrent setting		
2EP100R	65 kHz, 103 kHz	33%, 50%	*OCSET,4*	Pin strapping	2EP100
2EP101R	50 kHz, 65 kHz	12%, 17%	*OCSET,4*	Pin strapping	2EP101
2EP110R	50 kHz, 65 kHz	10% .. 50%	*OCSET,4*	Pin strapping and resistor (*DC*)	2EP110
2EP130R	50 kHz .. 695 kHz	10% .. 50%	*OCSET,1 .. 5*	Resistor	2EP130

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1 Block diagram

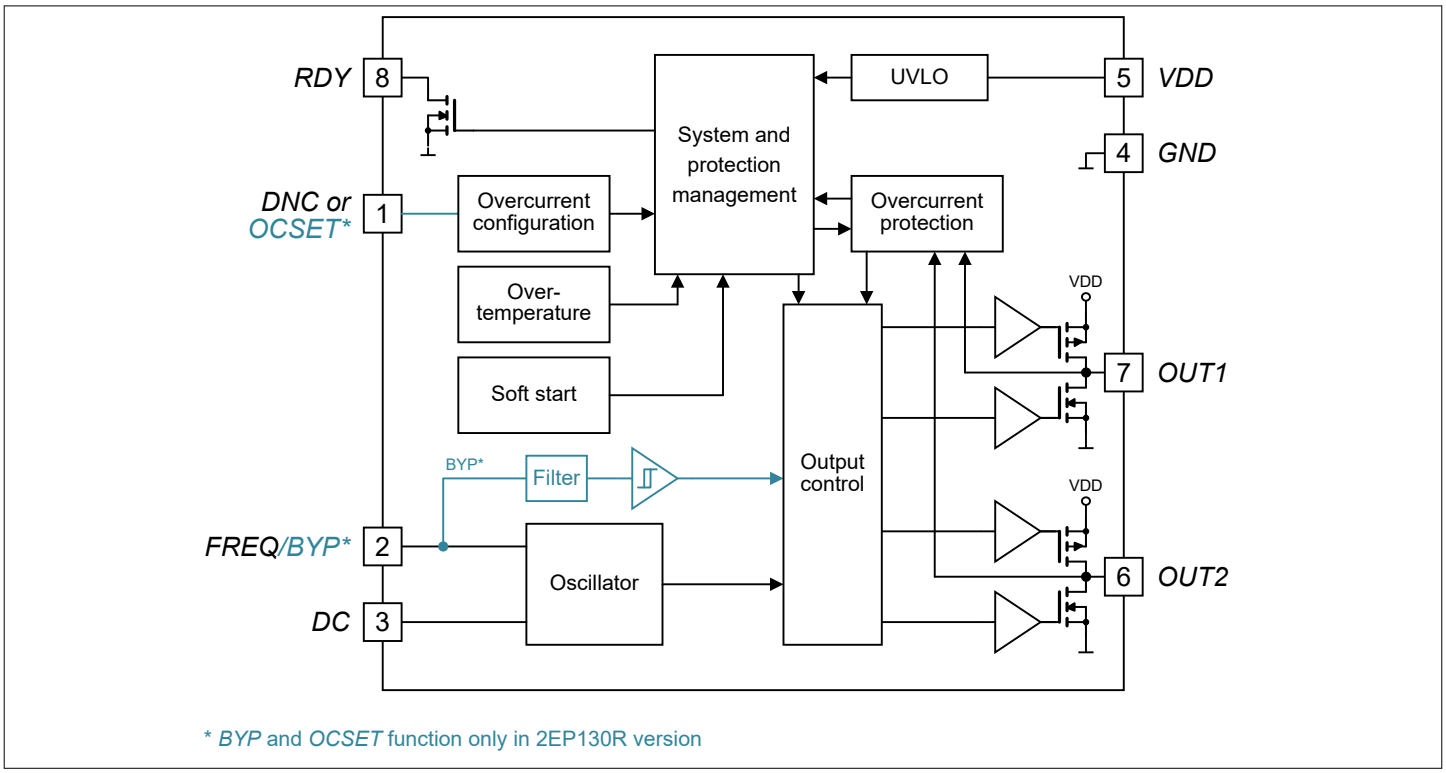


Figure 2 Block diagram 2EP1xxR family

2 Pin configuration and functionality

2.1 Pin configuration for 2EP100R, 2EP101R, and 2EP110R

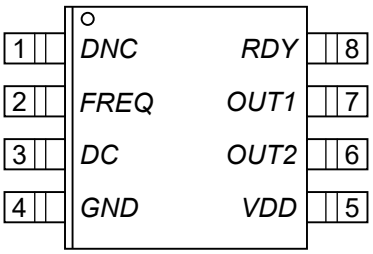


Figure 3 Pin-out for 2EP100R, 2EP101R, and 2EP110R in PG-TSSOP-8-1 (top view)

Table 1 Pin configuration for 2EP100R, 2EP101R, and 2EP110R

Pin no.	Pin name	Pin type	Buffer type	2EP110R	2EP100R and 2EP101R
1	*DNC*	-	-	DNC or connect to *GND*	
2	*FREQ*	DI, logic	digital	Connect to *GND* or leave floating/connect to voltage > 3 V	
3	*DC*	AI, logic	analog, digital	Duty cycle adjustment input (place a resistor to *GND*)	Connect to *GND* or leave floating/connect to voltage > 3 V
4	*GND*	GND	-	Power and signal ground	

(table continues...)

Table 1 (continued) Pin configuration for 2EP100R, 2EP101R, and 2EP110R

Pin no.	Pin name	Pin type	Buffer type	2EP110R	2EP100R and 2EP101R
5	*VDD*	PWR	-	Positive power supply	
6	*OUT2*	PWR	PP	Second output of the full-bridge	
7	*OUT1*	PWR	PP	First output of the full-bridge	
8	*RDY*	O	OD	Ready output, high active, reports correct device operation, switching outputs	
EP	*GND*	GND	-	Exposed pad, connect to *GND*	

2.2 Pin configuration for 2EP130R

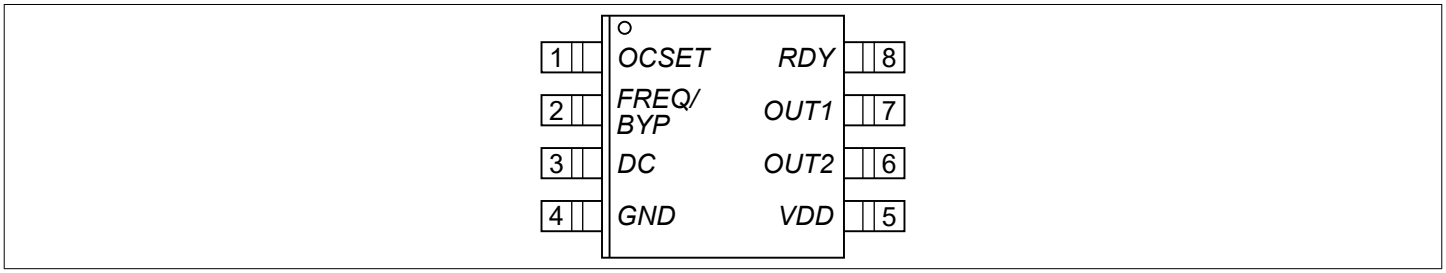


Figure 4 Pin-out for 2EP130R in PG-TSSOP-8-1 (top view)

Table 2 Pin configuration for 2EP130R

Pin no.	Pin name	Pin type	Buffer type	Function for 2EP130R
1	*OCSET*	AI, logic	analog	Average overcurrent set input (place a resistor to *GND*)
2	*FREQ/BYP*	AI, logic	analog, TTL	Frequency adjustment input (place a resistor to *GND*) or external clock input in bypass mode (connect a PWM signal with required frequency and duty cycle)
3	*DC*	AI, logic	analog	Duty cycle adjustment input (place a resistor to *GND*) or bypass enable (connect to *GND*)
4	*GND*	GND	-	Power and signal ground
5	*VDD*	PWR	-	Positive power supply
6	*OUT2*	PWR	PP	Second output of the full-bridge
7	*OUT1*	PWR	PP	First output of the full-bridge
8	*RDY*	O	OD	Ready output, high active, reports correct device operation, switching outputs
EP	*GND*	GND	-	Exposed pad, connect to *GND*

3 Functional description

The 2EP1xxR is optimized for asymmetric gate driver supply due its unique duty-cycle adjustment options. It still supports symmetric output supply as well as a wide variety of other single or dual output voltages.

The 2EP1xxR products directly drive a transformer in different topologies, for example:

- Full-bridge with a direct-coupled transformer and a voltage-doubler output rectification for output voltage with a ratio of 2:1

- Full-bridge with a direct-coupled transformer and peak rectification for symmetric output supplies
- Full-bridge with a series capacitor between *OUT1*/*OUT2* and transformer, and peak rectification for asymmetric output supplies

2EP1xxR reads its configuration from the *FREQ*, *FREQ/BYP*, *OCSET*, and *DC* pins after powering up and stores it internally during operation. A change of configuration at these pins is effective with the next read cycle after a power up.

3.1 Output stage

The 2EP1xxR family uses a low-ohmic, integrated, rail-to-rail, full-bridge power stage with fast slew rate. This enables the transformer driver to switch efficiently at a high switching speed.

3.2 Monitoring and protection

The 2EP1xxR family is equipped with several monitoring and protection features to ensure device safe operation for both, application and device:

- UVLO protection to ensure that the device operates correctly above the UVLO threshold. It preliminary prevents incorrect operation of the device below the UVLO threshold
- Detecting if the adjustment resistor is out of range
- Ready indication via *RDY* output
- Adjustable average overcurrent protection
- Short circuit protection (peak overcurrent)
- Overtemperature protection

The overcurrent protection and overtemperature protection are designed as protection elements. Do not operate under overload conditions for a prolonged periods to avoid reducing the lifetime or damaging the device.

3.2.1 Average overcurrent protection

The overcurrent protection is an average overcurrent protection of *OUT1*/*OUT2*.

The average overcurrent triggers a shutdown if the output current of the device is above the dedicated overcurrent threshold, $I_{OCthr,x}$, for more than half the on-time for two consecutive cycles. The same rule applies for the off-time, at that same output with its overcurrent threshold. Due to the open loop nature of the IC, the effectiveness of overcurrent protection at the output of the isolated supply is dependent on the circuit between *OUT1*/*OUT2* and the isolated power supply outputs.

Overcurrent sensing principal

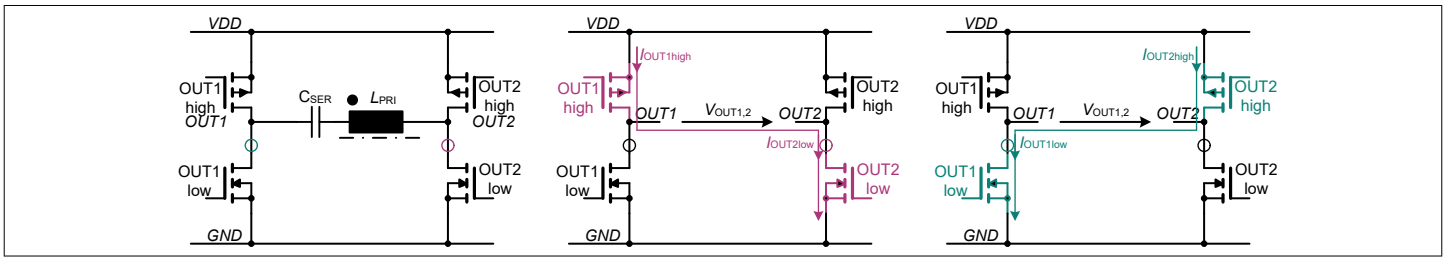


Figure 5 Location of current sensing and current path during operation

The following figures show the current path and the current sensing location of the transformer driver, 2EP1xxR. The current sensing is implemented at the low side switches as indicated by the circles close to the *OUT1* and *OUT2* drain connections. As the series capacitor, C_{SER}, and the primary side of the transformer, L_{PRI}, are connected in series between the pins *OUT1* and *OUT2*, the current path will always include one high side switch and one low side switch.

Asymmetric load current at duty cycles below 50%

Every duty cycle configuration except 50% introduces a DC offset to the transformer input voltage. This DC offset allows for asymmetric output voltages after peak rectification. However, the application requires a constant output power that is not dependent on the output voltage level. This results in asymmetric input currents for individual sections during the switching period. To compensate for these asymmetric currents, the transformer driver 2EP1xxR adjusts the individual overcurrent limits according to the configured duty cycle.

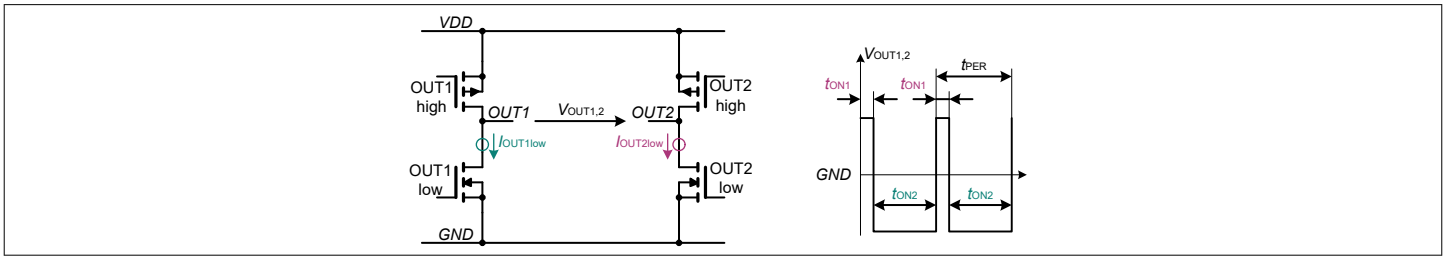


Figure 6 Current path mapping to individual segments of the switching period

This diagram shows the mapping of the individual current paths to the timing diagram of the outputs:

- Current during t_{ON1} flows through the *OUT1* high-side and the *OUT2* low-side switch
- Current during t_{ON2} flows through the *OUT2* high-side and the *OUT1* low-side switch

The duration of t_{ON1} together with the time period, t_{PER}, defines the duty cycle $D = \frac{t_{ON1}}{t_{PER}}$

The absolute thresholds of these individual overcurrent limits depend on the product variant. 2EP100R, 2EP101R, and 2EP110R use the overcurrent setting level 4. 2EP130R offers a dedicated pin, *OCSET,* to configure the overcurrent setting level.

Table 3 Individual overcurrent thresholds depending on the configured duty cycle, *D,* and overcurrent setting level, *OCSET*

OCSET	**Ranges of duty cycle *D***					
	10% - 14%		**15% - 35%**		**36% - 50%**	
	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**	***OUT1* high *OUT2* low**	***OUT2* high *OUT1* low**
1	$I_{OCthr,3}$	$I_{OCthr,0}$	$I_{OCthr,2}$	$I_{OCthr,0}$	$I_{OCthr,1}$	$I_{OCthr,1}$
2	$I_{OCthr,4}$	$I_{OCthr,0}$	$I_{OCthr,3}$	$I_{OCthr,1}$	$I_{OCthr,2}$	$I_{OCthr,2}$
3	$I_{OCthr,5}$	$I_{OCthr,1}$	$I_{OCthr,4}$	$I_{OCthr,2}$	$I_{OCthr,3}$	$I_{OCthr,3}$
4	$I_{OCthr,6}$	$I_{OCthr,2}$	$I_{OCthr,5}$	$I_{OCthr,3}$	$I_{OCthr,4}$	$I_{OCthr,4}$
5	$I_{OCthr,7}$	$I_{OCthr,3}$	$I_{OCthr,6}$	$I_{OCthr,4}$	$I_{OCthr,5}$	$I_{OCthr,5}$

3.2.1.1 Fixed average overcurrent protection in 2EP100R, 2EP101R, and 2EP110R

Average overcurrent limit (*OUT1*, *OUT2*) for 2EP100R, 2EP101R, and 2EP110R is set to *OCSET,4*.

The duty-cycle dependent overcurrent settings as shown in Table 3 allow the transformer driver to maximize its output power. Please note that the duty cycle for the *OUT2* high-side and *OUT1* low-side switch become more than 50% for duty cycle selections of $D < 50\%$. Figure 7 shows therefore, the average overcurrent threshold values over the whole duty-cycle range for *OCSET,4*.

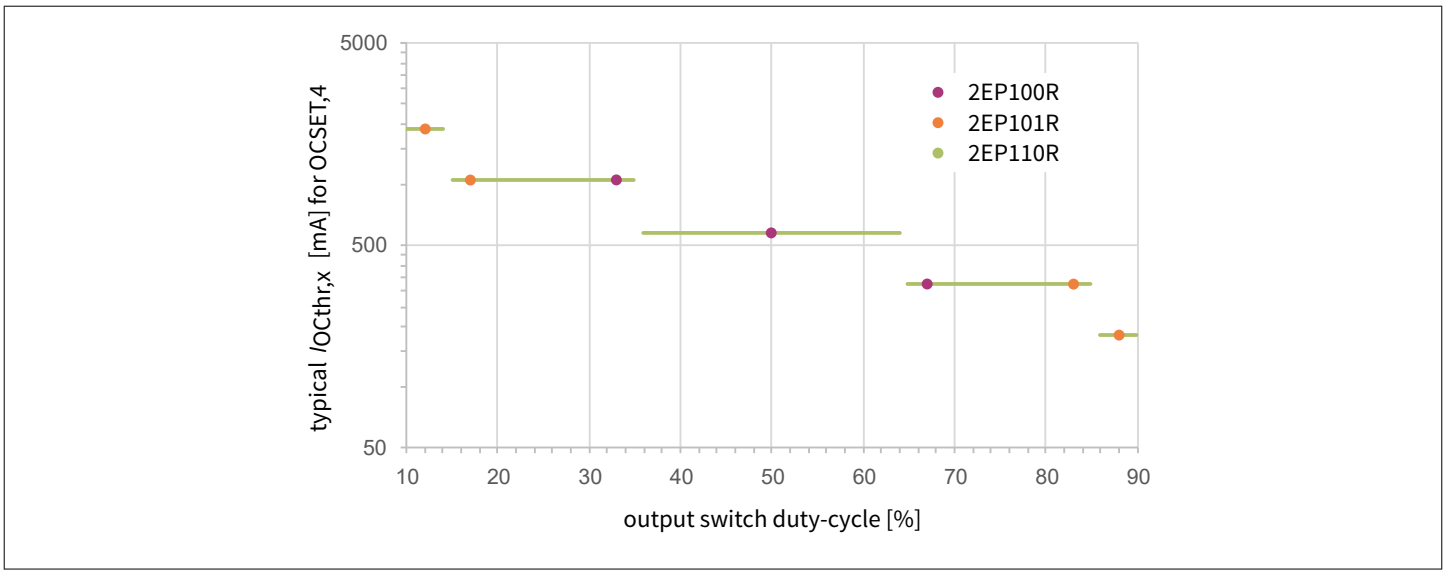


Figure 7 Duty-cycle dependent average overcurrent threshold for 2EP100R, 2EP101R, and 2EP110R

3.2.1.2 Adjustable average overcurrent protection in 2EP130R

The adjustable average overcurrent protection feature of 2EP130R allows users to tailor the overcurrent protection for different application power levels.

A resistor from *OCSET* pin to *GND* sets one out of the five average overcurrent settings, *OCSET,x*. Figure 8 shows the recommended E96 resistor values. Within the resistor value range resulting in the same overcurrent setting *OCSET,x* any resistor value is acceptable. For example: *OCSET,4* has a resistor value range of 9530 Ω to 23700 Ω.

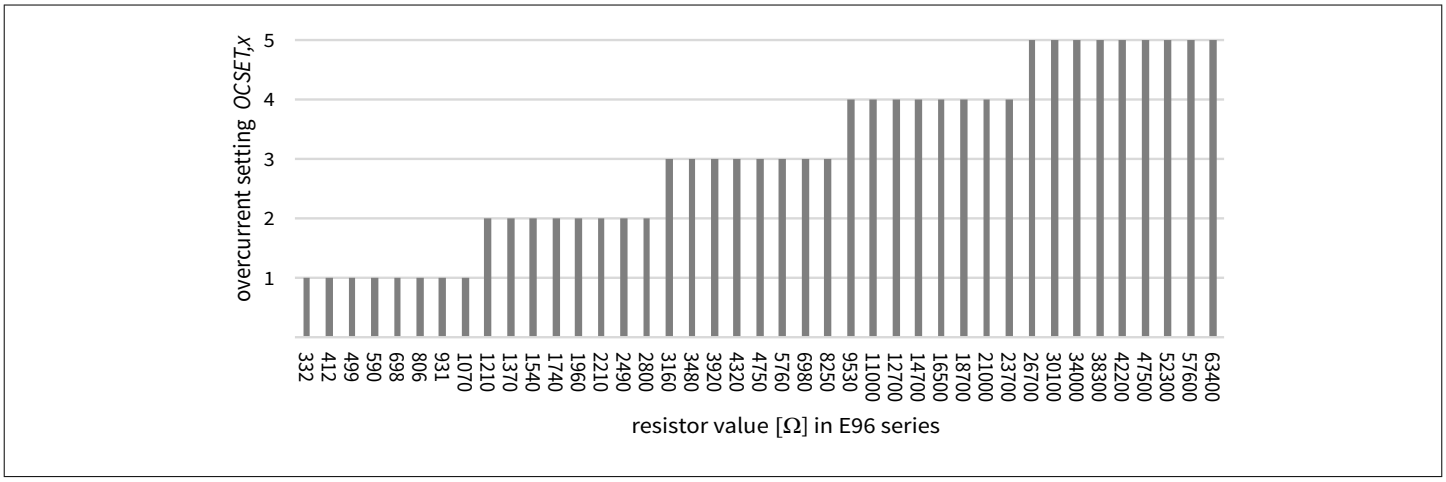


Figure 8 Average overcurrent protection settings via resistor configuration for 2EP130R

The duty-cycle dependent overcurrent settings as shown in Table 3 allow the transformer driver to maximize its output power. Please note that the duty cycle for the *OUT2* high-side and *OUT1* low-side switch becomes more than 50% for duty cycle selections of $D < 50\%$. Figure 9 shows therefore, the average overcurrent threshold values over the whole duty cycle range. The five overcurrent settings share a total of eight average overcurrent threshold values.

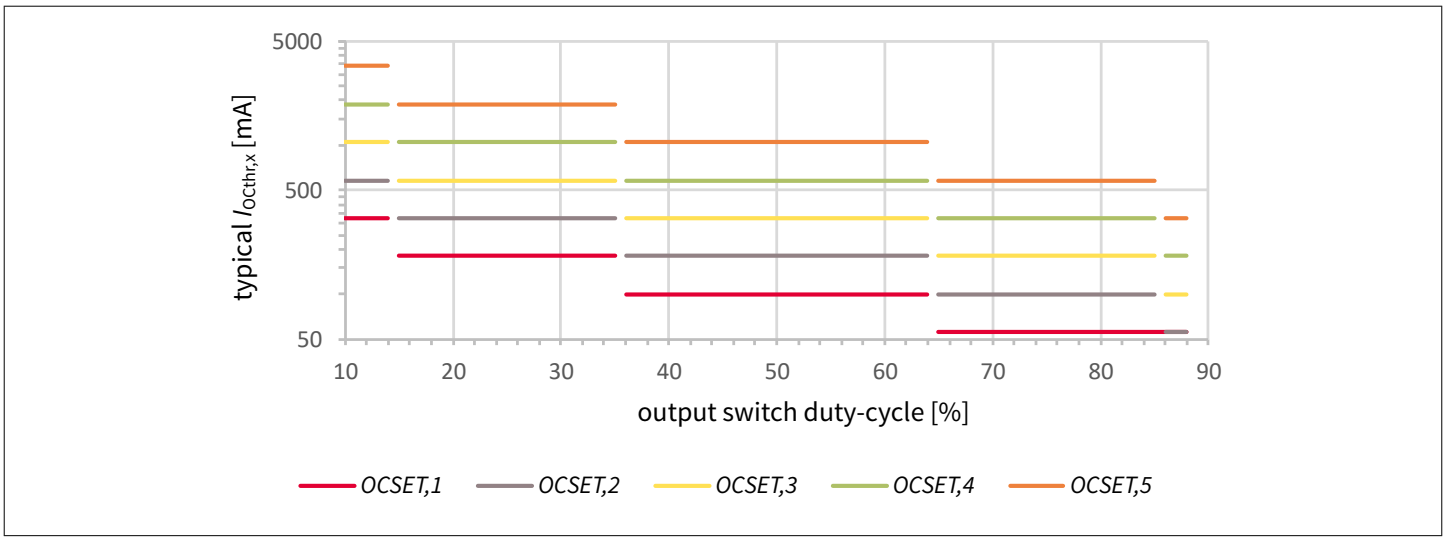


Figure 9 Duty-cycle dependent average overcurrent threshold for 2EP130R

3.2.2 Short circuit protection

All variants of the 2EP1xxR family protect the device through a fixed but filtered short circuit protection (peak current protection).

The short circuit protection (peak overcurrent) of the outputs protect against solder splash or other low-ohmic shorts of the outputs *OUT1*/*OUT2* to supply *VDD* or *GND* rail.

3.2.3 Overtemperature protection

The overtemperature protection triggers a shutdown of the IC in high ambient temperature environments or without sufficient cooling. This protects the IC against thermal stress beyond its maximum rating.

3.2.4 Out-of-range detection for external resistors in 2EP110R and 2EP130R

The input pins of the 2EP110R (*DC* pin only) and the 2EP130R (*DC*, *FREQ/BYP*, *OCSET* pins) for the external resistors have an out-of-range detection circuit.

This ensures that the transformer drivers only start if those resistor values are within their specified operating range (200 Ω < R_{set} < 82 kΩ) or activate an alternative operating mode (2EP130R *DC* pin to *GND*: bypass mode). 2EP1xxR continuously repeats the resistor read-out at start-up until all resistor values are within the range. During the repetitive read-out phase, the *RDY* pin stays low and the output stage stays in tri-state. The following table lists the out-of-range detection values for 2EP110R and 2EP130R.

Pin name	Product	R_{set} < 200 Ω	R_{set} > 82 kΩ
DC	2EP130R	Activates bypass mode	Out of range
DC	2EP110R	Out of range	
OCSET	2EP130R		
FREQ/BYP	2EP130R		

3.2.5 Adjustable resistor's filtering capacitor range

The transformer driver 2EP110R and 2EP130R support filter capacitors at the input pins for external resistors, depending on the individual resistor value connected to that pin. This filtering method is suitable for application circuits with high noise expectancy even at power supply start-up.

This selection of optional filter capacitor value applies to the following pins and product variants:

- *DC*: 2EP110R and 2EP130R

- *FREQ/BYP*: 2EP130R only
- *OCSET*: 2EP130R only

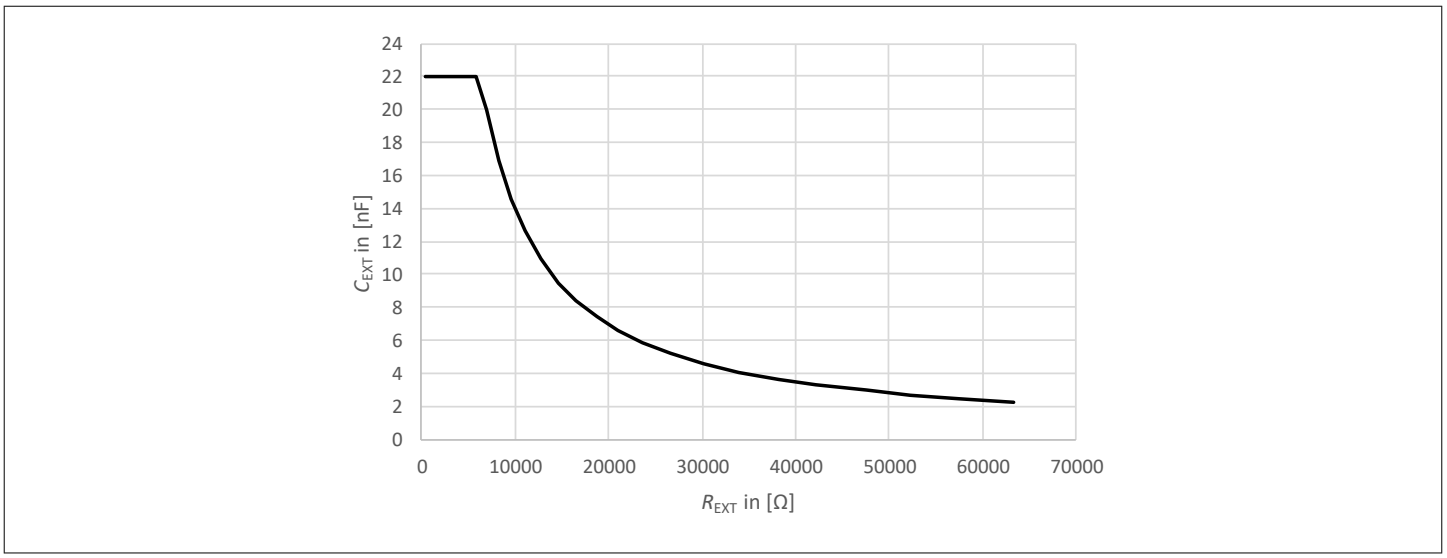


Figure 10 Maximum filtering capacitor value C_{EXT} over adjustment resistor value R_{EXT}

3.2.6 Ready output –*RDY*

The ready output, *RDY,* is an open-drain output. Use an external pull-up circuit to a voltage supply of up to 5.5 V for a proper logic output signal.

During operation, a high at the *RDY* pin indicates that the:

- Device is properly supplied (>UVLO)
- Device is configured
- Soft start has finished
- Outputs are switching

During operation, a low at the *RDY* pin indicates that the:

- Device has a fault status:
  - Average overcurrent protection triggered
  - Peak current protection triggered
  - Overtemperature triggered
  - Loss of synchronization
- Read-out resistor is out of range
- Waiting for the bypass signal
- Device in wait cycle
- Device in soft start

3.3 Frequency setting

The 2EP1xxR family offers three operating modes to adjust the switching frequency:

- Pin strapping: 2EP100R, 2EP101R, and 2EP110R
- Resistor adjustment: 2EP130R
- Bypass mode: 2EP130R, see Chapter 3.5

3.3.1 Frequency setting by pin strapping in 2EP100R, 2EP101R, and 2EP110R

The products 2EP100R, 2EP101R, and 2EP110R provide the option of selecting a frequency via the following pin strapping methods:

- Connecting the pin *FREQ* to *GND* with a resistance lower than 1 kΩ enables a lower switching frequency
- Leaving the pin *FREQ* open or connecting a resistance larger than 4.7 kΩ to *GND* enables a higher switching frequency

3.3.2 Frequency setting by resistor configuration in 2EP130R

2EP130R provides the option to select frequencies over a wide range, from 50 kHz to 695 kHz. This helps in adapting the device to different application conditions, including transformer parameters.

A resistor from *FREQ/BYP* pin to *GND* sets one out of 41 discrete switching frequencies. Figure 11 shows the resulting switching frequency over the recommended E96 series resistor values. In case any other value within the allowed external resistor value range has been selected, the transformer driver selects the frequency matching to the closest resistor value of these recommended E96 resistor values.

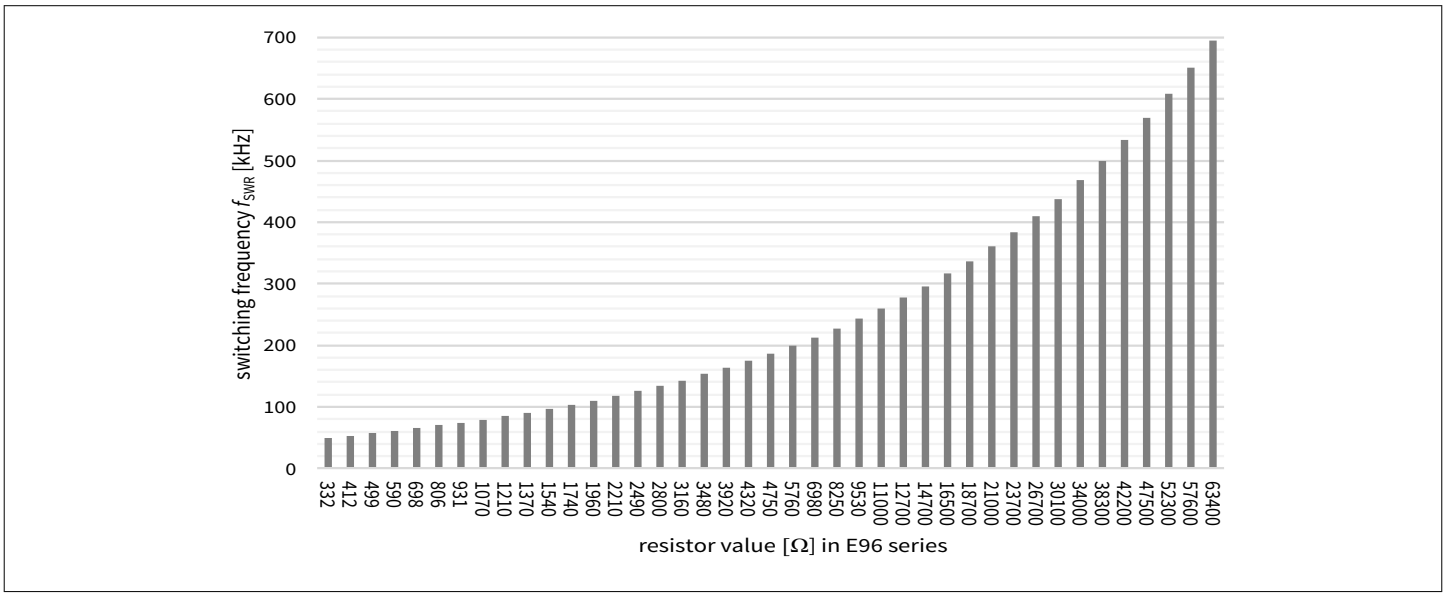


Figure 11 Frequency setting by resistor configuration for 2EP130R

3.4 Duty-cycle setting

The 2EP1xxR family offers three operating modes to adjust the highly accurate duty cycle:

- Pin strapping for 2EP100R and 2EP101R
- Resistor setting for 2EP110R and 2EP130R
- Bypass mode for 2EP130R, see Chapter 3.5

A duty-cycle setting other than 50% is mainly used in application circuits with a series capacitor at the primary side and peak rectification at the secondary side of the transformer. Such a configuration allows users to adjust the ratio of the positive to the negative isolated output voltage. The transfer ratio of the transformer defines the relation between the transformer's input and output voltages. Both measures together enable the adjustment of the output voltage for positive and negative rail in a wide voltage range.

3.4.1 Duty-cycle setting by pin strapping in 2EP100R and 2EP101R

The products 2EP100R and 2EP101R provide the option of selecting a duty cycle via the following pin strapping methods:

- Connecting the pin *DC* to *GND* with a resistance lower than 1 kΩ enables a lower duty cycle
- Leaving the pin *DC* open or connecting a resistance larger than 4.7 kΩ to *GND* enables a higher duty cycle

3.4.2 Duty-cycle setting by resistor configuration in 2EP110R and 2EP130R

The products 2EP110R and 2EP130R provide the option of selecting duty cycle over a wide range, from 10% to 50%. A resistor from *DC* pin to *GND* sets one out of the 41 duty cycles in single percentage steps.

Figure 12 shows the resulting duty cycle over the recommended E96 series resistor values. In case any other value within the allowed external resistor value range has been selected, the transformer driver selects the duty cycle matching to the closest resistor value of these recommended E96 resistor values.

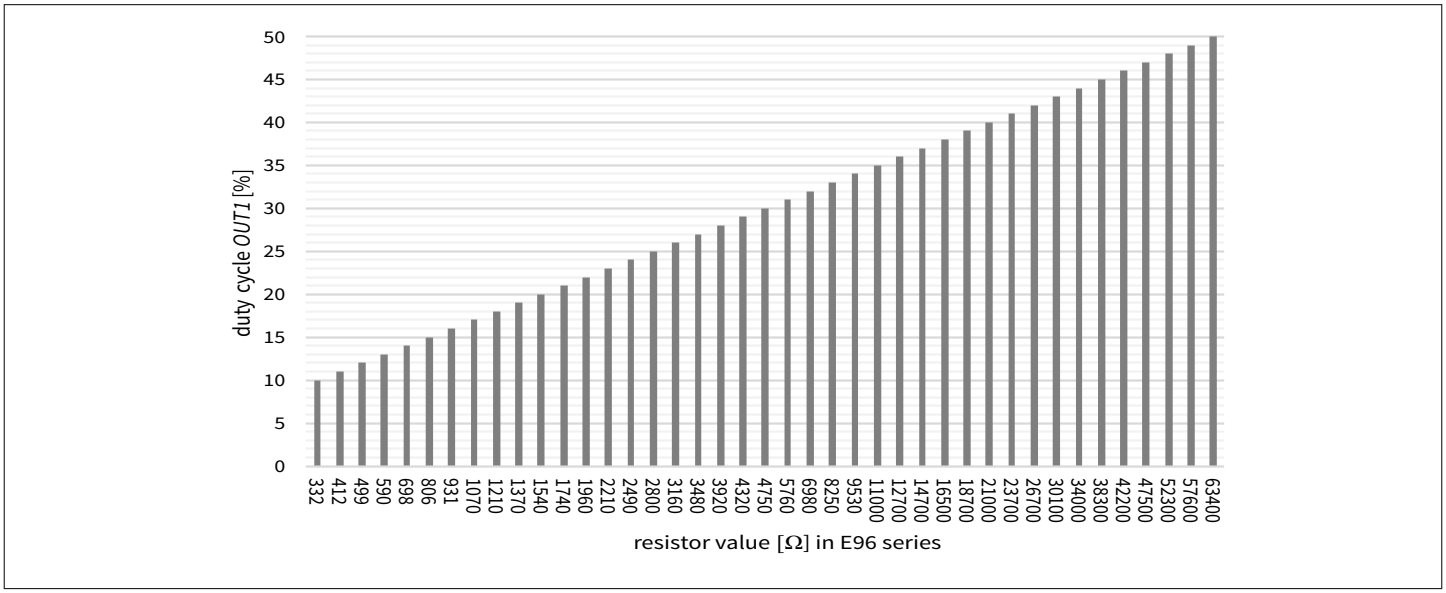


Figure 12 Duty-cycle setting by resistor configuration for 2EP110R and 2EP130R

3.5 Frequency and duty-cycle setting in bypass mode in 2EP130R

2EP130R offers a bypass mode. When operating in this mode, the external PWM signal bypasses the internal oscillator and modulates directly to the output stage of 2EP130R.

In the bypass mode, 2EP130R supports frequencies in the range of 50 kHz to 695 kHz and a duty cycle in the range of 10% to 50%. For more information regarding useful operating ranges of frequency and duty cycle combinations, see Chapter 3.6.

2EP130R uses the soft start feature in bypass mode, including frequency rise during soft start. Soft start is, therefore, asynchronous to the external PWM signal.

For more information regarding soft start, see Chapter 3.8.6.

3.5.1 Start-up in bypass mode

Connecting the *DC* pin to *GND* signals 2EP130R to operate in the bypass mode. After powering up, the externally applied PWM signal at the pin *FREQ/BYP* begins the start-up synchronization and configuration of the device.

Start-up synchronization

After the supply passes the UVLO threshold, 2EP130R uses the first three consecutive PWM cycles applied to the *FREQ/BYP* pin to synchronize and sample both frequency and duty cycle.

Configuration

2EP130R uses the applied and synchronized duty cycle to configure:

- Duty-cycle dependent, average overcurrent setting (see Chapter 3.2.1)
- Duty-cycle setting for soft start
- Pre-charge activation

The following table shows the resulting configuration of duty cycle and pre-charge setting for any allowed input PWM duty cycle.

Table 4 Bypass mode configuration for 2EP130R

Input PWM duty cycle at *FREQ/BYP*		Output duty cycle at *OUT1*	Pre-charge
Minimum	**Maximum**		
9.0%	10.50%	10%	Yes
10.5%	11.40%	11%	
11.4%	12.50%	12%	
12.5%	13.30%	13%	
13.3%	14.30%	14%	
14.3%	15.40%	15%	
15.4%	16.70%	16%	
16.7%	17.40%	17%	
17.4%	18.20%	18%	
18.2%	19%	19%	
19.0%	20%	20%	
20.0%	21.10%	21%	
21.1%	22.20%	22%	
22.2%	23.50%	23%	
23.5%	25%	24%	
25,0%	26.70%	26%	
26.7%	28.60%	28%	
28.6%	30.80%	30%	
30.8%	33.30%	32%	
33.3%	36.40%	35%	
36.4%	40%	38%	
40.0%	44.40%	43%	
44.4%	60%	50%	No

After start-up synchronization and configuration, the IC performs a soft start. During soft start, 2EP130R ignores the *FREQ/BYP* signal and uses its internal frequency generator. For proper start-up synchronization, the external PWM signal (frequency and duty cycle) must be kept constant during start-up until 2EP130R signals the end of soft start by releasing the *RDY* pin.

3.5.2 Entering operation in bypass mode

After the soft start phase, 2EP130R synchronizes to the applied external PWM frequency and duty cycle connected to the *FREQ/BYP* pin. Ensure that the frequency and duty cycle are stable during the soft start to prevent frequency or duty-cycle steps that may create a system overcurrent event.

While operating in the bypass mode, 2EP130R follows the applied frequency and duty cycle. Changes in duty cycle during operation will not cause the transformer driver to change the already identified overcurrent threshold levels, $I_{OCthr,x}$. These levels are only set during start-up and the initial duty cycle evaluation.

3.5.3 Stopping operation in bypass mode

2EP130R stops synchronous switching operation in the bypass mode in case of an UVLO event or one of the following fault events:

- Loss of synchronization fault
  - Doubling of the switching period time compared to the current period time
  - Increase beyond the maximum switching period
- Average overcurrent protection fault
- Peak overcurrent protection fault
- Overtemperature fault

For these faults or UVLO events, the IC sets *RDY* to low, and the output stage to tri-state.

After all faults are cleared, or after the supply passes the UVLO threshold, 2EP130R restarts in the bypass mode.

Doubling the switching period time compared to the current period time

2EP130R validates cycle-over-cycle,if the on-time or off-time at the *FREQ/BYP* pin has increased more than a factor of 2 compared to the previous on-time or off-time.

Increase beyond the maximum switching period

2EP130R validates if the on-time plus the off-time at the *FREQ/BYP* pin is more than the maximum allowed switching period of typically 22.5 µs.

3.6 Useful operating range of duty cycle and switching frequency

2EP130R offers a wide frequency and duty-cycle operating range. To ensure proper operation of the overcurrent protection, respect the minimal on-time, t_{ONmin}, of the outputs *OUT1*/*OUT2*.

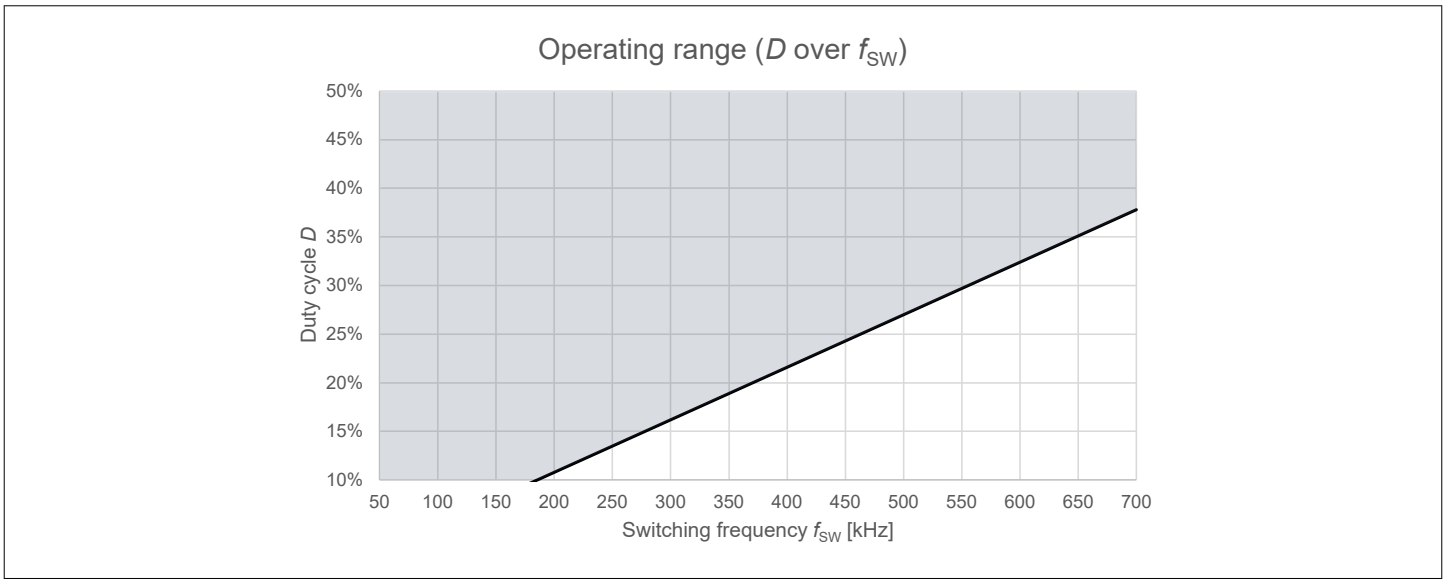


Figure 13 Operating range of 2EP130R

3.7 Resistor adjustment table for 2EP110R and 2EP130R

Resistor function table for resistor $R_{FREQ/BYP}$, R_{DC}, and R_{OCSET} when connected to ground with resistor R_{set}.

Table 5 Resistor values: Duty cycle *D* for 2EP110R and 2EP130R; Frequency, f_{SWR}, and overcurrent setting, *OCSET*, for 2EP130R only

R_{set}	f_{SWR}	*D*	*OCSET*		R_{set}	f_{SWR}	*D*	*OCSET*
Ohm	kHz	%			Ohm	kHz	%	
332	50	10	1		5760	199	31	3
412	53	11	1		6980	213	32	3
499	57	12	1		8250	227	33	3
590	61	13	1		9530	243	34	4
698	65	14	1		11000	259	35	4
806	70	15	1		12700	277	36	4
931	74	16	1		14700	295	37	4
1070	79	17	1		16500	316	38	4
1210	85	18	2		18700	337	39	4
1370	90	19	2		21000	360	40	4
1540	97	20	2		23700	384	41	4
1740	103	21	2		26700	410	42	5
1960	110	22	2		30100	438	43	5
2210	118	23	2		34000	468	44	5
2490	126	24	2		38300	500	45	5
2800	134	25	2		42200	534	46	5
3160	143	26	3		47500	570	47	5
3480	153	27	3		52300	609	48	5
3920	163	28	3		57600	651	49	5
4320	175	29	3		63400	695	50	5
4750	186	30	3					

3.8 Description of operating states

The 2EP1xxR transformer driver ICs implement the following states:

- OFF state
- Read configuration state
- Self-test state
- Pre-charge state
- Soft start state
- Run state
- Fault state
- Wait state

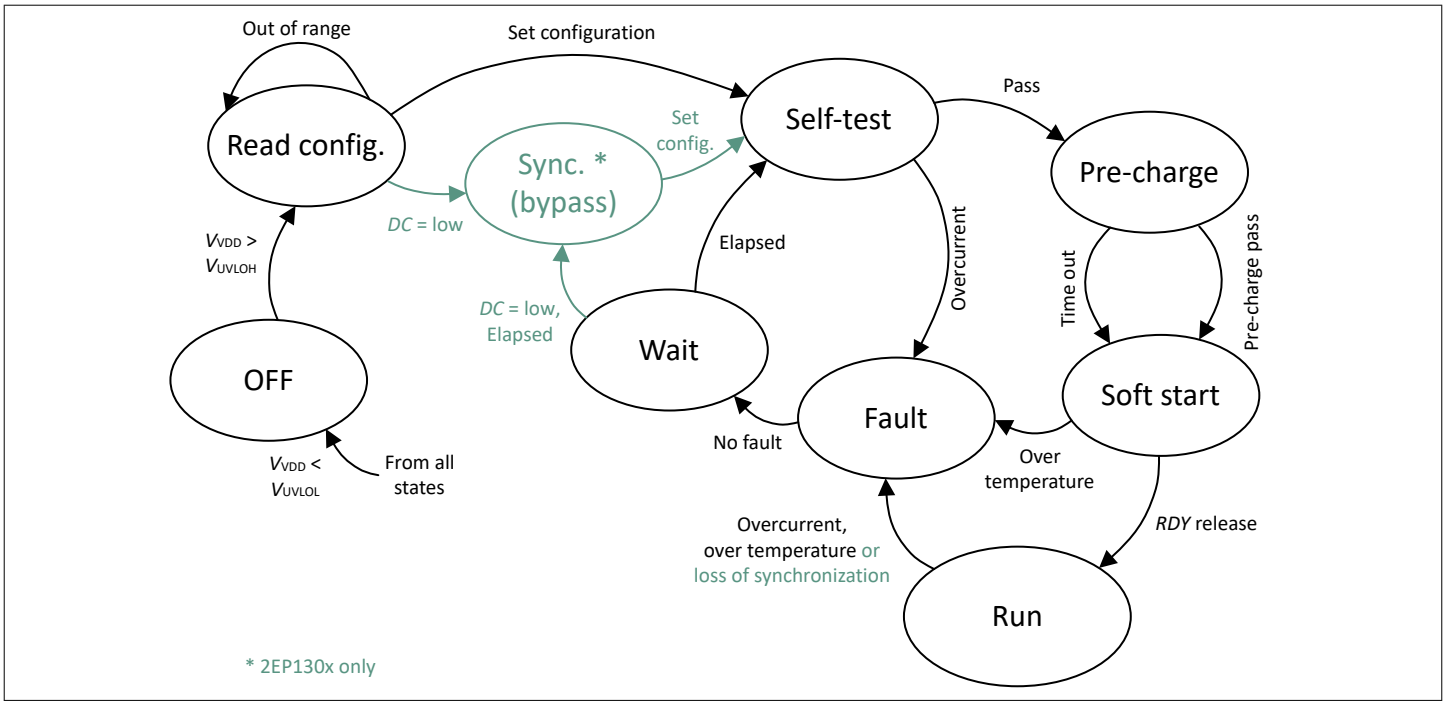


Figure 14 Operating state diagram

3.8.1 Off state

The device is not powered or supplied with a voltage below the UVLO threshold. Default output stages are in tri-state.

3.8.2 Read configuration state

When supplied, and after passing the UVLO threshold, 2EP1xxR enters the read configuration state.

2EP1xxR reads the configuration data from corresponding pins (pin strapping, resistor setting, and bypass mode). After a successful read-out, the transformer driver transitions to the next state by setting the device configuration. The output stage is set to tri-state.

3.8.3 Synchronisation state (bypass mode only)

Following the configuration state in the case of bypass mode (*DC* pin is low), the device enters the synchronization state. In the synchronization state, 2EP130R uses the first three consecutive cycles of an applied PWM signal at the *FREQ/BYP* pin to synchronize to the external PWM.

The read-out frequency and duty cycle are used to configure:

- Duty-cycle dependent average overcurrent offset
- Duty cycle for soft start
- Pre-charge activation

The output stage is set to tri-state.

3.8.4 Self-test state

The built-in self-test ensures that both outputs, *OUT1* and *OUT2,* have neither a short to supply pin *VDD*, nor a short to ground pin *GND*. A detected short leads to a fault state. The device switches the outputs between active and tri-state.

3.8.5 Pre-charge state

The pre-charge function charges the series capacitor with the pre-charge current of typically 18 mA until the series capacitor reaches the pre-charge voltage. 2EP1xxR switches *OUT1* to *GND* and *OUT2* operates as a current source from *VDD*. The pre-charge function depends on the configured duty cycle:

- Duty cycle < 45%: Perform pre-charge
- Duty cycle > 45%: Skip pre-charge

A timeout of typically 20 ms is built in to overcome any stalled conditions caused by pre-charge overtime fault.

3.8.6 Soft start state

2EP1xxR uses the soft start feature to limit the application inrush current. It also results in a smooth ramp-up of the isolated output voltage. The soft start, therefore, operates with a potentially increased frequency and a soft start specific peak current mode.

Frequency increase

- Increases switching frequency typically to 360 kHz for configured frequencies below 360 kHz
- Uses configured frequency for frequency settings above 360 kHz

Soft start specific peak current mode

To secure a stable start-up for capacitive and base loads, 2EP1xxR starts in the peak current mode with the overcurrent threshold value $I_{OCthr,6}$ for both outputs. During the remaining soft start phase, the overcurrent threshold value gradually adjusts to its individual target value. In case the peak current detection is triggered permanently due to overload, 2EP1xxR stays in the soft start mode indefinitely.

If the transformer driver starts with a higher frequency, the soft start frequency decreases gradually to the configured value. The soft start function ends as soon as the target frequency is reached. 2EP1xxR then releases the *RDY* pin to high.

3.8.7 Run state

In this state, the device is in full operation. The outputs are actively switching according to the requested frequency and duty cycle, and the *RDY* signal is released to high. 2EP1xxR exits the run state when any of the following events occur:

- Transition to a fault state:
  - Average overcurrent fault
  - Peak overcurrent fault
  - Overtemperature fault
  - Loss of synchronization fault (only applicable in the bypass mode)
- Transition to OFF state: an UVLO event, passing the V_{UVLOL} threshold

3.8.8 Fault state

When 2EP1xxR detects a fault, the device stays in the fault state until all faults disappear. 2EP1xxR switches the output state to tri-state and the *RDY* signal to low to signal a failure.

3.8.9 Wait state

After a fault has passed, the device enters a wait state to bring the system to a stable initial state and to reduce the stress on the components.

The output stage is kept in tri-state. After the wait cycle time, t_{Wait}, has elapsed, the system continues in a self-test state to restart.

4 Electrical characteristics and parameters

4.1 Absolute maximum ratings

Table 6 Absolute maximum ratings

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	-0.3		22	V	
Output voltage (OUT1, OUT2)	V_{OUT}	-0.3		V_{VDD} +0.3	V	
Output voltage transient (OUT1, OUT2)	V_{OUT}	-2		V_{VDD} +2	V	1) Repetitive pulse < 200 ns
Logic input voltages	V_{LOGIC}	-0.3		6.5	V	2)
Logic input voltages	V_{LOGIC}	-0.3		V_{VDD} +0.3	V	V_{VDD} < 6.5 V 2)
RDY sink current	I_{RDY}	-		10	mA	
RDY signal voltage	V_{RDY}	-0.3		6.5	V	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_S	-55		150	°C	
Power dissipation PG-TSSOP-8	P_D			930	mW	PG-TSSOP-8, dT = 70 °C
ESD robustness - human body model	$\lvert V_{ESD,HBM} \rvert$			2	kV	3)
ESD capability - charged device model	*ESD,CDM*			TC 500		4)

1) Parameter is not subject to production test - verified by design/characterization
2) Valid for externally applied voltages
3) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
4) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

4.2 Thermal characteristics

Table 7 Thermal characteristics

Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance, junction-to-ambient PG-TSSOP-8	R_{THJA}			75	K/W	T_A = 25°C, P_D = 930 mW, PG-TSSOP-8
Characterization parameter, junction-to-package top-side PG-TSSOP-8	Ψ_{JPtop}			14	K/W	T_A = 25°C, P_D = 930 mW, PG-TSSOP-8

4.3 Operating parameters

Table 8 Operating parameters

Within the operating range, the IC operates as described in the functional description and electrical characteristics.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage, operating	V_{VDD}	4.5		20	V	
Logic input voltages, operating	V_{LOGIC}	-0.3		5.5	V	V_{VDD} > 5.5 V [1]
Logic input voltages, operating	V_{LOGIC}	-0.3		V_{VDD} +0.3	V	V_{VDD} < 5.5 V [1]
Minimum on-time	t_{ONmin}	540			ns	
Switching frequency	f_{SW}	50		695	kHz	only 2EP130x
Ambient temperature, operating	T_A	-40		125	°C	T_J < T_{OTPOFF} [2]

1) Valid for externally applied voltages
2) For life time calculations, please contact your local Infineon quality team.

4.4 Electrical characteristics

The electrical characteristics include the spread of values within the operating parameters. Electrical characteristics are tested in production at T_A = 25°C. Typical values represent the median values measured at V_{VDD} = 15 V, and T_A = 25°C. Minimum and maximum characteristics are verified by characterization/design. This note is valid for all electrical characteristics unless specified otherwise.

4.4.1 Power supply

Table 9 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage UVLO threshold upper limit	V_{UVLOH}	3.95	4.2	4.45	V	
Supply voltage UVLO threshold lower limit	V_{UVLOL}	3.65	3.9	4.15	V	
Supply voltage UVLO hysteresis	$V_{UVLOHys}$	0.2	0.3	0.4	V	
VDD supply current	I_{VDD}			6	mA	No load, V_{VDD} = 15 V, f_{SW} = 103 kHz or 65 kHz, D = 12%/ 50%, *OCSET,4* for 2EP130

4.4.2 Logic input and output

Table 10 Logic input and output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Logic input voltage low	$V_{Logic,L}$			1.0	V	1)
Logic input voltage high	$V_{Logic,H}$	2.4			V	1)
Logic input voltage hysteresis	$V_{Logic,Hys}$	0.8			V	1)
Logic input filter time	$t_{Logic,filt}$	120	180	280	ns	V_{Logic} = 3.3 V, V_{Logic} rise time < 10 ns, 1)
Logic output voltage low RDY	$V_{RDY,5}$			0.3	V	V_{VDD} = 15 V, I_{sink} = 5 mA

1) Only for 2EP130x at *FREQ/BYP* pin in bypass mode.

4.4.3 Adjustment and protection

Table 11 Adjustment and protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
2EP100, 2EP101, 2EP110						
Maximum resistance for low detection	R_{ISMGND}	1800			Ω	

(table continues...)

Table 11 (continued) Adjustment and protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum resistance for high detection	$R_{ISMFLOAT}$			2.43	kΩ	
Switching frequency 50	f_{SW50}	46	50	53	kHz	2EP101, 2EP110, *FREQ* connected to *GND*
Switching frequency 65	f_{SW65}	62.5	65.1	67.1	kHz	2EP100: *FREQ* connected to *GND;* 2EP101, 2EP110: *FREQ* left floating
Switching frequency 103	f_{SW103}	99	103.1	106.2	kHz	2EP100: *FREQ* left floating
Duty cycle, fixed 1	D_1	11	12	13	%	2EP101, *DC* connected to *GND*
Duty cycle, fixed 2	D_2	16	17	18	%	2EP101, *DC* floating or 3 V < V_{DC} < 5.5 V
Duty cycle, fixed 3	D_3	32	33	34	%	2EP100, *DC* connected to *GND*
Duty cycle, fixed 4	D_4	49	50	51	%	2EP100, *DC* floating or 3 V < V_{DC} < 5.5 V
2EP110x, 2EP130x						
External resistor value range	R_{EXT}	0.332		63.4	kΩ	
External filter capacitor value range	C_{EXT}	0		22	nF	1) 2)
Duty-cycle range resistor adjusted	D_R	10		50	%	resistor adjusted at *DC*
Duty-cycle accuracy, low frequency	$D_{ACC,LF}$	-1		1	% points	integer duty cycle in 1% steps, f_{SW} ≤ 150 kHz
Duty-cycle accuracy, high frequency	$D_{ACC, HF}$	-2		2	% points	integer duty-cycle in 1% steps, f_{SW} > 150 kHz
2EP130x						
Switching frequency self-oscillating, min	$f_{SWR,min}$	46	50	53	kHz	$R_{FREQ/BYP}$ = 332 Ω
Switching frequency self-oscillating, max	$f_{SWR,max}$	645	695	735	kHz	$R_{FREQ/BYP}$ = 63.4 kΩ
Bypass mode grounding resistance	R_{BYPGND}	0		200	Ω	
Frequency synchronization range	$f_{SW,SYNC}$	50		695	kHz	D_{SYNC} = 50%, 3)
Synchronization propagation delay	$t_{PD,SYNC}$	225	280	340	ns	V_{OUTx} at 10% or 90%, C_{LOAD} = 1 nF, 3)
Duty-cycle synchronization range 1	D_{SYNC1}	10		50	%	$f_{SW,SYNC}$ < 185 kHz, 3)
Duty-cycle synchronization range 2	D_{SYNC2}	38		50	%	$f_{SW,SYNC}$ = 695 kHz, 3)
Protection						
Overcurrent threshold 0	$I_{OCthr,0}$	25	60	85	mA	
Overcurrent threshold 1	$I_{OCthr,1}$	60	110	140	mA	
Overcurrent threshold 2	$I_{OCthr,2}$	108	195	252	mA	
Overcurrent threshold 3	$I_{OCthr,3}$	200	340	450	mA	

(table continues...)

Table 11 (continued) Adjustment and protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overcurrent threshold 4	$I_{OCthr,4}$	350	585	820	mA	
Overcurrent threshold 5	$I_{OCthr,5}$	650	1175	1450	mA	
Overcurrent threshold 6	$I_{OCthr,6}$	1300	1970	2400	mA	
Overcurrent threshold 7	$I_{OCthr,7}$	2900	3375	3800	mA	
Peak-overcurrent threshold	I_{PkOCP}	4	4.8	6	A	
Peak-overcurrent reaction time	t_{OCPRDY}	100		540	ns	
Overtemperature threshold	T_{OTPOFF}	150			°C	1)
Overtemperature hysteresis	T_{OTPHys}	20			°C	1)
Wait cycle after fault	t_{Wait}	0		50	ms	1)

1) Parameter is not subject to production test - verified by design/characterization
2) For detailed information see graph external filter capacitance C_{EXT} vs. external resistance R_{EXT}.
3) Device in bypass mode, *DC* connected to *GND*, signal applied at *FREQ/BYP* with V_{Logic} = 3.3 V, rise time < 10 ns.

4.4.4 Output power stage

Table 12 Output power stage

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Driver output resistance high	$R_{ON,H}$		0.63	0.95	Ω	I_{OUT} = 50 mA, T_J = 125°C 1)
Driver output resistance low	$R_{ON,L}$		0.48	0.73	Ω	I_{OUT} = -50 mA, T_J = 125°C 1)
Rise time	t_{RISE}	8	15	25	ns	V_{VDD} = 15 V, C_{LOAD} = 1 nF, V_{OUT} from 10% to 90%
Fall time	t_{FALL}	8	15	25	ns	V_{VDD} = 15 V, C_{LOAD} = 1 nF, V_{OUT} from 90% to 10%

1) Parameter is not subject to production test - verified by design/characterization

5 Application section

Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The application circuits with a 2EP transformer driver can use a broad range of voltage rectification topologies. This application section will focus on the voltage doubler and peak rectification topologies. The voltage doubler rectification is a known topology in the industry to generate output voltages with a ratio of 2:1. Peak rectification with 50% duty cycle delivers output voltages with a ratio of 1:1. Combining peak rectification with the adjustable duty cycle of the 2EP enables a wide range of output voltage ratios.

5.1 Theory of the 2EP1xxR using the voltage doubler topology

This section describes the theory behind the full-bridge power stage of 2EP1xxR together with the voltage doubler topology to provide two isolated output voltages. Each transformer output winding supports a positive and a negative output voltage. The positive output voltage has double the voltage level compared to the negative output voltage.

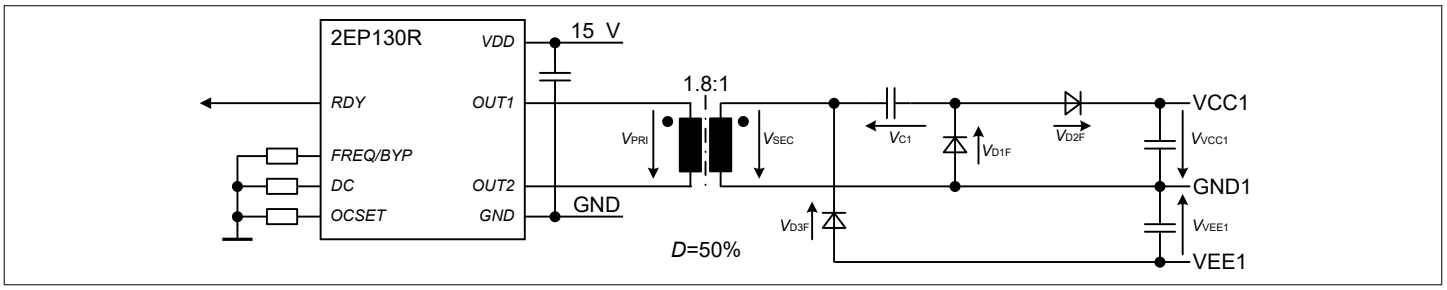


Figure 15 Simplified schematic of 2EP130R using voltage doubler topology

The voltage arrows indicate the polarity of the corresponding symbol used in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, V_{C1} the voltage of the voltage doubler capacitor (flying capacitor), and V_{VCC1}/V_{VEE1} the output voltage of one of the rails.

The following sections describe how to determine the output voltages of a voltage doubler topology connected to 2EP130R.

Full-bridge transformer driver 2EP130R

For output rectification using the voltage doubler topology, the configured duty cycle needs to be at 50%. 2EP130R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency. The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$. In the schematic shown above, this voltage is referred to as the primary transformer voltage, V_{PRI}.

$$V_{PRI} = \pm V_{VDD}$$

Transformer, transformer turn ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, to the secondary side voltage based on the transformer turn ratio (*TTR*). The secondary transformer voltage V_{SEC} is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm \frac{V_{VDD}}{TTR}$$

If the output voltages are loaded asymmetrically or the input duty cycle is not exactly at 50%, the transformer could drift into saturation. The evaluation board EVAL-2EP130R-VD includes, therefore, a series capacitor between *OUT1* and the primary winding. For the sake of simplification, this component is not shown nor considered in the calculations given in this section. This capacitor ensures an equal voltage×time product for primary winding. The equal voltage×time product prevents the transformer from saturating, even when driven with asymmetric loads.

Voltage doubler current rectification

Due to the diodes in the voltage doubler circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage must be applied only when calculating the expected output capacitor voltages.

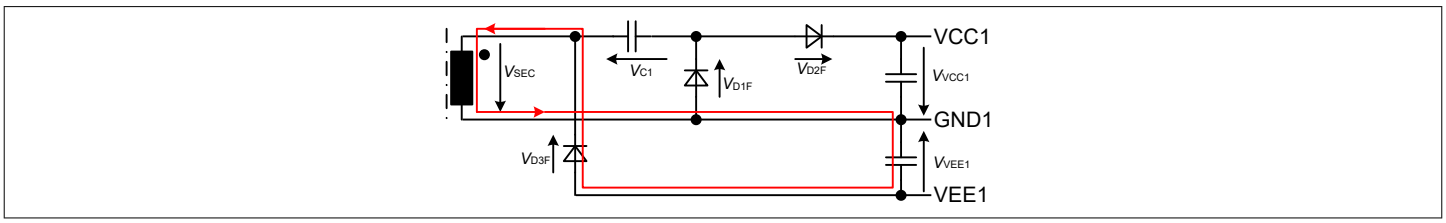


Figure 16 Current path of the negative voltage rail

The current path to charge the negative voltage rail requires V_{SEC} to be in reverse polarity. The current charges the negative output voltage capacitor. The current then closes the circuit via diode D3 in the forward direction resulting in V_{D3F} voltage drop.

The negative output voltage results in: $V_{VEE1} = V_{SEC(neg)} + V_{D3F}$

Since the secondary transformer voltage is negative at that half wave, the resulting output voltage is also negative but lowered by the diode's forward voltage.

The positive output voltage requires a two-step approach for the full output voltage. In the first step, the flying capacitor is charged. In the second step, this pre-charged capacitor boosts the voltage for a positive output rail.

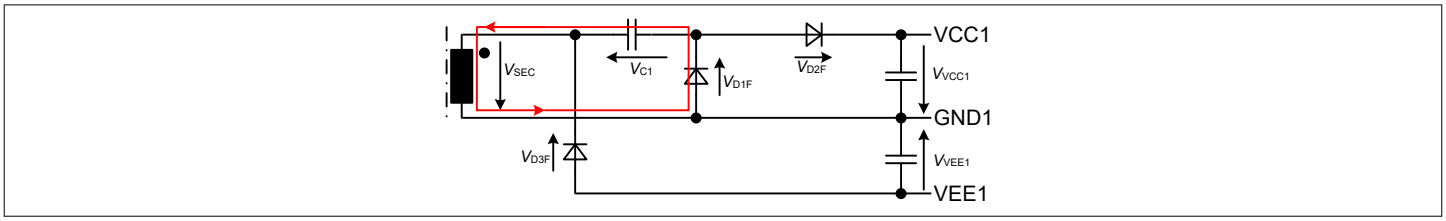


Figure 17 Current path to charge the bootstrap capacitor of the positive voltage rail

The current path to charge the flying capacitor requires V_{SEC} to be in reverse polarity. The direction of current is the same as that for the negative output voltage. Therefore, the current during the negative half wave of the secondary winding is doubled compared to the positive half wave. The current flows through the diode, D1, resulting in V_{D1F} voltage drop. It then charges the flying capacitor before closing the circuit.

The flying capacitor, therefore, has a positive voltage that results in: $V_{C1} = -V_{SEC(neg)} - V_{D1F}$

As the secondary transformer voltage is negative at that half wave, the resulting flying capacitor voltage, according to the indicated polarity, is positive but reduced by the diode's forward voltage.

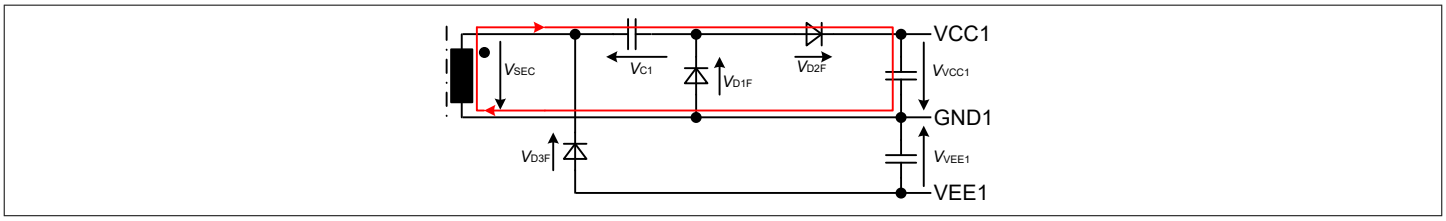


Figure 18 Current path of the positive voltage rail via the bootstrap capacitor

The current path to finally charge the positive output voltage capacitor requires V_{SEC} to be in the indicated polarity (positive half wave). It has, therefore, the same polarity as the flying capacitor voltage, V_{C1}. The resulting current will pass through D2 resulting in a V_{D2F} voltage drop. It then charges the positive output voltage capacitor before closing the circuit.

The positive output voltage results in: $V_{VCC1} = V_{SEC(pos)} + V_{C1} - V_{D2F}$

Both output voltages can then be written as:

Assumption 1: All diode forward voltages are equal

$$V_F = V_{D1F} = V_{D2F} = V_{D3F}$$

Assumption 2: Amplitudes of positive and negative half wave are equal

$$|V_{SEC}| = V_{SEC(pos)} = -V_{SEC(neg)} = \frac{V_{VDD}}{TTR}$$

positive output voltage

$$V_{CC1} = 2 \cdot \left(\frac{V_{VDD}}{TTR} - V_F\right)$$

negative output voltage

$$V_{EE1} = -\left(\frac{V_{VDD}}{TTR} - V_F\right)$$

Equation 1

Voltage doubler application impact

For simplicity the descriptions and formulas were derived for a single transformer output winding. But single rail voltage doubler output has asymmetric current during positive and negative half waves. These asymmetric currents create, at the input side, an asymmetric voltage drop across the resistive elements. The result is a non-equal voltage×time product for the positive and the negative voltage applied to the transformer. This will create a shift in the operating point at the B-H-curve with partial transformer saturation.

There are two ways to compensate for this shift:

1. A series capacitor at the primary side of the transformer to equalize the voltage×time product mismatch

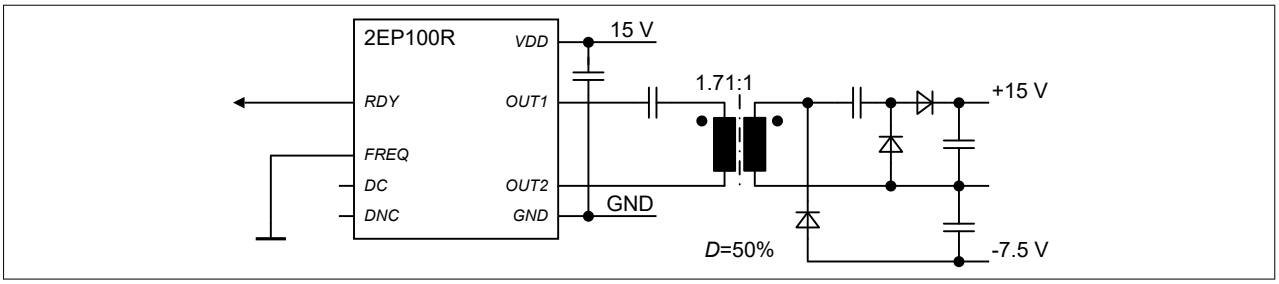


Figure 19 2EP100R application example with series capacitor and single rail voltage doubler

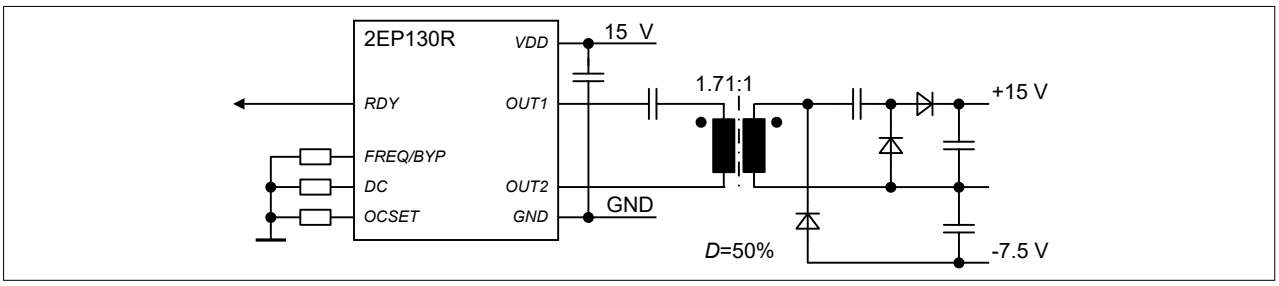


Figure 20 2EP130R application example with series capacitor and single rail voltage doubler

2. Different winding polarities for the two separate output rails in applications with equal loads and dual output transformer

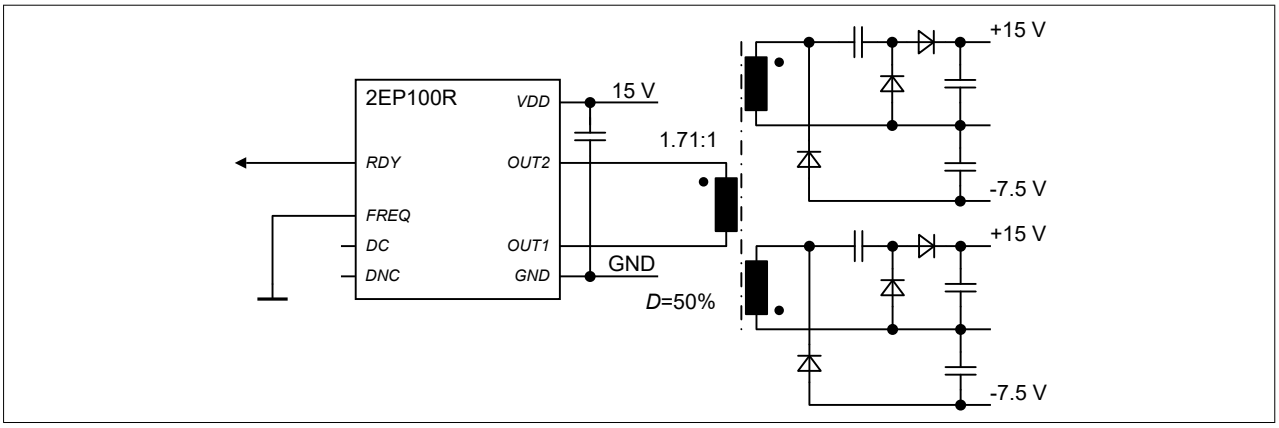


Figure 21 2EP100R application example with voltage doubler on two output rails

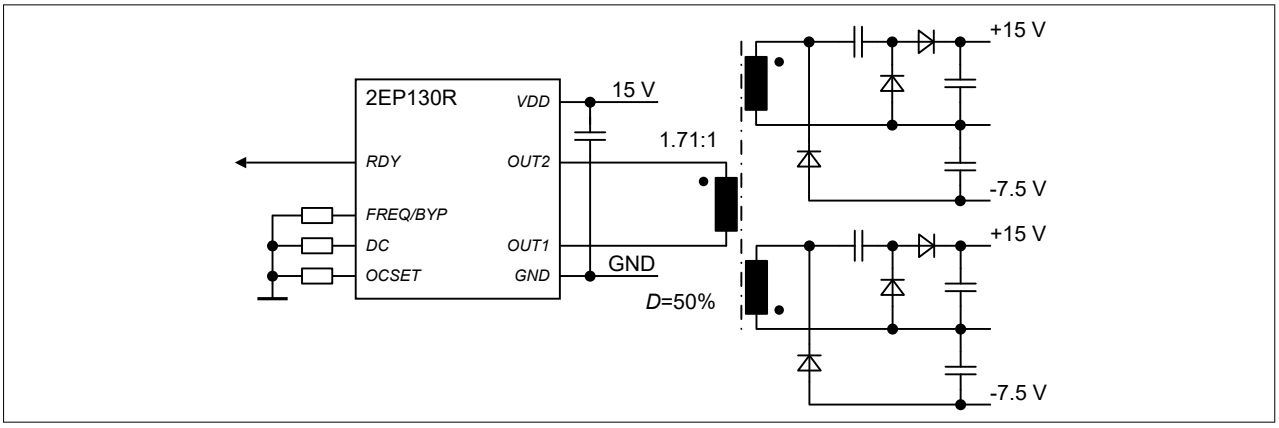


Figure 22 2EP130R application example with voltage doubler on two output rails

The voltage doubler topology with dual output transformer allows for the highest output current due to the interleaved current compensation. An additional series capacitor might still be needed for asymmetric load currents on the different rails.

5.2 Theory of the 2EP1xxR using peak rectification topology

This section describes the theory behind the full-bridge power stage of 2EP1xxR and the peak rectification topology to provide two isolated output voltages. Each transformer output winding supports a positive and a negative output voltage. The ratio between the positive voltage and negative voltage is defined by the duty cycle.

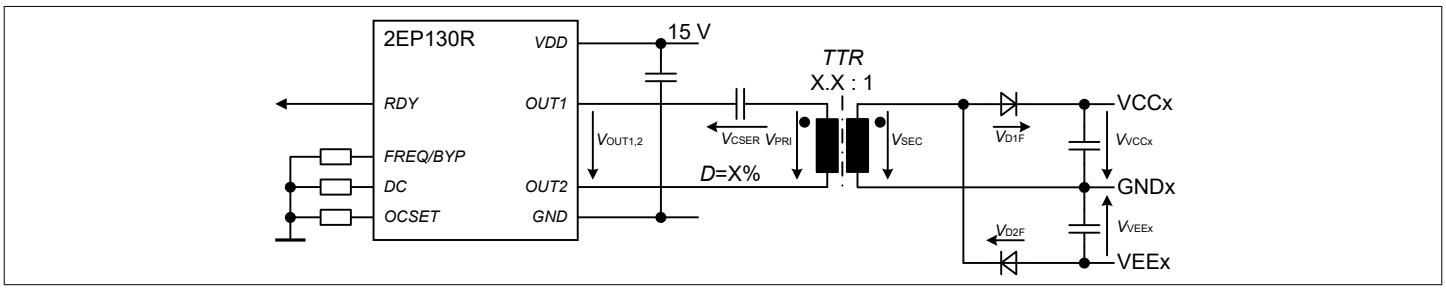


Figure 23 Simplified schematic of 2EP130R using peak rectification topology

The voltage arrows indicate the polarity of the corresponding symbol for use in the equations provided later. V_{PRI} and V_{SEC} represent the transformer voltages, V_{DxF} the individual diode forward voltages, V_{CSER} the voltage across the primary series capacitor, and V_{VCCx}/V_{VEEx} the output voltage.

The following sections describe how to determine the output voltages of a peak rectification according to:

- the applied input voltage to 2EP

- the applied duty cycle by chopping the input voltage
- the level-shift (offset) of the series capacitor
- the transformer turn ratio
- the peak current rectification

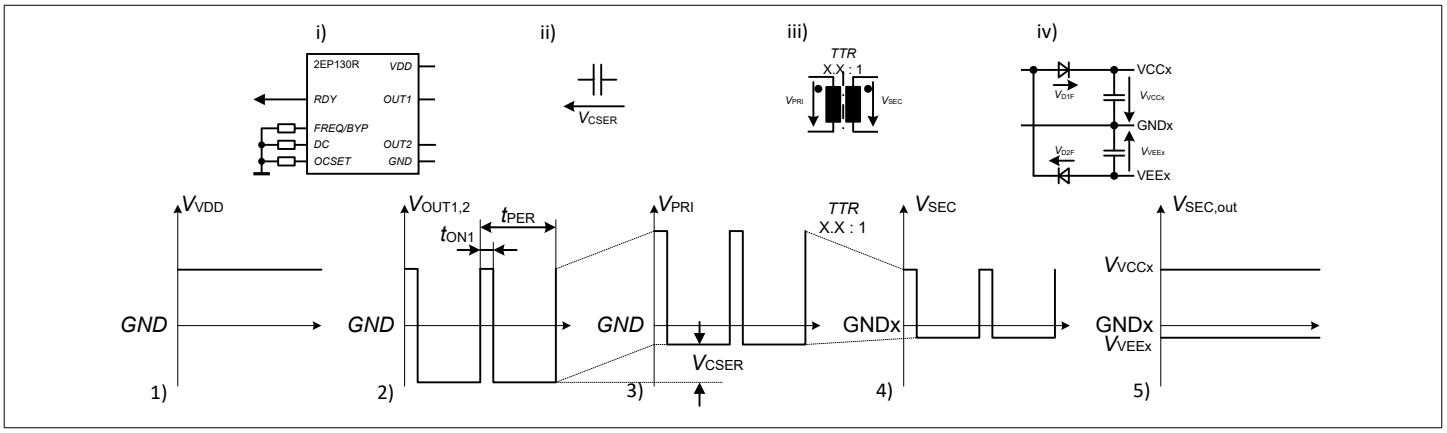


Figure 24 DC offset voltage and influence of transformer turn ratio output voltage

The figure shows the idealized voltage wave forms at each step (1-5) and the involved components at the intermediate step (i-iv). The input supply voltage V_{VDD} (1) is applied to 2EP130R (i). It provides the output voltage $V_{OUT1,2}$ (2) to the series capacitor (ii). This results in the shifted input voltage V_{PRI} (3) for the transformer (iii). The transformer scales the input voltage to the secondary side as V_{SEC} (4). The last step is peak current rectification (iv) and its output voltages (5).

Full-bridge transformer driver – 2EP130R

2EP130R chops the applied supply voltage, V_{VDD}, according to the configured switching frequency and duty cycle (*D*). The output of *OUT1* is switched between *VDD* and *GND*. The same is valid for *OUT2*. However, its switching pattern is inverted. This results in twice the amplitude of V_{VDD} across the outputs $V_{OUT1,2}$ or with a *GND* reference:

$$V_{OUT1,2} = \pm V_{VDD}$$

The duty cycle is calculated as: $D = \frac{t_{ON1}}{t_{PER}}$ with the on duration of output 1, t_{ON1}, and the period time, t_{PER}, of the switching frequency. The duty cycle for *OUT2* always complements that of *OUT1*. The duty cycle always refers to *OUT1*.

Series capacitor – C_{SER}

The series capacitor creates an offset derived from the duty cycle. The DC offset voltage, V_{CSER}, is therefore an integral component for calculating output voltages. The capacitor voltage level during steady state operation is calculated as:

$$V_{CSER} = V_{VDD}\left(1 - \frac{2 \cdot D}{100\,\%}\right)$$

The offset voltage V_{CSER} varies between 80% of the V_{VDD} at 10% and 0% of the V_{VDD} at 50% duty cycle. Since 2EP130R only allows duty cycles between 10% to 50%, the resulting offset voltage is positive according to its indicated polarity. Any waveform with a duty cycle not equal to 50% has a DC offset voltage component. The series capacitor, basically, removes the direct component from the chopped supply voltage. Due to this, the series capacitor converts the symmetric peak voltages, $V_{OUT1,2}$, into asymmetric peak voltages:

$$V_{RPI} = \pm V_{VDD} + V_{CSER}$$

The primary transformer voltage alternates between ($+V_{VDD}+V_{CSER}$) and ($-V_{VDD}+V_{CSER}$) due to the full-bridge output stage of 2EP130R and the aforementioned offset voltage stored within V_{CSER}.

Transformer, transformer turn ratio (*TTR*), and transformer saturation

The transformer transforms the primary input voltage, V_{PRI}, according to the transformer turn ratio (*TTR*) to the secondary side. The secondary transformer voltage, V_{SEC}, is calculated as:

$$V_{SEC} = \frac{V_{PRI}}{TTR} = \pm\frac{V_{VDD}}{TTR} + \frac{V_{CSER}}{TTR}$$

The aforementioned V_{CSER} offset voltage ensures an equal voltage×time product for the primary winding. This equal voltage×time product prevents the transformer from saturating, even when driven with asymmetric peak voltages.

Peak current rectification

Due to the diodes in the peak rectification circuit, individual current paths must be considered separately. The matching voltage polarity of the secondary transformer voltage should be taken into account when calculating the expected output capacitor voltages.

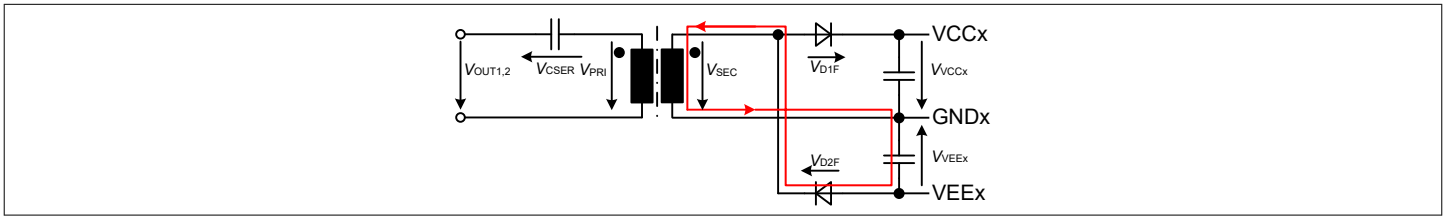


Figure 25 Current path of the negative voltage rail

The current path to charge the negative voltage rail requires V_{SEC} to be in reverse polarity. The current charges the negative output voltage capacitor and closes the circuit via the diode, D2, in forward direction resulting in the V_{D2F} voltage drop.

The negative output voltage then results in: $V_{VEEx} = V_{SEC(neg)} + V_{D2F}$

As the secondary transformer voltage is negative at that half-wave, the resulting output voltage is also negative, but reduced by the diode forward voltage.

The positive output voltage behaves similar to the negative output voltage.

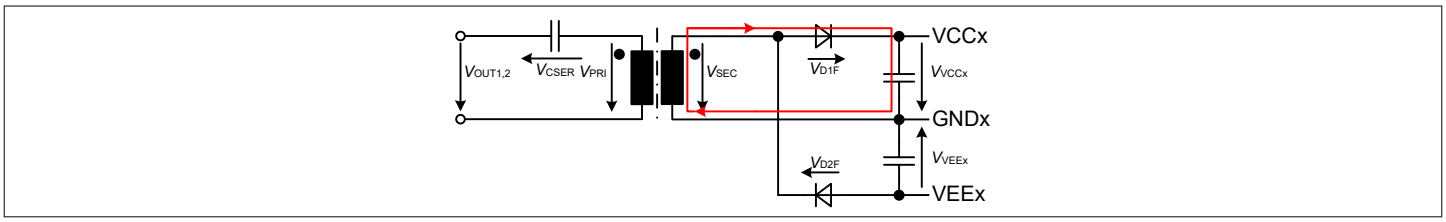


Figure 26 Current path of the positive voltage rail

The current path to charge the positive voltage rail requires V_{SEC} to be in the indicated polarity (positive half-wave). The current charges the positive output voltage capacitor and closes the circuit via the diode, D1, in forward direction resulting in the V_{D1F} voltage drop.

The positive output voltage then results in: $V_{VCCx} = V_{SEC(pos)} - V_{D1F}$

Both output voltages can be written as:

Assumption 1: All forward voltages are equal:

$$V_{\mathrm{F}} = V_{\mathrm{D1F}} = V_{\mathrm{D2F}}$$

Assumption 2: Amplitudes of both the positive and negative half-waves experience the same offset:

$$V_{\mathrm{SEC}} = \pm \frac{V_{\mathrm{VDD}}}{TTR} + \frac{V_{\mathrm{CSER}}}{TTR}$$

Positive output voltage:

$$V_{\mathrm{VCCx}} = \left(\frac{V_{\mathrm{VDD}}}{\mathrm{TTR}} + \frac{V_{\mathrm{CSER}}}{\mathrm{TTR}} - V_{\mathrm{F}} \right)$$

Negative output voltage:

$$V_{\mathrm{VEEx}} = -\left(\frac{V_{\mathrm{VDD}}}{\mathrm{TTR}} - \frac{V_{\mathrm{CSER}}}{\mathrm{TTR}} - V_{\mathrm{F}} \right)$$

Equation 2

***Note**: Equal load at positive and negative voltage rails results in asymmetric currents for positive and negative half waves. This can result in unequal output voltage drops for positive and negative output voltages. The actual output voltages may differ slightly from the ones calculated using the equations given in this section. When designing a peak rectifier circuit with dual output rails, the same winding polarity should be used for both rails.*

Inserting the series capacitor voltage V_{CSER} equation into the output voltage equations results in:

Positive output voltage:

$$V_{\mathrm{CCx}} = \frac{2 \cdot V_{\mathrm{VDD}}}{\mathrm{TTR}}(1 - D) - V_{\mathrm{F}}$$

Negative output voltage:

$$V_{\mathrm{EEx}} = \frac{2 \cdot V_{\mathrm{VDD}}}{\mathrm{TTR}}(-D) + V_{\mathrm{F}}$$

Equation 3

Selection of the switching frequency

The selection of the switching frequency follows the basic rule “as high as necessary, as low as possible”. The voltage transfer principle is independent of the switching frequency, but the transformer driver IC, the transformer, and especially the parasitics require a selection of the switching frequency. Examples of important parasitics are leakage inductance, main inductance, diode capacitance and reverse recovery charge, switching losses, core losses, and AC wire resistance. It is basically a trade-off between several items.

Increasing the switching frequency introduces some penalties:

- Lower efficiency due to increasing switching losses
- Larger increase of output voltage at light load
- Larger output voltage drop over load

However, there are also benefits:

- Lower magnetizing current allows smaller main inductance
- Lower voltage×time product resulting in smaller core size
- Lower number of windings resulting in lower interwinding capacitance

Based on the design priorities, the design engineer can select the appropriate switching frequency.

For example, a transformer with higher isolation rating does not gain too much from a smaller core size, because the transformer size is given by the large creepage and clearance requirement. This was the design basis for choosing the switching frequency between 50 and 103 kHz for the 2EP transformer driver evaluation boards.

5.3 Load behavior for open loop converter

5.3.1 Light-load output voltage increase

The light-load output voltage increase is a known effect for open loop converters. It is mainly caused by switching frequency, leakage inductance of the transformer, and the rectifier diode's capacitance.

Increased leakage inductance, switching frequency, or rectifier diode's capacitance leads to a higher increase in the light-load output voltage. The following measures can be evaluated for a dedicated application:

- Keep leakage inductance of the transformer low
- Keep switching frequencies low
- Use diodes with low capacitance
- Suppress light-load output voltage increase with a minimal load resistor

Do not suppress the light-load voltage increase at the output with Zener diodes. These diodes might interact with the peak current mode start-up and keep 2EP in its start-up phase.

5.3.2 Isolated output voltage drop over load versus parasitics

In all open loop converters, the isolated output voltage is dependent on the load. The larger the output current the larger the output voltage drop. The 2EP transformer driver is an open loop system, voltage decrease over load cannot be compensated by the transformer driver, therefore, it has to be considered.

There are two major influencing factors:

- Resistance in the input-to-output loop
- Leakage inductance of the transformer

Voltage drop due to resistance in the loop

There are several resistances in the loop, such as the R_{DSon} of the 2EP output stage, the series resistance, the input and output winding resistance, and the diode's dynamic forward resistance. All resistances create a voltage drop according to the current flow in these elements (duty-cycle and output-current dependent). Drops in the input voltage have to be converted with the TTR to get output voltage drops. All of these voltage drops have to be summed up.

Voltage drop due to leakage inductance

Leakage inductance is an additional source of output voltage drop. It limits the *dI/dt* of the current transfer. To keep the transferred charge constant, the peak current value increases. This increased peak current forces a larger resistive voltage drop across the resistive elements in the loop. This behavior is similar to the voltage drop across a resistor and is also, therefore, dependent on the output current and duty cycle.

5.4 Soft start in application

At start-up, the output capacitor voltages are at 0 V, resulting in the converter working against the low impedance of the discharged output capacitor. According to the general transformer transfer equation, the charging current is primarily constrained by parasitic elements such as resistance in the loop and leakage inductance. Without additional measures, these elements can lead to a high charging current.

To address this challenge, the 2EP1xxR employs a sophisticated peak-current-mode control scheme with increased switching frequency. The increased switching frequency during soft start only applies to configured switching frequencies of below 360 kHz.

The peak-current-mode utilizes the current limiting properties of the leakage inductance and the loop resistance at the input side, along with the overcurrent threshold $I_{OCthr,6}$, to limit the soft start current. This leakage inductance and the loop resistance together build a minimal impedance required for a successful start-up. While the leakage inductance influences the maximum charge transfer from the input to the output capacitors, both together are vital to achieve a charge balance within the series capacitor. This charge balance ensures a constant voltage across this series

capacitor which ensures the stable ramp-up of the output voltages. The minimal usable impedance depends on various parameters, including supply voltage, duty cycle, series capacitance, output capacitance, and output current.

Neglecting charge balance at start-up could lead to a discharging of the series capacitor, resulting in a temporary undershoot of the negative output voltage.

It is crucial not to suppress a negative output voltage undershoot at the outputs with a Zener diode. These diodes might keep the 2EP1xxR in its peak current mode start-up phase.

To ensure optimal charge balance, it is recommended to consider the following counter measures:

- Increasing the leakage inductance of the transformer
- Increasing loop resistance at the input side, for instance, by adding a series resistance

To validate the start-up behavior, it is essential to conduct thorough verification over the temperature and supply voltage range according to specific requirements. This ensures that the system operates reliably and consistently under varying conditions.

5.5 Dimensioning of components for peak rectification topology

5.5.1 Capacitors (capacitance and ripple current)

5.5.1.1 2EP ripple current estimation

The ripple current is an important design parameter for all capacitors in the circuitry.

There are three capacitor positions:

- Input capacitor – C_{VDD}
- Series capacitor – C_{SER}
- Output capacitor – C_{VCC}/C_{VEE}

All three positions have different RMS ripple current amplitude, where the ripple current has to be estimated for dimensioning the relevant capacitors.

The ripple current is influenced by several factors. The main factors influencing the ripple current are I_{OUT} (I_{VCC}, I_{VEE}), duty cycle, and transformer transfer ratio. The output voltage influence of *VCC* and *VEE* is covered via the main influence factor's duty cycle and transformer transfer ratio.

For the following estimation, the output current is used as a basis for ripple current estimation. The following graph shows the factor of ripple current divided by output current on the y-axis and the duty cycle on the x-axis. The influence of the transformer turn ratio is different for every capacitor position. This figure shows the relative currents for a transformer transfer ratio of one.

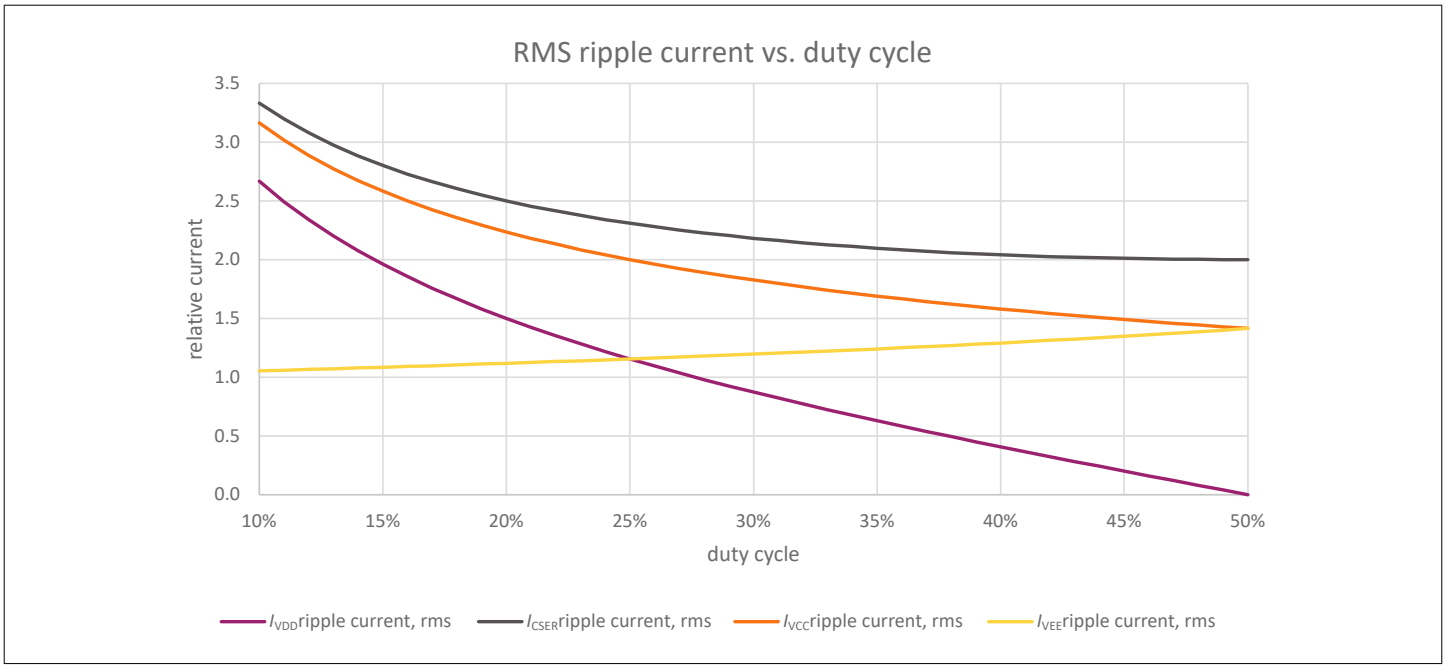


Figure 27 Relative RMS ripple current vs. duty cycle

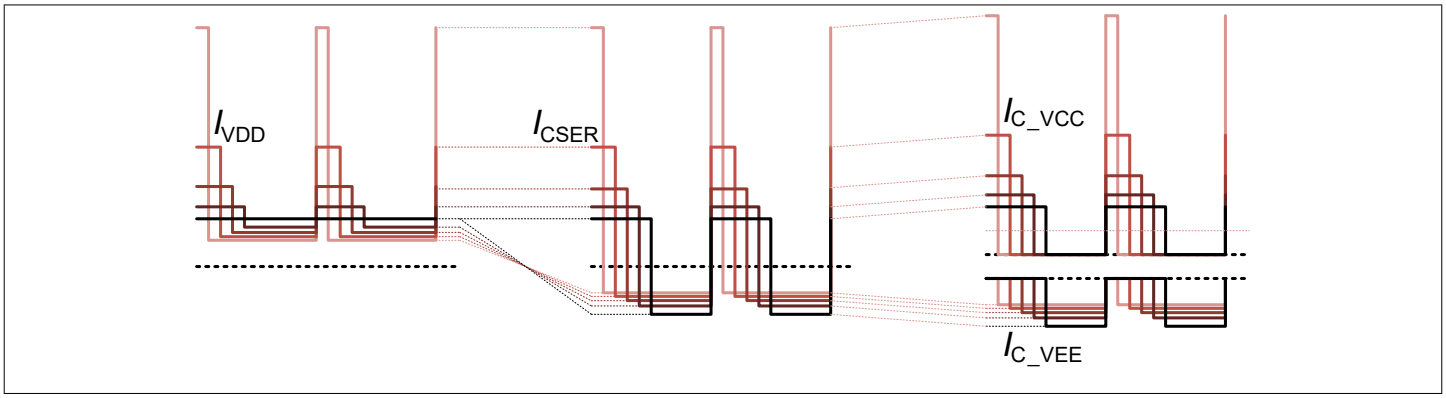


Figure 28 Simplified capacitor ripple current wave form for 10% to 50% duty cycle

5.5.1.2 Output decoupling

Ripple current of the output capacitor C_{VCC}/C_{VEE}

Depending on the duty cycle, the RMS charging current will vary. In addition, the duty cycle for positive and negative output voltage is different (D vs. 1-D). Therefore, two graphs are required to visualize the ripple current for both output voltages.

- The orange curve in Figure 27 shows the VCC ripple current factor
- The yellow curve in Figure 27 shows the VEE ripple current factor
- Approximation formula:
  - $I_{R,VCC} = |I_{OUT}|\sqrt{\frac{1}{D}}$
  - $I_{R,VEE} = |I_{OUT}|\sqrt{\frac{1}{1-D}}$
  - The output capacitors should be designed to handle the ripple current

Capacitance of the output capacitor C_{VCC}/C_{VEE}

The output capacitors, C_{VCC}/C_{VEE}, are used to decouple the gate driver as well as to smoothen the rectified transformer voltage. The decoupling capacitor should be placed close to the gate driver to shrink the gate driver loop. The isolated output voltage decoupling capacitors should be placed close to the rectifier diodes to keep the stray field small. Therefore, this capacitor is typically split into two capacitors. For a given isolated output voltage ripple, the decoupling capacitance can be calculated with the approximation formula:

$$C_{Vxx} \geq \frac{I_{OUT} \cdot (1 - D)}{V_{OUT,\,pp} \cdot f_{SW}}$$

Example

- Estimated output load current: I_{OUT} = 0.1 A
- Target voltage ripple: $V_{OUT,pp}$ = 0.25 V
- 2EP switching frequency: f_{SW} = 50 kHz
- 2EP duty cycle: D = 10%

For this example, a voltage ripple, peak-to-peak, of 0.25 V and an output current of 0.1 A should be assumed. The minimum capacitor value for the positive output voltage *VCC* will be 7.2 µF with a required RMS ripple current capability of 320 mA. It is a best practice to choose the same decoupling capacitor values for both C_{VCC}/C_{VEE} so that a second calculation for *VEE* can be omitted. The capacitance reduction over bias voltage should also be considered.

5.5.1.3 Series capacitor

Ripple current of series capacitor C_{SER}

The RMS current across the series capacitor is dependent on the duty cycle. The duty cycle creates an asymmetric current wave form with equal charges per polarity, and the average current is zero. The amplitude of the ripple current at C_{SER} is the largest ripple current in the supply. The TTR scales the output ripple current and has a linear effect. The higher the TTR, the larger the rise in the ripple current ($TTR = I_{OUT}/I_{IN}$).

- The gray curve in Figure 27 shows the series capacitor ripple current factor
- Approximation formula:
  - $I_{CSER} = \frac{|I_{OUT}|}{TTR}\sqrt{\frac{1}{D - D^2}}$
  - The series capacitor should be designed to handle the ripple current

Capacitance of the series capacitor C_{SER}

The series capacitor, C_{SER}, is used to handle the offset voltage of the PWM driven from the 2EP. This DC current filtering ensures pure AC driving of the transformer. The series capacitor ripple voltage is less critical than for decoupling capacitor. However, a very small series capacitor increases the resonance frequency and the ripple current. For a given series capacitor voltage ripple, the series capacitance can be calculated with the following approximation formula:

$$C_{SER} \geq \frac{I_{OUT}}{TTR \cdot V_{CSER,\,pp} \cdot f_{SW}}$$

The capacitance should be limited to 20 µF to ensure a proper pre-charge during start-up.

Example

- Estimated output load current: I_{OUT} = 0.1 A
- Target voltage ripple: $V_{CSER,pp}$ = 0.25 V
- Transformer turn ratio: TTR = 1.5 : 1
- 2EP switching frequency: f_{SW} = 50 kHz
- 2EP duty cycle: D = 10%

For this example, a voltage ripple, peak-to-peak, of 0.25 V and an output current of 0.1 A should be assumed. The minimum capacitor value will be 5.33 µF with a required RMS ripple current capability of 222 mA. The capacitance reduction over bias voltage should also be considered.

5.5.1.4 Input decoupling

Ripple current of the input decoupling capacitor C_{VDD}

The RMS current at the capacitor C_{VDD} is duty-cycle dependent. Due to the full-bridge output stage, the input capacitor is loaded with the difference in the scaled output currents. This results in a lower ripple current compared to a series capacitor. At 50%, the positive and negative output currents compensate each other and the resulting ripple current is zero. The *TTR* scales the output current and has a linear effect on the input ripple current. The lower the *TTR*, the larger the ripple current at the input side ($TTR = I_{OUT}/I_{IN}$) for a given output current.

- The magenta curve in Figure 27 shows the VDD ripple current factor
- Approximation formula:
  - $I_{R,VDD} = \frac{|I_{OUT}|}{TTR}\sqrt{\frac{1-4D+4D^2}{D-D^2}}$
  - The input decoupling capacitor has to be designed to handle the ripple current

Capacitance of the input decoupling capacitor C_{VDD}

The input decoupling capacitor is used to decouple the 2EP internal supply as well as the power stage to provide current to the transformer. It should be placed closely between the *VDD* supply pin and the *GND* pin.

$$C_{VDD} \geq \frac{I_{OUT} \cdot (1-2D)}{(1-D) \cdot TTR \cdot V_{VDD,pp} \cdot f_{SW}}$$

Example

- Estimated output load current: I_{OUT} = 0.1 A
- Target voltage ripple: $V_{VDD,pp}$ = 0.25 V
- Transformer turn ratio: *TTR* = 1.5 : 1
- 2EP switching frequency: f_{SW} = 50 kHz
- 2EP duty cycle: *D* = 10%

In this example, assume a peak-to-peak voltage ripple of 0.25 V and an output current of 0.1 A. The minimum capacitor value is 4.7 µF with a required RMS ripple current capability of 178 mA. Also, capacitance reduction over bias voltage should be considered.

5.5.2 Dimensioning of transformer

5.5.2.1 Voltage×time product

The voltage×time product is an important parameter in transformer design. It defines the limit of the voltage that can be applied to the input winding of a transformer for a given time.

If the voltage×time product is violated, the transformer will saturate. This means that the core material saturates and the coupling and main inductance collapse to basically an air core. As a result, the magnetizing current increases dramatically. Fulfilling the voltage×time product sets a lower limit for the switching frequency.

For the 2EP full-bridge output stage, the bipolar voltage×time product was chosen to select the transformer.

The voltage×time product for a given switching frequency and input voltage is duty-cycle dependent. The following graph shows an example of the voltage×time product over duty cycle at a switching frequency of 50 kHz and an input voltage of 15 V.

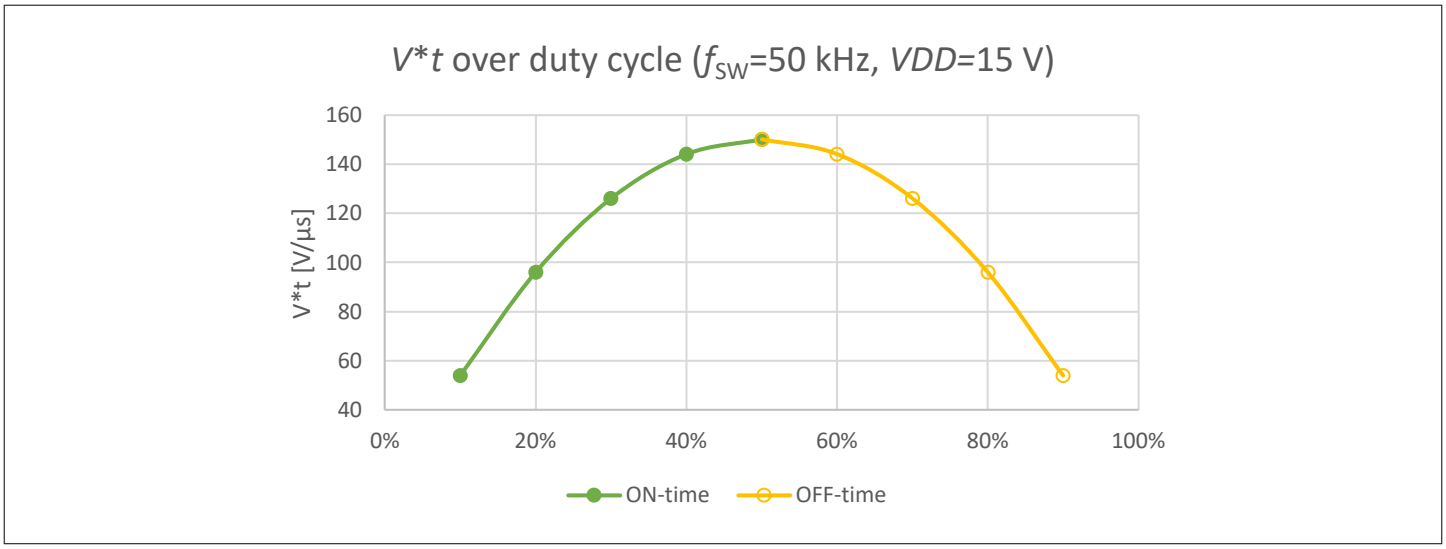


Figure 29 Example bipolar voltage×time product over duty cycle

The voltage×time product can be calculated from the supply voltage (VDD), the duty cycle, and the switching frequency:

$$(V \cdot t)_{bipolar} = \frac{2 \cdot V_{VDD} \cdot D}{f_{SW}} \cdot (1 - D)$$

5.5.2.2 Main inductance

Main inductance converts the applied voltage×time product into a magnetizing current. This means that the magnetizing current is dependent on the input voltage, the duty cycle, and the frequency. It can be calculated using the formula:

$$I_{Lmain,\,pp} = \frac{2 \cdot V_{VDD} \cdot D}{f_{SW} \cdot L_{main}} \cdot (1 - D)$$

In general, the main inductance should follow the rule – “the larger, the better” – for lower magnetizing current and, therefore, lower ohmic losses. However, a large main inductance comes with penalties such as bigger cores and higher number of windings. The coupling capacitance between input and output winding also increases with the number of windings. A good rule of thumb is to define the main inductance such that the peak-to-peak ripple current caused by the load current is a factor of 20 to 100 times larger than the ripple current caused by the main inductance. Lower switching frequencies allow a higher ripple of magnetizing current because core losses are dependent on the frequency.

5.5.2.3 Leakage inductance

Leakage inductance limits the current slope of the transferred current. This has several aspects:

- A lower EMI, but larger isolated output voltage drop over load
- A larger light-load voltage increase

The leakage inductance, as part of the input side impedance, influences the start-up behavior in peak current mode . Paralleling transformers lowers the effective leakage inductance. The leakage inductance versus the required load must be verified during start-up. Typical leakage inductance values of transformers are in the range of 0.1 … 2 µH.

5.5.2.4 Winding resistance

Winding resistance consists out of the DC-resistance and the AC-resistance. The winding resistance increases the losses and the converter's output voltage drop over load.

Typically, the DC-winding resistance is only a small portion of the overall loop resistance, but special care has to be taken for multi-layer windings. Multi-layer windings increase the AC-resistance quite dramatically and, therefore, the converter output voltage drop over load, especially at higher switching frequencies. In general, the winding resistance

should follow the rule – “the smaller, the better” – to reduce transformer losses, especially ohmic losses. Typical transformer values for gate driver supply are dependent on the output current, and in a range of 0.05 to 0.5 Ohm.

5.5.2.5 Winding ratio or transformer turns ratio

The transformer turns ratio (*TTR*) or the winding ratio is a calculation factor of primary-to-secondary voltage relation or equivalent to the primary-to-secondary turns relation.

$$TTR = \frac{V_{PRI}}{V_{SEC}} = \frac{N_{PRI}}{N_{SEC}}$$

The impedance of primary-to-secondary side relates with *TTR*-squared.

$$\frac{Z_{PRI}}{Z_{SEC}} = TTR^2$$

This impacts specifically the output voltage drop at higher load conditions in application scenarios with small *TTR* values to transfer a low input voltage to a higher output voltage.

5.5.2.6 Coupling capacitance

The coupling capacitance between the primary and secondary windings of the transformer plays a major role in EMI, especially in high switching speed applications such as the SiC MOSFET inverter.

The coupling capacitance, C_{IO}, transfers the switching speed *dV/dt* into a common mode current spike. For example, a switching speed of 100 V/ns and a coupling capacitor of 5 pF creates a common mode current spike of up to 0.5 A. This current spike is transferred from the high-power switch side via the transformer coupling capacitance and the output stage of the 2EP to the input side grounding. The combination of high switching speed and large coupling capacitance should be avoided. The typical coupling capacitance for fast switching should be lower than 10 pF.

5.5.3 Dimensioning of rectification diodes

5.5.3.1 Repetitive peak reverse voltage rating – V_{RRM}

The repetitive peak reverse voltage rating of the diode should be more than:

$$V_{RRM} > \frac{2 \cdot V_{VDD}}{TTR} \quad \text{or} \quad V_{RRM} > V_{VCC} - V_{VEE}$$

Margins should be kept for voltage spikes during current transition and light-load output voltage increase. Also, the voltage dependency of the diode reverse leakage currents at higher temperatures should be considered when selecting the voltage rating. Typical reverse breakdown voltage ratings of these diodes in IGBT or SiC MOSFET gate driver supplies are V_{RRM} = 40 V … 60 V.

5.5.3.2 Repetitive peak forward current rating – I_{FRM}

Steady-state operation

During operation, the repetitive peak forward current can be calculated from the output current and the used duty cycle.

- Positive output VCC: repetitive peak forward current $I_{FRM} = \frac{I_{VCC}}{D}$
- Negative output VEE: repetitive peak forward current $I_{FRM} = \frac{I_{VEE}}{1 - D}$

The diodes should withstand the configured and transferred maximum value of the average overcurrent limit of 2EP. This is important for any abnormal operating event, such as overload. This value depends on the selected current setting and duty cycle, see Figure 7 and Figure 9

- Positive output VCC: $I_{FRM} = \frac{I_{OCthr,x} \cdot TTR}{D}$
- Negative output VEE: $I_{FRM} = \frac{I_{OCthr,y} \cdot TTR}{1 - D}$

Start-up operation

2EP uses the $I_{OCthr,6}$ setting for approximately 5 ms during a normal start-up operation. This is independent of the product variant and the configured current setting. Therefore, the diode has to support at least this repetitive peak forward current.

- Positive output VCC: $I_{FRM} = \frac{I_{OCthr,6} \cdot TTR}{D}$
- Negative output VEE: $I_{FRM} = \frac{I_{OCthr,6} \cdot TTR}{1 - D}$

The 2EP transformer driver can be held in start-up mode with its$I_{OCthr,6}$ current setting by overload or short circuit of the isolated output voltage. In such cases, the diode continuously operates with this current until the system reacts and removes the short circuit. Therefore, the diode should be able to withstand this current rating for the system reaction time.

5.5.3.3 Average forward current rating – $I_{F(av)}$

The average forward current rating of the diode should be larger than the average isolated output current. This includes the expected power loss capability of the diode in all operating modes.

5.5.3.4 Forward voltage drop – V_F

The forward voltage drop across diodes is important for calculating the efficiency and output voltage of the isolated power supply. Diodes with low voltage drop must be chosen for highest efficiency. The diode voltage drop at peak forward current must be considered while calculating the output voltage.

5.5.3.5 Diode reverse current – I_R

The diode reverse current impacts the diode's power losses and the overall power loss in an isolated power supply. High reverse current can lead, under worst case conditions, to a thermal runaway of the diode.

If Schottky diodes are used, consider this reverse current during off-time. Schottky diodes are optimized for low forward voltage and typically have large reverse currents with the risk of a thermal runaway. Reverse current is mainly a factor of temperature and reverse voltage. Diodes rated with higher breakdown voltages typically have lower leakage current.

5.5.3.6 Diode capacitance and reverse recovery charge

Diode capacitance and reverse recovery charge play a major role in the rise in light-load output voltage. To minimize this effect, diodes with low capacitance and low reverse recovery charge must be chosen.

5.5.4 Configuration resistor selection

The configuration resistors are read-out and digitized during start-up. All resistor values can be used at the configuration pins, but the IC is optimized for 1% resistors of the E96 series to achieve the highest read-out accuracy.

Please note that the 2EP does not interpolate resistor values. Each value read is matched to exactly one discrete configuration value as indicated in Table 5.

The configuration resistors are only used for a short time after reaching UVLO to configure the IC. To read-out the applied resistors, a current of less than 0.5 mA is applied for a duration of 2 ms. Due to this low power loss (maximum 16 mW) within the resistor for a duration of 2 ms, smaller resistors such as 0402 or 0603 can be used.

5.6 Use case: IGBT driver supply with 2EP100R and 2EP130R

The transformer driver 2EP100R simplifies an isolated IGBT driver supply for output voltages of +15 V/-7.5 V or ±15 V.

The asymmetric output voltage uses peak rectification for the negative rail and voltage doubling for the positive rail. Whereas, the symmetric output voltage uses peak rectification for both rails. The duty cycle for these topologies is always 50%.

2EP100R offers the basic functionality of isolated power supply with classical voltage doubler configuration for +15 V/-7.5 V or peak rectification for ±15 V.

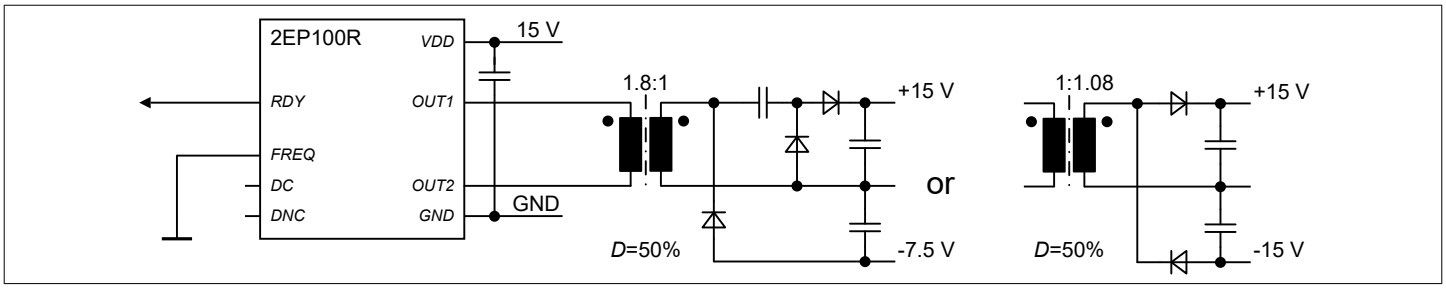


Figure 30 2EP100R example application for asymmetric or symmetric IGBT supply, 66 kHz and 50% duty-cycle

Due to the available duty-cycle setting of 33% in 2EP100R, it can be also be combined with peak rectification for asymmetric output voltage of +15 V/-7.5 V. This configuration achieves the lowest BOM cost.

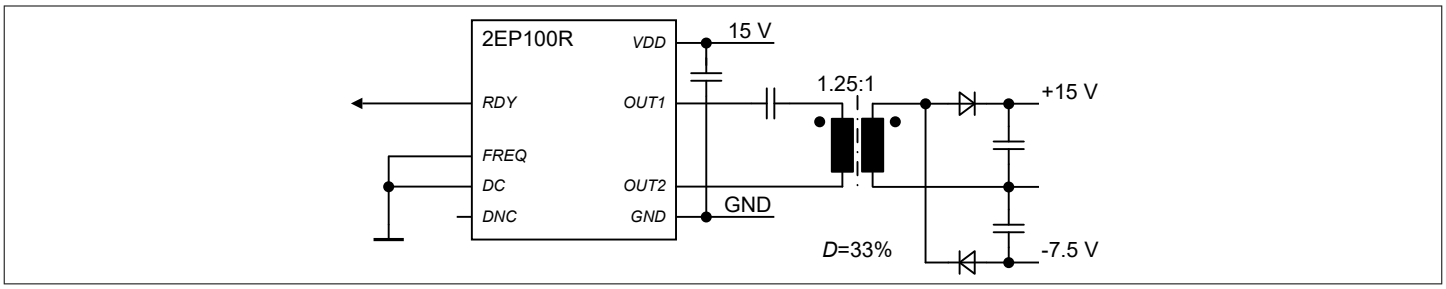


Figure 31 2EP100R example application for asymmetric IGBT supply, 66 kHz and 33% duty cycle

A series capacitor between output *OUT1* and the transformer terminal transfers the unbalanced voltage time product from the 2EP100R outputs with equal peak voltages to a signal with an equal voltage×time product but asymmetric peak voltages. The series capacitor blocks the DC voltage for the transformer by adding an offset.

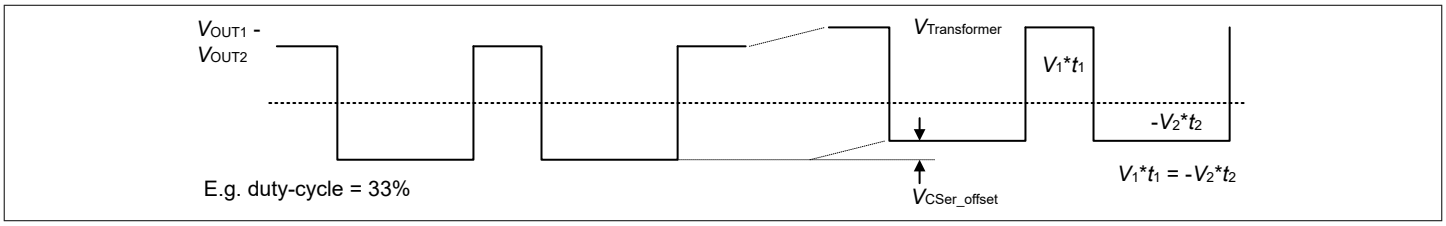


Figure 32 Waveforms at *OUT1-OUT2* before and after the series capacitor vs *OUT1*, duty cycle 33%

2EP130R as an upgrade to 2EP100R offers full flexibility via resistor setting for frequency, duty cycle, or average overcurrent.

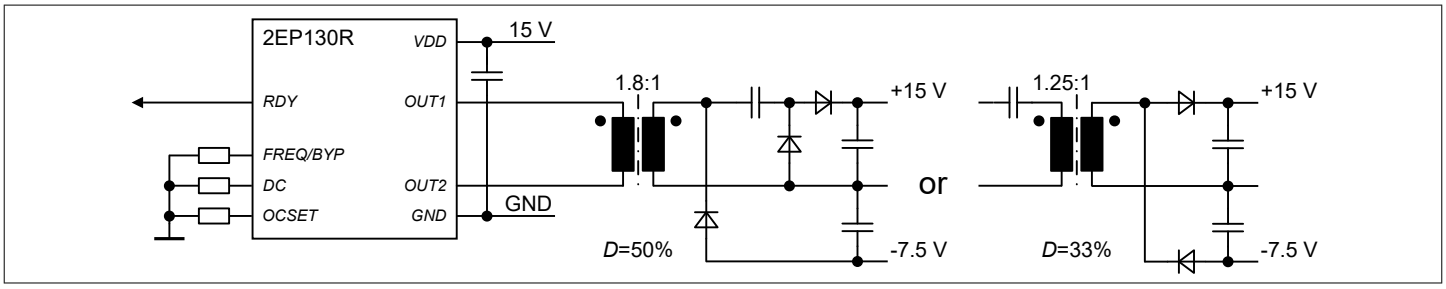


Figure 33 2EP130R example application for asymmetric or symmetric IGBT supply

In the bypass mode, 2EP130R follows a synchronizing signal applied at the *FREQ/BYP* pin. The average overcurrent can be adjusted via the resistor. 2EP130R performs a soft start after applying a PWM signal.

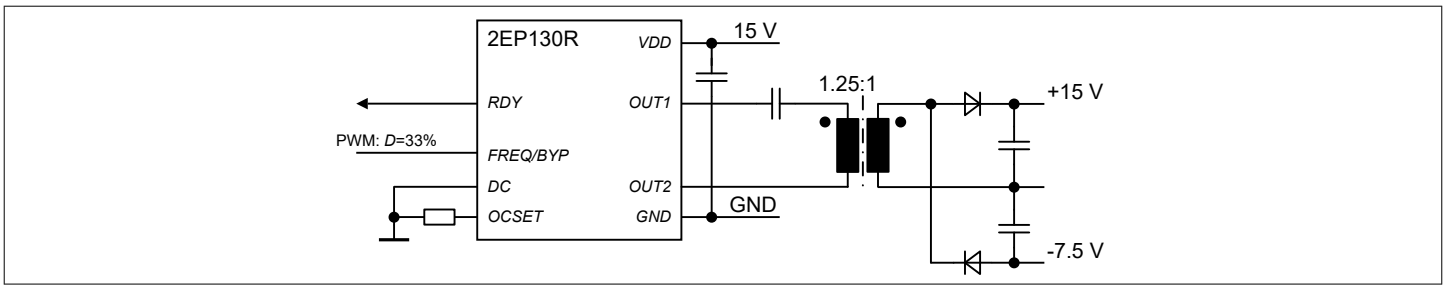


Figure 34 Example application with 2EP130R configured in bypass mode

5.7 Use case: Example of SiC MOSFET driver supply

The calculations in this section are based on the equations from Chapter 5.2. They have been rearranged to calculate the duty cycle and transformer turn ratio (*TTR*) from the requested voltages. The purpose for this example is to get an output voltage suitable for SiC MOSFET gate driver ICs.

Application parameters (input)

- Input supply voltage for 2EP130R: V_{VDD} = 15 V
- Nominal target positive output voltage after peak rectification: V_{VCCx} = 18 V
- Nominal target negative output voltage after peak rectification: V_{VEEx} = *-2.5 V*
- Expected diode forward voltage: V_F = 0.4 V

The output voltages provided here are considered nominal when the increase in light load output voltage and the drop in load-dependent output voltage are negligible. For the transformer suggested in this example, the nominal load is approximately 15 mA. To consider the impact of the diode forward voltage on the output voltages, a more accurate calculation of parameters is required.

Calculating and selecting the duty cycle

To calculate the duty cycle (*D*) for 2EP1xxR, the positive output voltage V_{VCCx} should be put relative to the total output voltage. The voltage at the transformer should be one forward voltage drop higher than each of the expected output voltages. The whole value then needs to be subtracted from 1 to get the duty cycle for *OUT1*:

$$D = 1 - \frac{V_{\mathrm{VCCx}} + V_{\mathrm{F}}}{2 \cdot V_{\mathrm{F}} + V_{\mathrm{VCCx}} - V_{\mathrm{VEEx}}}$$

$$D = 1 - \frac{18\,V + 0.4\,V}{2 \cdot 0.4\,V + 18\,V - (-2.5\,V)}$$

$$D = 0.136 \Rightarrow D_{\mathrm{selected}} = 14\,\%$$

The percentage value needs to be an integer to be compatible with 2EP. The selected duty cycle, in this example, is rounded to 14%. According to the resistor selection table given in the 2EP1xxR datasheet, this duty cycle setting requires a resistor value of 698 Ω at the *DC* pin. It introduces a slight offset in the actual output voltage compared to the target value.

***Note**: 2EP1xxR supports duty cycles in the range of 10% and 50%.*

Calculating and selecting the transformer turn ratio

To calculate the transformer turn ratio (*TTR*), the total primary transformer voltage needs to be put relative to the total output voltage of the transformer on the secondary side as required by the application. As 2EP1xxR is a full-bridge transformer driver, the total voltage at the primary transformer winding is twice the input supply voltage of 2EP1xxR. The series capacitor between 2EP1xxR and the transformer does not influence the total input voltage of the transformer. Its offset is applied to both polarities so that the absolute voltage remains constant:

$$\mathrm{TTR} = \frac{2 \cdot V_{\mathrm{VDD}}}{2 \cdot V_F + V_{\mathrm{VCCx}} - V_{\mathrm{VEEx}}}$$

$$\mathrm{TTR} = \frac{2 \cdot 15\,V}{2 \cdot 0.4\,V + 18\,V - (-2.5\,V)}$$

$$TTR = 1.41 \Rightarrow TTR_{selected} = 1.4$$

In this example, the calculated transformer turn ratio is very close to that of the Würth Elektronik transformer (part number 750319377) that has a transformer turn ratio of 1.4:1. Calculating and selecting a matching transformer again introduces an offset from the target values. It is, therefore, recommended that the selection be verified as the last step.

Verifying the selection

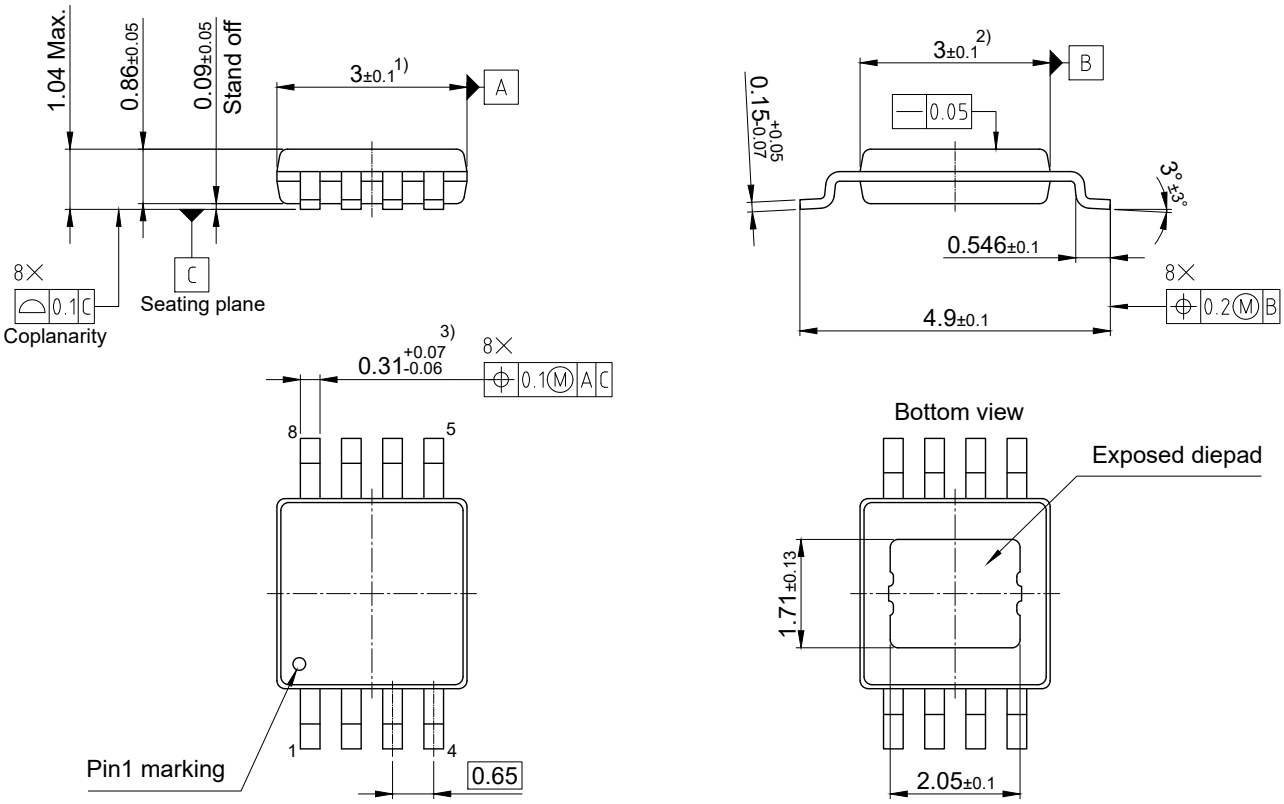
After all the required parameters are identified and matched to their components, the resulting output voltage can be calculated and compared with the target voltages:

$$V_{\mathrm{VCC}} = \frac{2 \cdot V_{\mathrm{VDD}} \cdot (1 - D_{\mathrm{selected}})}{\mathrm{TTR}_{\mathrm{selected}}} - V_F \Rightarrow V_{\mathrm{VCC}} = 18.03\,V$$

$$V_{\mathrm{VEE}} = \frac{2 \cdot V_{\mathrm{VDD}} \cdot (-D_{\mathrm{selected}})}{\mathrm{TTR}_{\mathrm{selected}}} + V_F \Rightarrow V_{\mathrm{VEE}} = -2.60\,V$$

In this example, the output voltages match with the target values quite well and only deviate by 0.2% for the positive and 4% for the negative output voltage. Considering that 2EP1xxR is an open loop transformer driver, the actual output voltages also depend on the stability of the input voltages and the load conditions of these output voltages.

6 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include plastic or metal protrusion of 0.25 max. per side
3) Does not include dambar protrusion of 0.13 max.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]

Figure 35 PG-TSSOP-8-1 package outline

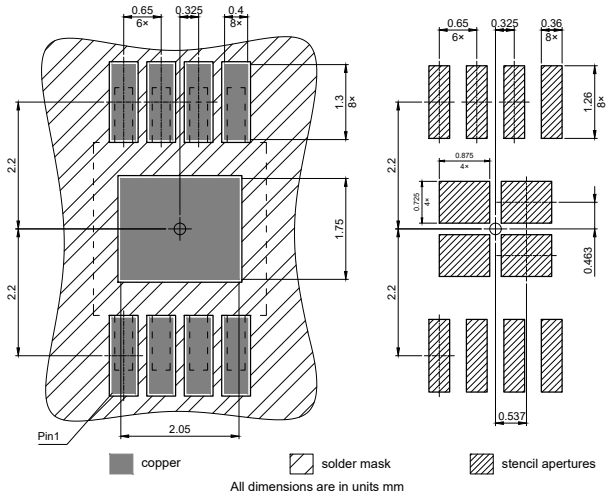


Figure 36 PG-TSSOP-8-1 footprint

Revision history

Document version	Date of release	Description of changes
v1.00	2024-08-31	• Correction of voltage×time product and related formulas
v0.70	2024-06-14	• Added the Application section for preliminary datasheet • Updated parameter names, diagrams, and descriptions for clarity reasons
v0.5	2021-11	Initial version of the target datasheet

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Edition 2024-08-31

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-bhc1653462652419

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