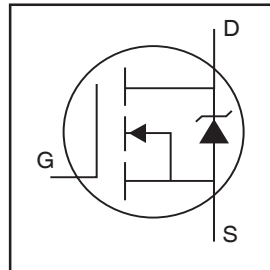


IRL3803VSPbF
IRL3803VLPbF
 HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL3803VS)
- Low-profile through-hole (IRL3803VL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

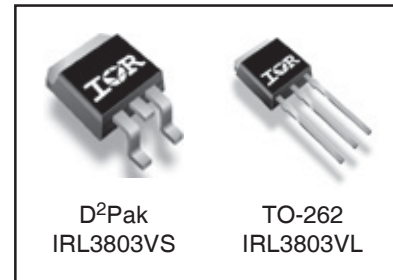


$V_{DS} = 30V$
$R_{DS(on)} = 5.5m\Omega$
$I_D = 140A$ ⑦

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑧	140 ⑦	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ⑧	110	
I_{DM}	Pulsed Drain Current ① ⑧	470	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
I_{AR}	Avalanche Current ①	71	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑧	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady state) ⑨	—	40	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.028	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	5.5	m Ω	$V_{GS} = 10V, I_D = 71A$ ④
		—	—	7.5		$V_{GS} = 4.5V, I_D = 59A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ ③
g_{fs}	Forward Transconductance	82	—	—	S	$V_{DS} = 25V, I_D = 71A$ ④③
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	76	nC	$I_D = 71A$
Q_{gs}	Gate-to-Source Charge	—	—	19		$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	35		$V_{GS} = 4.5V$, See Fig. 6 and 13 ③
$t_{d(on)}$	Turn-On Delay Time	—	16	—	nH	$V_{DD} = 15V$ $I_D = 71A$ $R_G = 1.3\Omega$ $V_{GS} = 4.5V$, See Fig. 10 ④③
t_r	Rise Time	—	180	—		
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		
t_f	Fall Time	—	37	—		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3720	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5 ③
C_{oss}	Output Capacitance	—	1480	—		
C_{rss}	Reverse Transfer Capacitance	—	270	—		
E_{AS}	Single Pulse Avalanche Energy ②③	—	1560③	400⑥	mJ	$I_{AS} = 71A, L = 0.16\text{mH}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	140⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	470		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 71A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	52	78	ns	$T_J = 25^\circ\text{C}, I_F = 71A$
Q_{rr}	Reverse Recovery Charge	—	91	140	nC	$di/dt = 100A/\mu s$ ④③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}, L = 160\mu\text{H}$
 $R_G = 25\Omega, I_{AS} = 71A, V_{GS} = 10V$ (See Figure 12)
- ③ $I_{SD} \leq 71A, di/dt \leq 110A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.

- ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑧ Uses IRL3803 data and test conditions.
- ⑨ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

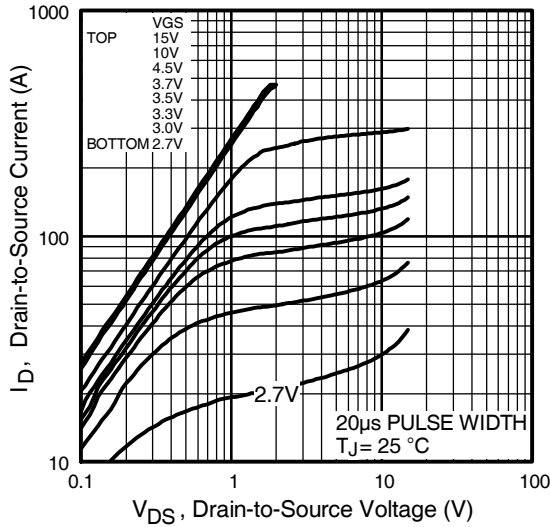


Fig 1. Typical Output Characteristics

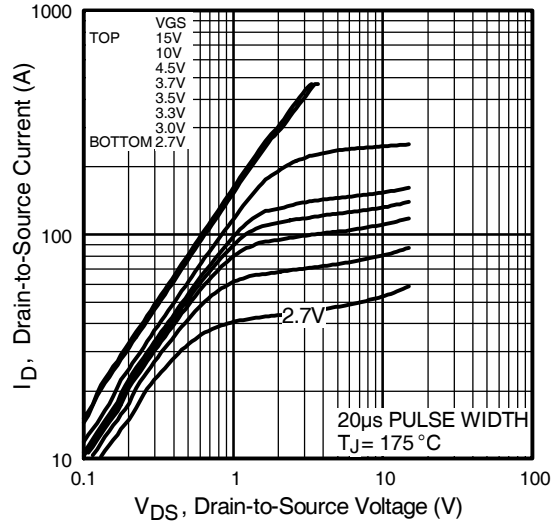


Fig 2. Typical Output Characteristics

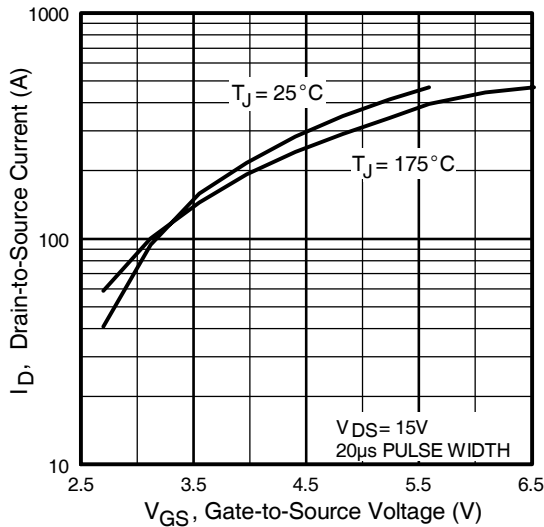


Fig 3. Typical Transfer Characteristics

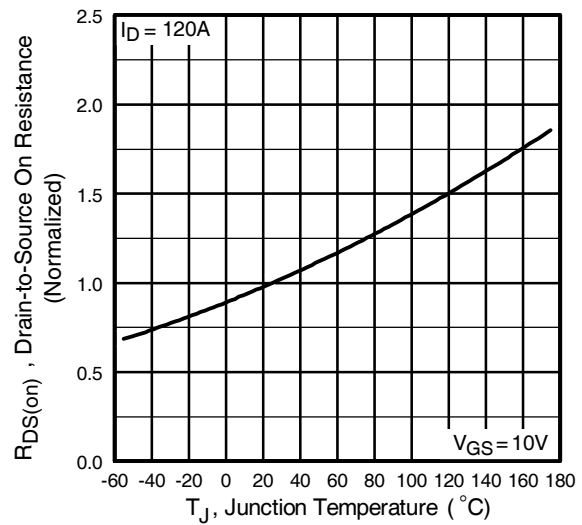


Fig 4. Normalized On-Resistance Vs. Temperature

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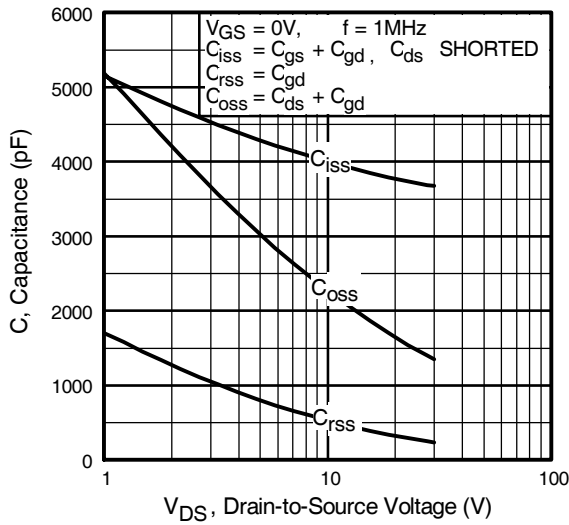


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

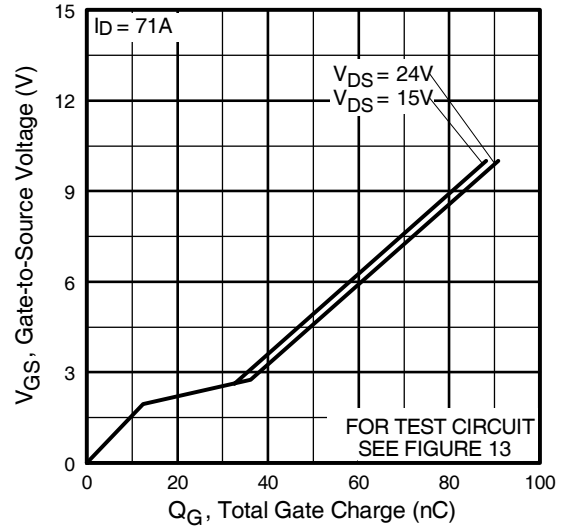


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

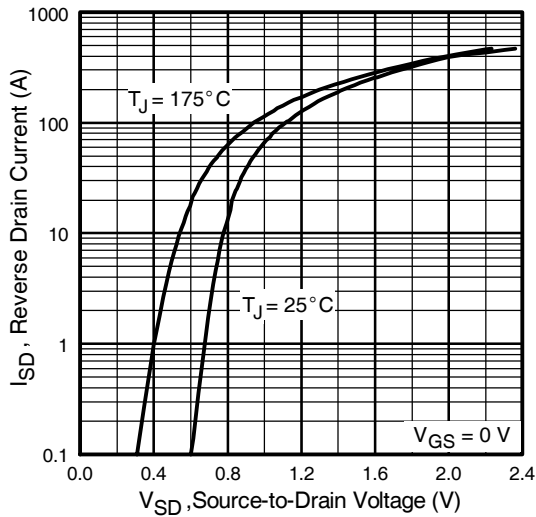


Fig 7. Typical Source-Drain Diode Forward Voltage

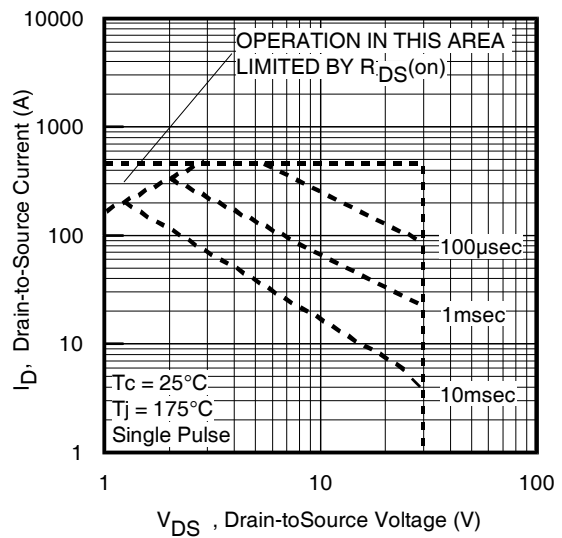


Fig 8. Maximum Safe Operating Area

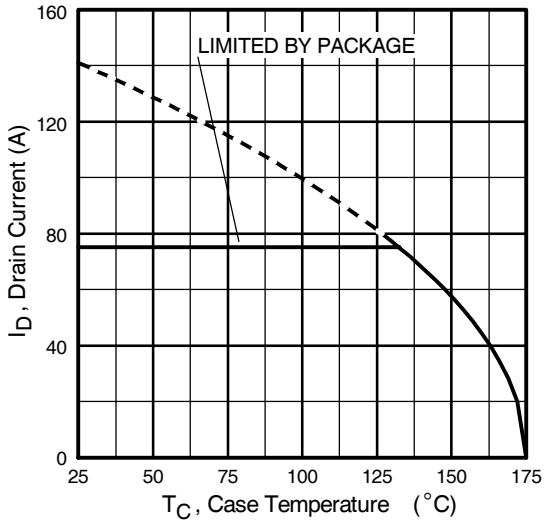


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

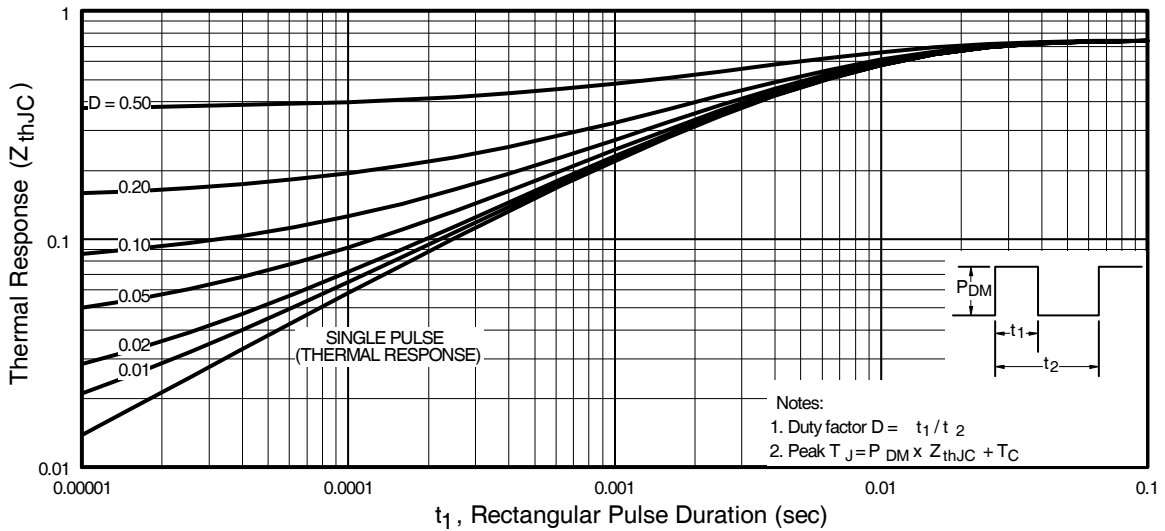


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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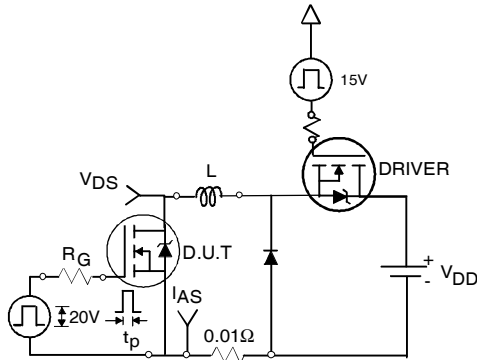


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

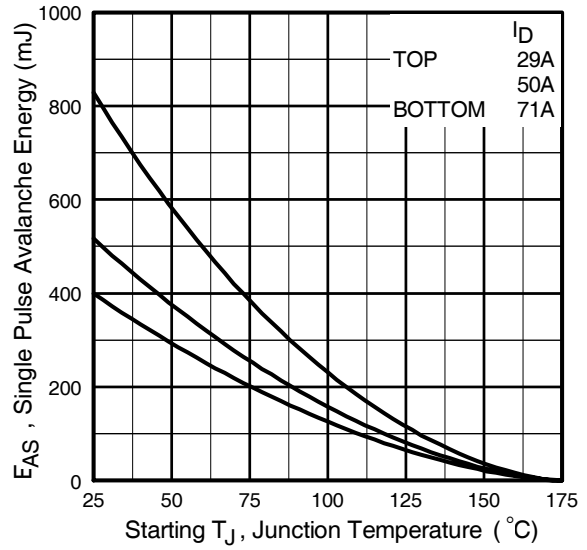


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

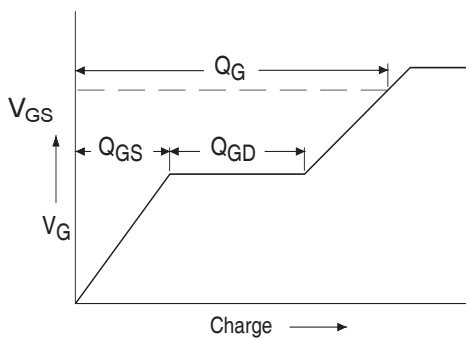


Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

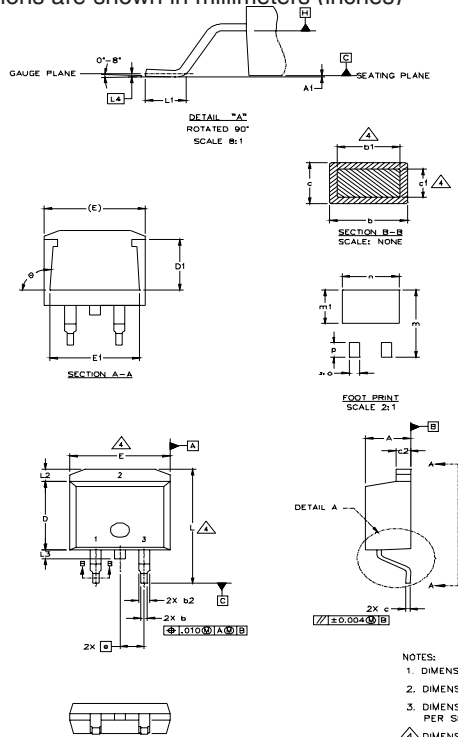
Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	4
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25	BSC	.010	BSC	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
theta	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE -
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

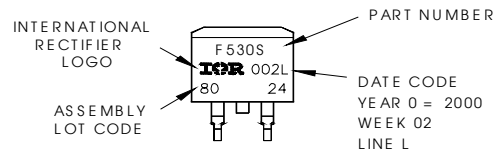
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

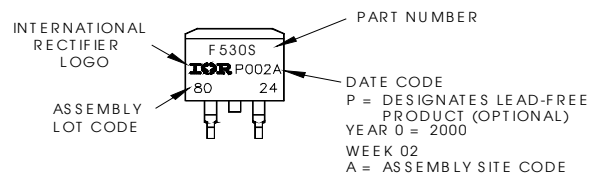
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

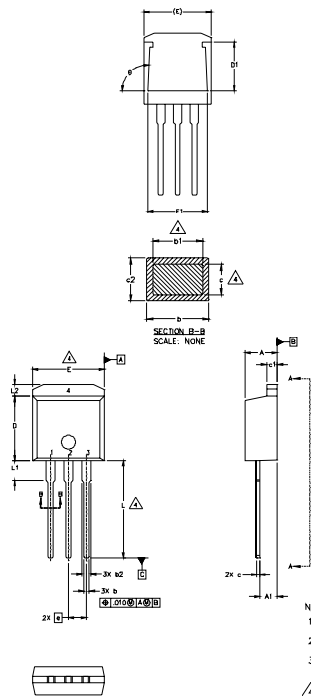


OR



IRL3803VS/IRL3803VLPbF

TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

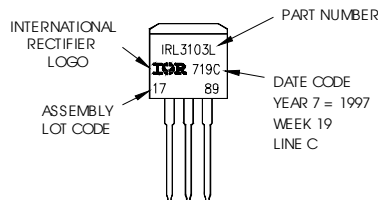
HEXFET	IGBT
1.- GATE	1- GATE
2.- DRAIN	2- COLLECTOR
3.- SOURCE	3- EMITTER
4.- DRAIN	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSIONS INCH.

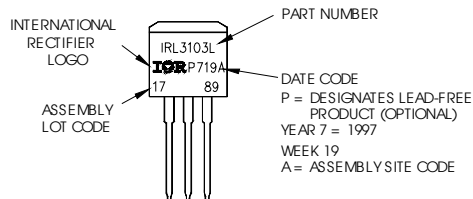
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



OR

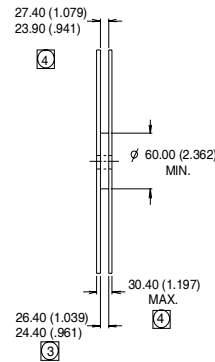
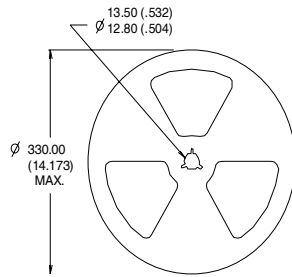
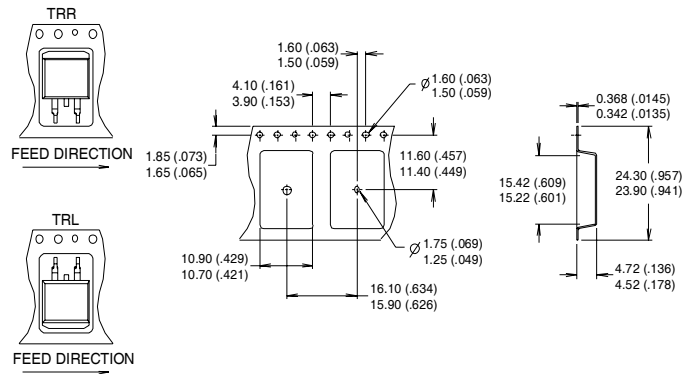


IRL3803VS/IRL3803VLPbF

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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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Visit us at www.irf.com for sales contact information. 01/05

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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[JANTX2N6784U](#) [JANTXV2N5416U4](#) [SQM110N05-06L-GE3](#) [SIHF35N60E-GE3](#) [2SK2614\(TE16L1,Q\)](#)