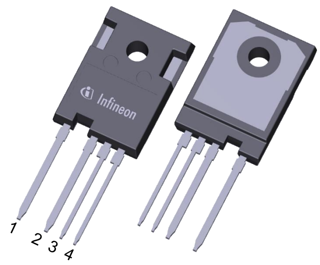
Final datasheet
CoolSiC™ 1200 V SiC Trench MOSFET



Features

- V_{DSS} = 1200 V at T_{vj} = -55...175°C
- I_{DDC} = 38 A at T_C = 25°C
- $R_{DS(on)}$ = 60 mΩ at V_{GS} = 20 V, T_{vj} = 25°C
- New performance-optimized chip technology (Gen1p) with improved R_{DSon}* A FOM
- Increased recommended turn-on voltage ($V_{GS(on)}$ = 20 V) for lower $R_{DS(on)}$
- Best in class switching energy for lower switching losses and reduced cooling efforts
- Lowest device capacitances for higher switching speeds and higher power density
- A combination of low C_{rss}/C_{iss} ratio and high $V_{GS(th)}$ to avoid parasitic turn-on and enable unipolar gate driving
- Reduced total gate charge Q_{Gtot} for lower driving power and losses
- .XT die attach technology for best in class thermal performance
- Sense pin for optimized switching performance
- Suitable for HV creepage requirements

Halogen-free
Green
Lead-free
RoHS
AEC Qualified

Potential applications

- On-board charger
- DC/DC converter
- Auxiliary drives

Product validation

- Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

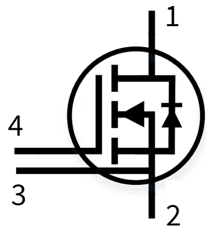
Pin definition:

1 – drain

2 – source

3 – Kelvin sense contact

4 – gate



Type	Package	Marking
AIMZH120R060M1T	PG-TO247-4-STD-NT6.7	A12M1T060

Table of contents

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}				260	°C
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.58	0.76	K/W

***Note**: Not subject to production test. Parameter verified by design/characterization.*

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	V_{GS} = 20 V	T_c = 25 °C	38	A
			T_c = 100 °C	27	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	V_{GS} = 20 V		97	A
Gate-source voltage, max. transient voltage[1)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage	V_{GS}			-5...23	V
Avalanche energy, single pulse	E_{AS}	I_D = 10 A, V_{DD} = 50 V, L = 3.6 mH		180	mJ
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		T_c = 25 °C	197	W
			T_c = 100 °C	99	

1) **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		20	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values Min.	Values Typ.	Values Max.	Unit
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 13 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 20 V		60	75	mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 20 V		84		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 20 V		120		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		65		
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 4.3 mA, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.3	5.1	V
			T_{vj} = 175 °C		3.8		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C		0.3	13	µA
			T_{vj} = 175 °C		50		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 25 V			100	nA
			V_{GS} = -10 V			-100	
Forward transconductance	g_{fs}	I_D = 13 A, V_{DS} = 20 V			8.5		S
Short-circuit withstand time[1)]	t_{SC}	V_{DD} ≤ 800 V, $V_{DS,peak}$ < 1200 V, $T_{vj(start)}$ = 25 °C, $R_{G,ext}$ = 2 Ω	$V_{GS(on)}$ = 20 V		1.5		µs
			$V_{GS(on)}$ = 18 V		2		
			$V_{GS(on)}$ = 15 V		2.5		
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			3.7		Ω
Input capacitance	C_{iss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			880		pF
Output capacitance	C_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			43		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			2		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			18		µJ
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, turn-on pulse			32		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, turn-on pulse			8		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, turn-on pulse			5		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, L_σ = 15 nH	T_{vj} = 25 °C		9		ns
			T_{vj} = 175 °C		9		

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		6		ns
			T_{vj} = 175 °C		8		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		17		ns
			T_{vj} = 175 °C		18		
Fall time	t_f	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		9		ns
			T_{vj} = 175 °C		10		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		77		µJ
			T_{vj} = 175 °C		128		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		50		µJ
			T_{vj} = 175 °C		51		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 13 A, V_{GS} = 0/20 V, $R_{GS(on)}$ = 2 Ω, $R_{GS(off)}$ = 2 Ω, $L_σ$ = 15 nH	T_{vj} = 25 °C		127		µJ
			T_{vj} = 175 °C		179		
Virtual junction temperature	T_{vj}			-55		175	°C

1) verified by the design/characterization

***Note**:* *Dynamic test circuit see Fig. F.*

3 Body diode (MOSFET)

Table 5 Maximum rated values

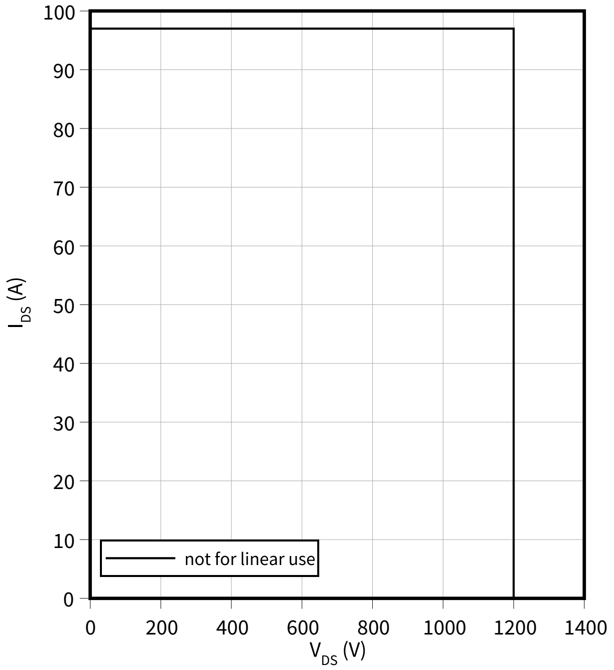
Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	30	A
			T_c = 100 °C	21	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		30	A

Table 6 Characteristic values

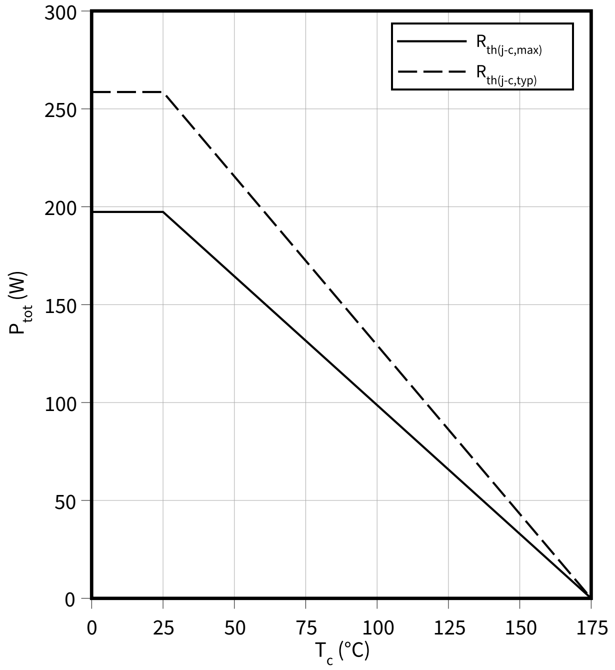
Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 13 A, V_{GS} = 0 V	T_{vj} = 25 °C		3.9	5	V
			T_{vj} = 100 °C		3.8		
			T_{vj} = 175 °C		3.7		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 13 A, V_{GS} = 0 V, di_{SD}/dt = 3000 A/µs, Q_{fr} includes also Q_C	T_{vj} = 25 °C		120		nC
			T_{vj} = 175 °C		203		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 13 A, V_{GS} = 0 V, di_{SD}/dt = 3000 A/µs, Q_{fr} includes also Q_C	T_{vj} = 25 °C		8.5		A
			T_{vj} = 175 °C		17		
Virtual junction temperature	T_{vj}			-55		175	°C

4 Characteristics diagrams

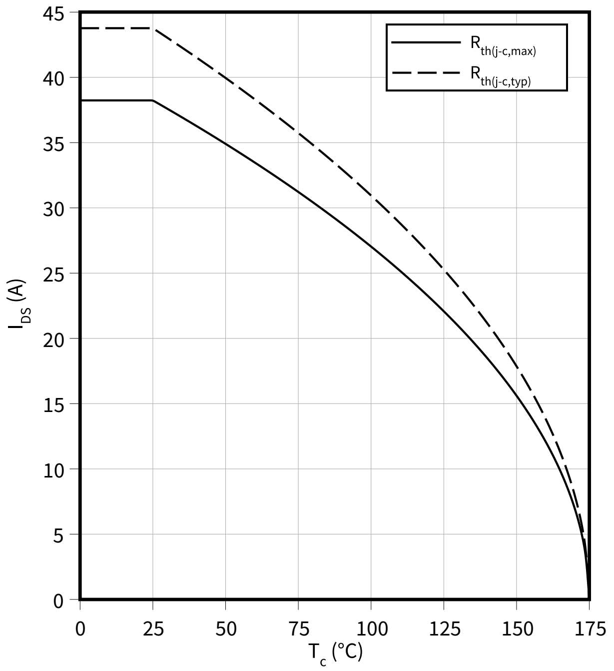
Reverse bias safe operating area (RBSOA)
$I_{DS} = f(V_{DS})$
$T_{vj} \leq 175\ °C$, $V_{GS} = 0/20\ V$, $T_c = 25\ °C$



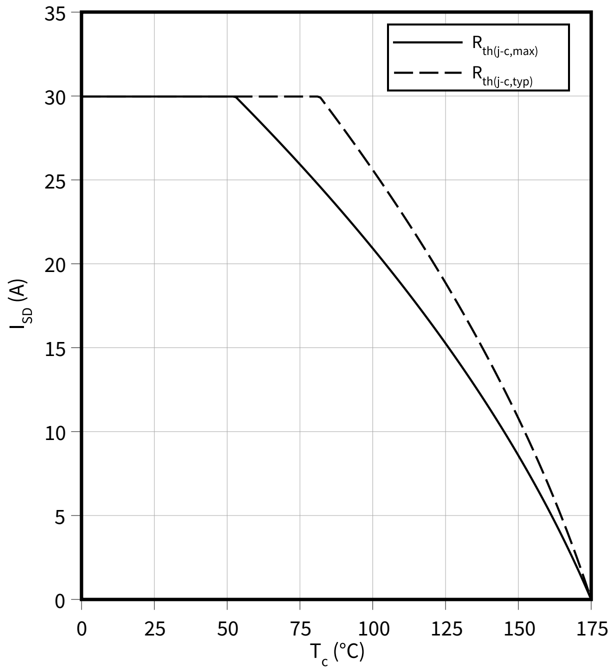
Power dissipation as a function of case temperature
$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature
$I_{DS} = f(T_c)$



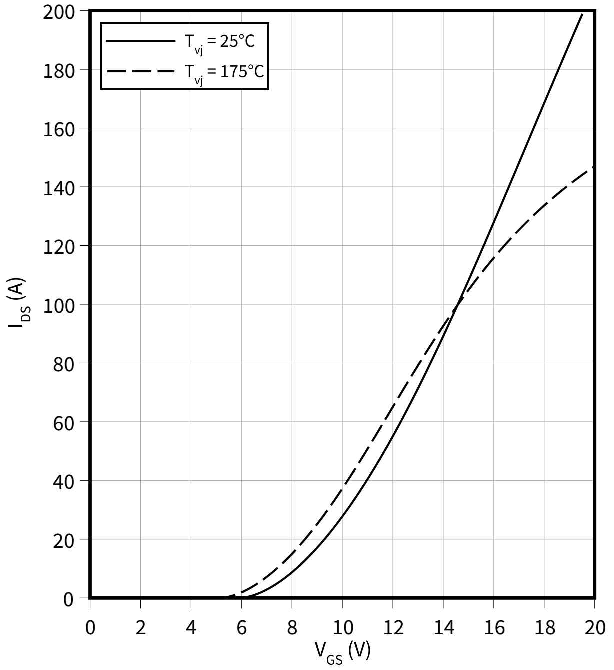
Maximum source to drain current as a function of case temperature
$I_{SD} = f(T_c)$
$V_{GS} = 0\ V$



Typical transfer characteristic

$I_{DS} = f(V_{GS})$

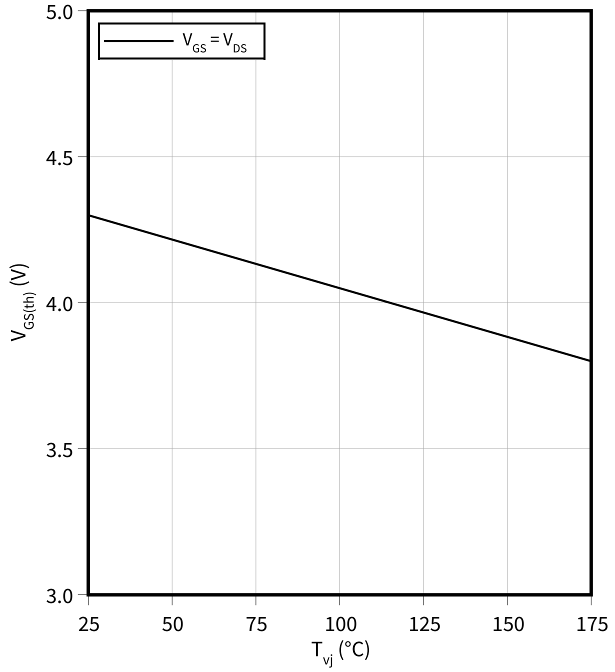
$V_{DS} = 20\ V$



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

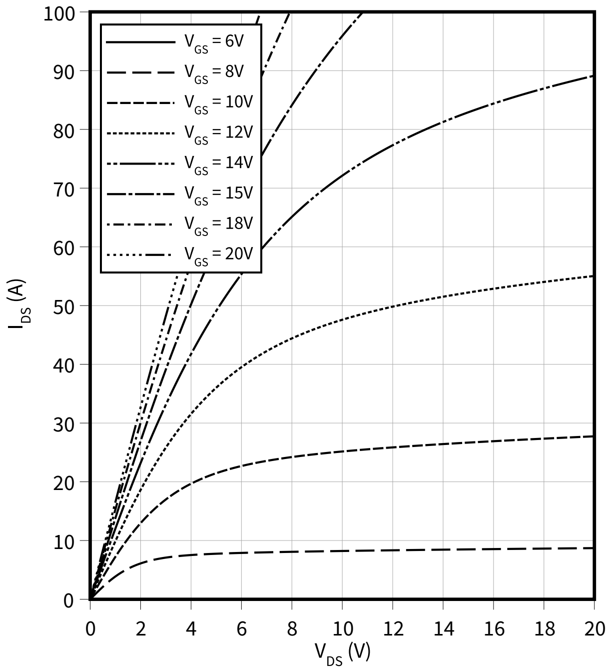
$I_D = 4.3\ mA$



Typical output characteristic, V_{GS} as parameter

$I_{DS} = f(V_{DS})$

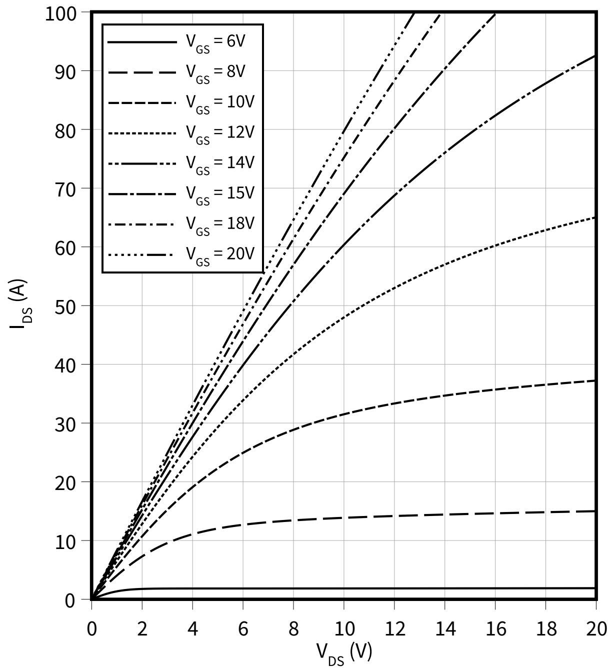
$T_{vj} = 25\ °C$



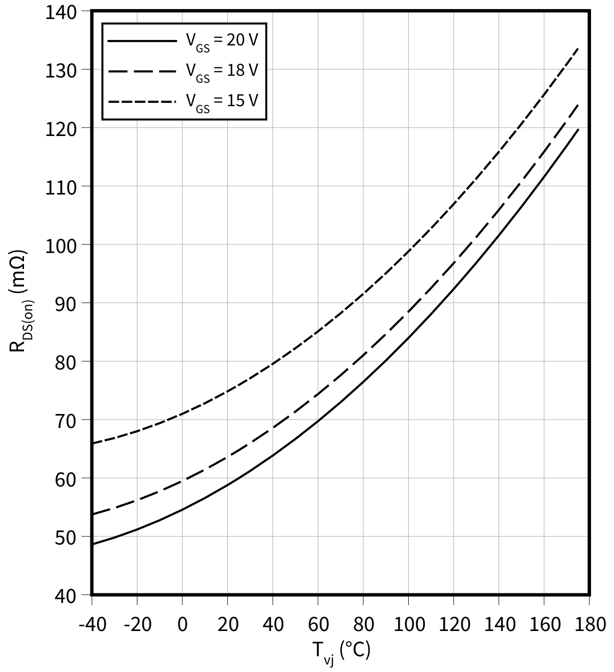
Typical output characteristic, V_{GS} as parameter

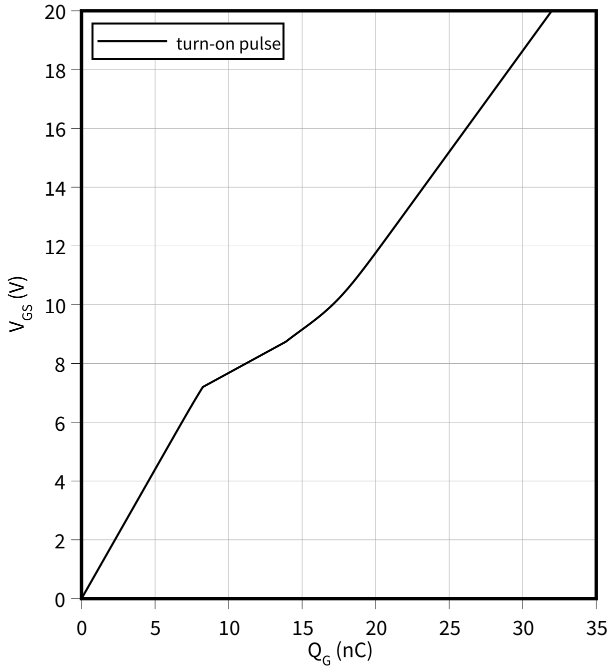
$I_{DS} = f(V_{DS})$

$T_{vj} = 175\ °C$

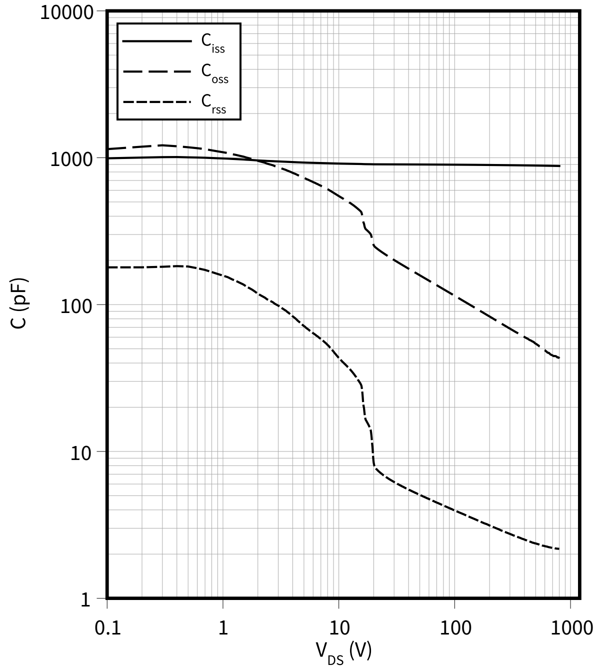


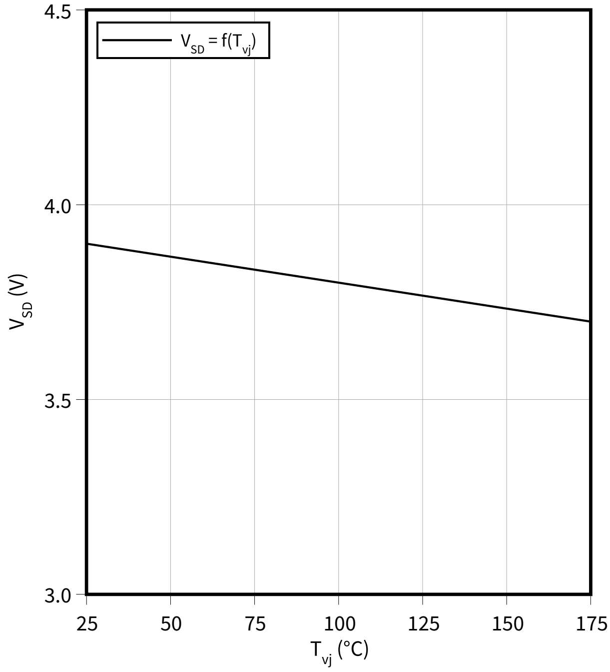
Typical on-state resistance as a function of junction temperature	Typical gate charge
$R_{DS(on)} = f(T_{vj})$	$V_{GS} = f(Q_G)$
$I_D = 13$ A	$I_D = 13$ A, $V_{DS} = 800$ V





Typical capacitance as a function of drain-source voltage	Typical reverse drain voltage as function of junction temperature
$C = f(V_{DS})$	$V_{SD} = f(T_{vj})$
$f = 100$ kHz, $V_{GS} = 0$ V	$I_{SD} = 13$ A, $V_{GS} = 0$ V

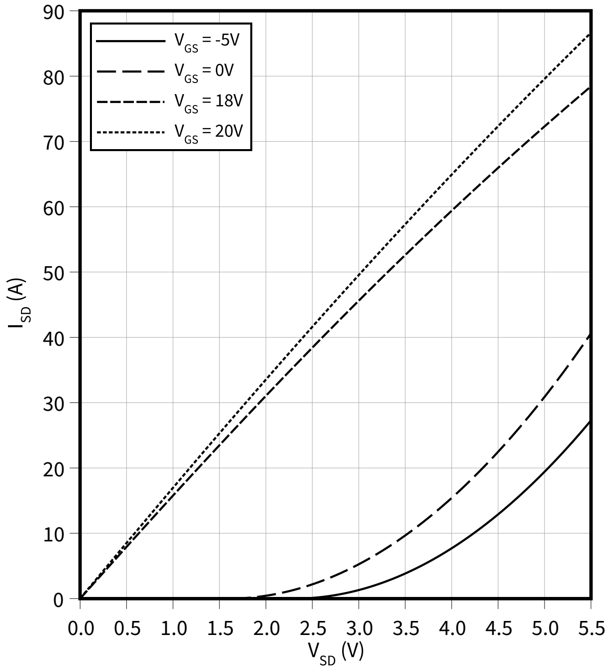




Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

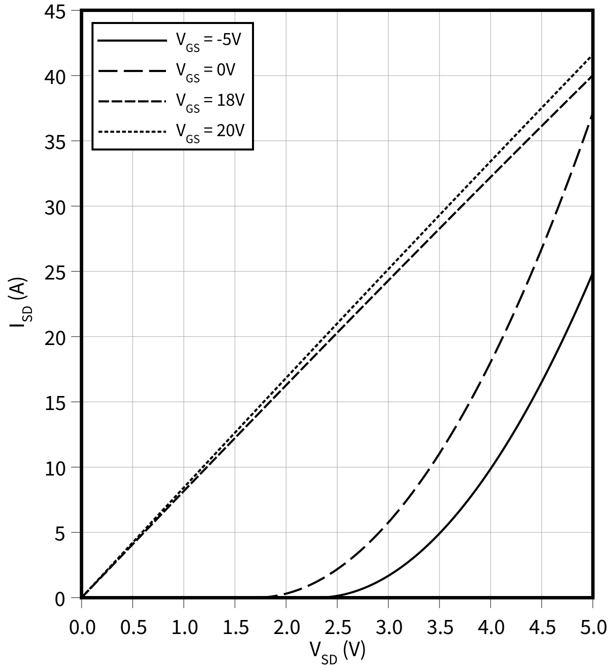
$T_{vj} = 25\ °C$



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

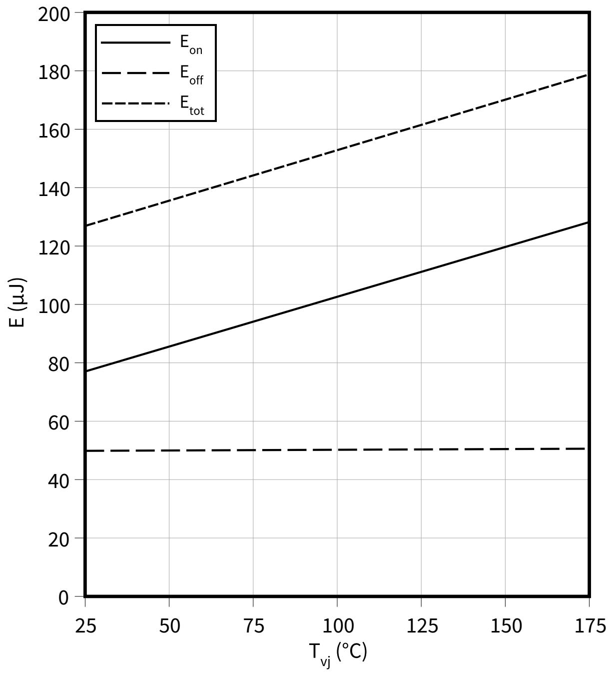
$T_{vj} = 175\ °C$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\ V$

$E = f(T_{vj})$

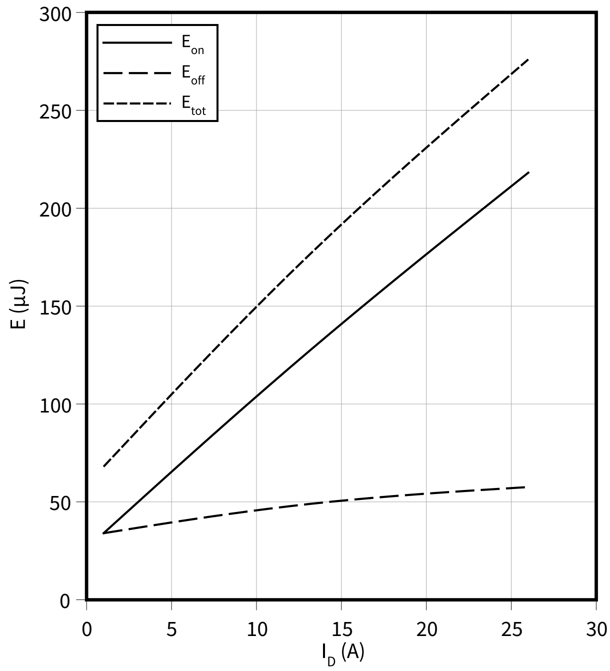
$V_{GS} = 0/20\ V$, $I_D = 13\ A$, $R_{G,ext} = 2\ \Omega$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0\ V$

$E = f(I_D)$

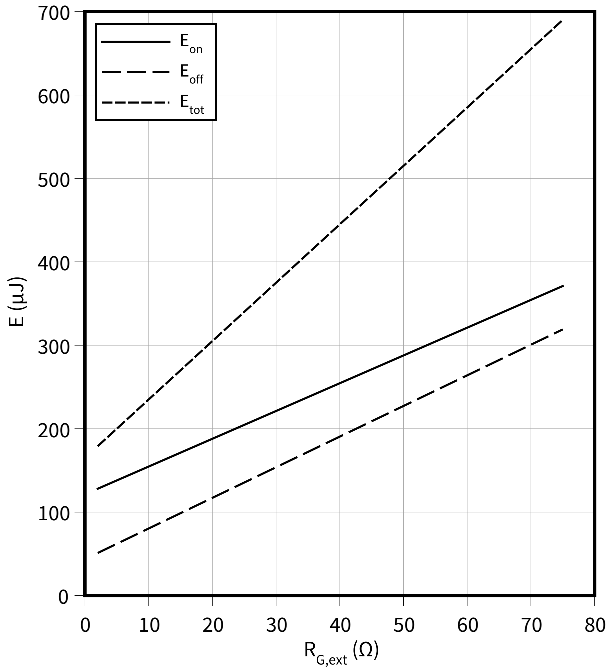
$V_{GS} = 0/20\ V$, $T_{vj} = 175\ °C$, $R_{G,ext} = 2\ \Omega$, $V_{DD} = 800\ V$



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

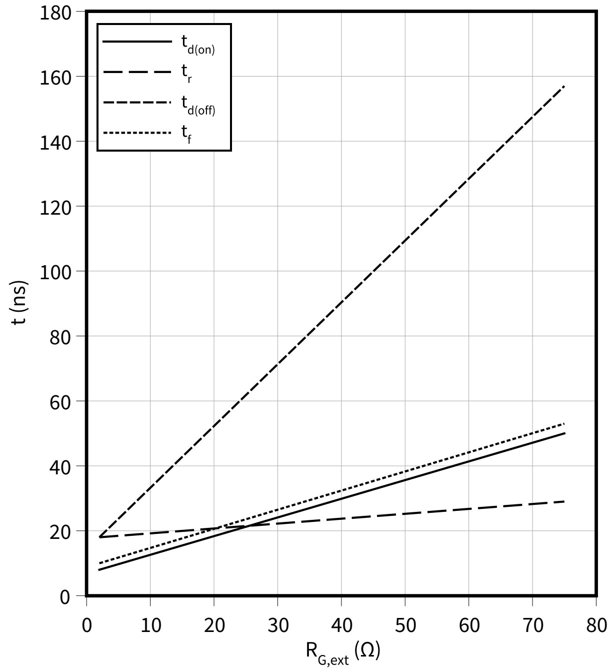
V_{GS} = 0/20 V, I_D = 13 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

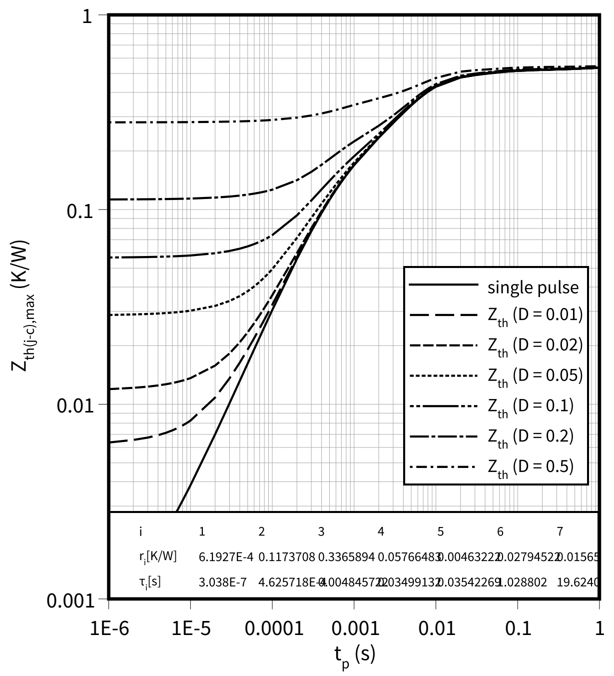
V_{GS} = 0/20 V, I_D = 13 A, T_{vj} = 175 °C, V_{DD} = 800 V



Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j-c),max} = f(t_p)$

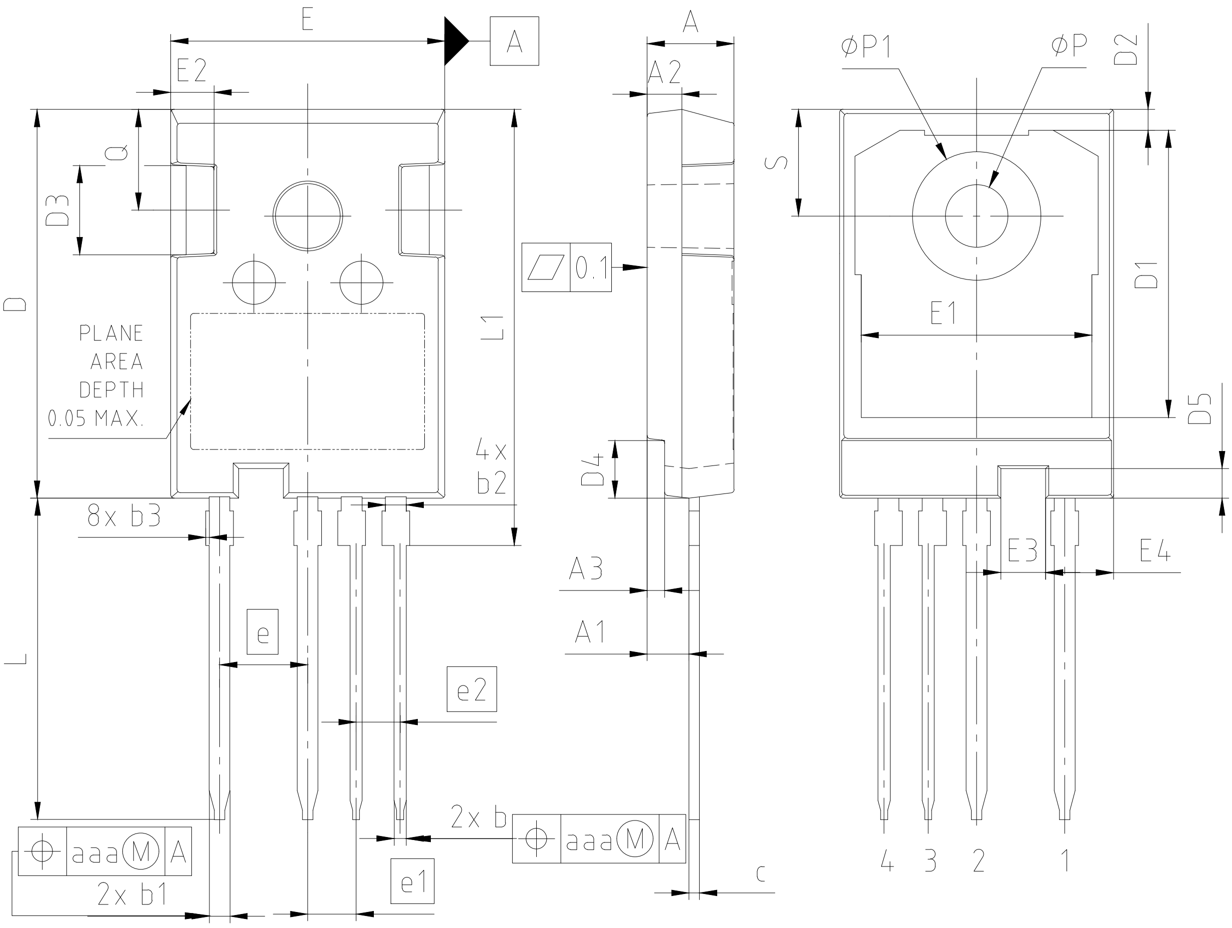
$D = t_p/T$



i	1	2	3	4	5	6	7
r_i[K/W]	6.1927E-4	0.1173708	0.3365894	0.05766483	0.00463222	0.02794522	0.01565
τ_i[s]	3.038E-7	4.625718E-4	0.00484572	0.03499132	0.03542269	1.028802	19.6240

5 Package outlines

PG-TO247-4-STD-NT6.7



PACKAGE - GROUP NUMBER:	PG-TO247-4-U03				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	**E**	15.70	15.90
A1	2.31	2.51	**E1**	13.10	13.50
A2	1.90	2.10	**E2**	2.40	2.60
A3	0.90	1.10	**E3**	2.48	2.68
b	0.66	0.79	**E4**	3.82	4.02
b1	1.16	1.29	**e**	5.08	
b2	1.16	1.29	**e1**	2.79	
b3		0.20	**e2**	2.54	
c	0.59	0.66	**N**	4	
D	22.30	22.50	**L**	18.40	18.70
D1	16.25	16.85	**L1**	24.97	25.27
D2	1.05	1.35	**øP**	3.50	3.70
D3	5.00	5.20	**øP1**		7.40
D4	3.22	3.42	**Q**	5.60	6.00
D5	1.60	1.80	**S**	6.00	6.30
			aaa	0.25	

NOTE: DIMENSIONS DO NOT INCLUDE MOLDFLASH; PROTRUSION OR GARE BURRS

Figure 1

6 Testing conditions

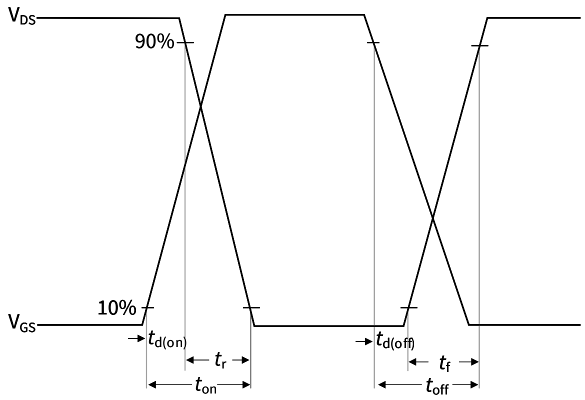


Figure A. **Definition of switching times**

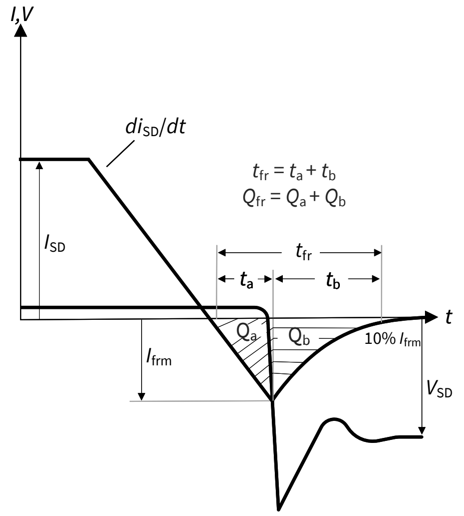


Figure B. **Definition of body diode switching characteristics**

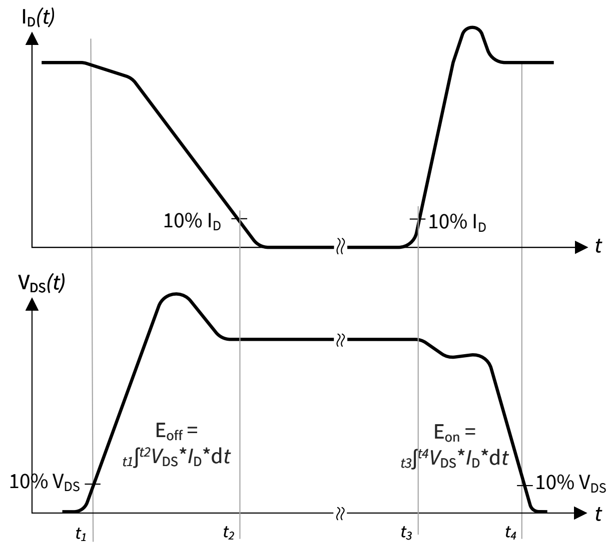


Figure C. **Definition of switching losses**

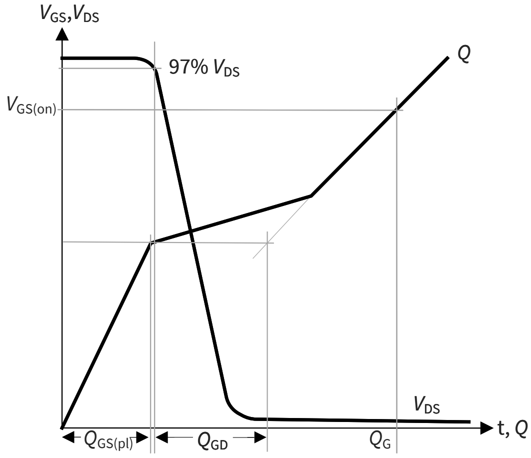


Figure D. **Definition of QGD**

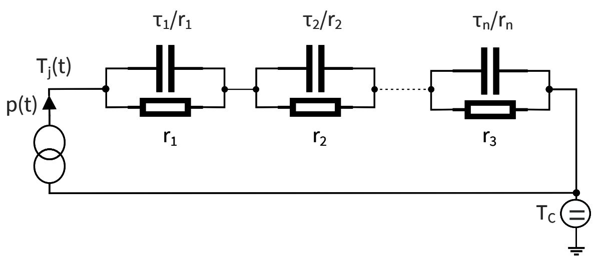


Figure E. **Thermal equivalent circuit**

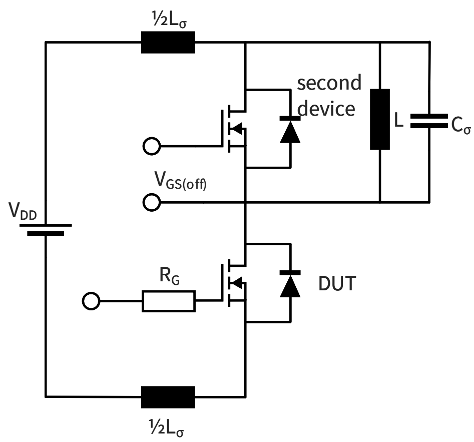


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2022-04-19	Target datasheet
0.20	2023-07-31	Preliminary datasheet
0.30	2023-08-03	Parameter change from IDCC to IDDC (p.1) Correction of inductance unit (p. 3) Correction of diagram template E(Id)
1.00	2023-11-29	Final datasheet

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