

## BUFFER GATE DRIVER INTEGRATED CIRCUIT

### Features

- High peak output current
- Negative turn-off bias
- Separate Ron / Roff resistors
- Low supply current
- Under-voltage lockout
- Full time ON capability
- Low propagation delay time
- Gate clamping when no supply
- Automotive qualified

### Applications

- High power inverters
- EV/HEV power trains

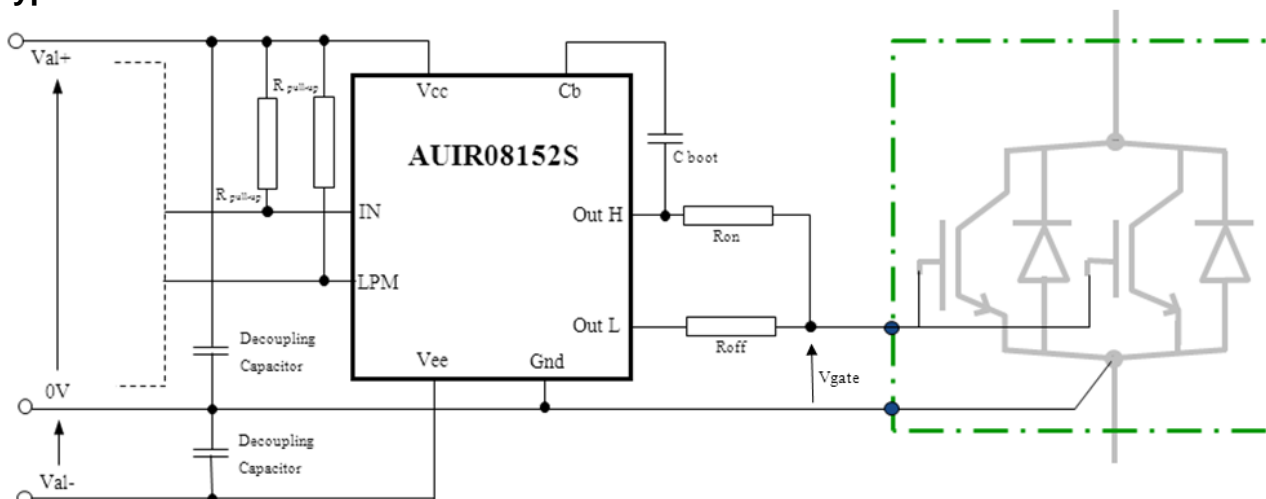
### Description

The AUIR08152 buffer brings high power gate drive capability to all pre-driver stages. It is the output extension of the wide I.R gate driver families. It features a negative Gate bias for applications requiring high levels of dv/dt immunity, a low power consumption mode as well as the full time ON gate drive ability. Shoot-through prevention is extended even when the AUIR08152S supplies are absent by mean of a Gate to Emitter self-clamping impedance.

### Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIR08152S	SOIC8	Tube	95	AUIR08152S
		Tape and reel	2500	AUIR08152STR

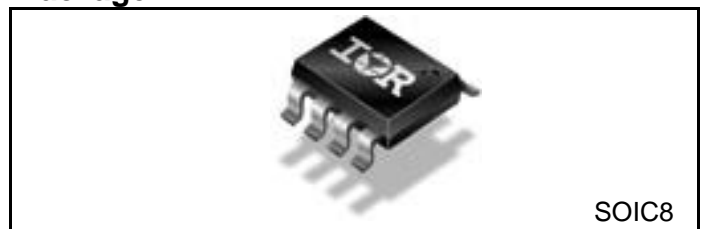
### Typical Connection



### Product Summary

Outputs Current:	+/- 10A
Operating Voltage:	13V to 25V
Negative Gate Bias:	0 to -10V

### Package



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which permanent damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured mounted on board in free air condition.

Symbol	Definition	Min	Max	Units
V <sub>CC-Gnd</sub>	V <sub>CC</sub> to Gnd maximum voltage	-0.3	+37	V
V <sub>CC-Vee</sub>	V <sub>CC</sub> to V <sub>ee</sub> maximum voltage	-0.3	+37	
V <sub>CC-VIN</sub>	V <sub>CC</sub> to V <sub>in</sub> maximum voltage	-0.3	+37	
V <sub>CC-V<sub>LPM</sub></sub>	V <sub>CC</sub> to V <sub>LPM</sub> maximum voltage	-0.3	+37	
V <sub>CB</sub>	CB to OUTH max voltage	-0.3	+5.5	mA
I <sub>LPM</sub>	LPM pin maximum current	-10	+10	
I <sub>in</sub>	IN pin maximum current	-10	+10	V
V <sub>OUTH</sub>	OUTH pin maximum voltage, DC operation	V <sub>CC</sub> - 37	V <sub>CC</sub> + 0.3	
V <sub>OUTL</sub>	OUTL pin maximum voltage, DC operation	V <sub>EE</sub> - 0.2	V <sub>CC</sub> + 0.3	A
I <sub>OUTH</sub>	Maximum input transient current to OUTH pin (t < 1us, Ron = 2Ω)	---	2	
I <sub>OUTL</sub>	Maximum output transient current from OUTL pin (t < 1us, Roff = 2Ω)	---	1.5	W
PD	Package power dissipation @ T <sub>A</sub> ≤ 25 °C	—	1	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	80	K/W
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The recommended conditions represent the AUIR08152 optimum performances for the typical application

Symbol	Definition	Min.	Max.	Units
V <sub>CC-GND</sub>	Gate driver positive supply voltage	15	25	V
GND-VEE	Recommended negative gate bias	0	-10	
V <sub>CC-VEE</sub>	Total supply voltage	15	35	
V <sub>OUTH</sub>	OUTH Output voltage	V <sub>CC</sub> - 35	V <sub>CC</sub>	
V <sub>IN,lpn</sub>	IN and LPM pins voltage range	V <sub>CC</sub> -35	V <sub>CC</sub>	
C <sub>boot</sub>	Recommended bootstrap ceramic capacitor	10	47	nF
C <sub>load</sub>	Maximum recommended equivalent gate capacitor	—	240	
C <sub>dec</sub>	Recommended V <sub>CC</sub> & V <sub>ee</sub> decoupling capacitors*	22	33	μF
R <sub>on</sub>	OUTH series resistor to gate	1.5	20	Ω
R <sub>off</sub>	OUTL series resistor to gate	1.5	20	
R <sub>pull-up</sub>	Recommended pull-up resistor for IN and LPM pins	10	100	kΩ
P <sub>Woff</sub>	Minimum recommended OFF time on the IN pin	1	—	μs
P <sub>Won</sub>	Minimum recommended ON time on the IN pin	1	—	

\* Due to the high current application a good quality low ESR capacitor has to be used. Numbers are indicative, a value about 40 times the load capacitance seen at the OutH and OutL pins is suggested.

## Static Electrical Characteristics

$V_{CC} - Gnd = 15V$ ,  $V_{EE} - Gnd = -5V$ ,  $C_{boot} = 15nF$ ,  $R_{on} = R_{off} = 3\Omega$ ,  $-40\text{ }^{\circ}C < T_A < 125\text{ }^{\circ}C$  unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$V_{CCUV+}$	$V_{CC}$ -GND under-voltage rising edge	—	11.7	12.8	V	LPM = X, IN = $V_{CC}$ , $V_{EE} = Gnd$ ;
$V_{CCUV-}$	$V_{CC}$ -GND under-voltage falling edge	9.6	10.5	—		
$V_{CCUVH}$	$V_{CC}$ -GND under-voltage hysteresis	0.5	1.2	—		
$V_{CBUV} (*)$	VCB under-voltage lockout	2.8	4	5.7		
$I_{QGG}$	Current out of the Gnd pin	—	20	60	$\mu A$	IN = X, LPM = X
$I_{QOUTL1}$	Current flowing into the OUTL pin	—	0	1.5		IN = $V_{CC}$ , LPM = X, OUTH = NC, $V_{OUTL-Gnd} = 15V$
$I_{QEESW}$	$V_{EE}$ pin current, IN cycling	—	3	8	mA	IN = 10kHz - 50% duty cycle LPM = $V_{CC}$ , $C_{LOAD} = 0nF$
$I_{QEE0}$	$V_{EE}$ pin current – output OFF – normal mode	—	1.5	4		IN = Gnd, LPM = $V_{CC}$
$I_{QEE1}$	$V_{EE}$ pin current – output ON – normal mode	—	0.8	1.6		IN = $V_{CC}$ , LPM = $V_{CC}$
$I_{QEELQ0}$	$V_{EE}$ pin current – output OFF – low power mode	—	0.6	2.0		IN = Gnd, LPM = Gnd
$I_{QEELQ1}$	$V_{EE}$ pin current – output ON – low power mode	—	0.8	1.6		IN = $V_{CC}$ , LPM = Gnd
$I_{QEEUV}$	$V_{EE}$ pin current at low $V_{CC}$ supply	—	0.6	1.6		IN = X, LPM = X, $V_{CC} < V_{CCUV-}$
$I_{QB}$	CB pin sink current	—	0.5	1		IN = $V_{CC}$ , LPM = $V_{CC}$ , $V_{CB-VOUTH} = 5.5V$
$I_{QOUTH0}$	OUTH pin sourced current – normal mode	—	1	3.5		IN = Gnd, LPM = $V_{CC}$ OUTH = $V_{EE}$ , OUTL = NC
$I_{QOUTH0LQ}$	OUTH pin sourced current – low power mode	—	0.2	0.5		IN = Gnd, LPM = Gnd OUTH = $V_{EE}$ , OUTL = NC
$I_{BOUTH}$	CB pin sourced current – normal mode	30	90	—		IN = Gnd, LPM = $V_{CC}$ , OUTL = NC, CB = OUTH = $V_{EE}$
$I_{BOUTH\_pl}$	CB pin pulsed sourced current – normal mode	90	200	—		Min pulse length 2us guaranteed by design
$I_{BOUTH\_LQ}$	CB pin sourced current – low power mode	0.5	5	23		IN = Gnd, LPM = Gnd, OUTL = NC, CB = OUTH = $V_{EE}$
$I_{OUTH+} / I_{OUTL-}$	OUTH /OUTL pins output current capability	10	—	—		A LPM = X $V_{OUTL-}$ : $t < 100us$ , $V_{OUTH+}$ : CB charged
$V_{CC-VinH}$	IN pin – output ON voltage	1.5	2.5	—		V
$V_{CC-VinL}$	IN pin – output OFF voltage	—	4.5	5.5		
$V_{INhys}$	IN pin voltage hysteresis	1	2	—		
$V_{CC-VLPMH}$	LPM pin normal mode voltage	1.4	2	—		
$V_{CC-VLPML}$	LPM pin low power mode voltage	—	3.2	3.8		
$V_{LPMhys}$	LPM pin voltage hysteresis	0.3	1.1	—		
$I_{IN15}$	IN pin sourced current	40	90	180	$\mu A$	IN = Gnd
$I_{LPM15}$	LPM pin sourced current	10	25	50		LPM = Gnd
$R_{dson\ OUTH}$	OUTH transistor $R_{dson}$	—	100	200	m $\Omega$	IN = $V_{CC}$ , $I_{out} = 10A$ , $t < 100us$ , Gnd = $V_{EE}$ , $V_{CB} = V_{OUTH} + 5.5V$
$R_{dson\ OUTL}$	OUTL transistor $R_{dson}$	—	200	400		-IN = Gnd, $I_{out} = 10A$ , $t < 100us$ , Gnd = $V_{EE}$
$I_{PMOS} (*)$	OUTH Pulling- up current source	15	30	120	mA	IN = $V_{CC}$ , LPM = X, $V_{CC} - V_{OUTH} = 1.5V$

(\*)When  $V_{CB} - V_{OUTH} < V_{CBUV}$ , OUTH pin remaining pulled-up to  $V_{CC}$  is guaranteed for at least 3usec with low impedance (=Ron) via VDmos then continuously with higher impedance via PMos (=Ipmos, see block diagram).

## Switching Electrical Characteristics

$V_{CC} - Gnd = 15V$ ,  $V_{EE} - Gnd = -9V$ ,  $C_{boot} = 15nF$ ,  $R_{on} = R_{off} = 3\Omega$ ,  $C_{LOAD} = 220nF$ ,  $-40\text{ }^\circ\text{C} < T_A < 125\text{ }^\circ\text{C}$  unless otherwise specified.

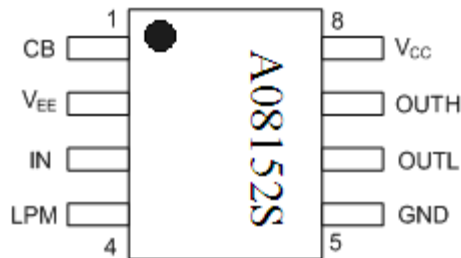
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
$t_{on}$	OUTH turn on propagation delay	—	150	350	ns	See parameters definitions LPM = X	
$t_{off}$	OUTL turn off propagation delay	—	230	350			
$t_{off\_VCBuv}$	OUTL turn off prop. delay when $V_{CB} < V_{CBuv}$ *	—	90	350			
$t_r$	OUTH rise time	—	50	150			
$t_f$	OUTL fall time	—	50	150			
$t_{rLQ}$	OUTH rise time (IN=1, $V_{CC}$ ramping up, LPM = Gnd)	—	50	250			$V_{EE} = LPM = Gnd$ , IN = $V_{CC}$
$t_{fLQ}$	OUTL fall time (IN=1, $V_{CC}$ ramping down, LPM = Gnd)	—	50	250			$V_{EE} = LPM = Gnd$ , IN = $V_{CC}$
Min Out-ON	ON time for 0.5 $\mu$ s IN pulse	200	600	900			Clod = open
Min Out-OFF cb discharged	OFF time for 0.5 $\mu$ s IN pulse, CB discharged	200	500	900			Clod = open, CB = 15 nF
Min Out-OFF cb charged	OFF time for 0.5 $\mu$ s IN pulse, CB charged	200	400	900	Clod = open, CB = 15 nF		
$t_{onLPM}$	LPM activation time (from LPM edge to $I_{cb} < I_{BOUTh/2}$ )	—	0.6	3	$\mu$ s	by design	
$t_{offLPM}$	LPM deactivation time (from LPM edge to $I_{cb} > I_{BOUTh/2}$ )	—	0.6	3			

\* See also Fig. 5

## Truth Table

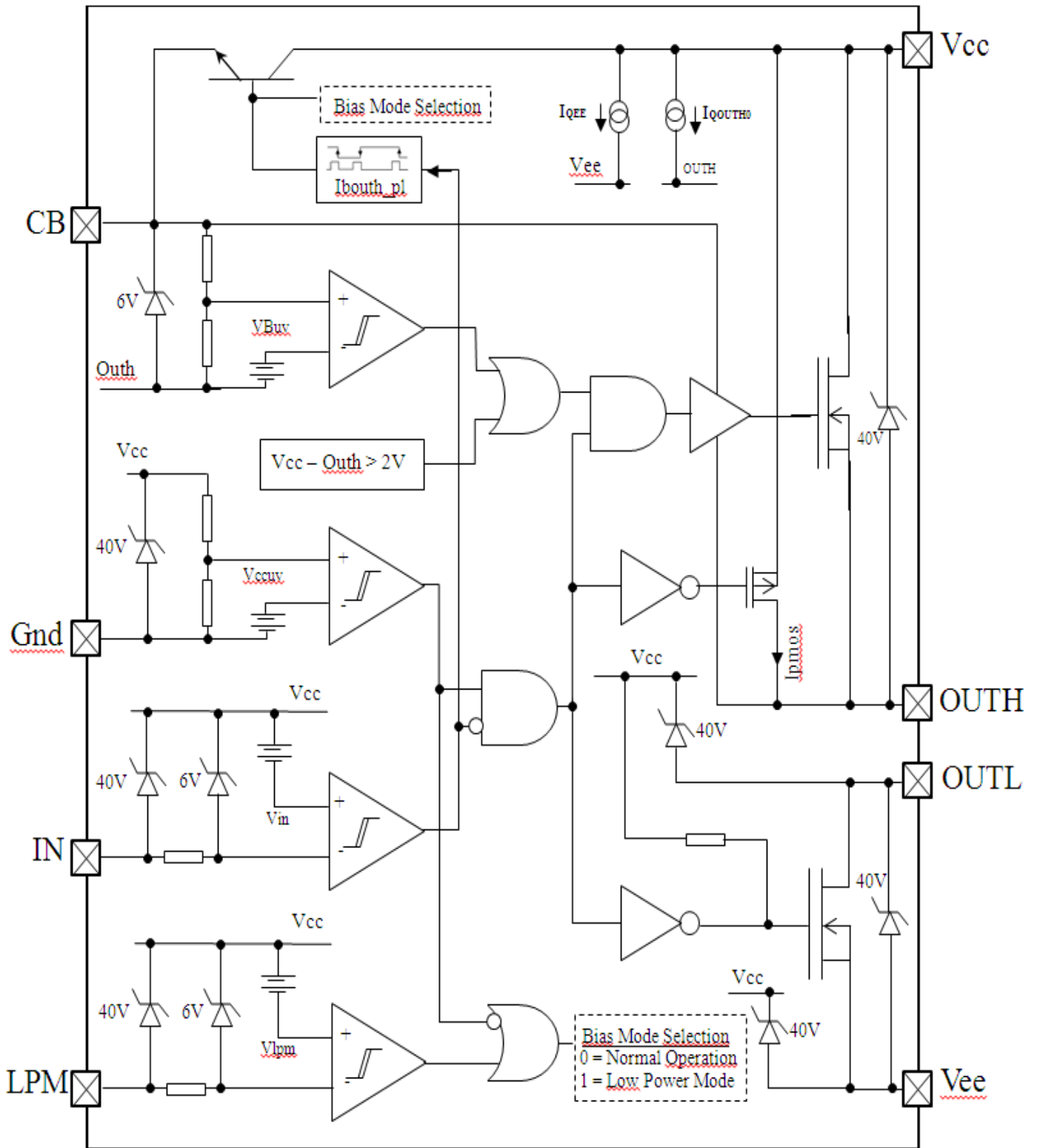
IN	LPM	VCC	OUTH	OUTL	Status
X	X	< $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Gnd	> $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Low power mode
Gnd	Vcc	> $V_{CCuv}$	Open	Vee	IGBT or MOSFET = OFF – Normal mode
Vcc	Gnd	> $V_{CCuv}$	Vcc	Open	IGBT or MOSFET = ON – Low power mode
Vcc	Vcc	> $V_{CCuv}$	Vcc	Open	IGBT or MOSFET = ON – Normal mode

## Lead Assignments

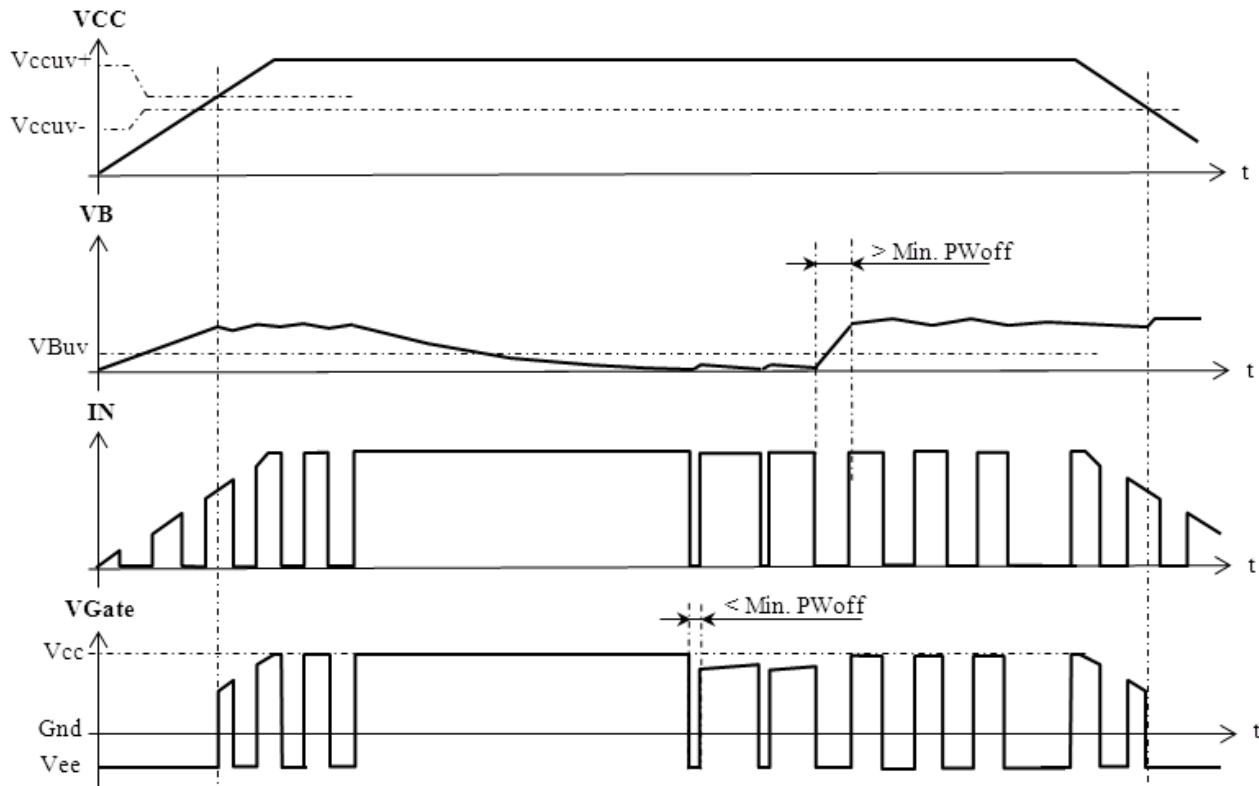


## Lead Definitions

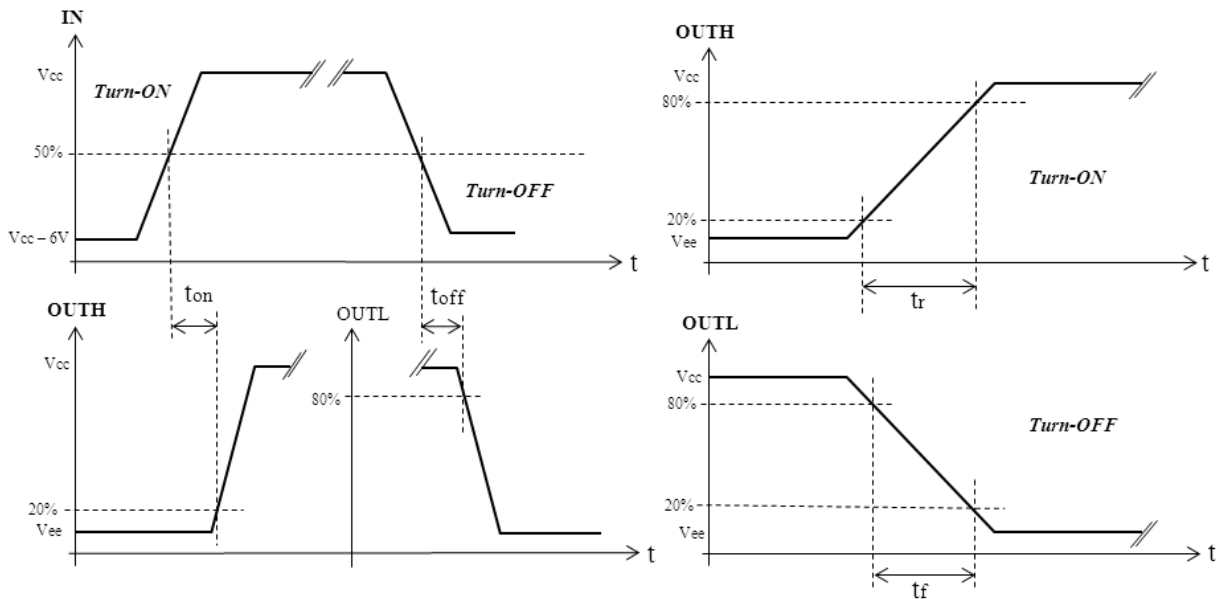
Symbol	Description	Pin
CB	External Bootstrap capacitor (cf. typical connection schematic)	1
Vee	Negative Supply Pin	2
IN	Gate Drive Input, (IN= $V_{CC}$ forces OutH = high)	3
LPM	Low Power Mode Input, LPM= GND activates the Low Power Mode	4
GND	0V – IGBT Emitter or MOSFET Source Connection (cf. typical connection schematic)	5
OUTL	Gate Drive Output Pull down	6
OUTH	Gate Drive Output Pull up	7
Vcc	Positive Supply Pin	8

**Functional Block Diagram**


### Timing Diagram



### Parameters Definitions

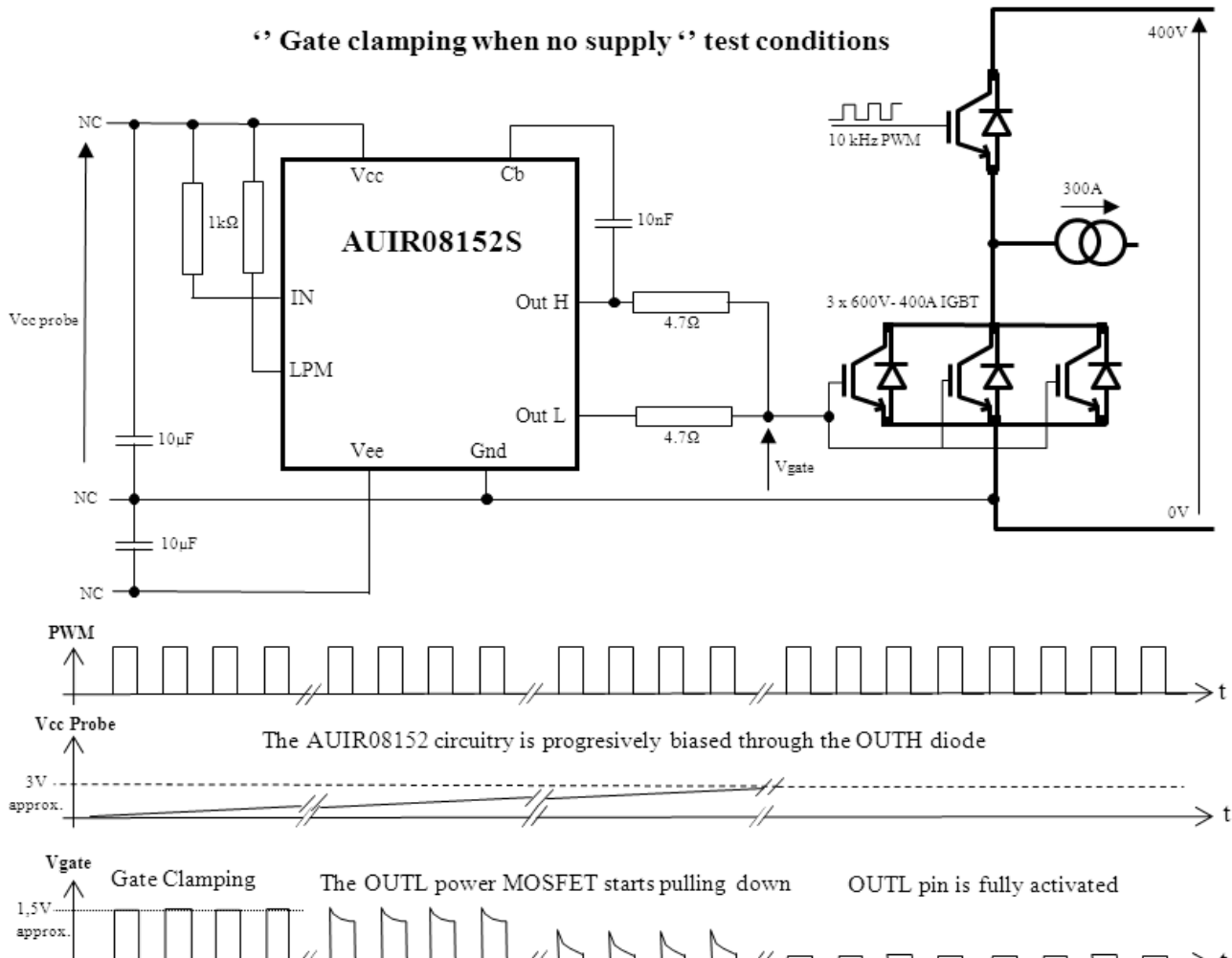


Propagation delay definitions

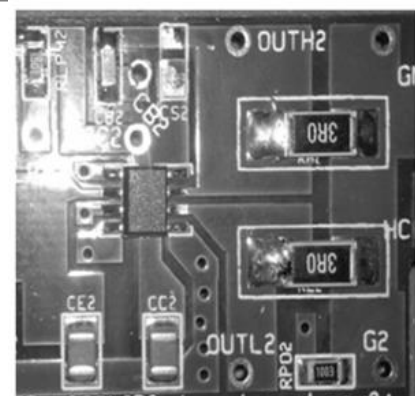
Rise and fall time definitions

## Application Tips

The AUIR08152S features a self-clamping gate protection in case of the auxiliary power supply disappears. A resistor is pulling up the gate of the OUTL internal power MOSFET to keep OutL pulled down until a minimum Vcc is applied, when Vcc disappears (< about 3V) then the Vgate is clamped via the OUTH ESD diode. In this situation forcing OutL high injects current into the pin that charges the Vcc decoupling capacitor and reactivates the internal OUTL output power MOSFET (for more info see the Functional Block Diagram).



- If no negative bias is used, Vee shall be connected to Gnd
- OUTH and OUTL pins shall never be shorted together
- Decoupling capacitors shall be ceramic types and implemented as close as possible of the AUIR08152S supply pins
- The decoupling capacitors shall be at least 40 times bigger than the max. Cloud and of low ESR type, in order to avoid any Vccuv oscillations
- IN and LPM pins shall never be left open



PCB Layout Example

## Parameters

Figures are given for typical value @  $T_j=25^\circ\text{C}$  otherwise specified

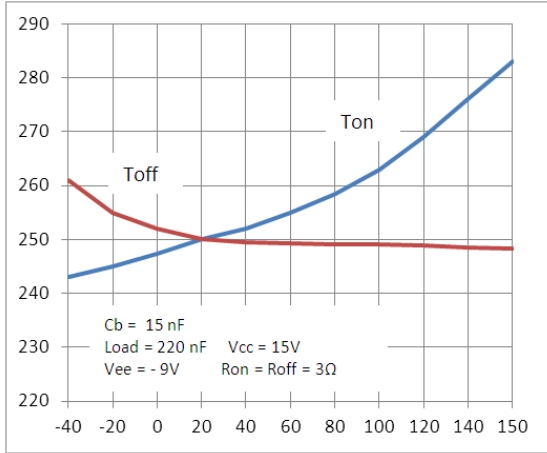


Figure 1: Ton and Toff (ns) Vs Temperature ( $^\circ\text{C}$ )

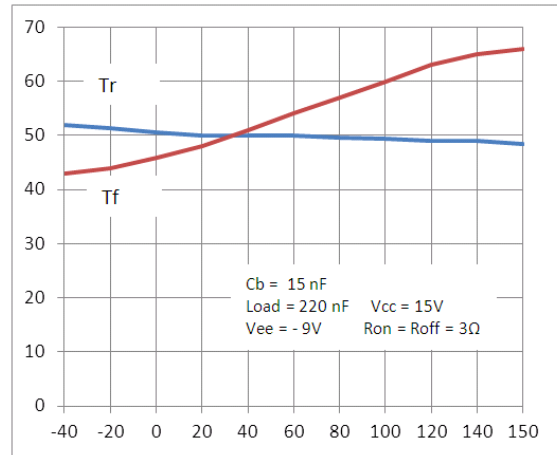


Figure 2: Tr and Tf (ns) Vs Temperature ( $^\circ\text{C}$ )

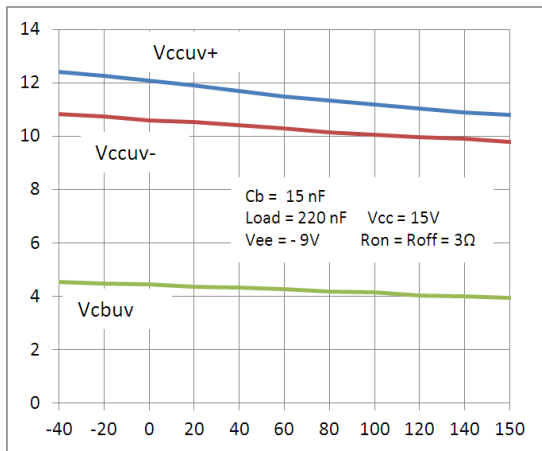


Figure 3: Vccuv+, Vccuv- and Vcbuv (V) Vs Temperature ( $^\circ\text{C}$ )

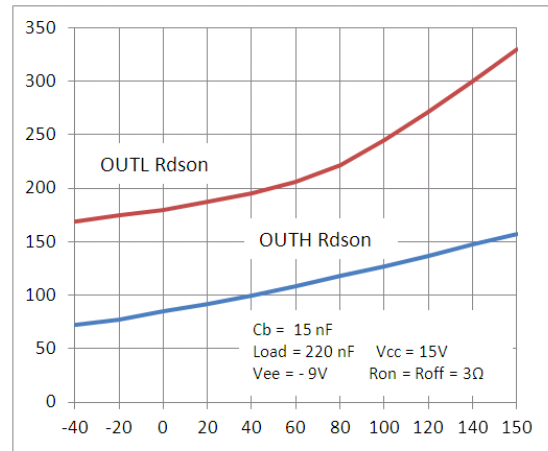


Figure 4: OUTH & OUTL Rdson's Vs Temperature ( $^\circ\text{C}$ )

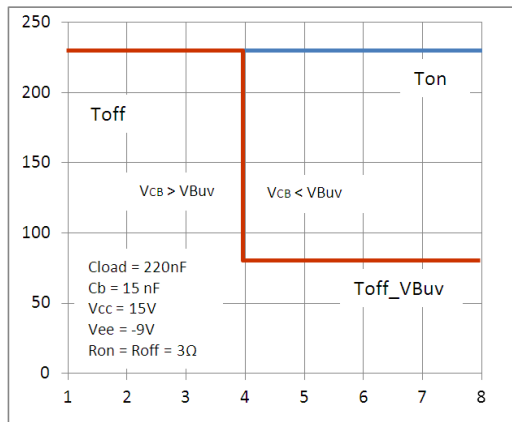


Figure 5: Ton, Toff (ns) Vs IN pulse duration ( $\mu\text{s}$ )

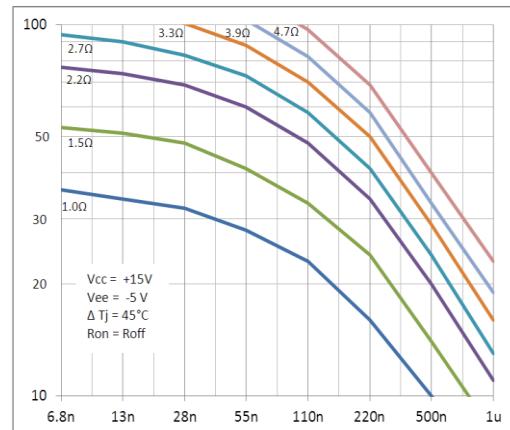
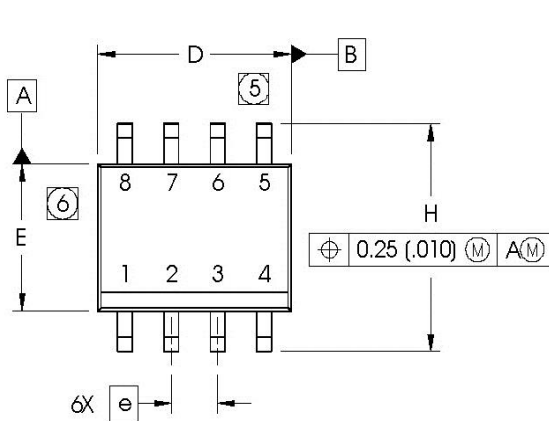


Figure 6: Max PWM Frequency (kHz) Vs Gate Capacitance (F) & Rg ( $\Omega$ )

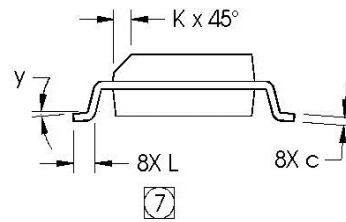
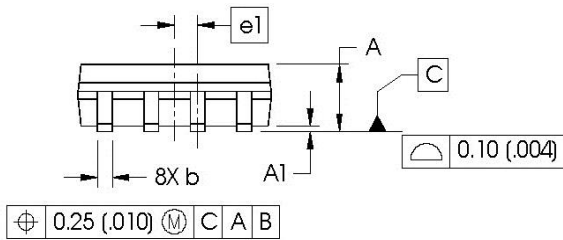


**Case Outline – S08**

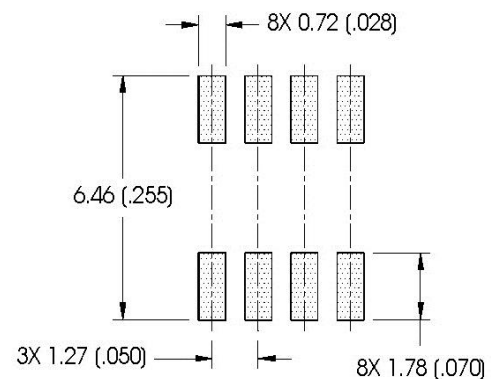
Dimensions are shown in millimeters (inches)

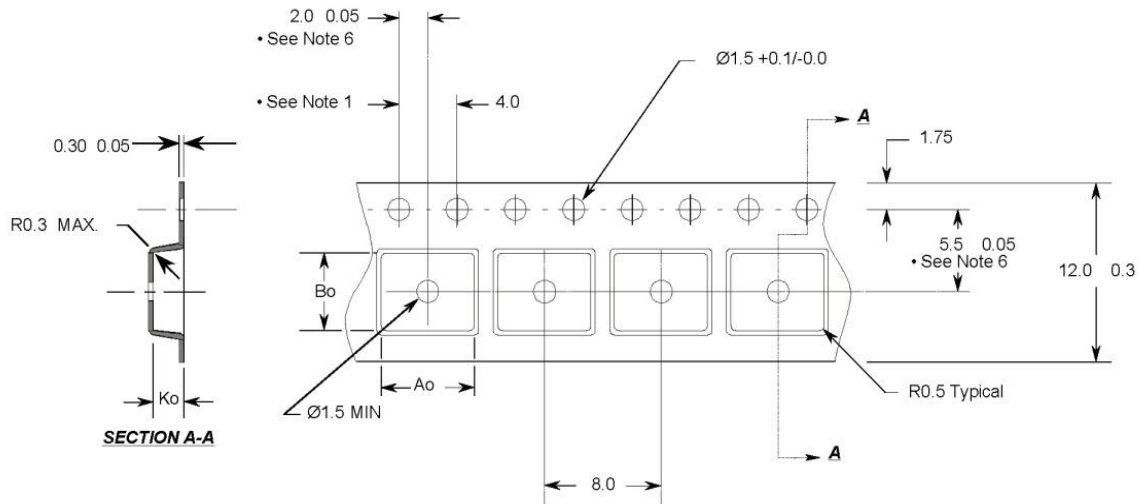


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUT LINE CONFORMS TO JEDEC OUT LINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROT RUSIONS. MOLD PROT RUSIONS NOT TO EXCEED 0.15 (.006).
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROT RUSIONS. MOLD PROT RUSIONS NOT TO EXCEED 0.25 (.010).
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

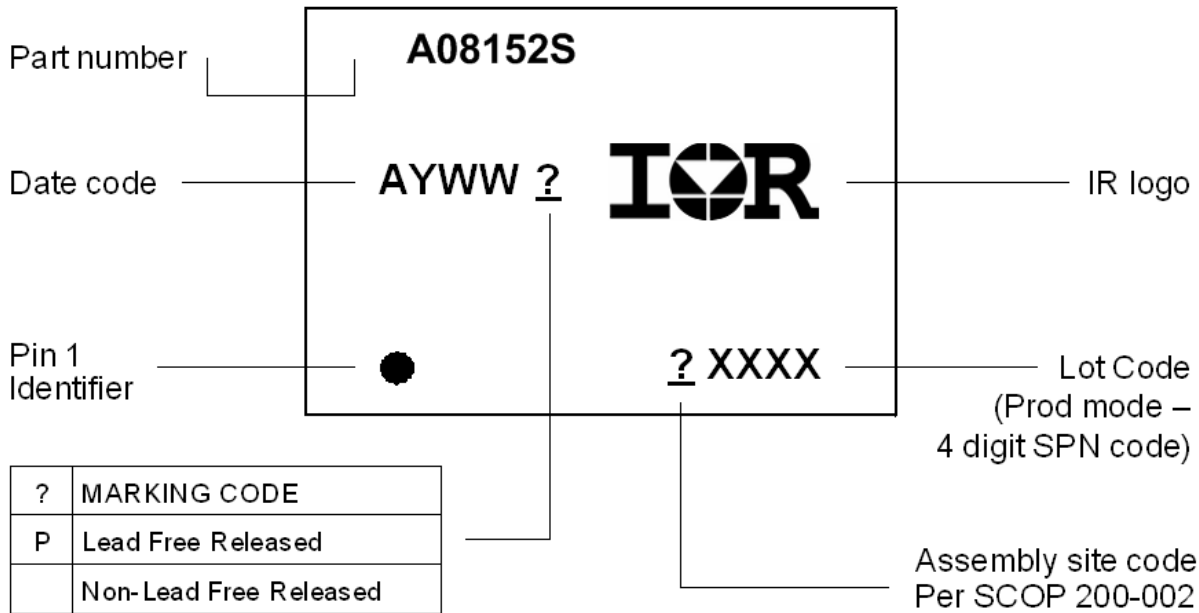
**FOOTPRINT**


**Tape & Reel S08**

**Notes:**

1. 10 sprocket hole pitch cumulative tolerance 0.2
2. Camber not to exceed 1mm in 100mm
3. Material: Black Conductive Advantek Polystyrene
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

**Ao = 6.4 mm**  
**Bo = 5.2 mm**  
**Ko = 2.1 mm**

- All Dimensions in Millimeters -

**Part Marking Information**

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Automotive (per AEC-Q100)	
	Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>	SOIC8N	MSL2 <sup>††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M2 (+/-200V) (per AEC-Q100-003)
	Human Body Model	Class H2 (+/-2500V) (per AEC-Q100-002)
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)
<b>IC Latch-Up Test</b>	Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

<sup>††</sup> Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Notes/Changes</b>
A1	August 5 <sup>th</sup> , 2013	Preliminary Datasheet AUIR08152S
A2	August 23 <sup>rd</sup> 2013	Advanced datasheet
A3	August 26 <sup>th</sup> 2013	Advanced datasheet
A4	September 2 <sup>nd</sup> 2013	Final datasheet, updated lout+ and lout- definition
A5	Dec. 5 <sup>th</sup> , 2013	Updated cosmetic for production
A6	Aug. 27 <sup>th</sup> , 2014	Updated note * on page 3, updated page footer

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