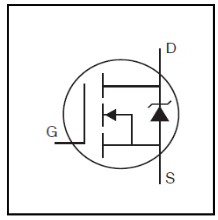
HEXFET® Power MOSFET

Application

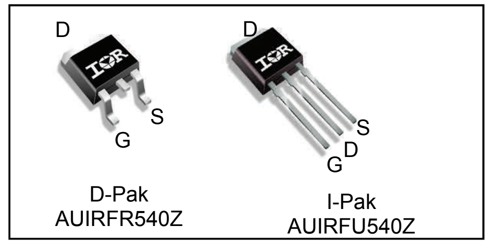
- Automatic Voltage Regulator (AVR)
- Solenoid Injection
- Body Control
- Low Power Automotive Applications



V_{DSS}		100V
$R_{DS(on)}$	typ.	22.5mΩ
	max.	28.5mΩ
I_D		35A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFU540Z	I-Pak	Tube	75	AUIRFU540Z
AUIRFR540Z	D-Pak	Tube	75	AUIRFR540Z
		Tape and Reel Left	3000	AUIRFR540ZTRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	35	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	25	
I_{DM}	Pulsed Drain Current ①	140	
P_D @T_C = 25°C	Maximum Power Dissipation	91	W
	Linear Derating Factor	0.61	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	39	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	75	
I_{AR}	Avalanche Current ①	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.64	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	——	50	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

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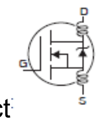
*Qualification standards can be found at www.infineon.com

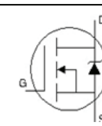
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.092	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	22.5	28.5	mΩ	V_{GS} = 10V, I_D = 21A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 50μA
gfs	Forward Trans conductance	28	——	——	S	V_{DS} = 25V, I_D = 21A ③
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 100V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	39	59	nC	I_D = 21A
Q_{gs}	Gate-to-Source Charge	——	11	——		V_{DS} = 50V
Q_{gd}	Gate-to-Drain Charge	——	12	——		V_{GS} = 10V③
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = 50V
t_r	Rise Time	——	42	——		I_D = 21A
$t_{d(off)}$	Turn-Off Delay Time	——	43	——		R_G = 13Ω
t_f	Fall Time	——	34	——		V_{GS} = 10V③
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) 
L_S	Internal Source Inductance	——	7.5	——		from package and center of die contact
C_{iss}	Input Capacitance	——	1690	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	180	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	100	——		f = 1.0MHz
C_{oss}	Output Capacitance	——	720	——		V_{GS} = 0V, V_{DS} = 1.0V f = 1.0MHz
C_{oss}	Output Capacitance	——	110	——		V_{GS} = 0V, V_{DS} = 80V f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	——	190	——		V_{GS} = 0V, V_{DS} = 0V to 80V ④

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	35	A	MOSFET symbol showing the 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	140		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 21A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	32	48	ns	T_J = 25°C ,I_F = 21A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	——	40	60	nC	di/dt = 100A/μs③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
② Limited by T_{Jmax} , starting T_J = 25°C, L = 0.17mH, R_G = 25Ω, I_{AS} = 21A, V_{GS} =10V. Part not recommended for use above this value.
③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
⑥ This value determined from sample failure population, 100% tested to this value in production.
⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
⑧ R_θ is measured at T_J approximately 90°C.

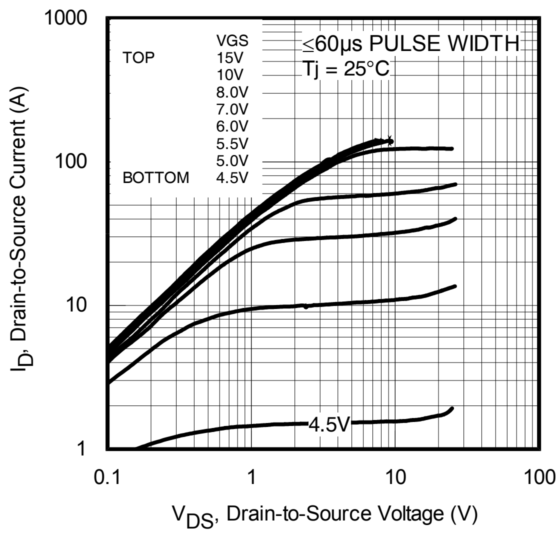


Fig. 1 Typical Output Characteristics

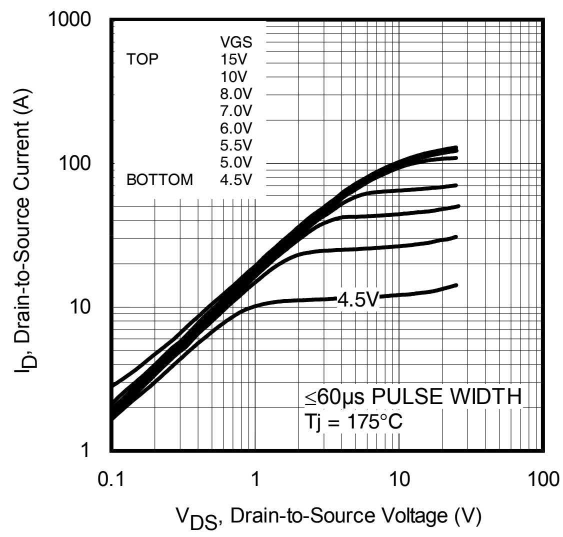


Fig. 2 Typical Output Characteristics

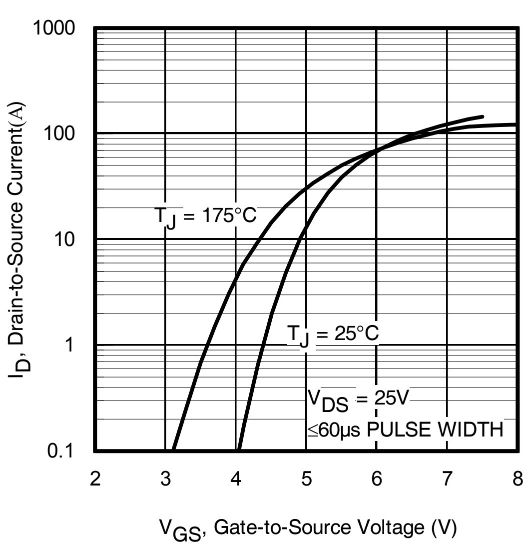


Fig. 3 Typical Transfer Characteristics

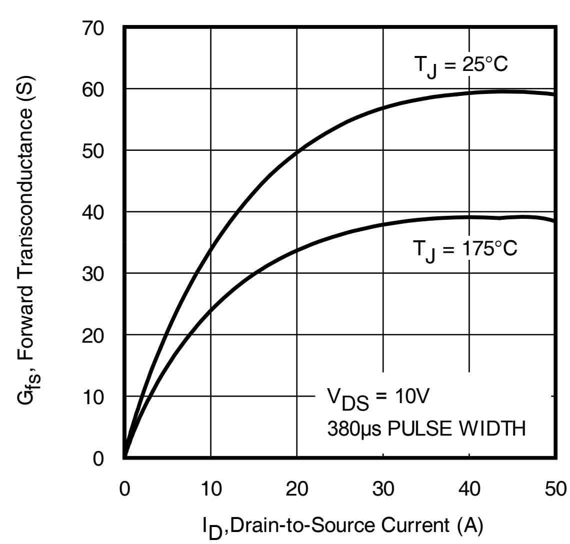
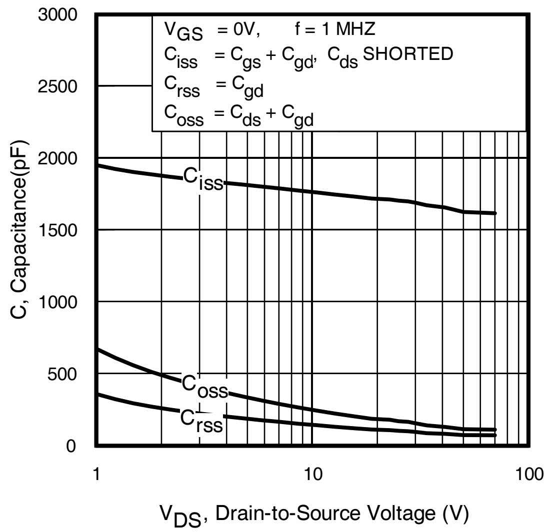


Fig. 4 Typical Forward Trans conductance Vs. Drain Current



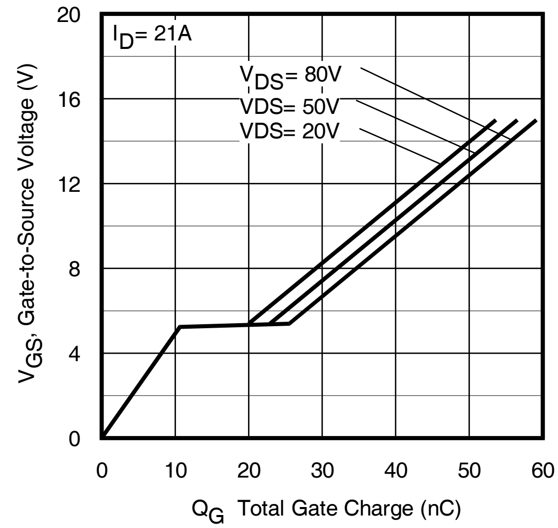
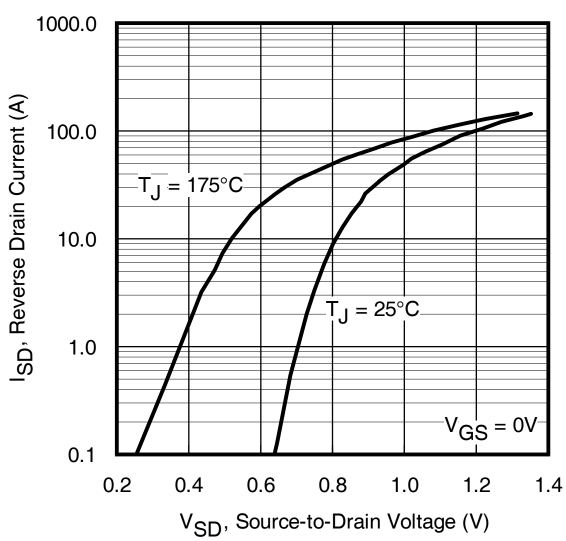


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



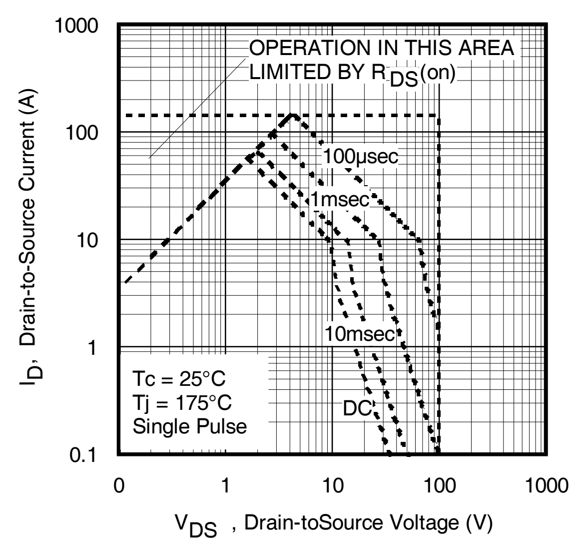


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

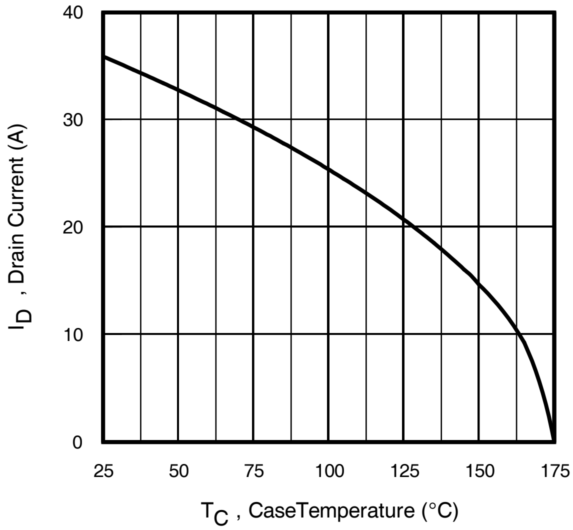


Fig 9. Maximum Drain Current Vs. Case Temperature

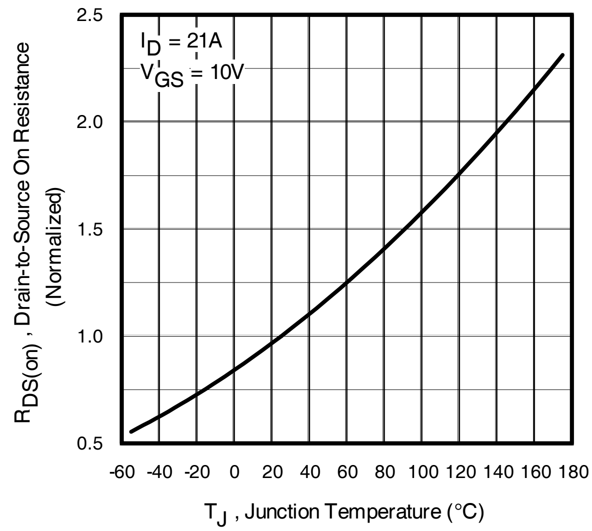
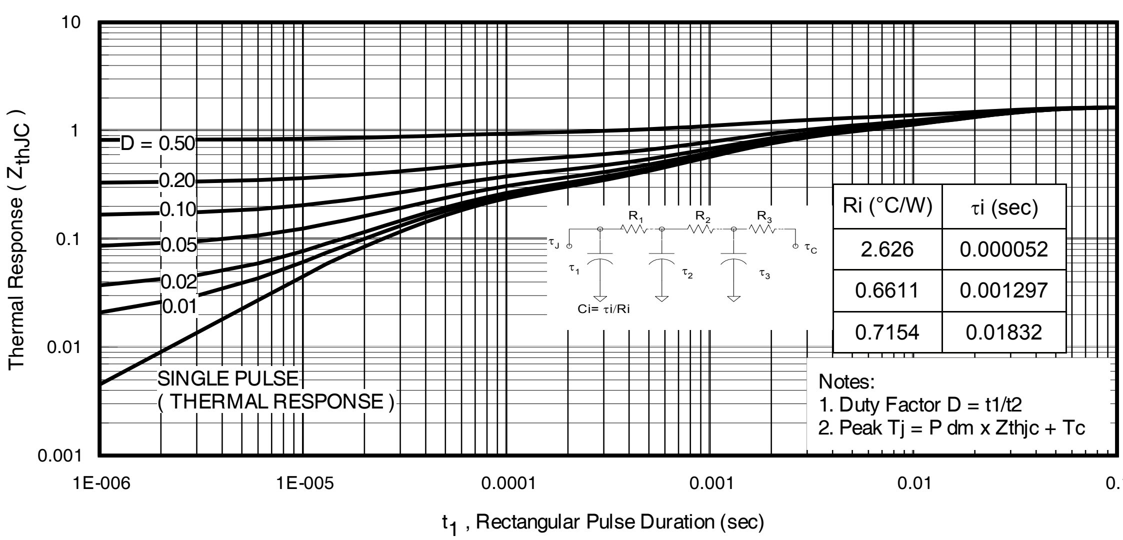


Fig 10. Normalized On-Resistance Vs. Temperature



Ri (°C/W)	τi (sec)
2.626	0.000052
0.6611	0.001297
0.7154	0.01832

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

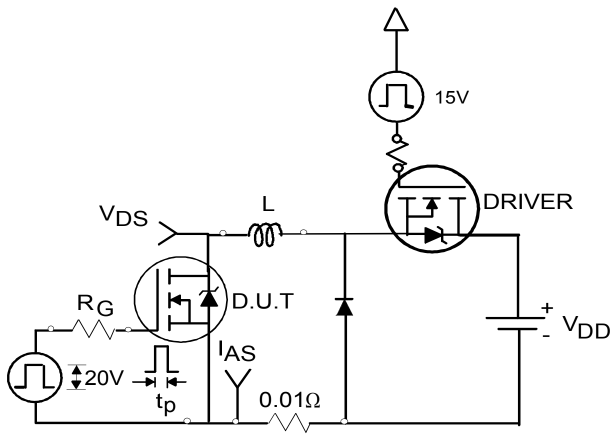


Fig 12a. Unclamped Inductive Test Circuit

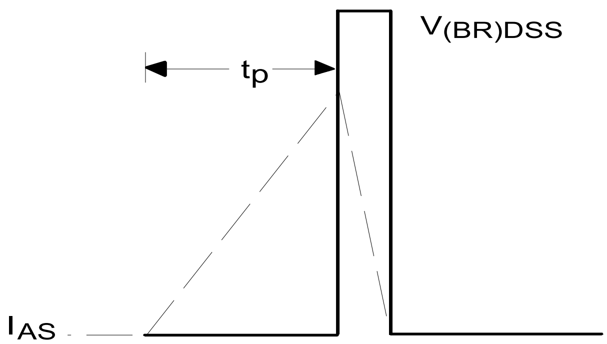


Fig 12b. Unclamped Inductive Waveforms

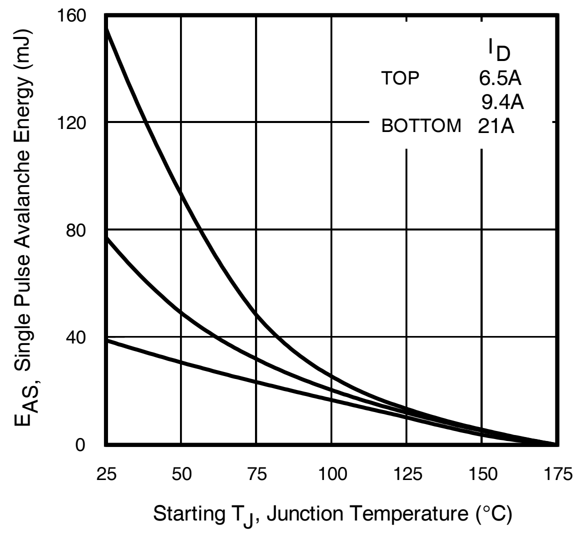


Fig 12c. Maximum Avalanche Energy vs. Drain Current

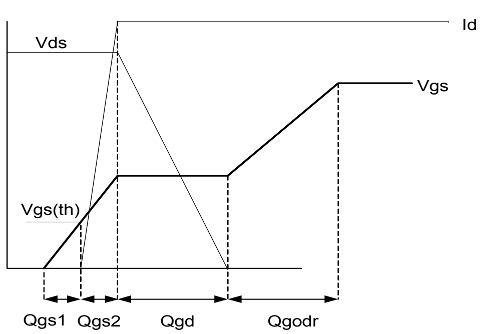


Fig 13a. Gate Charge Waveform

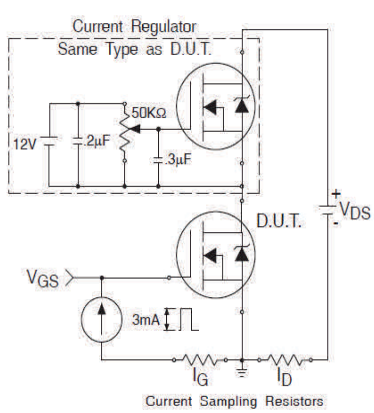


Fig 13b. Gate Charge Test Circuit

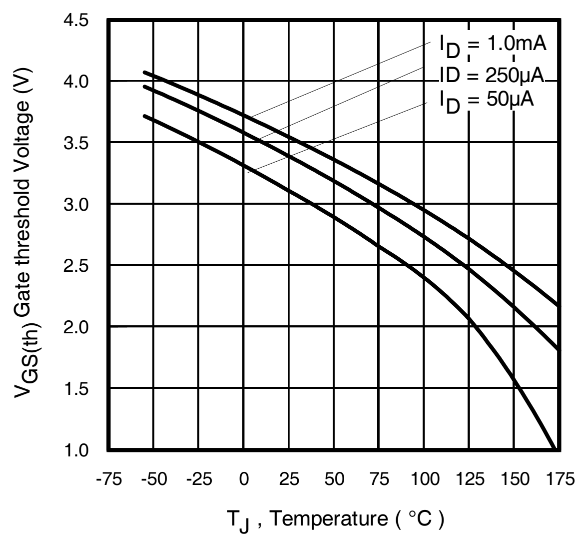


Fig 14. Threshold Voltage Vs. Temperature

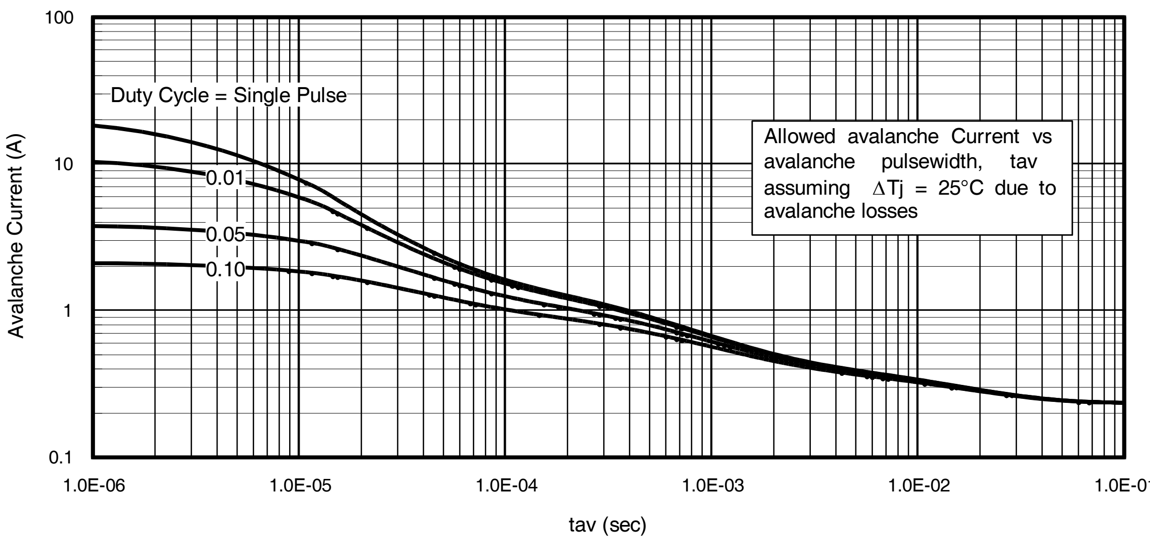


Fig 15. Typical Avalanche Current Vs. Pulse width

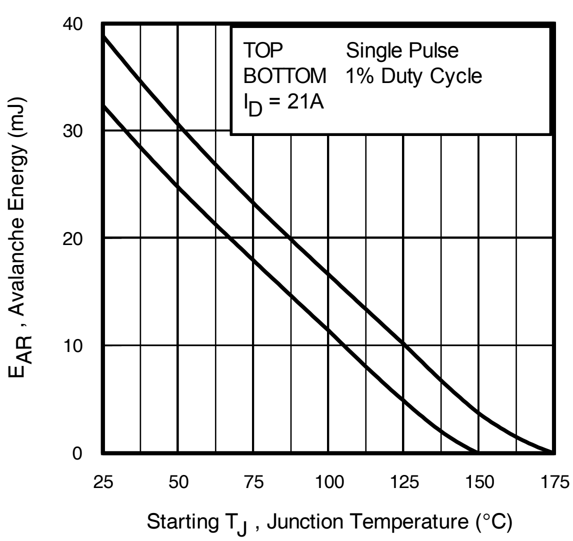


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:

(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

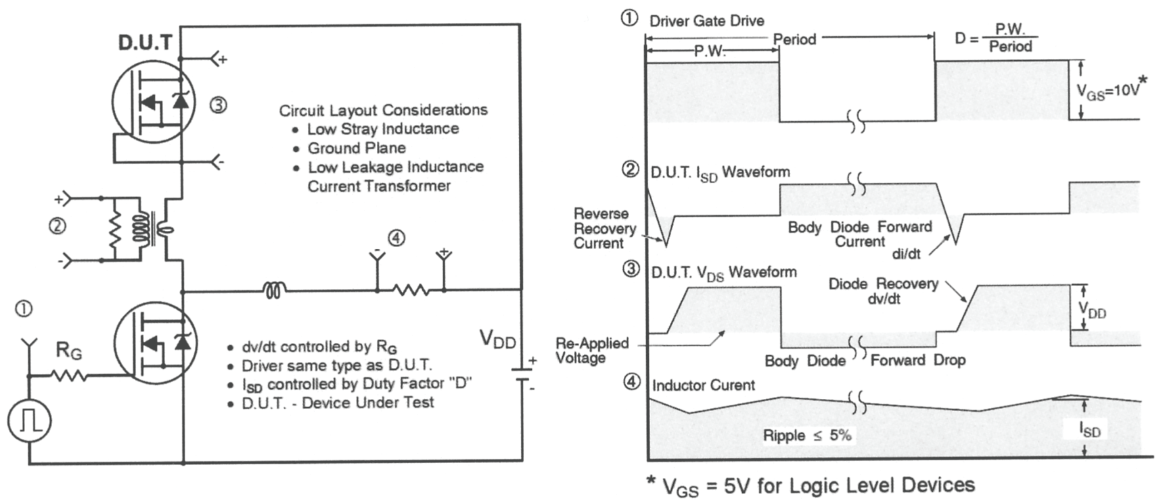


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

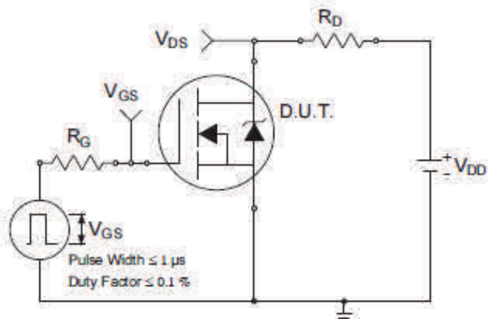


Fig 18a. Switching Time Test Circuit

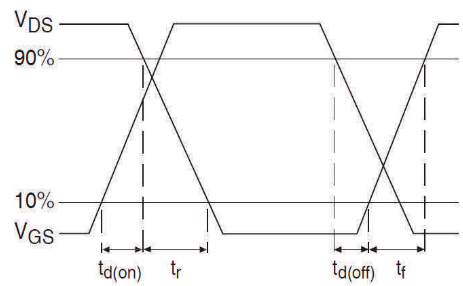
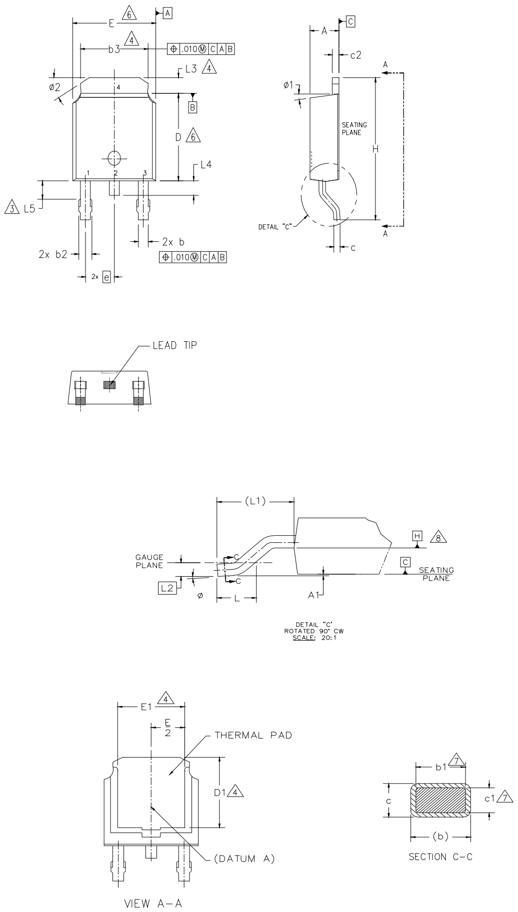


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3.– LEAD DIMENSION UNCONTROLLED IN L5.
4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

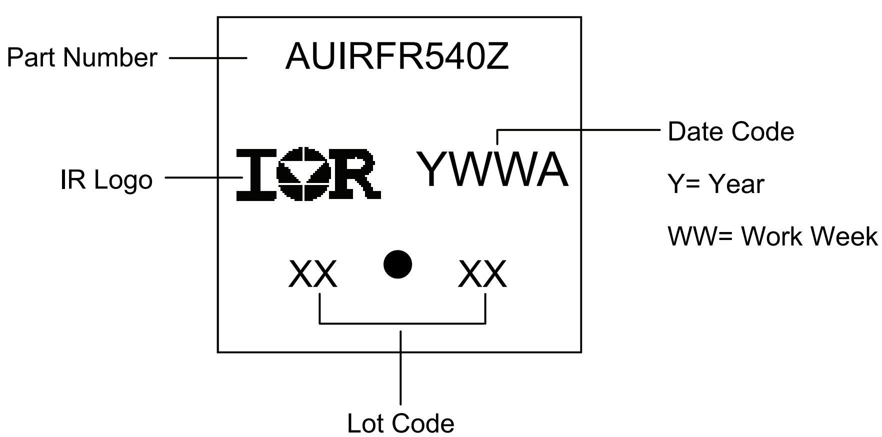
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

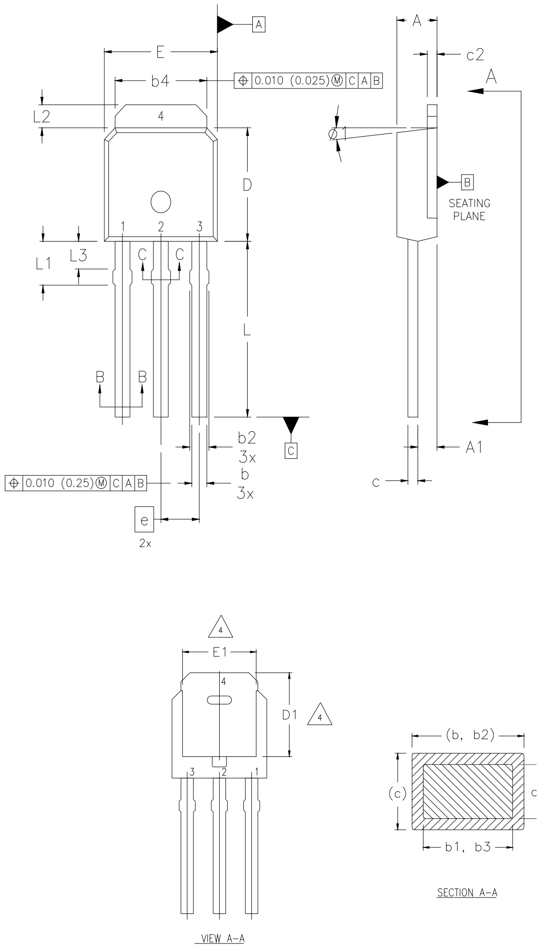
IGBT & CoPAK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) Part Marking Information



I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5 LEAD DIMENSION UNCONTROLLED IN L3.
6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8 CONTROLLING DIMENSION : INCHES.

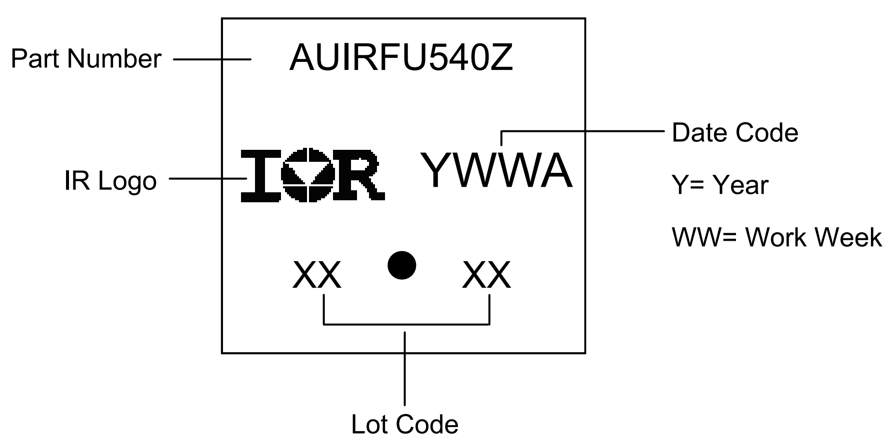
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	–	0.205	–	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	–	0.170	–	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

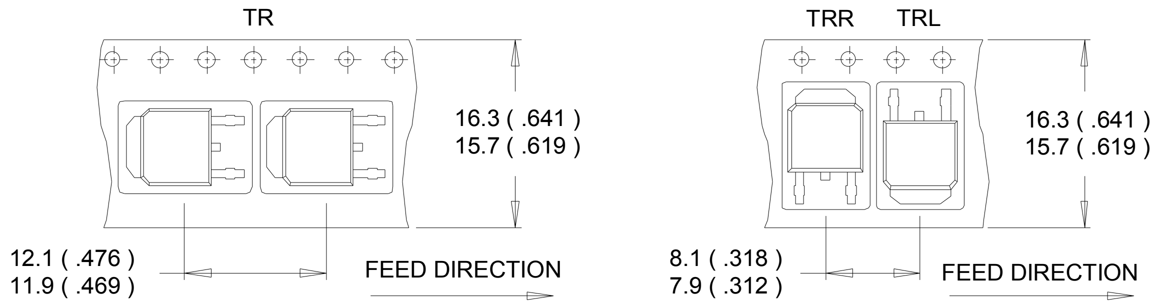
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

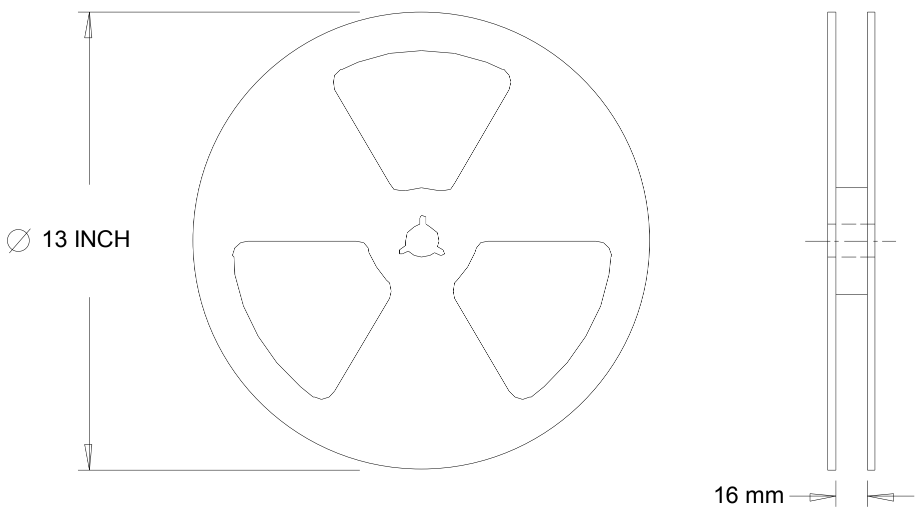
I-Pak (TO-251AA) Part Marking Information



D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-Pak	MSL1
		I-Pak	
ESD	Machine Model	Class M2 (+/-200V)† AEC-Q101-002	
	Human Body Model	Class H1B (+/-1000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/-2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
06/06/2014	• Updated part number by the pictures of the parts to AU nomenclature on page 1.
12/02/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1. • Corrected typo RthJA (PCB Mount) from “40°C/W” to “50°C/W” on page 1
10/03/2017	• Corrected typo error on package outline and part marking on page 9 and 10.

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