

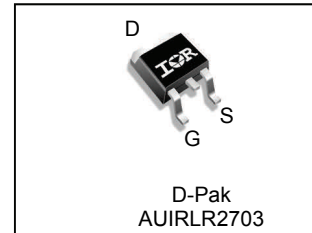
**Features**

- Advanced Planar Technology
- Logic Level Gate Drive
- Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

HEXFET® Power MOSFET



<b>V<sub>DSS</sub></b>		<b>30V</b>
<b>R<sub>DS(on)</sub></b>	<b>max.</b>	<b>45mΩ</b>
<b>I<sub>D</sub></b> (Silicon Limited)		<b>23A</b>
<b>I<sub>D</sub></b> (Package Limited)		<b>20A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLR2703	D-Pak	Tube	75	AUIRLR2703
		Tape and Reel Left	3000	AUIRLR2703TRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	23	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	16	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	20	
I <sub>DM</sub>	Pulsed Drain Current ①	96	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	45	W
	Linear Derating Factor	0.30	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 16	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	77	mJ
E <sub>AS (tested)</sub>	Single Pulse Avalanche Energy (tested Value) ⑥	200	
I <sub>AR</sub>	Avalanche Current ①	14	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	4.5	mJ
dv/dt	Peak Diode Recovery ③	5.0	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ⑧	—	3.3	°C/W
R <sub>θJA</sub>	Junction-to-Ambient ( PCB Mount) ②	—	50	
R <sub>θJA</sub>	Junction-to-Ambient	—	110	

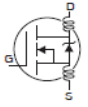
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\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

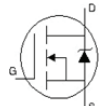
**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.030	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.045	$\Omega$	$V_{GS} = 10V, I_D = 14A$ ④
		—	—	0.065		$V_{GS} = 4.5V, I_D = 12A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Trans conductance	6.4	—	—	S	$V_{DS} = 25V, I_D = 14A$ ⑦
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$

**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

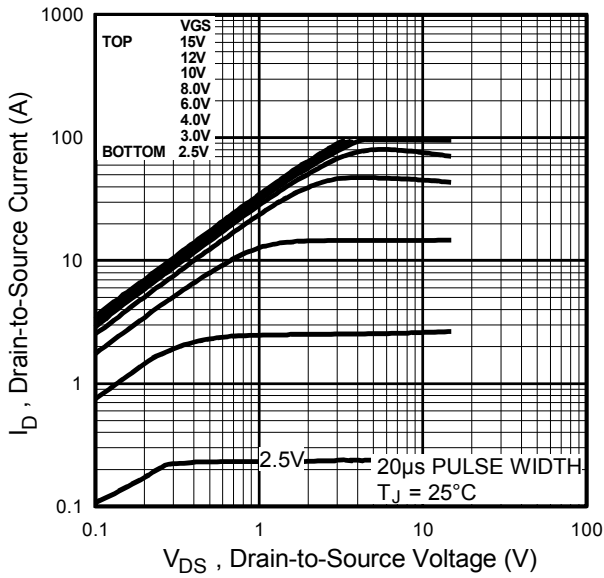
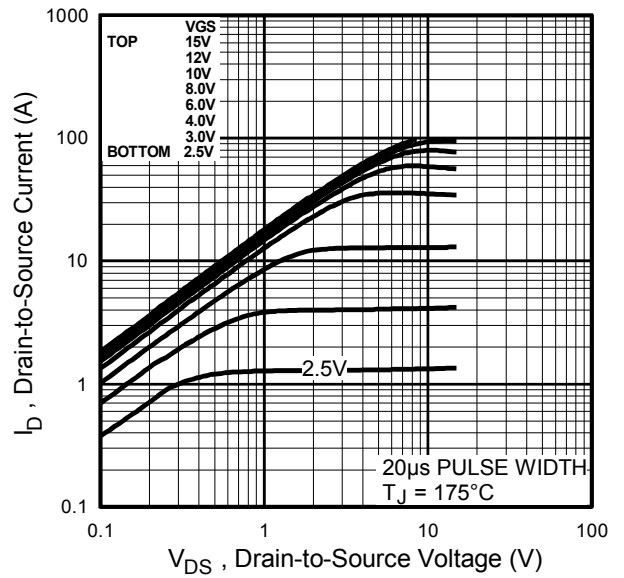
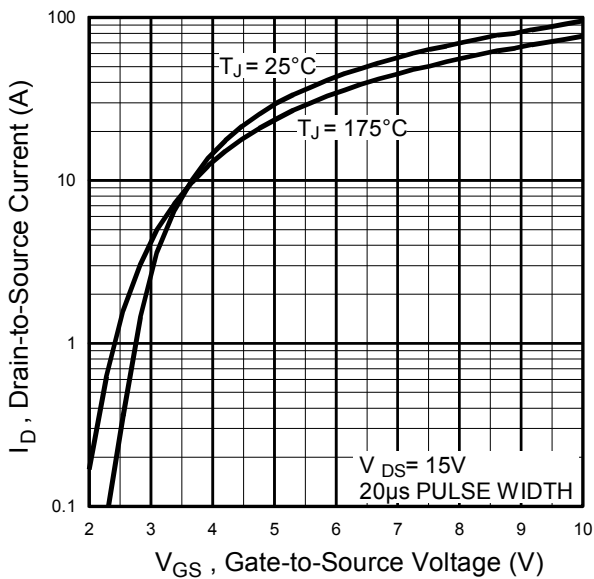
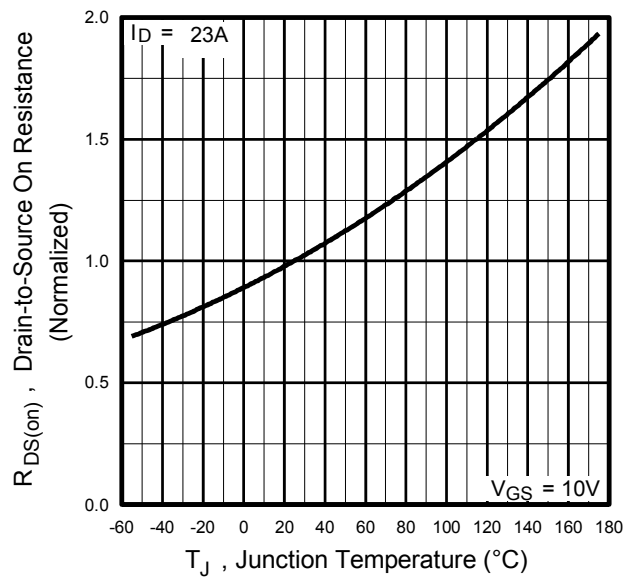
$Q_g$	Total Gate Charge	—	—	15	nC	$I_D = 14A$ $V_{DS} = 24V$ $V_{GS} = 4.5V$ ④⑦
$Q_{gs}$	Gate-to-Source Charge	—	—	4.6		
$Q_{gd}$	Gate-to-Drain Charge	—	—	9.3		
$t_{d(on)}$	Turn-On Delay Time	—	8.5	—	ns	$V_{DD} = 15V$ $I_D = 14A$ $R_G = 12\Omega, V_{GS} = 4.5V$ $R_D = 1.1\Omega$ ④⑦
$t_r$	Rise Time	—	140	—		
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		
$t_f$	Fall Time	—	20	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	450	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ ⑦
$C_{oss}$	Output Capacitance	—	210	—		
$C_{rss}$	Reverse Transfer Capacitance	—	110	—		

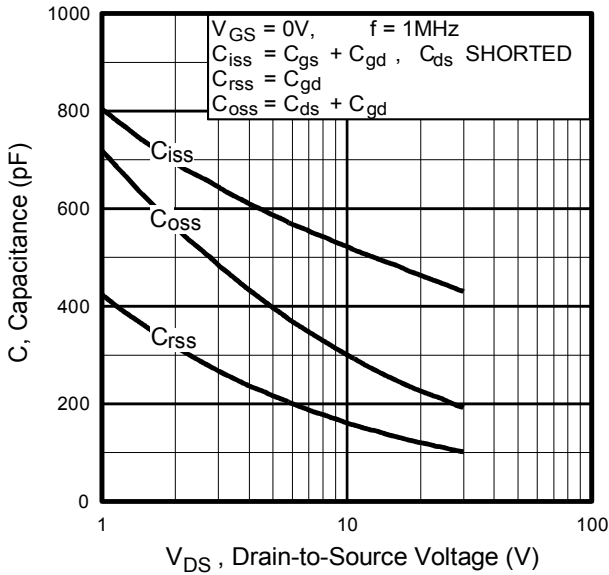
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	96		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 14A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	65	97	ns	$T_J = 25^\circ\text{C}, I_F = 14A$
$Q_{rr}$	Reverse Recovery Charge	—	140	210	nC	$di/dt = 100A/\mu s$ ④⑦
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

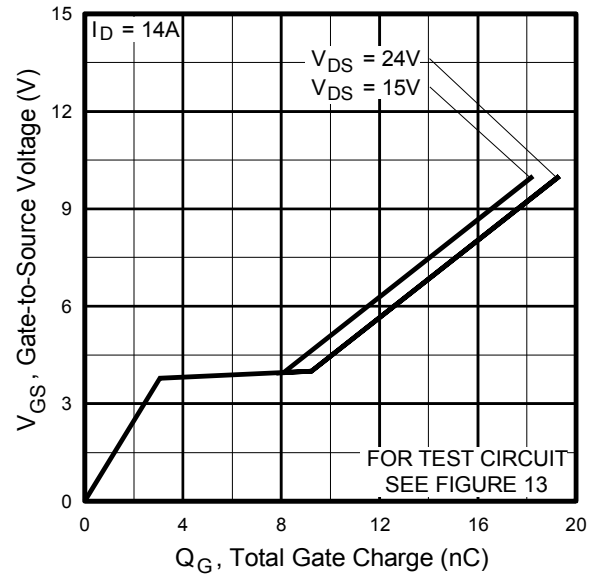
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ②  $V_{DD} = 15V$ , Starting  $T_J = 25^\circ\text{C}$ ,  $L = 570\mu H$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 14A$  (See fig. 12)
- ③  $I_{SD} \leq 14A$ ,  $di/dt \leq 140A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Calculated continuous current based on maximum allowable junction temperature. Package limitation current = 20A.
- ⑥ This is applied for I-PAK, LS of D-PAK is measured between lead and center of die contact.
- ⑦ Uses IRL2703 data and test conditions.

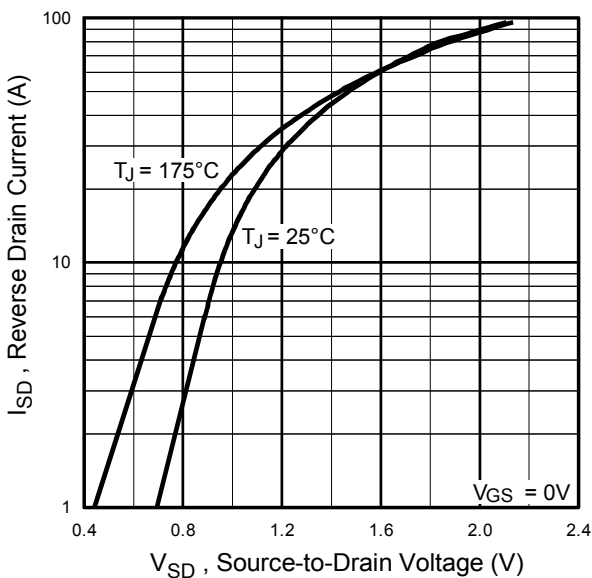

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance Vs. Temperature



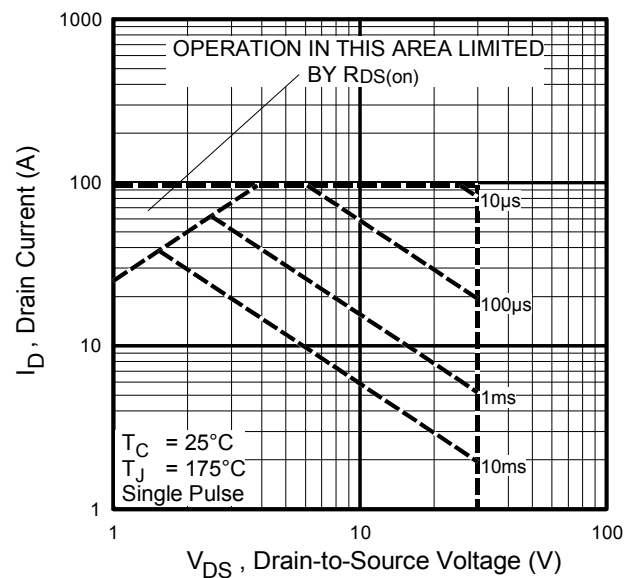
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



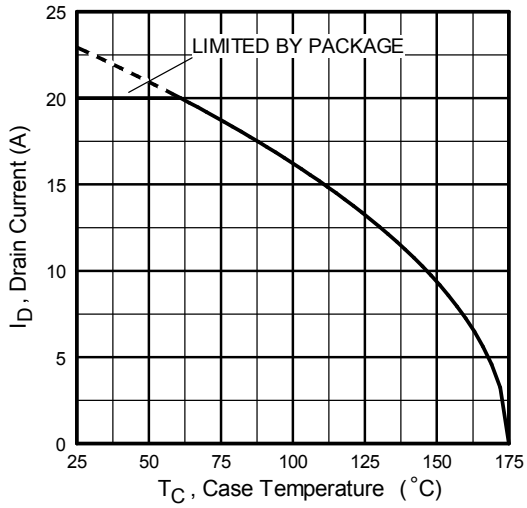
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



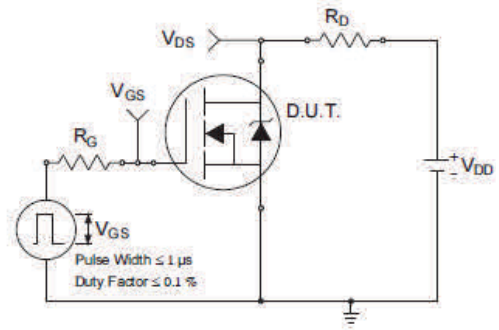
**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



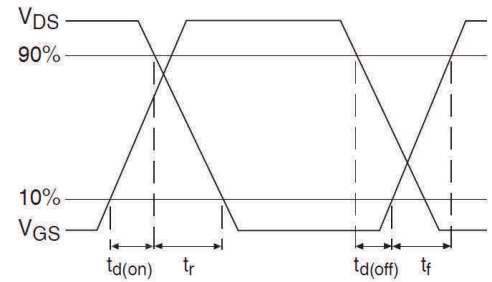
**Fig 8.** Maximum Safe Operating Area



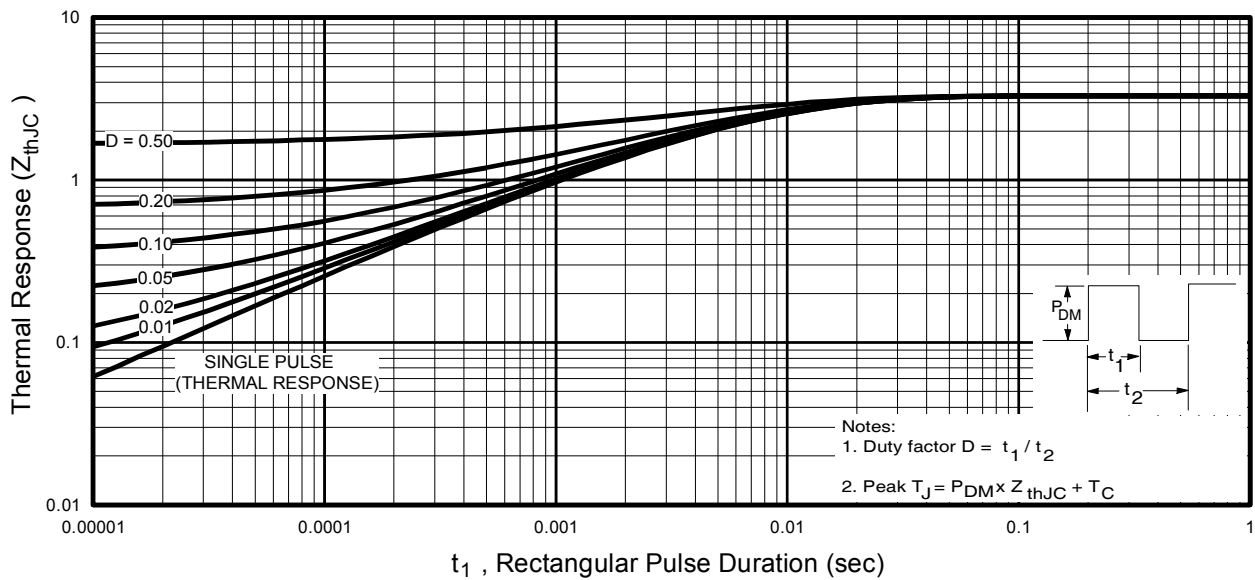
**Fig 9.** Maximum Drain Current Vs. Case Temperature



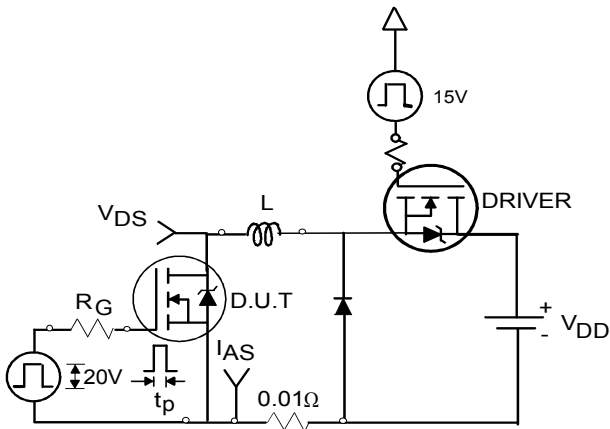
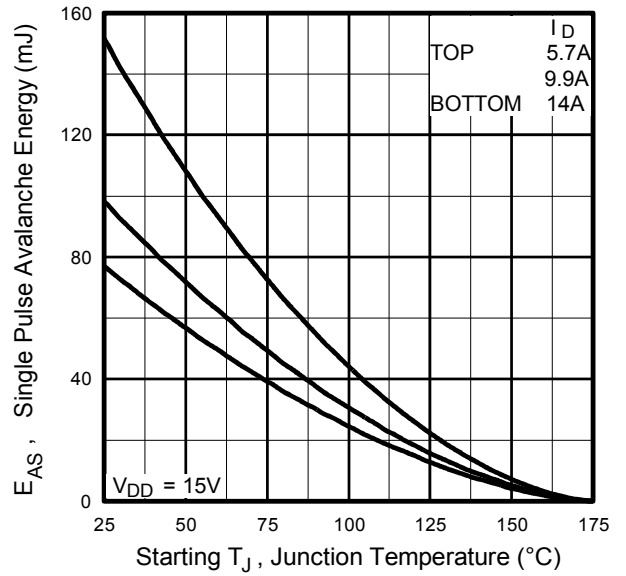
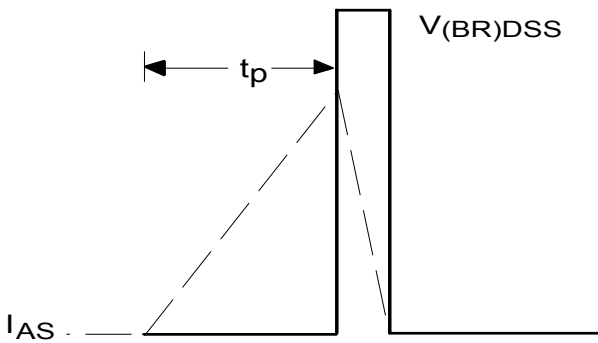
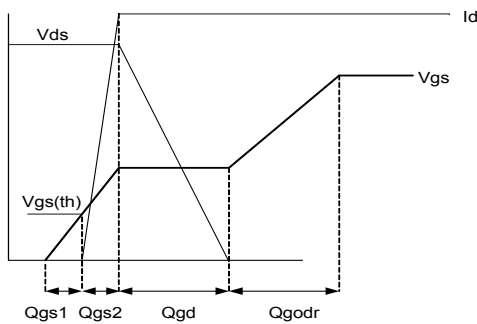
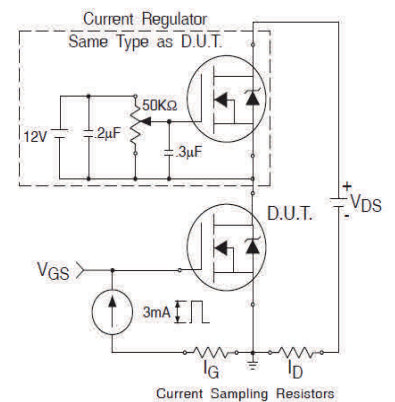
**Fig 10a.** Switching Time Test Circuit

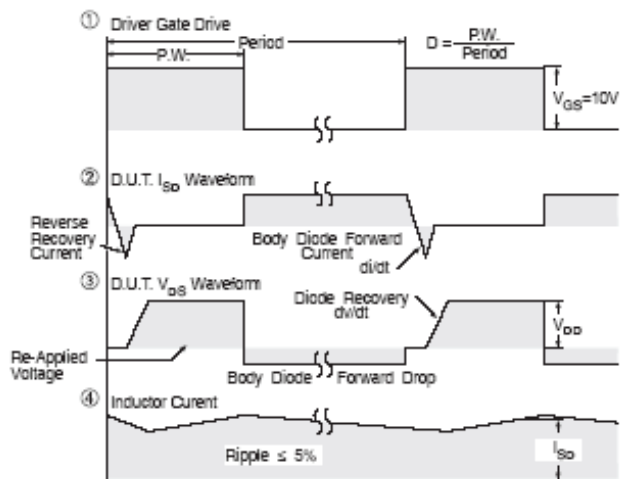
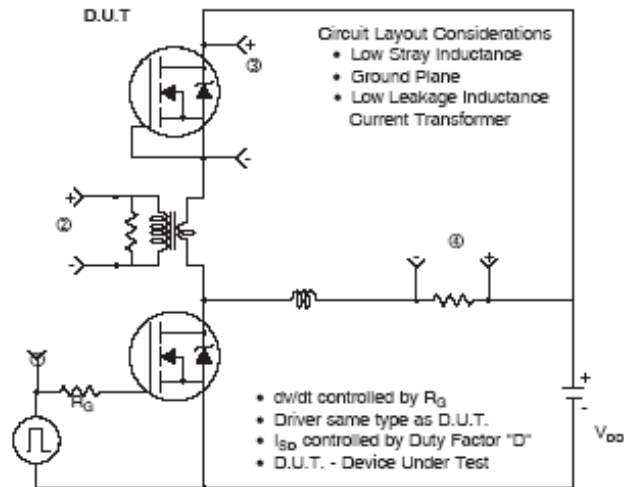


**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 13a. Gate Charge Waveform**

**Fig 13b. Gate Charge Test Circuit**

**Peak Diode Recovery dv/dt Test Circuit**


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

**D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

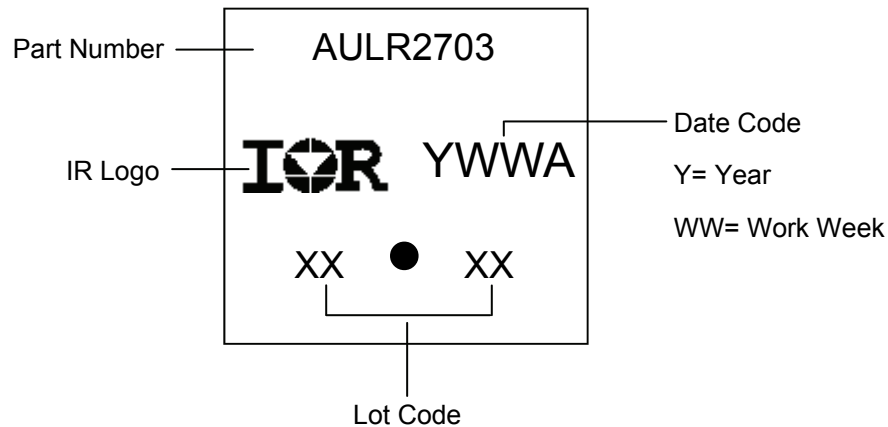
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	25"	35"	25"	35"	

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

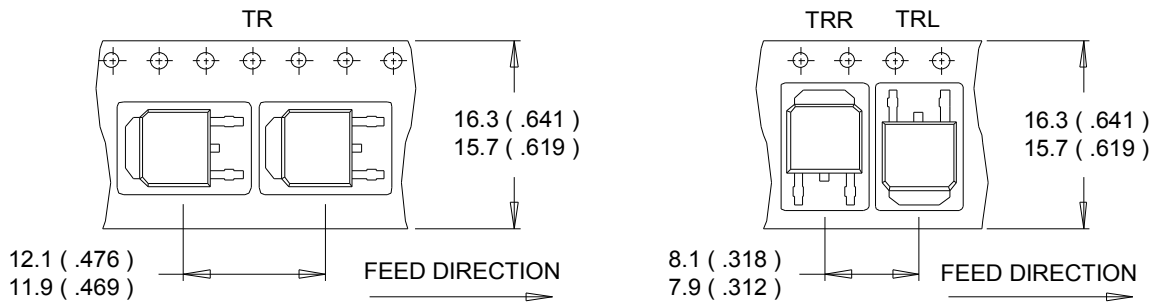
IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

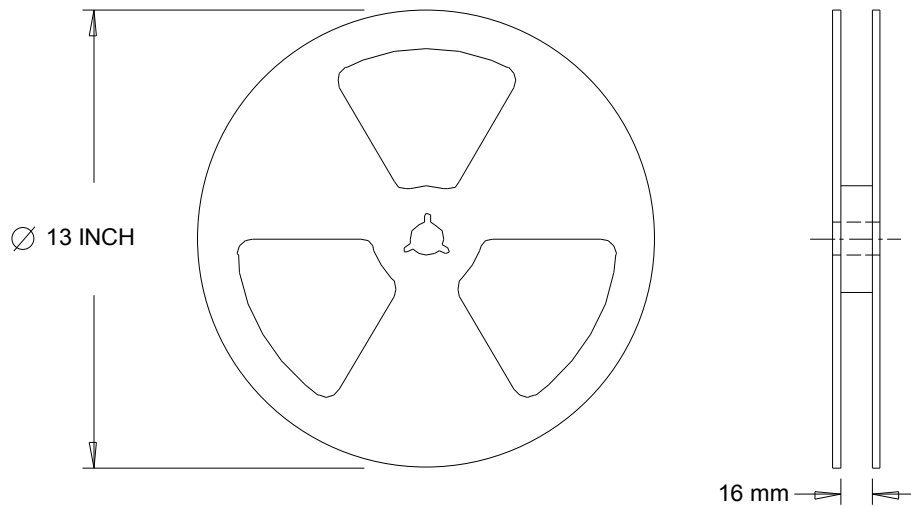
**D-Pak (TO-252AA) Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))**

**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D-Pak	MSL1
<b>ESD</b>	Machine Model	Class M2 (+/- 150V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1A (+/- 500V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
12/11/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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[RJK60S5DPK-M0#T0](#) [APT5010JVFR](#) [APT12031JFLL](#) [APT12040JVR](#) [DMN3404LQ-7](#) [NTE6400](#) [JANTX2N6796U](#) [JANTX2N6784U](#)  
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