

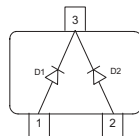
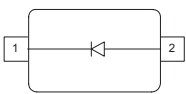
Silicon Tuning Diode

- Excellent linearity
- High Q hyperabrupt tuning diode
- Low series resistance
- High capacitance ratio
- Designed for low tuning voltage operation for VCO's in mobile communications equipment
- For control elements such as TCXOs and VCXOs
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101



BBY57-02L
BBY57-02V
BBY57-02W

BBY57-05W



| Type | Package | Configuration | L_S (nH) | Marking |
|-----------|---------|----------------|------------|---------|
| BBY57-02L | TSLP-2 | single | 0.4 | 55 |
| BBY57-02V | SC79 | single | 0.6 | 5 |
| BBY57-02W | SCD80 | single | 0.6 | 55 |
| BBY57-05W | SOT323 | common cathode | 1.4 | D5s |

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Value | Unit |
|-----------------------------|-----------|-------------|------|
| Diode reverse voltage | V_R | 10 | V |
| Forward current | I_F | 20 | mA |
| Operating temperature range | T_{op} | -55 ... 125 | °C |
| Storage temperature | T_{stg} | -55 ... 150 | |

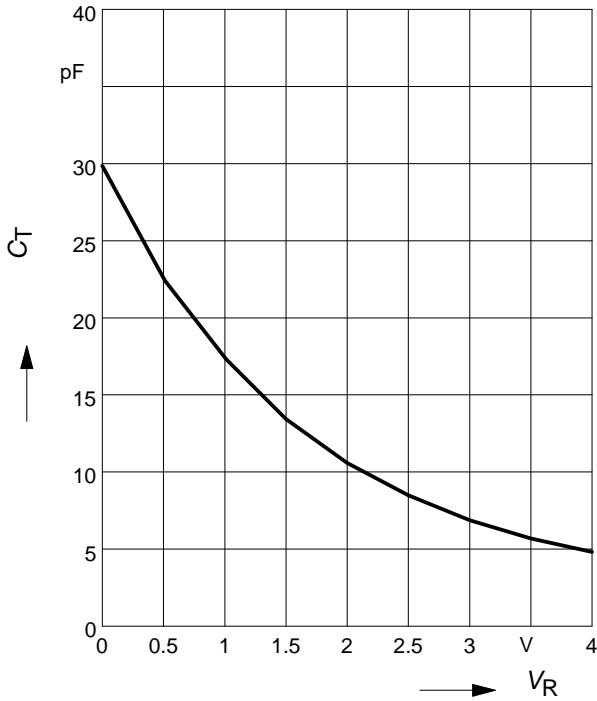
¹⁾Pb-containing package may be available upon special request

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|-----------------|--------|------|------|----------|
| | | min. | typ. | max. | |
| DC Characteristics | | | | | |
| Reverse current | I_R | | | | nA |
| $V_R = 8\text{ V}$ | | - | - | 10 | |
| $V_R = 8\text{ V}, T_A = 85^\circ\text{C}$ | | - | - | 100 | |
| AC Characteristics | | | | | |
| Diode capacitance | C_T | | | | pF |
| $V_R = 1\text{ V}, f = 1\text{ MHz}$ | | 16.5 | 17.5 | 18.6 | |
| $V_R = 2.5\text{ V}, f = 1\text{ MHz}$ | | - | 9.35 | - | |
| $V_R = 3\text{ V}, f = 1\text{ MHz}$ | | - | 7 | - | |
| $V_R = 4\text{ V}, f = 1\text{ MHz}$ | | 4 | 4.7 | 5.5 | |
| Capacitance ratio | C_{T1}/C_{T3} | - | 2.45 | - | |
| $V_R = 1\text{ V}, V_R = 3\text{ V}, f = 1\text{ MHz}$ | | | | | |
| Capacitance ratio | C_{T1}/C_{T4} | 3 | 3.7 | 4.5 | |
| $V_R = 1\text{ V}, V_R = 4\text{ V}, f = 1\text{ MHz}$ | | | | | |
| Series resistance | r_S | | | | Ω |
| $V_R = 1\text{ V}, f = 470\text{ MHz}, \text{BBY57-02L}$ | | - | 0.35 | - | |
| $V_R = 1\text{ V}, f = 470\text{ MHz}, \text{all others}$ | | - | 0.3 | - | |

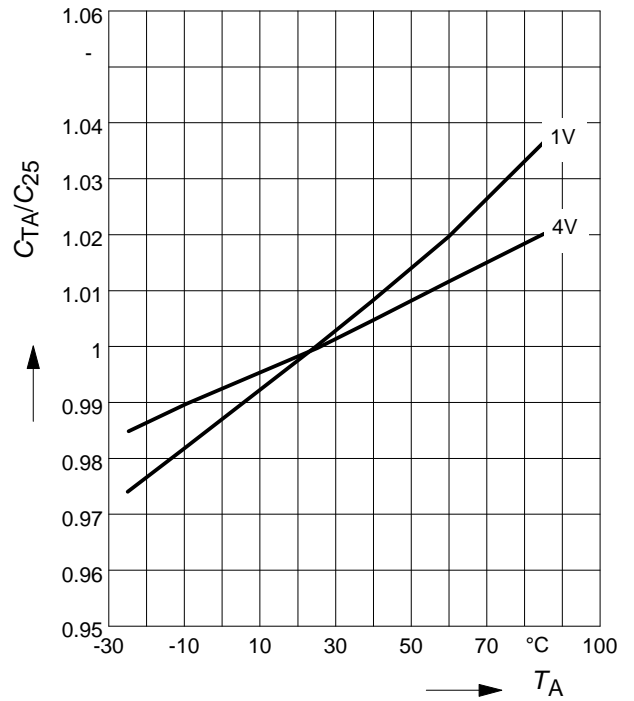
Diode capacitance $C_T = f(V_R)$

$f = 1\text{MHz}$

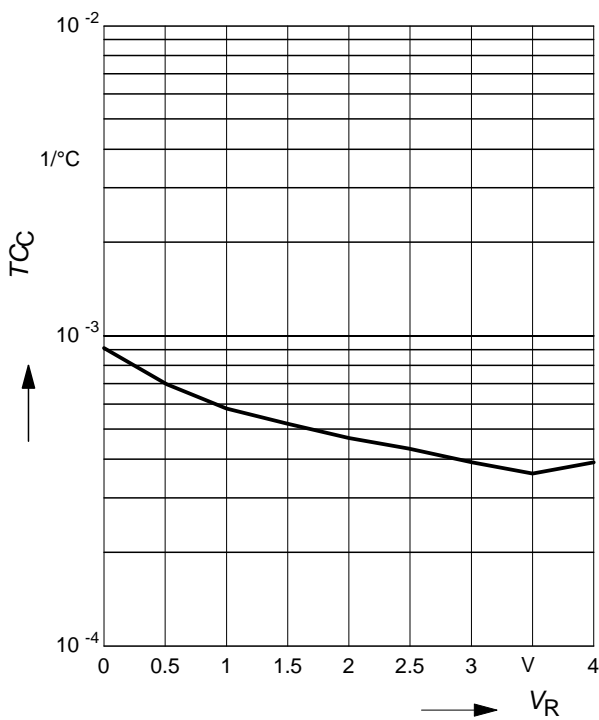


Normalized diode capacitance

$C_{(T_A)}/C_{(25^\circ\text{C})} = f(T_A); f = 1\text{MHz}$



Temperature coefficient of the diode capacitance $T_{CC} = f(V_R)$



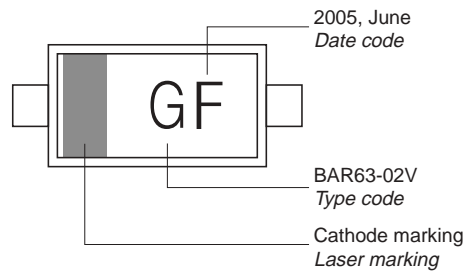
Package Outline



Foot Print



Marking Layout (Example)



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 180 mm = 8.000 Pieces/Reel (2 mm Pitch)
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



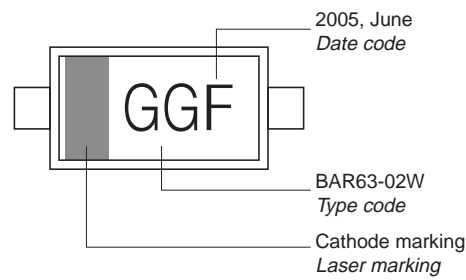
Package Outline



Foot Print

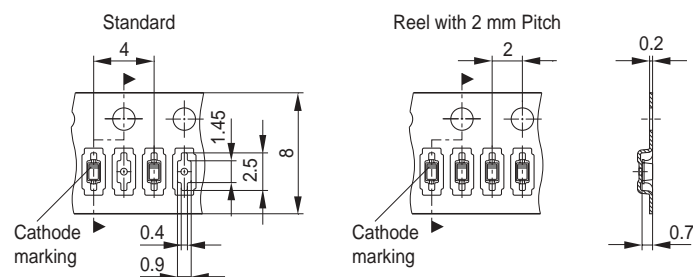


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø180 mm = 8.000 Pieces/Reel (2 mm Pitch)
 Reel ø330 mm = 10.000 Pieces/Reel

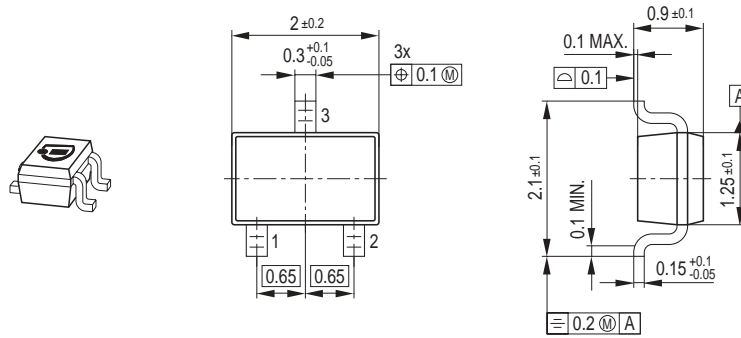


Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

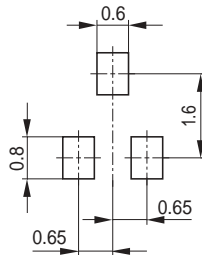
| Month | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|
| 01 | a | p | A | P | a | p | A | P | a | p | A | P |
| 02 | b | q | B | Q | b | q | B | Q | b | q | B | Q |
| 03 | c | r | C | R | c | r | C | R | c | r | C | R |
| 04 | d | s | D | S | d | s | D | S | d | s | D | S |
| 05 | e | t | E | T | e | t | E | T | e | t | E | T |
| 06 | f | u | F | U | f | u | F | U | f | u | F | U |
| 07 | g | v | G | V | g | v | G | V | g | v | G | V |
| 08 | h | x | H | X | h | x | H | X | h | x | H | X |
| 09 | j | y | J | Y | j | y | J | Y | j | y | J | Y |
| 10 | k | z | K | Z | k | z | K | Z | k | z | K | Z |
| 11 | l | 2 | L | 4 | l | 2 | L | 4 | l | 2 | L | 4 |
| 12 | n | 3 | N | 5 | n | 3 | N | 5 | n | 3 | N | 5 |

1) New Marking Layout for SC75, implemented at October 2005.

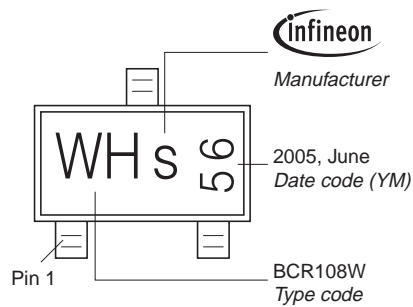
Package Outline



Foot Print

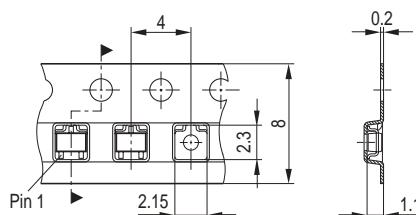


Marking Layout (Example)

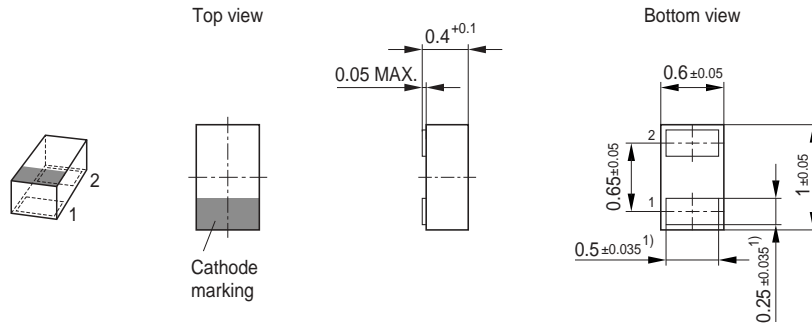


Standard Packing

Reel $\varnothing 180$ mm = 3.000 Pieces/Reel
 Reel $\varnothing 330$ mm = 10.000 Pieces/Reel



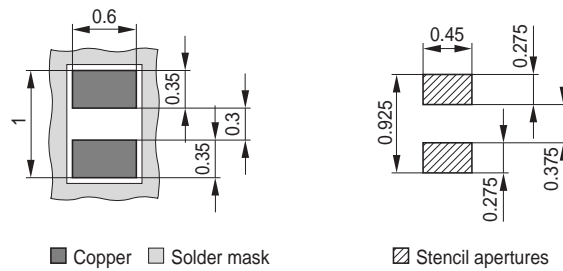
Package Outline



1) Dimension applies to plated terminal

Foot Print

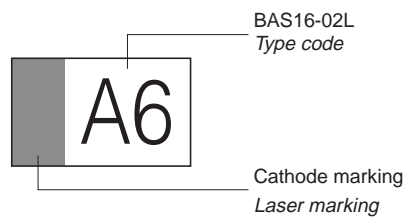
For board assembly information please refer to Infineon website "Packages"



■ Copper □ Solder mask

▨ Stencil apertures

Marking Layout (Example)

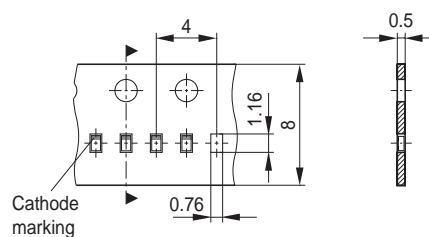


BAS16-02L
Type code

Cathode marking
Laser marking

Standard Packing

Reel \varnothing 180 mm = 15.000 Pieces/Reel
Reel \varnothing 330 mm = 50.000 Pieces/Reel (optional)



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