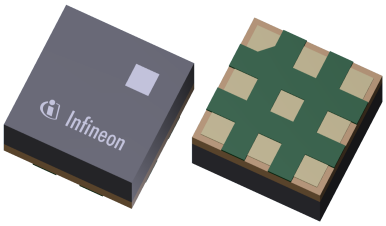
BGS14M8U9

High Power SP4T MIPI RF Switch

Features



- 39 dBm power handling capability
- Fast switching speed of 1.3 µs
- Operating up to 7.125 GHz to support latest 5G requirements
- Fully compatible with MIPI 2.1 RFFE standard with 2 USIDs
- Single VIO supply supporting both 1.2 V and 1.8 V
- High port-to-port-isolation
- No power supply decoupling required
- No blocking capacitors required if no DC applied on RF lines
- High EMI robustness
- Ultra low profile lead-less plastic package (MSL-3, 260 °C per IPC/JEDEC J-STD-20)

RoHS
Halogen-Free
Lead-Free
Green

Potential Applications

5G and 4G Cellular handsets and cellular modems

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Product Description

The BGS14M8U9 is a Single Pole Four Throw (SP4T) high power switch in a compact 9-pin package (1.1 x 1.1 mm^2).

The device is optimized for 5G and other cellular applications up to 7.125 GHz. With a low insertion loss, high isolation, high linearity and high power handling, BGS14M8U9 is perfect for 5G and LTE 4G applications, such as 5G SRS, Uplink-Carrier Aggregation, High Power User Equipment (HPUE Class 2).

Table 1: Ordering Information

Type	Package	Marking	Ordering Information
BGS14M8U9	PG-ULGA-9-1	K	BGS14M8U9 E6327

Block diagram

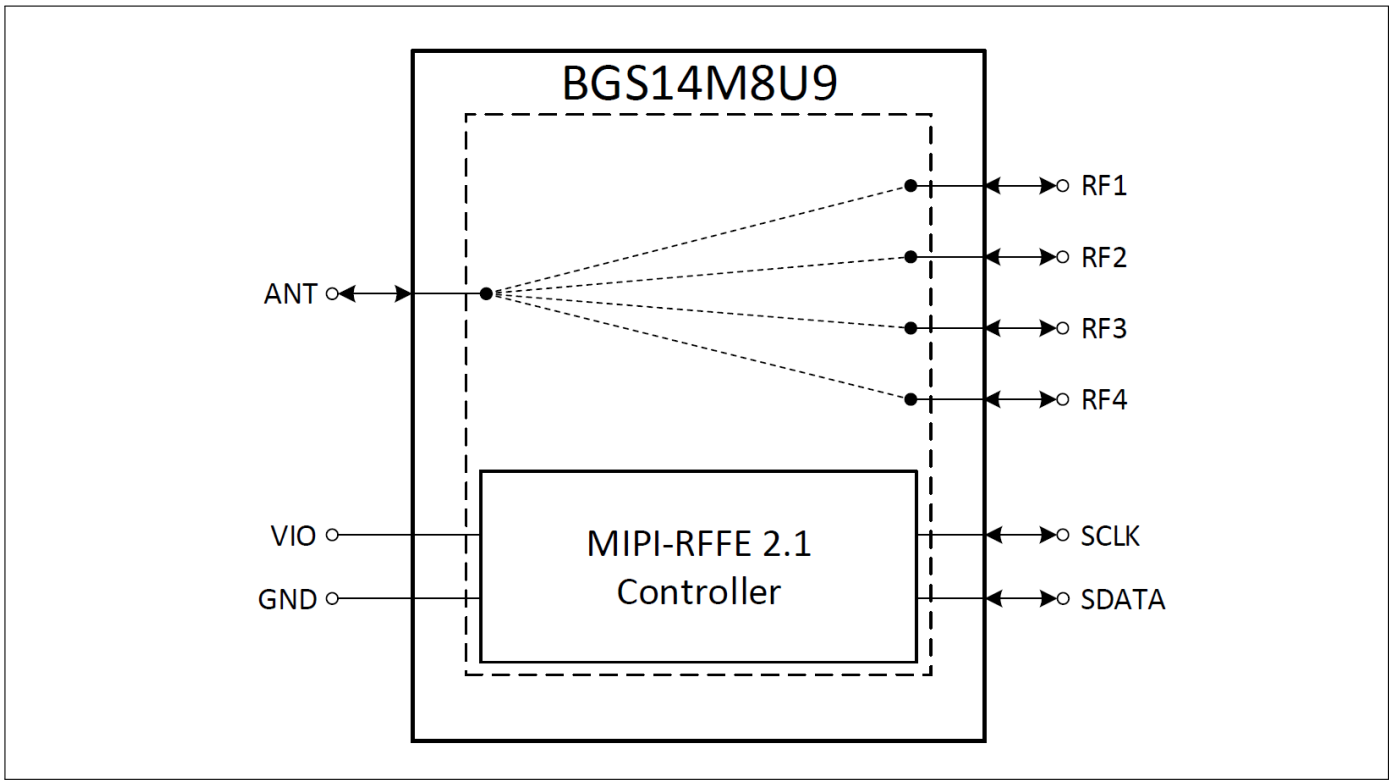


Table of Contents

Table of Contents 1

1 Absolute maximum ratings 2

2 Operation ranges 3

3 RF characteristics 4

4 MIPI RFFE specification 9

5 Package information 14

1 Absolute maximum ratings

Table 2: Absolute maximum ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{IO}	-0.5	–	2.2	V	–
RF input power	P_{RF_max}	–	–	39	dBm	Pulsed CW with 25% duty cycle and T_{period} = 4.615 ms / Switched through-path / VSWR 1:1 / 0.4 - 7.125 GHz
		–	–	35	dBm	CW with 100% duty cycle / Switched through-path / VSWR 1:1 / 0.4 - 7.125 GHz / T_A = 85°C
ESD robustness, CDM [1]	$V_{ESD,CDM}$	-1	–	+1	kV	
ESD robustness, HBM [2]	$V_{ESD,HBM}$	-2	–	+2	kV	
Junction temperature	T_j	–	–	125	°C	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Maximum DC-voltage on RF ports and RF-ground	V_{RFDC}	0	–	0	V	There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0 V
RFFE control voltage levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO} + 0.7 (max.2.2)	V	–

[1] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[2] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

2 Operation ranges

Table 3: Operation ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	MIPI 1.8 V Bus
		1.1	1.2	1.3	V	MIPI 1.2 V Bus
Supply current	I_{IO}	–	22	50	µA	MIPI 1.8 V operation Active mode (P_{RF} = 0 dBm)
		–	21	50	µA	MIPI 1.2 V operation Active mode (P_{RF} = 0 dBm)
		–	2	–	µA	Low-power mode
RFFE High-Level Input Voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE Low-Level Input Voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE High-Level Output Voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE Low-Level Output Voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE Ctrl Input Capacitance	C_{SCLK_I}, C_{SDATA_I}	–	2	3	pF	–
RFFE Ctrl Load Capacitance	C_{SDATA_L}	–	50	80	pF	Programmable through MIPI register; default value 50 pF
RFFE SCLK Write Frequency	f_{SCLK_W}	0.032	–	52	MHz	
RFFE SCLK Read Frequency	f_{SCLK_R}	0.032	–	26	MHz	
Ambient temperature range	T_A	-40	–	85	°C	–

[1)] SCLK and SDATA

Table 4: Maximum peak power at T_A = −40 °C...85 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power	$P_{RF\_operating}$	–	–	39	dBm	5G NR signal peak power / 9 dB PAPR / Switched through-path / VSWR 1:1 / 0.4 - 7.125 GHz
		–	–	37	dBm	Pulsed CW with 25% duty cycle and T_{period} = 4.615 ms / Switched through-path / VSWR 1:1 / 0.4 - 7.125 GHz
		–	–	32	dBm	RMS power of CW with 100% duty cycle / Switched through-path / VSWR 1:1 / 0.4 - 7.125 GHz

3 RF characteristics

Table 5: RF characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V / 1.1...1.3 V , unless specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion loss at 25°C						
All RF Ports	*IL*	–	0.27	0.35	dB	400–698 MHz
		–	0.28	0.36	dB	699–960 MHz
		–	0.31	0.47	dB	1200–2170 MHz
		–	0.34	0.49	dB	2171–2690 MHz
		–	0.37	0.55	dB	3300–4200 MHz
		–	0.40	0.63	dB	4400–5000 MHz
		–	0.44	0.69	dB	5150–5925 MHz
		–	0.52	0.87	dB	5925–7125 MHz
Insertion loss						
All RF Ports	*IL*	–	0.27	0.38	dB	400–698 MHz
		–	0.28	0.40	dB	699–960 MHz
		–	0.32	0.51	dB	1200–2170 MHz
		–	0.34	0.53	dB	2171–2690 MHz
		–	0.37	0.59	dB	3300–4200 MHz
		–	0.40	0.68	dB	4400–5000 MHz
		–	0.44	0.77	dB	5150–5925 MHz
		–	0.52	0.94	dB	5925–7125 MHz
Return loss						
All RF Ports	*RL*	32	35	–	dB	400–698 MHz
		31	34	–	dB	699–960 MHz
		26	33	–	dB	1200–2170 MHz
		23	30	–	dB	2171–2690 MHz
		21	28	–	dB	3300–4200 MHz
		22	28	–	dB	4400–5000 MHz
		18	25	–	dB	5150–5925 MHz
		17	23	–	dB	5925–7125 MHz
Isolation						
Input-output isolation (ANT port vs. RFx ports)	*ISO*	43	49	–	dB	400–698 MHz
		40	46	–	dB	699–960 MHz
		33	38	–	dB	1200–2170 MHz
		31	35	–	dB	2171–2690 MHz
		26	30	–	dB	3300–4200 MHz
		23	27	–	dB	4400–5000 MHz
		20	25	–	dB	5150–5925 MHz
		18	22	–	dB	5925–7125 MHz

Table 6: RF characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V / 1.1...1.3 V , unless specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic generation: ANT-RF1/2 at VSWR 1:1, 25 % duty cycle						
2nd Harmonic distortions	$H2_{LTE,LB}$	–	-85	-80	dBm	26 dBm, 50 Ω, 663 - 915 MHz
	$H2_{LTE,MB}$	–	-78	-74	dBm	26 dBm, 50 Ω, 1447 - 2020 MHz
	$H2_{LTE,HB}$	–	-70	-66	dBm	29 dBm, 50 Ω, 2300 - 2690 MHz
	$H2_{NR,n77}$	–	-65	-62	dBm	29 dBm, 50 Ω, 3300 - 4200 MHz
	$H2_{NR,n79}$	–	-62	-58	dBm	29 dBm, 50 Ω, 4400 - 5000 MHz
	$H2_{GSM,LB}$	–	-67	-62	dBm	35 dBm, 50 Ω, 824 - 915 MHz
	$H2_{GSM,HB}$	–	-65	-62	dBm	33 dBm, 50 Ω, 1710 - 1910 MHz
3rd Harmonic distortions	$H3_{LTE,LB}$	–	-87	-82	dBm	26 dBm, 50 Ω, 663 - 915 MHz
	$H3_{LTE,MB}$	–	-85	-81	dBm	26 dBm, 50 Ω, 1447 - 2020 MHz
	$H3_{LTE,HB}$	–	-74	-71	dBm	29 dBm, 50 Ω, 2300 - 2690 MHz
	$H3_{NR,n77}$	–	-71	-67	dBm	29 dBm, 50 Ω, 3300 - 4200 MHz
	$H3_{NR,n79}$	–	-67	-62	dBm	29 dBm, 50 Ω, 4400 - 5000 MHz
	$H3_{GSM,LB}$	–	-60	-57	dBm	35 dBm, 50 Ω, 824 - 915 MHz
	$H3_{GSM,HB}$	–	-63	-60	dBm	33 dBm, 50 Ω, 1710 - 1910 MHz
Harmonic generation: ANT-RF3/4 at VSWR 1:1, 25 % duty cycle						
2nd Harmonic distortions	$H2_{LTE,LB}$	–	-87	-82	dBm	26 dBm, 50 Ω, 663 - 915 MHz
	$H2_{LTE,MB}$	–	-84	-80	dBm	26 dBm, 50 Ω, 1447 - 2020 MHz
	$H2_{LTE,HB}$	–	-79	-74	dBm	29 dBm, 50 Ω, 2300 - 2690 MHz
	$H2_{NR,n77}$	–	-74	-70	dBm	29 dBm, 50 Ω, 3300 - 4200 MHz
	$H2_{NR,n79}$	–	-72	-68	dBm	29 dBm, 50 Ω, 4400 - 5000 MHz
	$H2_{GSM,LB}$	–	-68	-63	dBm	35 dBm, 50 Ω, 824 - 915 MHz
	$H2_{GSM,HB}$	–	-72	-67	dBm	33 dBm, 50 Ω, 1710 - 1910 MHz
3rd Harmonic distortions	$H3_{LTE,LB}$	–	-87	-83	dBm	26 dBm, 50 Ω, 663 - 915 MHz
	$H3_{LTE,MB}$	–	-85	-83	dBm	26 dBm, 50 Ω, 1447 - 2020 MHz
	$H3_{LTE,HB}$	–	-75	-71	dBm	29 dBm, 50 Ω, 2300 - 2690 MHz
	$H3_{NR,n77}$	–	-72	-68	dBm	29 dBm, 50 Ω, 3300 - 4200 MHz
	$H3_{NR,n79}$	–	-68	-65	dBm	29 dBm, 50 Ω, 4400 - 5000 MHz
	$H3_{GSM,LB}$	–	-60	-57	dBm	35 dBm, 50 Ω, 824 - 915 MHz
	$H3_{GSM,HB}$	–	-64	-61	dBm	33 dBm, 50 Ω, 1710 - 1910 MHz

Table 7: RF characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V / 1.1...1.3 V , unless specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Intermodulation distortion IMD2						
Band 1 IMD2 high	*IMD2*	–	-122	-115	dBm	Test conditions, see Table 8
Band 1 IMD2 low		–	-120	-112	dBm	
Band 5 IMD2 high		–	-124	-118	dBm	
Band 5 IMD2 low		–	-110	-101	dBm	
Band 7 IMD2 high		–	-119	-112	dBm	
Band 7 IMD2 low		–	-116	-108	dBm	
Band 3 + 5 IMD2 ULCA		–	-96	-90	dBm	
Band 3 + N77 IMD2 ENDC		–	-95	-88	dBm	
Intermodulation distortion IMD3						
Band 1 IMD3 half duplex	*IMD3*	–	-123	-118	dBm	Test conditions, see Table 9
Band 1 IMD3 double duplex		–	-134	-125	dBm	
Band 5 IMD3 half duplex		–	-127	-120	dBm	
Band 5 IMD3 double duplex		–	-130	-124	dBm	
Band 7 IMD3 half duplex		–	-128	-122	dBm	
Band 7 IMD3 double duplex		–	-130	-118	dBm	
Band 1 + 3 IMD3 ULCA		–	-104	-94	dBm	
Band 5 + N78 IMD3 ENDC		–	-93	-87	dBm	

Table 8: IMD2 testcases[1)]

Band	Symbol	In-band frequency (MHz)	Blocker frequency 1 (MHz)	Blocker power 1 (dBm)	Blocker frequency 2 (MHz)	Blocker power 2 (dBm)
Band 1	$B1_{IMD2,high}$	2140	1950	20	4090	-15
	$B1_{IMD2,low}$	2140	1950	20	190	-15
Band 5	$B5_{IMD2,high}$	881.5	836.5	20	1718	-15
	$B5_{IMD2,low}$	881.5	836.5	20	45	-15
Band 7	$B7_{IMD2,high}$	2655	2535	20	5190	-15
	$B7_{IMD2,low}$	2655	2535	20	120	-15
Band 3 + Band 5 ULCA	$B3B5_{IMD2,ULCA}$	881.5	836.5	23	1718	10
Band 3 + N77 ENDC	$B3N77_{IMD2,ENDC}$	1842.5	1747.5	23	3590	10

[1)] Both blockers applied to same RF path.

Table 9: IMD3 testcases[1)]

Band	Symbol	In-band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,half\ duplex}$	2140	1950	20	2045	-15
	$B1_{IMD3,double\ duplex}$	2140	1950	20	1760	-15
Band 5	$B5_{IMD3,half\ duplex}$	881.5	836.5	20	859	-15
	$B5_{IMD3,double\ duplex}$	881.5	836.5	20	791.5	-15
Band 7	$B7_{IMD3,half\ duplex}$	2655	2535	20	2595	-15
	$B7_{IMD3,double\ duplex}$	2655	2535	20	2415	-15
Band 1 + band 3 ULCA	$B1B3_{IMD3,ULCA}$	2140	1950	23	1760	10
Band 5 + N78 ENDC	$B5N78_{IMD3,ENDC}$	2140	836.5	26	3813	10

[1)] Both blockers applied to same RF path.

Table 10: RF characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V / 1.1...1.3 V , unless specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
Power up settling time	t_{pup}	–	7	20	µs	After power down mode
RF rise time	t_{RT}	–	0.6	0.8	µs	Time from 10% to 90% RF power
RF switching time - ON	$t_{ST,on}$	–	1	1.8	µs	50% last SCLK falling edge for Register Write Command to 90% of final voltage amplitude of the signal; switching between two RF paths and from isolation mode
RF switching time - OFF	$t_{ST,off}$	–	0.9	1.8	µs	50% last SCLK falling edge for Register Write Command to 10% initial voltage amplitude of the signal; switching between two RF paths and to isolation mode

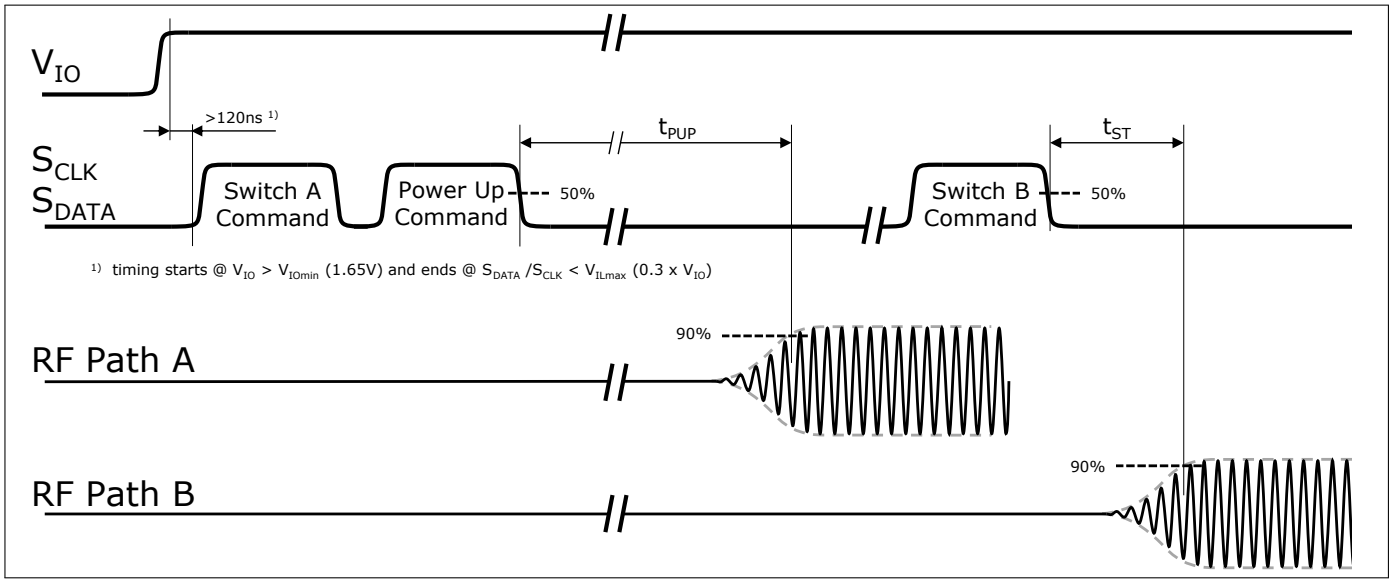


Figure 1: MIPI Timing Diagram

4 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 11: MIPI features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Standard reach RFFE bus length	Yes	RFFE Bus length of up to 15 cm (standard)
Longer reach RFFE bus length feature (MIPI RFFE 2.1 optional feature)	Yes	Longer reach allows for longer RFFE bus lengths. This requires a limitation to the standard frequency range of RFFE plus additional timing requirements for all devices on the bus
Programmable driver strength (MIPI RFFE 2.x feature)	Yes	Allows to program MIPI device bus driver strength (relevant for read back messages) up to 80 pF via BUS_LD-register (0x2B); Default value: 50 pF
Register 0 write command sequence	Yes	Shortened write sequence for register 0 Caution: only 7 LSBs in Reg 0 can be addressed
Register read and write command sequence	Yes	Standard register read/write procedure addressing standard register space of 0x00 – 0x1F
Extended register read and write command sequence	Yes	Register read/write procedure addressing extended register space of 0x00 – 0xFF
Masked write command sequence (MIPI 2.1 optional feature)	Yes	Allow only certain bits in a register to be updated during a write command. Relevant registers marked "MW" in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz – 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz – 52 MHz for write commands
sRead (synchronous Read) full speed or half speed up to 26 MHz (MIPI 2.x feature)	Yes	Relaxed slave setup time requirements as master samples data on rising edge of SCLK signal
Regular read full speed or half speed up to 13 MHz (MIPI RFFE 1.10-2.x feature)	Yes	Stricter slave setup time requirements as master samples data on falling edge of SCLK signal
Product ID + extended product ID register	Yes	PRODUCT_ID (address 0x1D) and EXT_PRODUCT_ID (address 0x20) registers
Extended manufacturer ID (10->12 bit) (MIPI 2.1 optional feature)	Yes	The new 2 bits In MIPI 2.1 are placed in RFFE USID register at address 0x1F; value is 0 in IFX products
Revision ID register	Yes	This register contains the device revision (address 0x21)

Table 11: MIPI features (continued)

Feature	Supported	Comment
Programmable GSID (group slave identifier)	Yes	RFFE 2.x GROUP_SID register (at address 0x22); Only in case RFFE 1.1 backwards compatibility is supported: GROUP_SID0 bit-field access at address 0x1B (copy of GROUP_SID0)
Programmable USID (unique slave identifier)	Yes	Device can be also explicitly addressed via combination of (old) USID, Manufacturer ID, and (extended) product ID to reprogram USID via (extended) register write sequence (see MIPI RFFE Spec v2.1 Chapter 6.2.1)
Trigger functionality	Yes	3 "standard" triggers via PM_TRIG[5:0] consisting of 3 Mask- and 3 trigger bits
Ignored trigger handling in low power mode	Yes	When device is and stays in low power mode, write to trigger registers will be ignored (Note: when changing power mode, writing to trigger registers are not ignored)
Extended triggers and trigger masks (MIPI 2.1 optional feature)	Yes	additional eight triggers and the associated trigger masks, have been added in MIPI 2.1 (registers at addresses 0x2D and 0x2E)
Broadcast / GSID write to PM TRIG register	Yes	The above mentioned trigger register (and extended trigger register) can be accessed via Broadcast/GSID writes to trigger several MIPI devices snychronously. NOTE: Trigger Mask bits are nor changed with Broadcast/GSID writes
Reset	Yes	Reset is possible via VIO, PM TRIG or register SW_RST (0x23); NOTE: SW_RST only resets user defined registers, it does not reset the values of any reserved registers
Status / error sum register	Yes	RFFE 2.x ERR_SUM register (address 0x24); only in case RFFE 1.1 backwards compatibility is supported: RFFE_STATUS register access at address 0x1A (copy of ERR_SUM)
USID select via SDATA/SCLK swap feature	Yes	An alternate set of USIDs can be obtained by swapping SDATA/SCLK, see Tab. 12

Table 12: USID table

# USID	SCLK/SDATA swapping	USID value (bin)	USID value (hex)
1	No	1010	0xA
2	Yes	1011	0xB

Table 13: Register mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	SW_CTRL0	7:4	SW_CTRL	Reserved for future use.	0x00	No	All Triggers (0 - 10)	R/W MW
		3:0	SW_CTRL	SW_CTRL Refer to Tab. 16				
0x1C	PM_TRIG	7	PWR_MODE[1], Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	N/A	R/W MW
		6	PWR_MODE[0], State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data writes to registers tied to TRIGGER_2 are masked. 1: Data writes to registers tied to TRIGGER_2 are not masked.	0	No		
		4	TRIGGER_MASK_1	0: Data writes to registers tied to TRIGGER_1 are masked. 1: Data writes to registers tied to TRIGGER_1 are not masked.				
0x1C	PM_TRIG	3	TRIGGER_MASK_0	0: Data writes to registers tied to TRIGGER_0 are masked. 1: Data writes to registers tied to TRIGGER_0 are not masked.	0	No	N/A	R/W MW
		2	TRIGGER_2	0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_2.	0	Yes		
0x1C	PM_TRIG	1	TRIGGER_1	0: No action. Data is held in shadow registers 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_1.	0	Yes	N/A	R/W MW
0x1C	PM_TRIG	0	TRIGGER_0	0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_0.	0	Yes	N/A	R/W MW
0x1D	PRODUCT_ID	7:0	PRODUCT_ID[7:0]	Product ID.	0x5E	No	N/A	R
0x1E	MANUFACTURER_ID	7:0	MANUFACTURER_ID[7:0]	Manufacturer ID.	0x1A	No	N/A	R
0x1F	USID	7:6	MANUFACTURER_ID[11:10]	Manufacturer ID.	00	No	N/A	R
		5:4	MANUFACTURER_ID[9:8]	Manufacturer ID.	01			
		3:0	USID[3:0]	These bits store the USID of the device.	See Tab. 12	No	N/A	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID[7:0]	Extension to PRODUCT_ID	0x00	No	N/A	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip Main Revision	0x0	No	N/A	R
		3:0	SUB_REVISION	Chip Sub Revision				
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID	0x0	No	N/A	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID				
0x23	UDR_RST	7	UDR_RST	Reset all configurable non—RFFE Reserved registers to default values. 0: Normal Operation 1: Software Reset	0	Yes	N/A	R/W
		6:0	RESERVED	Reserved for future use. Set to all 0	0000 000			

Table 14: Register mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x24	ERR_SUM	7	RESERVED	Reserved for future error codes.	0	No	N/A	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error—discard command.				
		5	COMMAND_LENGTH_ERR	Command length error.				
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.				
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.				
		2	READ_UNUSED_REG	Read command to an invalid address.				
		1	WRITE_UNUSED_REG	Write command to an invalid address.				
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.				
0x2B	BUS_LD	7:4	RESERVED	Reserved	0x0	No	N/A	R
		3:0	BUS_LD[3:0]	Set approximate bus load 0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 70 pF 0x7: 80 pF 0x8-0xF: Spare	0x04	No	N/A	R/W
0x2D	EXT_TRIG_MASK	7	EXT_TRIGGER_MASK_10	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)	1	No	N/A	R/W, MW
		6	EXT_TRIGGER_MASK_9	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				
		5	EXT_TRIGGER_MASK_8	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				
		4	EXT_TRIGGER_MASK_7	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				
		3	EXT_TRIGGER_MASK_6	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				
		2	EXT_TRIGGER_MASK_5	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				
0x2D	EXT_TRIG_MASK	1	EXT_TRIGGER_MASK_4	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)	1	No	N/A	R/W, MW
		0	EXT_TRIGGER_MASK_3	0: Data masked (held in shadow registers) 1: Data not masked (go directly to the active registers)				

Table 15: Register mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG_REG	7	EXT_TRIGGER_10	0: No action. Data is held in shadow registers 1: Data is transferred to active registers	0	Yes	N/A	R/W, MW
		6	EXT_TRIGGER_9	0: No action. Data is held in shadow registers 1: Data is transferred to active registers				
0x2E	EXT_TRIG_REG	5	EXT_TRIGGER_8	0: No action. Data is held in shadow registers 1: Data is transferred to active registers	0	Yes	N/A	R/W, MW
		4	EXT_TRIGGER_7	0: No action. Data is held in shadow registers 1: Data is transferred to active registers				
0x2E	EXT_TRIG_REG	3	EXT_TRIGGER_6	0: No action. Data is held in shadow registers 1: Data is transferred to active registers	0	Yes	N/A	R/W, MW
		2	EXT_TRIGGER_5	0: No action. Data is held in shadow registers 1: Data is transferred to active registers				
0x2E	EXT_TRIG_REG	1	EXT_TRIGGER_4	0: No action. Data is held in shadow registers 1: Data is transferred to active registers	0	Yes	N/A	R/W, MW
		0	EXT_TRIGGER_3	0: No action. Data is held in shadow registers 1: Data is transferred to active registers				

Table 16: Modes of operation (truth table)

State	Mode	SW_CTRL							
		D7	D6	D5	D4	D3	D2	D1	D0
1	ALL OFF (Isolation)	Reserved	Reserved	Reserved	Reserved	0	0	0	0
2	RF1 on	Reserved	Reserved	Reserved	Reserved	0	0	0	1
3	RF2 on	Reserved	Reserved	Reserved	Reserved	0	0	1	0
4	RF3 on	Reserved	Reserved	Reserved	Reserved	0	1	0	0
5	RF4 on	Reserved	Reserved	Reserved	Reserved	1	0	0	0

5 Package information

The switch has a package size of 1100 µm in X-dimension and 1100 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The pin definitions are listed in Tab. 18.

Table 17: Mechanical data

Parameter	Symbol	Value	Unit
Package X-dimension	*X*	1100 ± 50	µm
Package Y-dimension	*Y*	1100 ± 50	µm
Package height	*H*	530 ± 50	µm

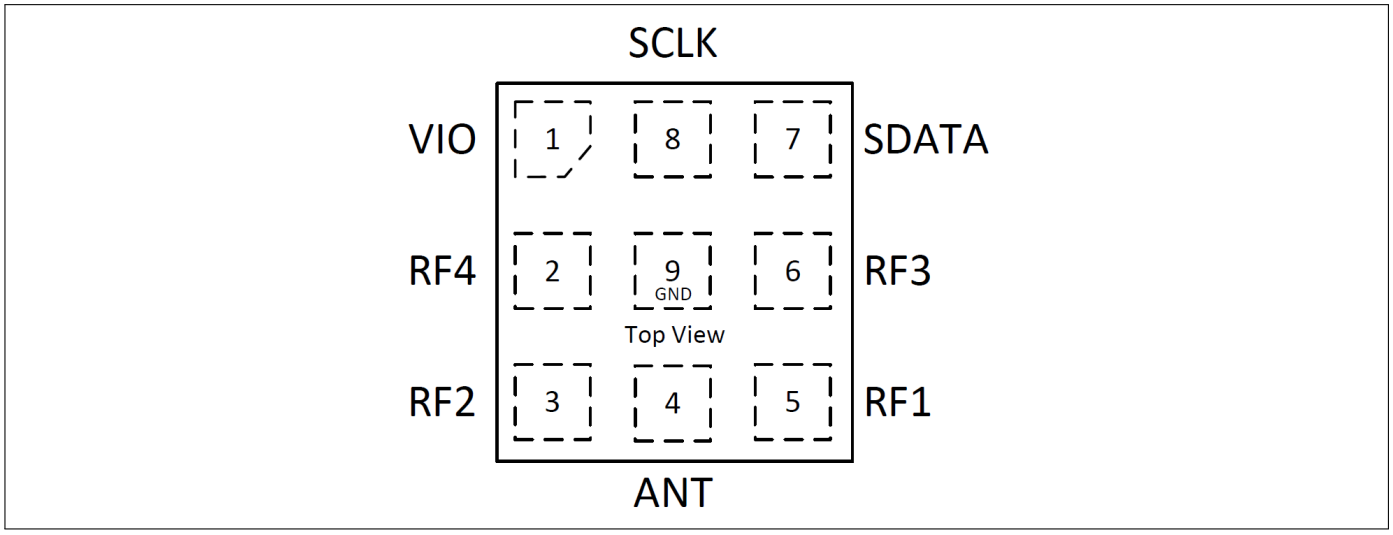


Figure 2: Pin configuration (top view)

Table 18: Pin definition and function

Pin No.	Name	Function
1	VIO	(MIPI) Power supply
2	RF4	Rx Port
3	RF2	Rx Port
4	ANT	RF Input
5	RF1	Rx Port
6	RF3	Rx Port
7	SDATA	MIPI Control
8	SCLK	MIPI Control
9	GND	GND

Table 19: ESD robustness, System Level Test (SLT)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD capability, SLT[1)]	$V_{ESD,SLT}$	-6	–	+6	kV	IEC61000-4-2; with shunt 56nH, all RF ports
		-8	–	+8	kV	IEC61000-4-2; with shunt 27nH, all RF ports

[1)] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

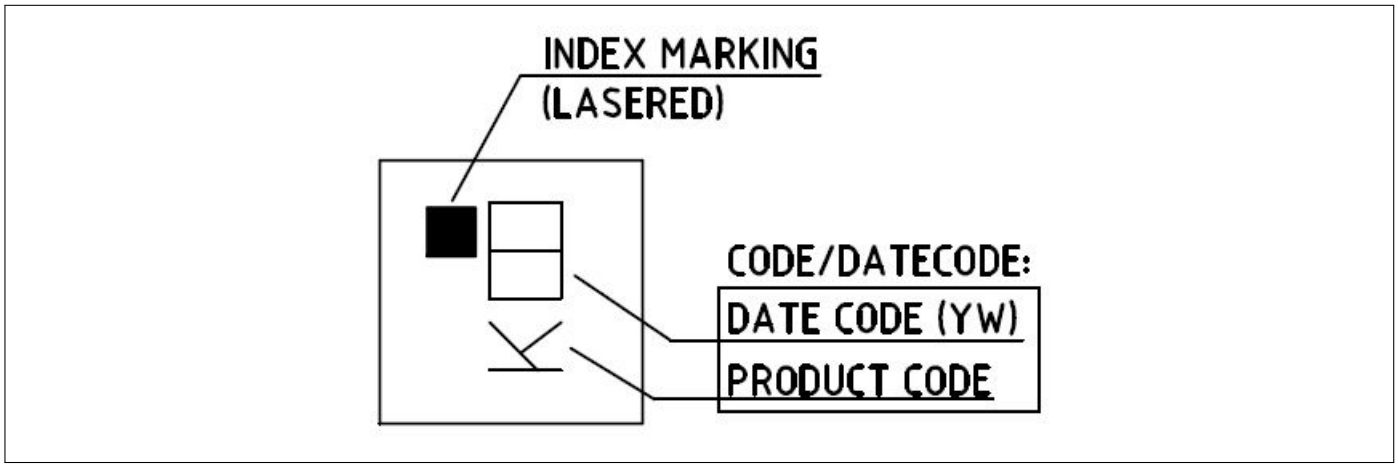


Figure 3: Marking specification (top view): Date code (YW) digits Y and W defined in Table 20/21

Table 20: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2020	0	2030	0
2021	1	2031	1
2022	2	2032	2
2023	3	2033	3
2024	4	2034	4
2025	5	2035	5
2026	6	2036	6
2027	7	2037	7
2028	8	2038	8
2029	9	2039	9

Table 21: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

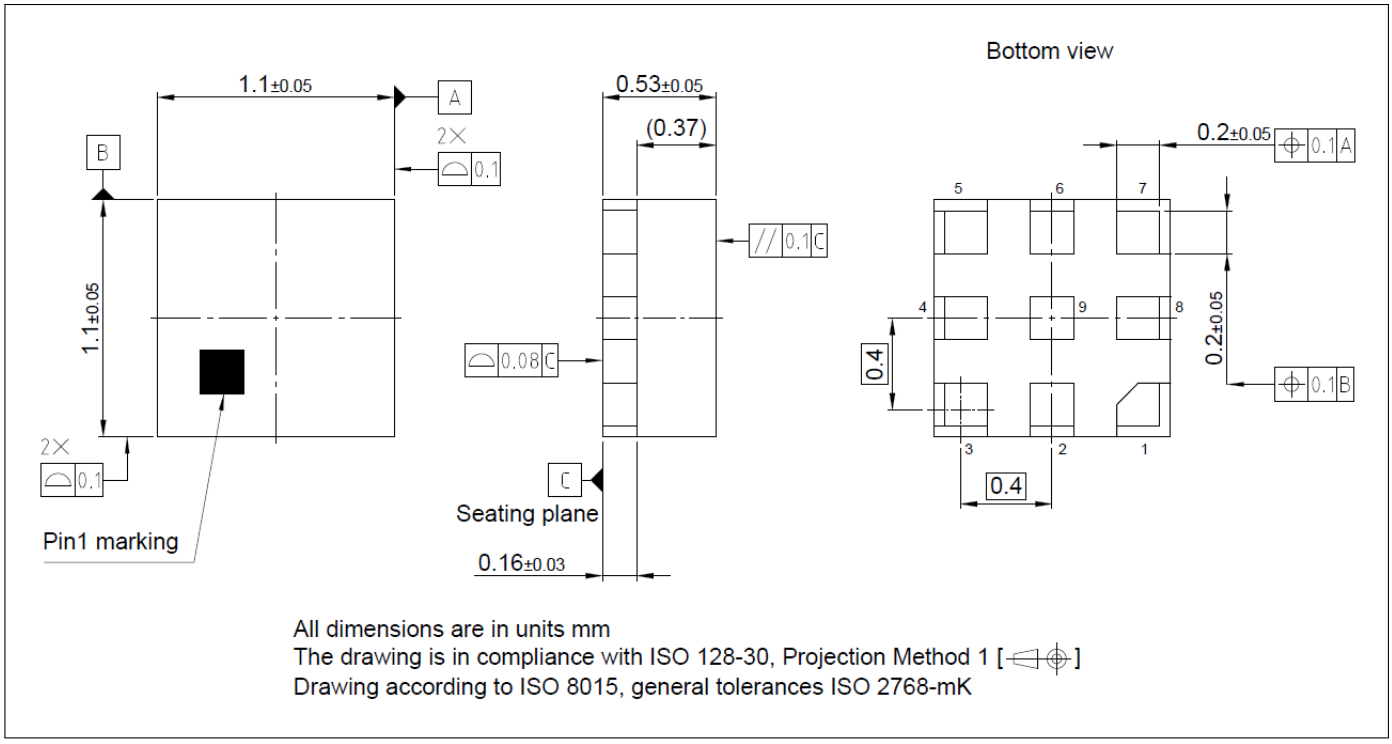


Figure 4: Package outline drawing (top, side and bottom views)

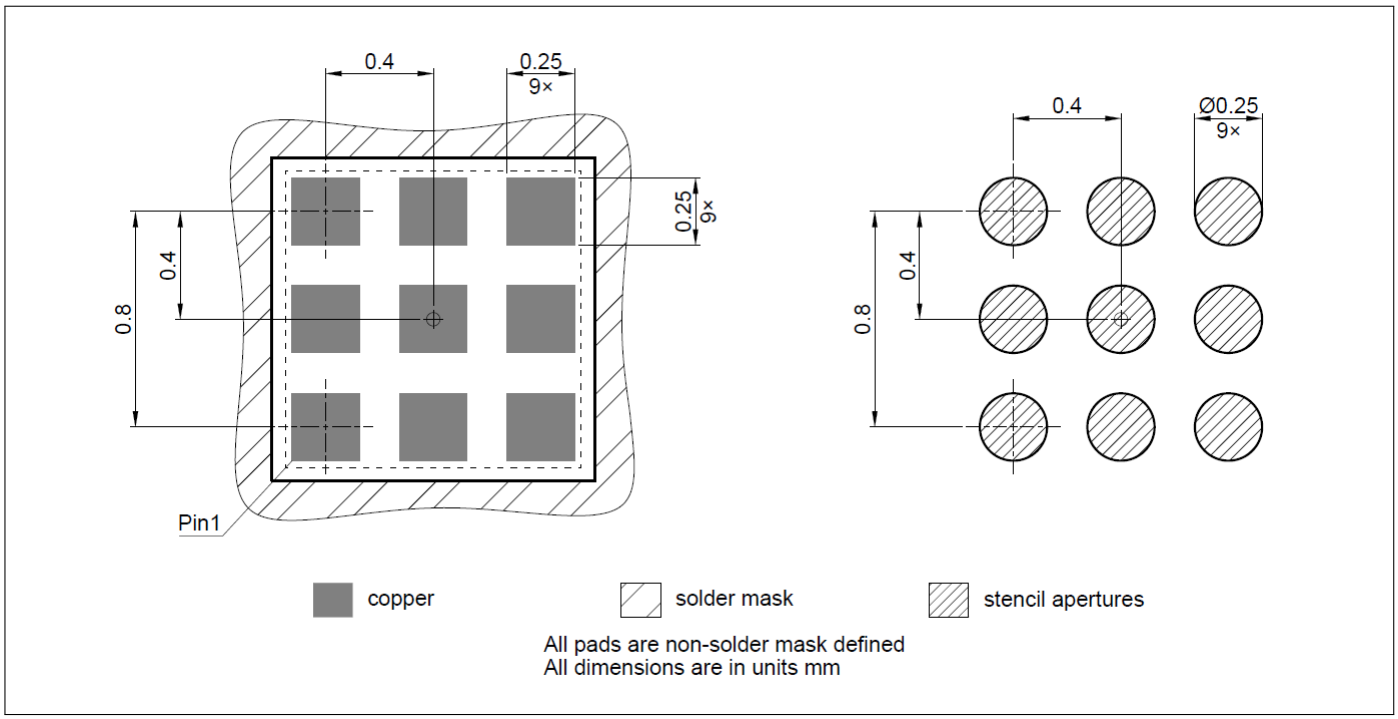


Figure 5: Footprint recommendation

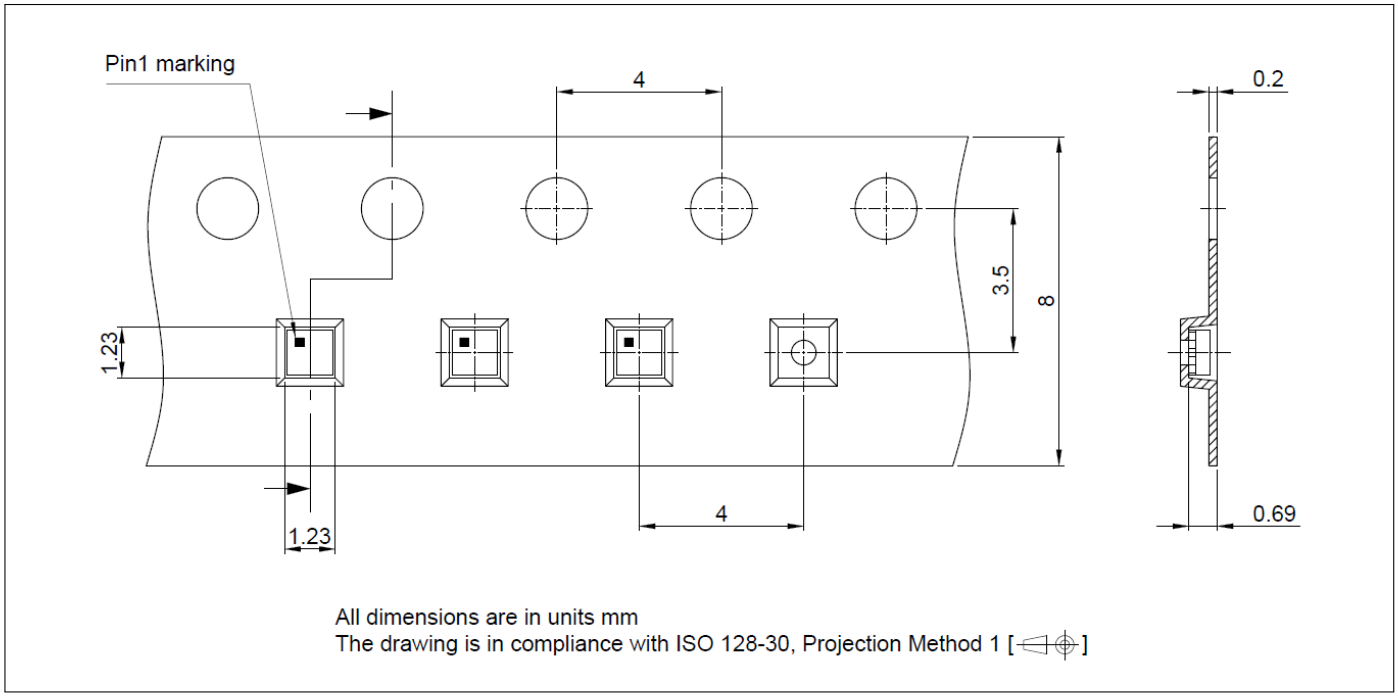


Figure 6: Carrier tape drawing (top and side views)

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.0, 2022-08-30	
Revision 2.0	Final Data Sheet Creation

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-08-30
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Doc_Number

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party. In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications. The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for RF Switch ICs ***category:***

Click to view products by Infineon ***manufacturer:***

Other Similar products are found below :

MASW-004100-11930W MASW-008853-TR3000 MASW6010G BGSX210MA18E6327XTSA1 CG2185X2 CG2415M6 MA4AGSW1A MA4SW410 MASW-002102-13580G MASW-005100-11940W BGS 12PL6 E6327 BGS1414MN20E6327XTSA1 BGS1515MN20E6327XTSA1 SKY13374-397LF CG2415M6-C2 AS222-92LF UPG2162T5N-E2-A MASWSS0201TR MASW-007075-000100 MASW-004103-13655P MASW-003102-13590G MASWSS0202TR-3000 MA4SW310B-1 MA4SW310 SW-313-PIN CG2430X1 SKY13405-490LF SKYA21001 SKY13415-485LF MMS008PP3 SKY13319-374LF SKY13404-466LF SKY13473-569LF SKY13626-685LF NJG1809ME7-TE1 SKY13343-92LF MASW-002103-13635P SKY13417-485LF MASW-003100-11920W MASW-004103-13650P NJG1649HB6 BGSA14GN10E6327 FM1694C XMSS1R6G0PA-001 AW13612FLR AW13102DNR FM3418C AW13508QNR AW13418RQNR FM8648M