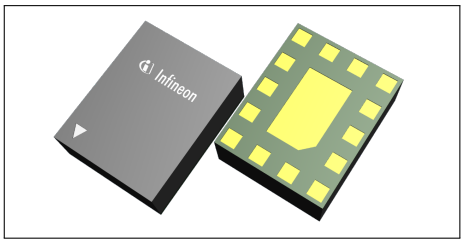
BGS15MU14

SP5T High Isolation Switch for Feedback Receive

Features

- High linearity up to 20 dBm input power
- Fast switching speed (180 ns).
- Low insertion loss and high port-to-port isolation up to 6.0 GHz
- Low current consumption
- MIPI RFFE 2.1 compliant control interface
- Ultra low profile leadless plastic package
- Small form factor 1.5mm x 1.9mm (MSL1, 260° C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



1.9 x 1.5 mm^2

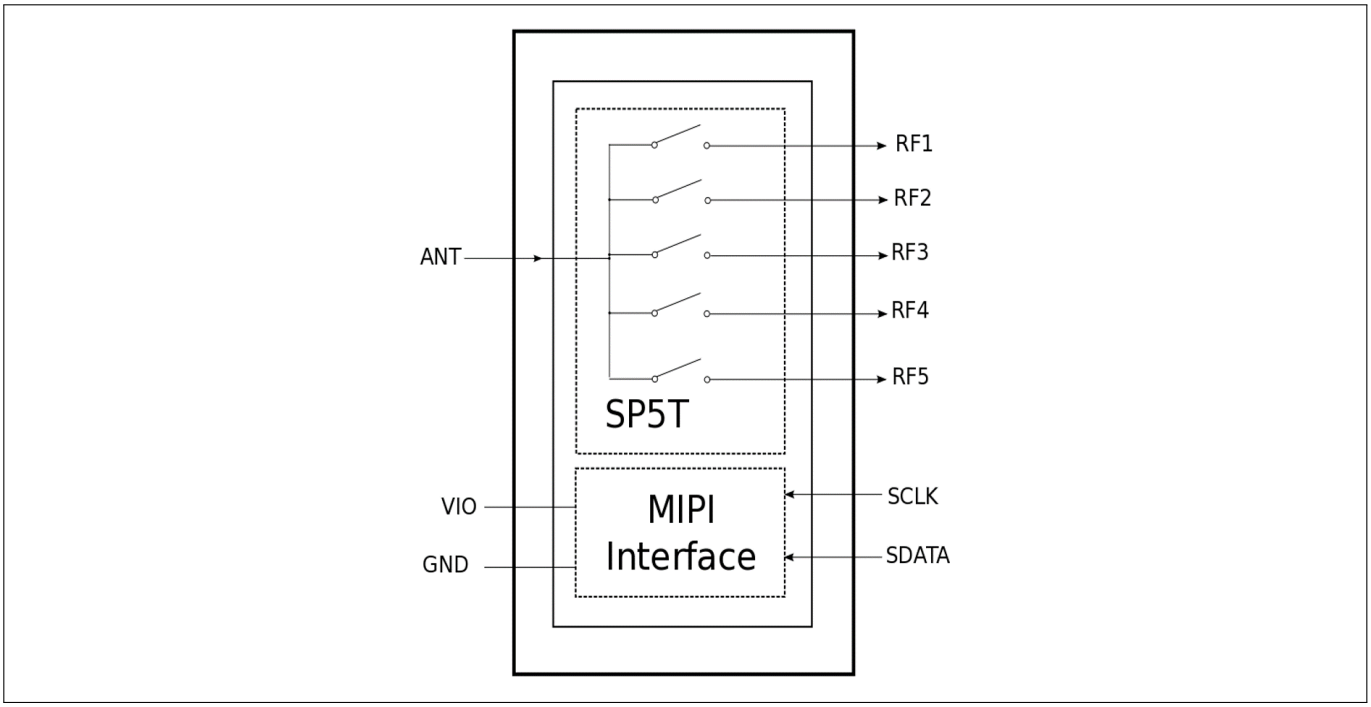
Potential Applications

Feedback receive signal routing from PA modules, high isolation general purpose Rx SP5T for LTE and 5G applicable up to 6GHz

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block Diagram



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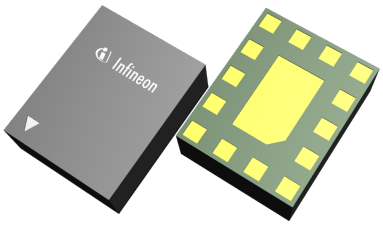
1 Features



- High linearity up to 20 dBm input power
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- Low insertion loss and high port-to-port isolation up to 6.0 GHz
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- MIPI RFFE 2.1 compliant control interface
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- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

2 Product Description

The BGS15MU14 RF CMOS switch is specifically designed for LTE and 5G feedback receive applications. It offers high isolation , low insertion loss and low harmonic generation up to 6 GHz.

It is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.65 to 1.95 V. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGS15MU14 RF Switch is manufactured using Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 1.9 x 1.5 mm^2 and a maximum thickness of 0.6 mm.

Table 1: Ordering Information

Type	Package	Marking	Ordering Information
BGS15MU14	PG-ULGA-14-1	K2	BGS15MU14 E6327

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range [1]	f	0.4	–	6.0	GHz	
Supply voltage	V_{IO}	-0.5	–	2.2	V	–
Max RF-input peak power	P_{RF}	–	–	23	dBm	CW; 50 Ohm
ESD robustness, CDM [2]	$V_{ESD,CDM}$	-0.5	–	+0.5	kV	
ESD robustness, HBM [3]	$V_{ESD,HBM}$	-1	–	+1	kV	
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
[2] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[4] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE control voltage levels	V_{SCLK}, V_{SDATA}, V_{SSEL}	-0.7	–	V_{IO} + 0.7 (max.2.5)	V	–

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{IO}	1.65	1.8	1.95	V	–
Supply current	I_{DD}	–	60	100	µA	Operating State, V_{IO} = 1.8 V
Supply current in standby mode	$I_{DD,sb}$	–	2	8.5	µA	Idle state, power down mode
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE supply current	I_{IO}	–	3	–	µA	–
Ambient temperature	T_A	-40	25	85	°C	–

[1)] SCLK and SDATA

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power	P_{RF}	–	–	20	dBm	CW; 50 Ohm

5 RF Characteristics

Table 6: RF Characteristics at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.8 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All RF Ports	*IL*	–	0.46	0.51	dB	400–698 MHz
		–	0.48	0.56	dB	699–960 MHz
		–	0.55	0.71	dB	1200–2170 MHz
		–	0.63	0.78	dB	2171–2690 MHz
		–	0.78	0.98	dB	3300–4200 MHz
		–	0.92	1.18	dB	4400–5000 MHz
		–	1.05	1.39	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 7: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All RF Ports	*IL*	–	0.46	0.62	dB	400–698 MHz
		–	0.48	0.71	dB	699–960 MHz
		–	0.55	0.81	dB	1200–2170 MHz
		–	0.63	0.86	dB	2171–2690 MHz
		–	0.78	1.10	dB	3300–4200 MHz
		–	0.92	1.35	dB	4400–5000 MHz
		–	1.05	1.57	dB	5150–5925 MHz
Return Loss[1]						
All RF Ports	*RL*	23	26	–	dB	400–698 MHz
		21	27	–	dB	699–960 MHz
		16	22	–	dB	1200–2170 MHz
		14	18	–	dB	2171–2690 MHz
		11	15	–	dB	3300–4200 MHz
		9	13	–	dB	4400–5000 MHz
		8	12	–	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 8: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation[1]						
ANT_RF1 vs RFx	*ISO*	64	66	–	dB	400–698 MHz
		60	63	–	dB	699–960 MHz
		55	57	–	dB	1200–2170 MHz
		54	55	–	dB	2171–2690 MHz
		51	55	–	dB	3300–4200 MHz
		49	55	–	dB	4400–5000 MHz
		46	51	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF2 vs RFx	*ISO*	66	70	–	dB	400–698 MHz
		62	67	–	dB	699–960 MHz
		56	61	–	dB	1200–2170 MHz
		55	59	–	dB	2171–2690 MHz
		52	58	–	dB	3300–4200 MHz
		51	58	–	dB	4400–5000 MHz
		48	56	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF3 vs RFx	*ISO*	64	68	–	dB	400–698 MHz
		60	65	–	dB	699–960 MHz
		53	59	–	dB	1200–2170 MHz
		52	56	–	dB	2171–2690 MHz
		50	55	–	dB	3300–4200 MHz
		49	55	–	dB	4400–5000 MHz
		47	56	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF4 vs RFx	*ISO*	63	66	–	dB	400–698 MHz
		58	62	–	dB	699–960 MHz
		52	57	–	dB	1200–2170 MHz
		50	54	–	dB	2171–2690 MHz
		48	52	–	dB	3300–4200 MHz
		47	51	–	dB	4400–5000 MHz
		46	51	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF5 vs RFx	*ISO*	63	65	–	dB	400–698 MHz
		59	62	–	dB	699–960 MHz
		53	56	–	dB	1200–2170 MHz
		52	54	–	dB	2171–2690 MHz
		48	52	–	dB	3300–4200 MHz
		46	51	–	dB	4400–5000 MHz
		42	48	–	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

RF Characteristics

Table 9: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation[1]						
Port to Port	*ISO*	62	67	–	dB	400–698 MHz
		58	64	–	dB	699–960 MHz
		51	58	–	dB	1200–2170 MHz
		50	55	–	dB	2171–2690 MHz
		47	54	–	dB	3300–4200 MHz
		45	54	–	dB	4400–5000 MHz
		41	52	–	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 10: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation[1] at VSWR 1:1, 12.5 % duty cycle, Pin +10 dBm						
2nd Harmonic distortions	H2	–	-101	-97	dBm	600 - 915 MHz
		–	-100	-95	dBm	1980 - 2170 MHz
		–	-100	-95	dBm	2300 - 2690 MHz
		–	-101	-95	dBm	3300 - 4200MHz
		–	-101	-97	dBm	4400 - 5000MHz
		–	-99[2]	-92[2]	dBm	5150 - 5925MHz
3rd Harmonic distortions	H3	–	-100	-97	dBm	600 - 915 MHz
		–	-98	-94	dBm	1980 - 2170 MHz
		–	-98	-96	dBm	2300 - 2690 MHz
		–	-97	-93	dBm	3300 - 4200MHz
		–	-96	-94	dBm	4400 - 5000MHz
		–	-96	-89	dBm	5150 - 5925MHz
Intermodulation Distortion[1]						
2nd intermodulation products	IMD2	–	-119	-115	dBm	B1 OOB Blocking at 2140M Interferer1: +10 dBm @ 1950 MHz Interferer2: -10 dBm @4090 MHz
		–	-120	-116	dBm	B7 OOB Blocking at 2655 MHz Interferer1: +10 dBm @ 2535 MHz Interferer2: -10 dBm @ 5190 MHz
3rd intermodulation products	IMD3	–	-121	-117	dBm	B1 OOB Blocking at 2140 MHz Interferer1: +10 dBm @ 1950 MHz Interferer2: -10 dBm @ 1760 MHz

[1] On EVB without any matching components.
[2] RF2 Port excluded.(When RF2 Port included: typ. 96 dBm, Max. 75 dBm)

Table 11: IMD2 Testcases

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	10	4090	-10
Band 2	1960	1880	10	3840	-10
Band 5	881.5	836.5	10	1718	-10
Band 7	2655	2535	10	5190	-10
Band 8	942	897	10	1839	-10

Table 12: IMD3 Testcases

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	10	1760	-10
Band 2	1960	1880	10	1800	-10
Band 5	881.5	836.5	10	791.5	-10
Band 7	2655	2535	10	2415	-10
Band 8	942	897	10	852	-10
Band 1	2132	1732	10	1332	-10

Table 13: Switching Time at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
Power Up Settling Time	T_{pup}	–	6	8	µs	Time from Power Up plus Switch command, 50 % last SCLK falling edge to 90 % RF signal
RF Switching Time ON	$T_{st,on}$	–	180	210	ns	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal
RF Switching Time OFF	$T_{st,off}$	–	45	55	ns	Time to switch between RF states, 50 % last SCLK falling edge to minimum 20dB isolation between ANT and switched RF port

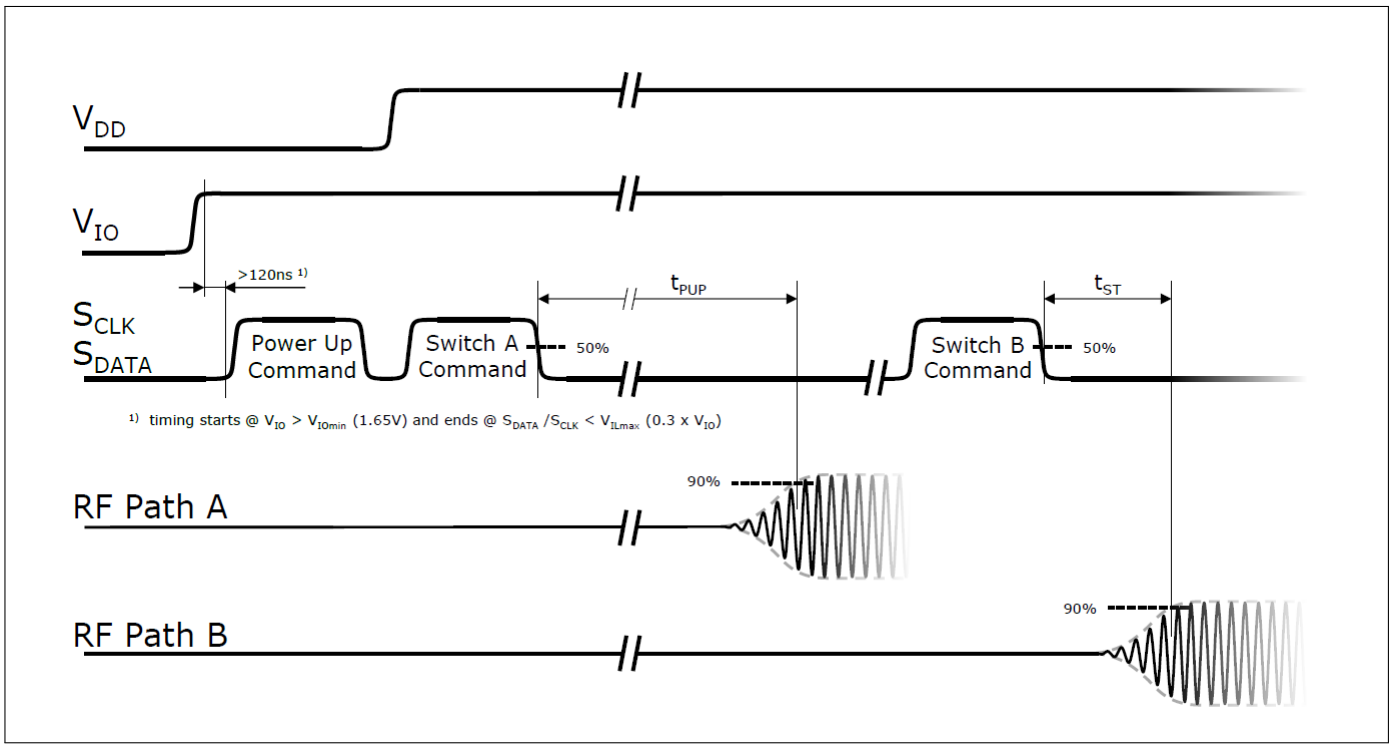

Figure 1: MIPI Timing Diagram

6 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017' as well as the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. W'.

Table 14: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as Mask Write
Support for standard frequency range operations for SCLK	Yes	SCLK range 32 kHz to 26 MHz for read and write commands
Support for extended frequency range operations for SCLK	Yes	SCLK range 26 MHz to 52 MHz for write commands
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	No	
USID selection via SDATA / SCLK swap feature	No	

Table 15: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 16: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	SW_CTRL0	7:5	RESERVED	Reserved for future use				
		4	SW_CTRL_RF5	0: RF5 off	0	No	Yes	R/W, Mask Write
				1: RF5 on				
		3	SW_CTRL_RF4	0: RF4 off	0			
				1: RF4 on				
		2	SW_CTRL_RF3	0: RF3 off	0			
				1: RF3 on				
		1	SW_CTRL_RF2	0: RF2 off	0			
				1: RF2 on				
		0	SW_CTRL_RF1	0: RF1 off	0			
				1: RF1 on				
0x1A	RFFE_STATUS	7	SOFTWARE RESET	0: Normal operation	0	No	No	R
				1: Software reset (reset of all configuration registers to default values except for USID, GSID and PM_TRIG)				
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x1B	GROUP_SID	7:4	RESERVED	RESERVED	0x0	No	No	R/W
		3:0	GROUP_SID[3:0]	Group slave ID	0x0			

Table 17: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x1C	PM_TRIG	7	PWR_MODE[1], Operation Mode	Defines normal ACTIVE operation and LOW POWER mode. 0: Normal operation (ACTIVE). 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W, Mask Write
		6	PWR_MODE[0], State Bit Vector	Single bit Powered Reset.0: No action (ACTIVE). 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	Trigger Mask 2. 0: Data writes to registers tied to TRIGGER_2 are masked. 1: Data writes to registers tied to TRIGGER_2 are not masked.	0	No		
		4	TRIGGER_MASK_1	Trigger Mask 1. 0: Data writes to registers tied to TRIGGER_1 are masked. 1: Data writes to registers tied to TRIGGER_1 are not masked.	0			
		3	TRIGGER_MASK_0	Trigger Mask 0. 0: Data writes to registers tied to TRIGGER_0 are masked. 1: Data writes to registers tied to TRIGGER_0 are not masked.	0			
		2	TRIGGER_2	Trigger 2. This bit has no effect if TRIGGER_MASK_2 is 1. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_2.	0	Yes		
		1	TRIGGER_1	Trigger 1. This bit has no effect if TRIGGER_MASK_1 is 1. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_1.	0			
		0	TRIGGER_0	Trigger 0. This bit has no effect if TRIGGER_MASK_0 is 1. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for registers tied to TRIGGER_0.	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID[7:0]	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	0xCE	No	No	R
0x1E	MANUFACTURER_ID	7:0	MANUFACTURER_ID[7:0]	Manufacturer ID.	0x1A	No	No	R
0x1F	MAN_USID	7:6	MANUFACTURER_ID[11:10]	Manufacturer ID.	00	No	No	R
		5:4	MANUFACTURER_ID[9:8]	Manufacturer ID.	01			
		3:0	USID[3:0]	These bits store the USID of the device.	0xA	No	No	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D.	0x00	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip Main Revision	0x0	No	No	R
		3:0	SUB_REVISION	Chip Sub Revision	0x1			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0x0	No	No	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0x0			
0x23	UDR_RST	7	UDR_RST	0: Normal Operation, 1: Software Reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use. Set to all 0.	0000 000			

Table 18: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x24	EPR_SUM	7	RESERVED	Reserved for future error codes.	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:4	RESERVED	RESERVED	0x0	No	No	R/W
		3:0	BUS_LD[3:0]	Set approximate bus load 0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 70 pF 0x7: 80 pF 0x8-0xF: Spare	0x04			
0x2C	TEST_PATT	7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Table 19: Register Mapping, Table IV

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2D	EXT_TRIGGER_MASK	7	EXT_TRIGGER_MASK_10	Extended Trigger Mask 10 0: Data writes to registers tied to EXT_TRIGGER_10 are masked. 1: Data writes to registers tied to EXT_TRIGGER_10 are not masked.	1	No	No	R/W, mask write
		6	EXT_TRIGGER_MASK_9	Extended Trigger Mask 9 0: Data writes to registers tied to EXT_TRIGGER_9 are masked. 1: Data writes to registers tied to EXT_TRIGGER_9 are not masked.	1			
		5	EXT_TRIGGER_MASK_8	Extended Trigger Mask 8 0: Data writes to registers tied to EXT_TRIGGER_8 are masked. 1: Data writes to registers tied to EXT_TRIGGER_8 are not masked.	1			
		4	EXT_TRIGGER_MASK_7	Extended Trigger Mask 7 0: Data writes to registers tied to EXT_TRIGGER_7 are masked. 1: Data writes to registers tied to EXT_TRIGGER_7 are not masked.	1			
		3	EXT_TRIGGER_MASK_6	Extended Trigger Mask 6 0: Data writes to registers tied to EXT_TRIGGER_6 are masked. 1: Data writes to registers tied to EXT_TRIGGER_6 are not masked.	1			
		2	EXT_TRIGGER_MASK_5	Extended Trigger Mask 5 0: Data writes to registers tied to EXT_TRIGGER_5 are masked. 1: Data writes to registers tied to EXT_TRIGGER_5 are not masked.	1			
		1	EXT_TRIGGER_MASK_4	Extended Trigger Mask 4 0: Data writes to registers tied to EXT_TRIGGER_4 are masked. 1: Data writes to registers tied to EXT_TRIGGER_4 are not masked.	1			
		0	EXT_TRIGGER_MASK_3	Extended Trigger Mask 3 0: Data writes to registers tied to EXT_TRIGGER_3 are masked. 1: Data writes to registers tied to EXT_TRIGGER_3 are not masked.	1			

Table 20: Register Mapping, Table V

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIGGER	7	EXT_TRIGGER_10	Extended Trigger 10. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_10	0	No	No	R/W, mask write
		6	EXT_TRIGGER_9	Extended Trigger 9. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_9	0			
		5	EXT_TRIGGER_8	Extended Trigger 8. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_8	0			
		4	EXT_TRIGGER_7	Extended Trigger 7. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_7	0			
		3	EXT_TRIGGER_6	Extended Trigger 6. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_6	0			
		2	EXT_TRIGGER_5	Extended Trigger 5. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_5	0			
		1	EXT_TRIGGER_4	Extended Trigger 4. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_4	0			
		0	EXT_TRIGGER_3	Extended Trigger 4. 0: No action. Data is held in shadow registers. 1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_3	0			
0x78	TEST_REG0	7	RESERVED	RESERVED	0	No	No	R/W
		6	RESERVED	RESERVED	0			
		5	RESERVED	RESERVED	0			
		4	RESERVED	RESERVED	0			
		3	RESERVED	RESERVED	0			
		2	EN_DIRECT_MAPPING	Enables the direct mapping functionality for testing-purposes.	0			
		1	EN_DIGITAL_TEST	Enables the loopback-test functionality. Deactivates the switch-control!	0			
		0	RESERVED	RESERVED	0			

Table 21: Modes of Operation (Truth Table)

		Register Bits							
State	**Mode**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
1	Isolation	x	x	x	0	0	0	0	0
2	RF5 on	x	x	x	1	0	0	0	0
3	RF4 on	x	x	x	0	1	0	0	0
4	RF3 on	x	x	x	0	0	1	0	0
5	RF2 on	x	x	x	0	0	0	1	0
6	RF1 on	x	x	x	0	0	0	0	1

7 Package Information

The switch has a package size of 1900 µm in X-dimension and 1500 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The pin definitions are listed in Tab. 23.

Table 22: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-dimension	*X*	1900 ± 50	µm
Package Y-dimension	*Y*	1500 ± 50	µm
Package height	*H*	600 ± 50	µm

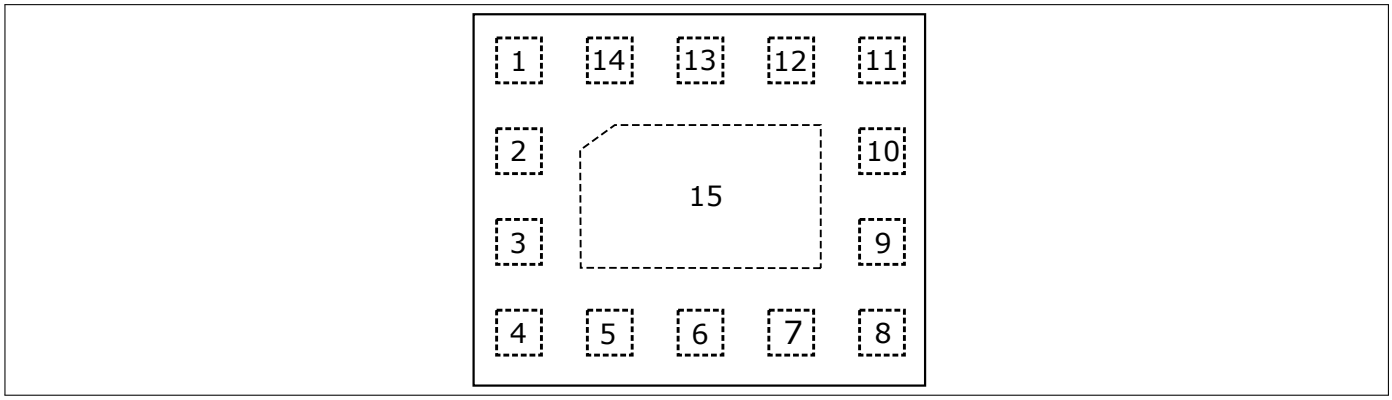

Figure 2: Pin Configuration (top view)

Table 23: Pin Definition and Function

Pin No.	Name	Function
1	RF1	RF input port 1
2	GND	RF ground
3	RF2	RF output port 2
4	SDATA	MIPI RFFE data
5	SCLK	MIPI RFFE clock
6	VIO	MIPI RFFE power supply
7	RF3	RF output port 3
8	GND	RF ground
9	RF4	RF output port 4
10	GND	RF ground
11	RF5	RF output port 5
12	GND	RF ground
13	ANT	Antenna
14	GND	RF ground
15	GND	RF ground

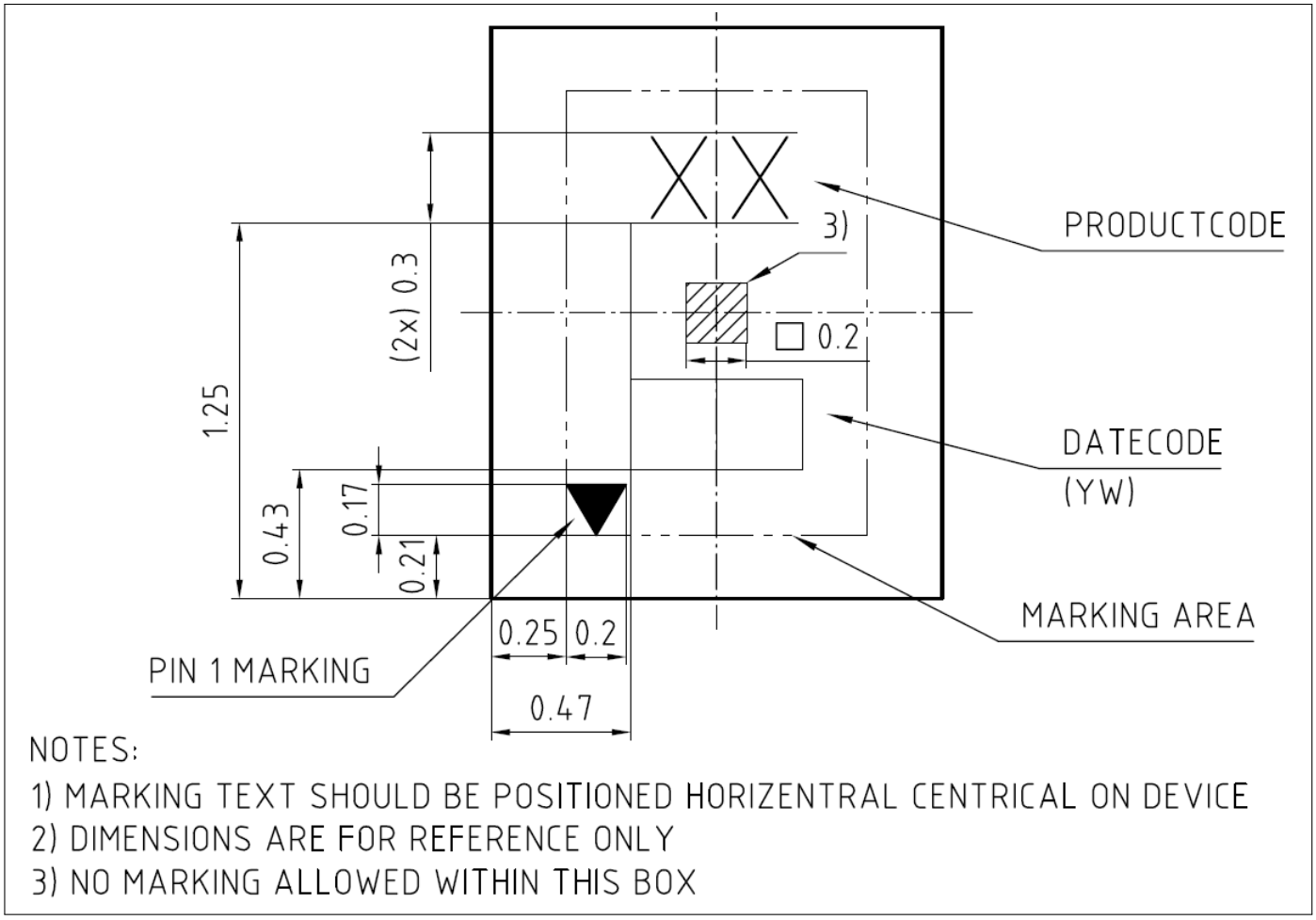

Figure 3: Marking Specification (top view)

Table 24: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

Table 25: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

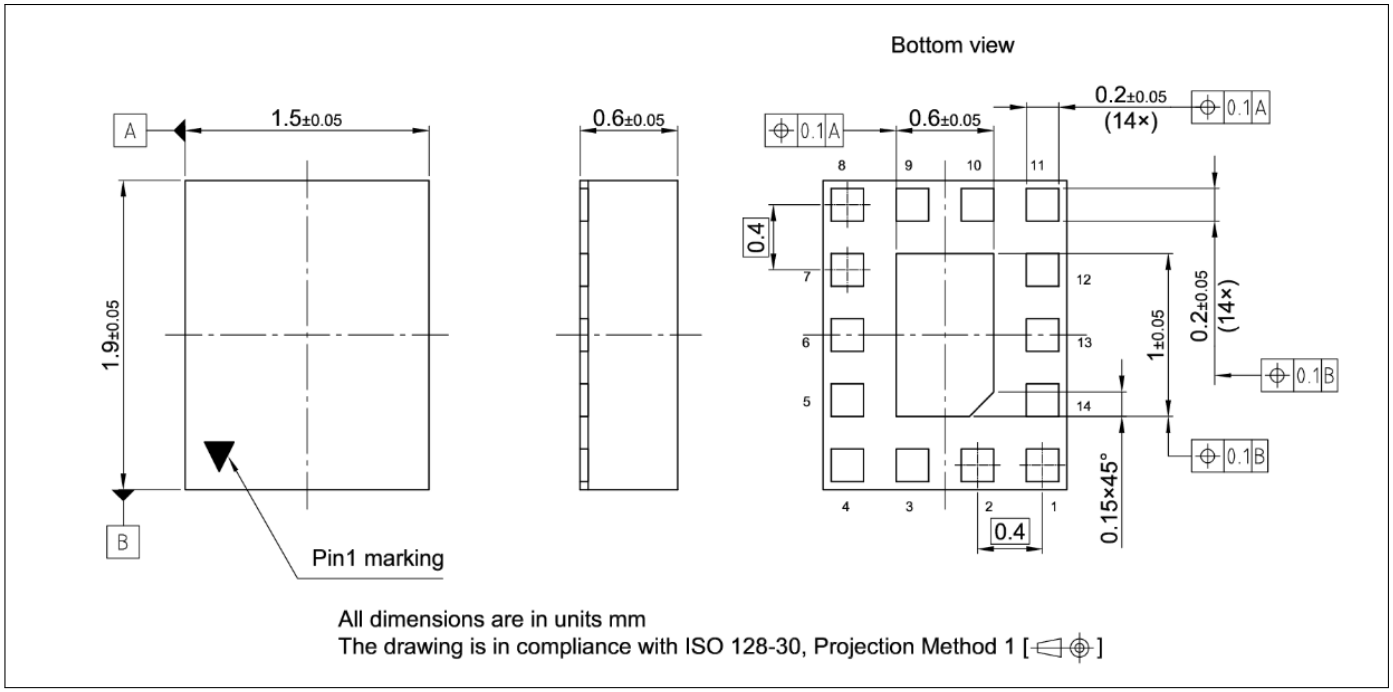

Figure 4: Package Outline Drawing (top, side and bottom views)

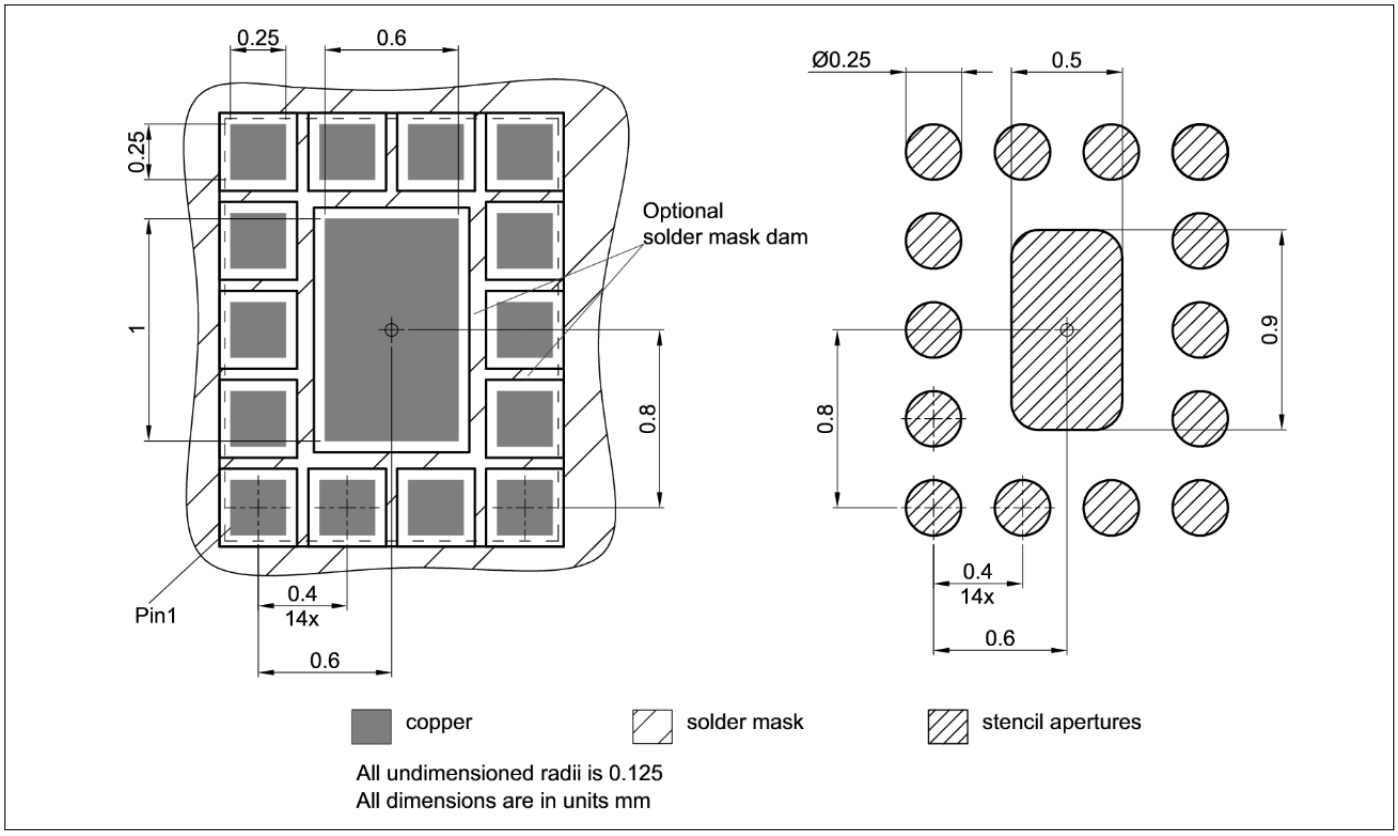

Figure 5: Footprint Recommendation

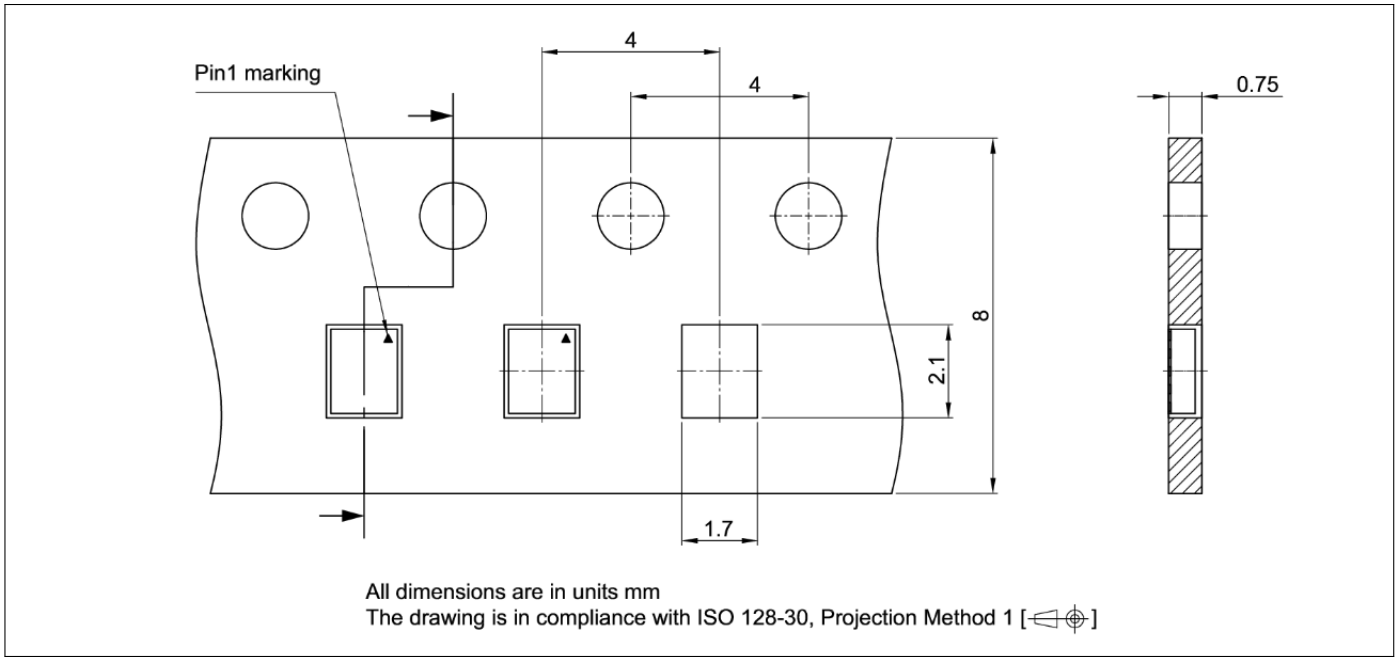

Figure 6: Carrier Tape Drawing (top and side views)

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
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All	"Preliminary" status removed, general update to final version

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