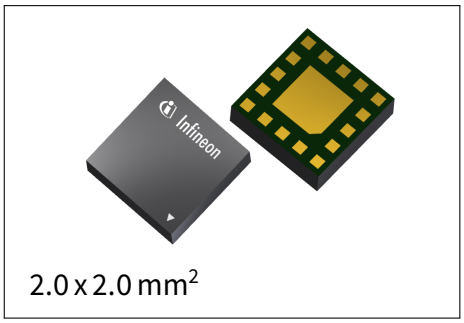
BGSX33MU16

3P3T Antenna Cross Switch with MIPI RFFE Control Interface

Features

- High linearity up to 36.5 dBm input power
- Low insertion loss and high port to port isolation up to 3.8 GHz
- Ultra high input intermodulation products
- Low current consumption
- MIPI RFFE 2.0 compliant control interface
- Software and hardware programmable USID
- RoHS and WEEE compliant package



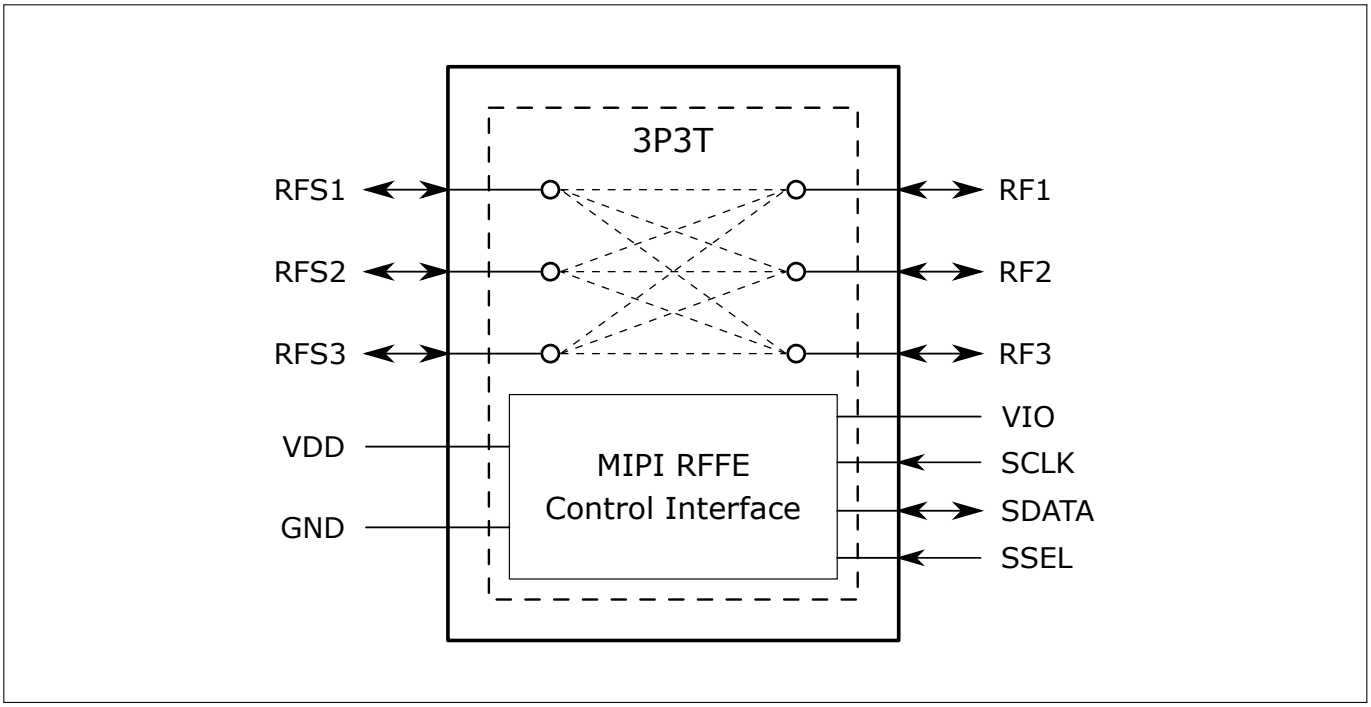
Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential Applications

Triple antenna routing/swapping for cellular mobile devices. GSM/WCDMA/LTE post PA power level routing switch.

Block Diagram



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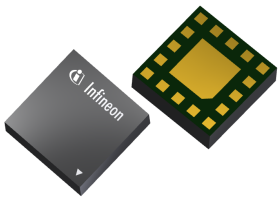
1 Features



- RF CMOS 3P3T antenna cross switch with power handling capability of up to 36.5 dBm
- Suitable for multi-mode LTE and WCDMA triple antenna applications
- Low insertion loss and harmonics generation
- 0.1 to 3.8 GHz coverage
- High port to port isolation
- No blocking capacitors required if no DC applied on RF lines
- Fully compatible with MIPI RFFE 2.0 standard operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Leadless and halogen free package PG-ULGA-16-3 with lateral size of 2.0 mm x 2.0 mm and thickness of 0.6 mm
- No power supply decoupling required
- High EMI robustness
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

2 Product Description

BGSX33MU16 is a Triple Pole Triple Throw (3P3T) RF switch which is specifically designed for LTE and WCDMA triple antenna applications in a compact package with very small size of only 2.0 x 2.0 mm^2 and thickness of 0.6 mm. This 3P3T offers low insertion loss and low harmonic generation.

The switch is controlled via a MIPI RFFE control interface. The on-chip controller allows power-supply voltages from 1.65 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGSX33MU16 RF switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness.

Table 1: Ordering Information

Type	Package	Marking
BGSX33MU16	PG-ULGA-16-3	33

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range [1]	f	0.1	–	3.8	GHz	
Supply voltage	V_{DD}	-0.5	–	3.6	V	–
RF input power at RFS/RF ports	P_{RF}	–	–	38.5	dBm	VSWR = 1:1
		–	–	36	dBm	VSWR = 6:1
		–	–	34	dBm	VSWR = 10:1
ESD capability, CDM [2]	$V_{ESD,CDM}$	-1	–	+1	kV	
ESD capability, HBM [3]	$V_{ESD,HBM}$	-1	–	+1	kV	
ESD capability RF ports, SLT[4]	$V_{ESD,RF}$	-8	–	+8	kV	RF versus GND, with 27 nH shunt inductor
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
[2] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[4] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	–	55	K/W	–
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE supply voltage	V_{IO}	-0.5	–	2.2	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}, V_{SSEL}	-0.7	–	V_{IO} + 0.7 (max. 2.2)	V	–

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.65	–	3.4	V	–
Supply current	I_{DD}	–	80	250	µA	Operating State
Supply current in standby mode	$I_{DD,sb}$	–	0.5	1	µA	VIO = low or MIPI low-power mode
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{IO}	–	2	10	µA	Idle State
Ambient temperature	T_A	-40	25	85	°C	–

[1)] SCLK, SDATA, and SSEL

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power	P_{RF}	–	–	36.5	dBm	VSWR = 1:1
		–	–	33	dBm	VSWR = 6:1
		–	–	32.5	dBm	VSWR = 10:1

5 RF Characteristics

Table 6: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1] at 25°C						
All RFS/RF ports	*IL*	–	0.35	0.45	dB	699–960 MHz
		–	0.45	0.60	dB	1710–2200 MHz
		–	0.50	0.70	dB	2300–2690 MHz
		–	0.80	1.20	dB	3400–3800 MHz
Insertion Loss[1]						
All RFS/RF ports	*IL*	–	0.35	0.55	dB	699–960 MHz
		–	0.45	0.75	dB	1710–2200 MHz
		–	0.50	0.90	dB	2300–2690 MHz
		–	0.80	1.50	dB	3400–3800 MHz
Return Loss[1]						
All RFS/RF ports	*RL*	21	30	–	dB	699–960 MHz
		16	24	–	dB	1710–2200 MHz
		14	21	–	dB	2300–2690 MHz
		8	13	–	dB	3400–3800 MHz
Isolation On-On[1]						
RFS-on to RF-on ports	*ISO*	40	48	–	dB	699–960 MHz
		33	41	–	dB	1710–2200 MHz
		31	39	–	dB	2300–2690 MHz
		30	37	–	dB	3400–3800 MHz
RFS-on to RFS-on ports	*ISO*	35	42	–	dB	699–960 MHz
		30	37	–	dB	1710–2200 MHz
		28	35	–	dB	2300–2690 MHz
		27	33	–	dB	3400–3800 MHz
RF-on to RF-on ports	*ISO*	35	42	–	dB	699–960 MHz
		30	37	–	dB	1710–2200 MHz
		28	35	–	dB	2300–2690 MHz
		27	33	–	dB	3400–3800 MHz
Isolation On-Off[1]						
RFS-on to RF-off ports	*ISO*	40	48	–	dB	699–960 MHz
		34	42	–	dB	1710–2200 MHz
		33	40	–	dB	2300–2690 MHz
		32	39	–	dB	3400–3800 MHz
RFS-on to RFS-off ports	*ISO*	39	46	–	dB	699–960 MHz
		32	39	–	dB	1710–2200 MHz
		31	37	–	dB	2300–2690 MHz
		28	34	–	dB	3400–3800 MHz
RF-on to RF-off ports	*ISO*	39	48	–	dB	699–960 MHz
		33	41	–	dB	1710–2200 MHz
		32	39	–	dB	2300–2690 MHz
		31	37	–	dB	3400–3800 MHz

[1] Measured on application board, without any matching components.

Table 7: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation[1] at P_{RF} = 25 dBm, CW, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-90	-80	dBm	600–915 MHz
		–	-80	-72	dBm	1447–1980 MHz
		–	-80	-72	dBm	2300–2690 MHz
3rd Harmonic	P_{H3}	–	-85	-80	dBm	600–915 MHz
		–	-80	-72	dBm	1447–1980 MHz
		–	-80	-72	dBm	2300–2690 MHz
Harmonic Generation[1] at 50 % duty cycle, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-67	-57	dBm	GSM LB, 36 dBm
		–	-63	-55	dBm	GSM HB, 33 dBm
3rd Harmonic	P_{H3}	–	-52	-46	dBm	GSM LB, 36 dBm
		–	-54	-49	dBm	GSM HB, 33 dBm
Intermodulation Distortion IMD2[1]						
IIP2, low	*IIP2*	105	125	–	dBm	IIP2 conditions, see Tab. 9
IIP2, high		105	125	–	dBm	
Intermodulation Distortion IMD3[1]						
IIP3	*IIP3*	70	80	–	dBm	IIP3 conditions, see Tab. 10

[1] Measured on application board, without any matching components.

Table 8: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, V_{DD}= 1.65 V...3.4 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time[1]						
Power Up Settling Time	t_{PUP}	–	10	25	µs	Time from Power Up plus Switch command, 50 % last SCLK falling edge to 90 % RF signal
Switching Time	t_{ST}	–	2	3	µs	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal

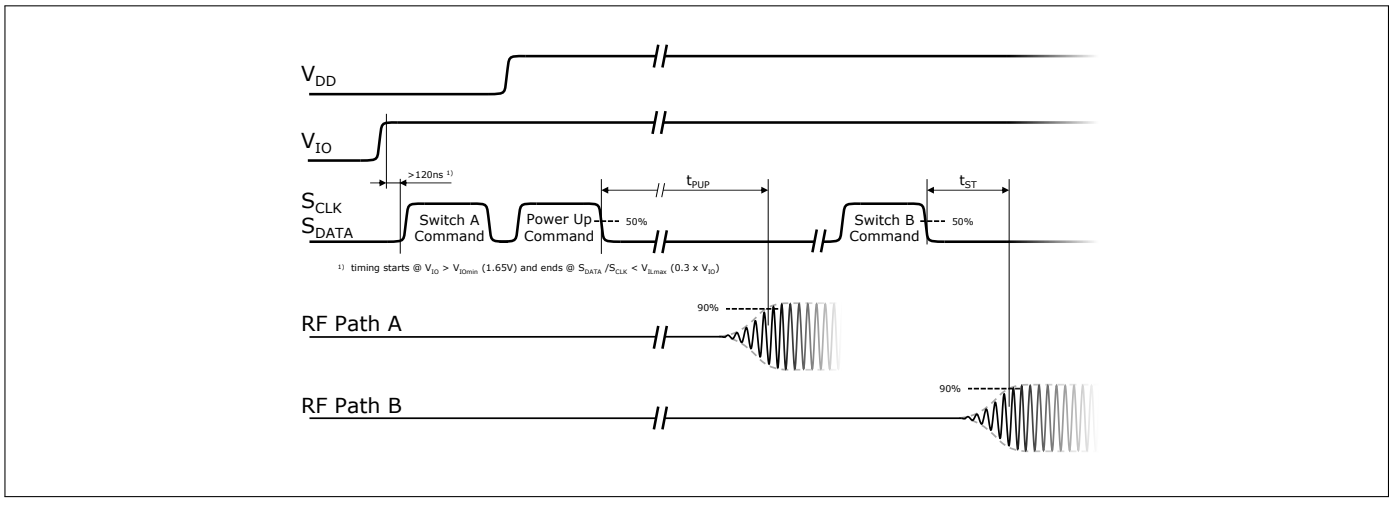


Figure 1: MIPI Timing Diagram

Table 9: IMD2 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD2,high}$	2140	1950	24	4090	-10
	$B1_{IMD2,low}$	2140	1950	24	190	-10
Band 4	$B4_{IMD2,high}$	2132	1732	24	3864	-10
	$B4_{IMD2,low}$	2132	1732	24	400	-10
Band 5	$B5_{IMD2,high}$	881.5	836.5	24	1718	-15
	$B5_{IMD2,low}$	881.5	836.5	24	45	-15
Band 7	$B7_{IMD2,high}$	2655	2535	24	5190	-10
	$B7_{IMD2,low}$	2655	2535	24	120	-10

Table 10: IMD3 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,high}$	2140	1950	24	6040	-10
	$B1_{IMD3,mid}$	2140	1950	24	1760	-10
Band 4	$B4_{IMD3,high}$	2132	1732	24	5596	-10
	$B4_{IMD3,mid}$	2132	1732	24	1332	-10
Band 5	$B5_{IMD3,high}$	881.5	836.5	24	2554.5	-10
	$B5_{IMD3,mid}$	881.5	836.5	24	791.5	-10
Band 7	$B7_{IMD3,high}$	2655	2535	24	7725	-10
	$B7_{IMD3,mid}$	2655	2535	24	2415	-10

6 MIPI RFFE Specification

The MIPI RFFE interface is working in systems following the 'MIPI Alliance Specification for RF Front-End Control Interface version 2.0 - 25. September 2014' as well as the 'Qualcomm RFFE Vendor specification 80-N7876-1 Rev. T'.

Table 11: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.0 standard	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	External pin for changing USID: SSEL = 0 → 1011 SSEL = 1 → 1010
USID selection via SDATA / SCLK swap feature	No	

Table 12: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 13: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x01	REGISTER_1	7:0	MODE_CTRL	Switch control	00000000	No	Yes	R/W
0x1C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	11100101	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 11	No	No	R/W

Table 14: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0001	No	No	R/W
		3:0	SUB_REVISION		0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

Table 15: Modes of Operation (Truth Table)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	RFS1-GND	x	x	x	x	x	0	0	0
2	RFS1-RF1	x	x	x	x	x	0	0	1
3	RFS1-RF2	x	x	x	x	x	0	1	0
4	RFS1-RF3	x	x	x	x	x	0	1	1
5	RFS1-OPEN	x	x	x	x	x	1	x	x
6	RFS2-GND	x	x	0	0	0	x	x	x
7	RFS2-RF1	x	x	0	0	1	x	x	x
8	RFS2-RF2	x	x	0	1	0	x	x	x
9	RFS2-RF3	x	x	0	1	1	x	x	x
10	RFS2-OPEN	x	x	1	x	x	x	x	x
		REGISTER_1 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
11	RFS3-GND	x	x	x	x	x	0	0	0
12	RFS3-RF1	x	x	x	x	x	0	0	1
13	RFS3-RF2	x	x	x	x	x	0	1	0
14	RFS3-RF3	x	x	x	x	x	0	1	1
15	RFS3-OPEN	x	x	x	x	x	1	x	x

BGSX33MA16 features a truth table which allows to connect multiple RFS ports to any RF port by combining individual states. As an example, all RFS ports can be connected to RF1 by combining states 2, 7, and 12 by following register settings: Register_0 = ’xx001001’ and Register_1 = ’xxxxx001’.

7 Package Information

The switch has a package size of 2000 µm in X-dimension and 2000 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The pin definitions are listed in Tab. 17.

Table 16: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-dimension	*X*	2000 ± 50	µm
Package Y-dimension	*Y*	2000 ± 50	µm
Package height	*H*	600 ± 50	µm

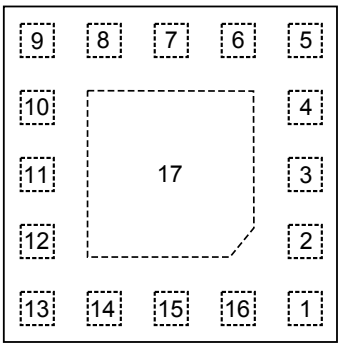


Figure 2: Footprint (top view)

Table 17: Pin Definition and Function

Pin No.	Name	Function
1	SSEL	MIPI USID select port (to be connected to VIO or GND)
2	RF1	RF port 1
3	GND	RF ground
4	RF2	RF port 2
5	GND	RF ground
6	RF3	RF port 3
7	GND	RF ground
8	RFS3	RFS port 3 - with internal shunt switch to GND
9	GND	RF ground
10	RFS2	RFS port 2 - with internal shunt switch to GND
11	GND	RF ground
12	RFS1	RFS port 1 - with internal shunt switch to GND
13	VDD	Power supply
14	VIO	MIPI RFFE power supply
15	SDATA	MIPI RFFE data
16	SCLK	MIPI RFFE clock
17	GND	RF ground

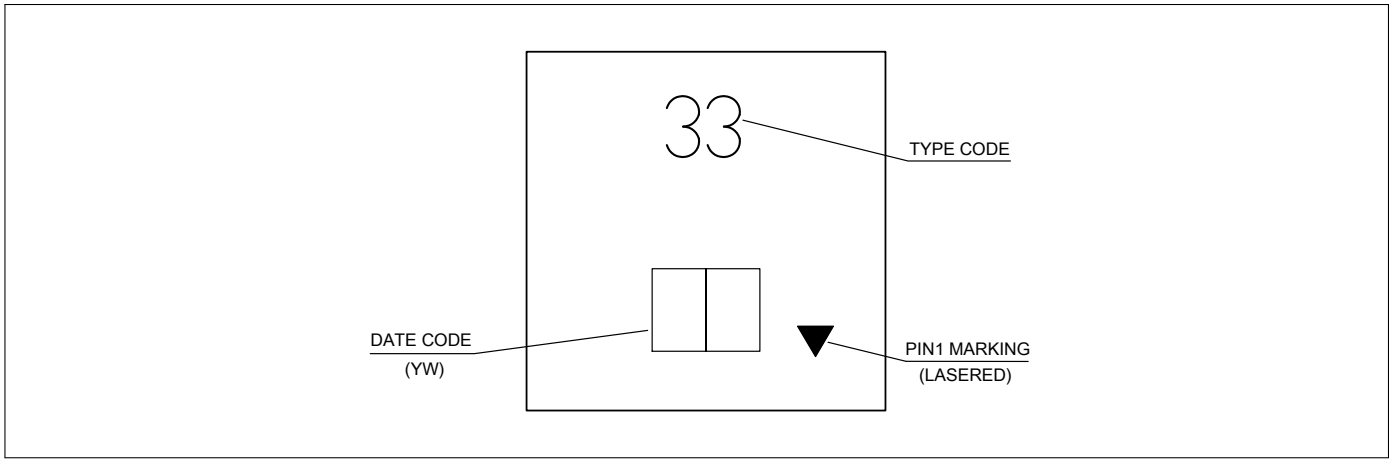


Figure 3: Marking Specification (top view)

Table 18: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

Table 19: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

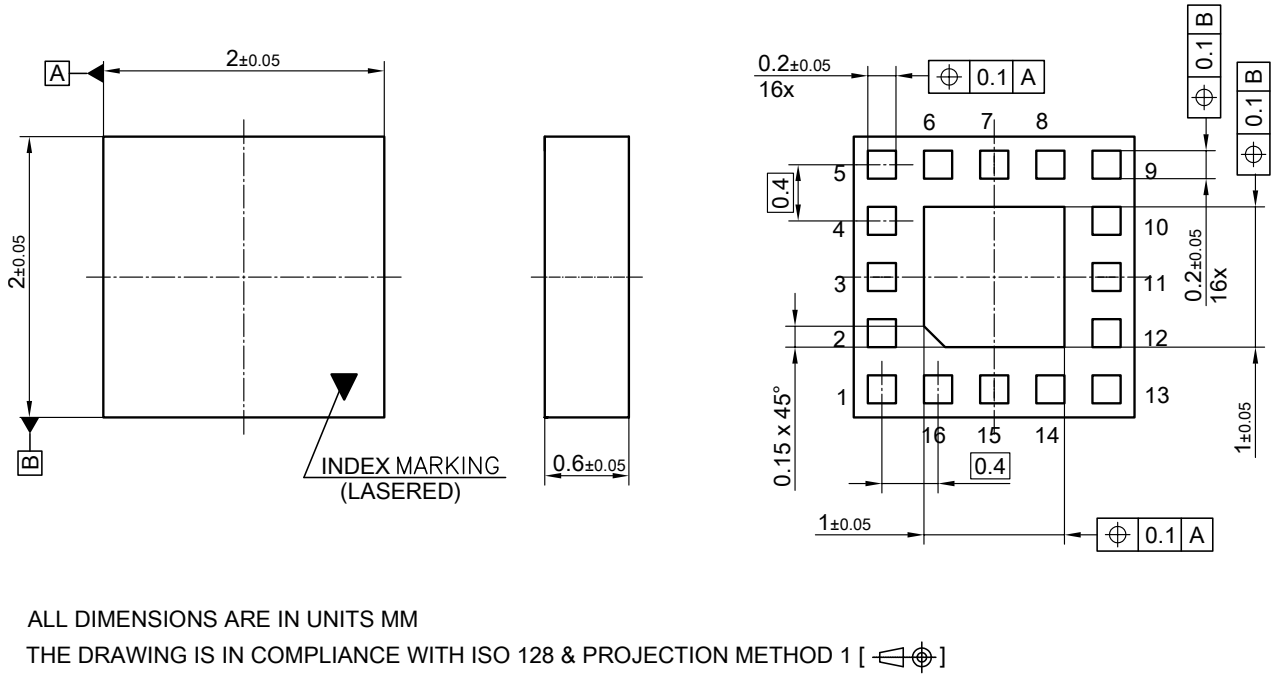


Figure 4: Package Outline Drawing (top, side and bottom views)

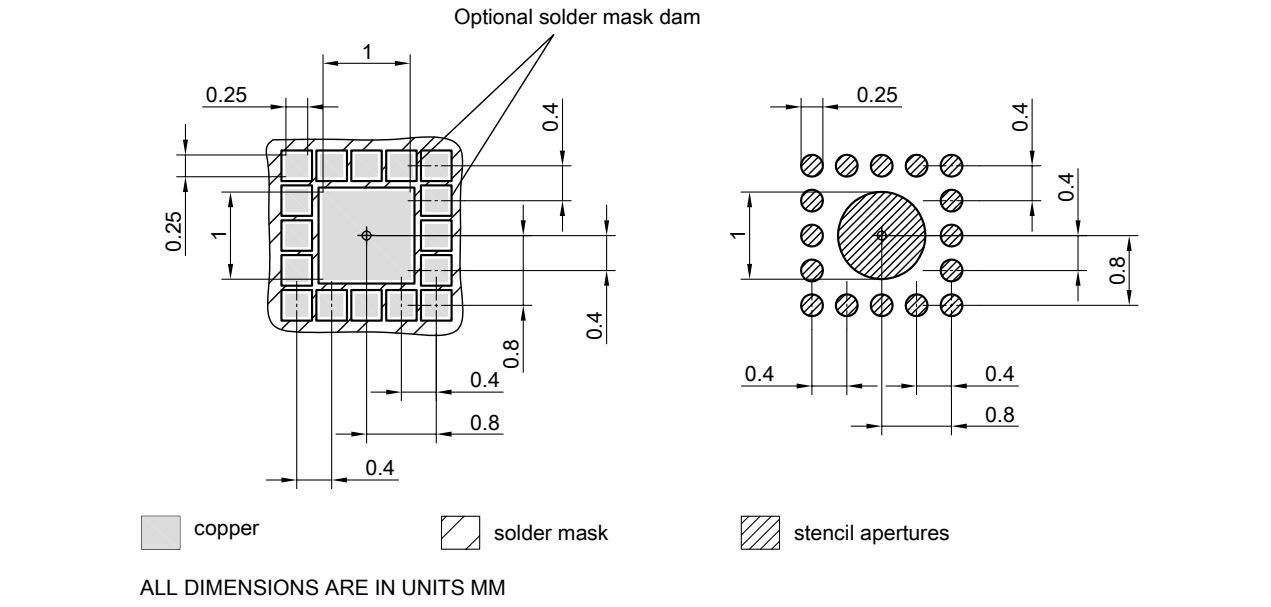


Figure 5: Footprint Recommendation

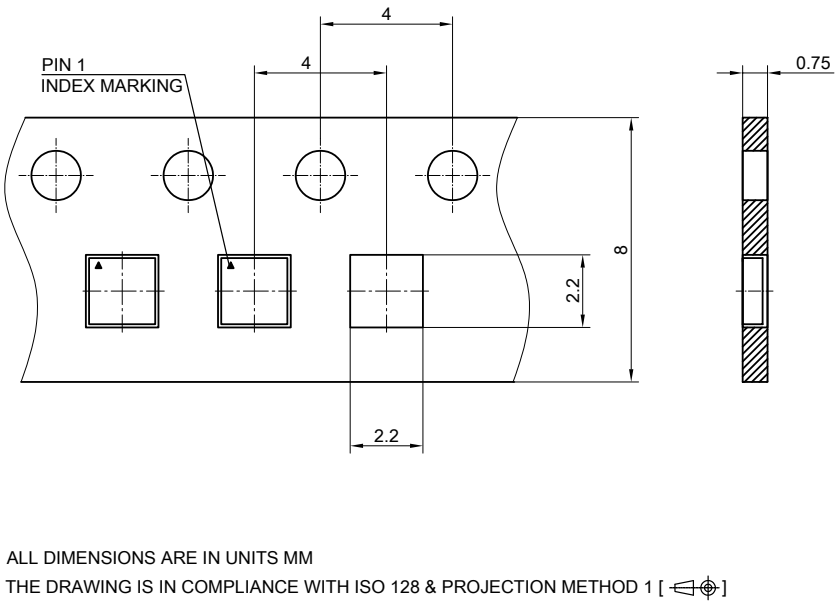


Figure 6: Carrier Tape Drawing (top and side views)

Revision History	
Preliminary, Revision v1.0 - 2019-01-22	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.0, 2019-06-24	
5	RF characteristics updated in Table 6
6	RF characteristics updated in Table 7
6	Switching time characteristics updated in Table 8

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Edition 2019-06-24
Published by
Infineon Technologies AG
81726 Munich, Germany

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