

# n-Channel Power MOSFET

OptiMOS™  
BSB015N04NX3 G

## Data Sheet

2.4, 2011-05-24  
Final

Industrial & Multimarket

## 1 Description

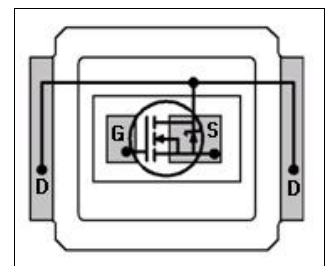
OptiMOS™40V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate- and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 40V the best choice for the demanding requirements of voltage regulator solutions in Servers, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space- efficiency and cost. OptiMOS™ products are designed to meet and exceed the energy efficiency and power density requirements of the sharpened next generation voltage regulation standards in computing applications

### Features

- Optimized for high switching frequency DC/DC converter
- 100% avalanche tested
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free plating; RoHS compliant
- Very low on-resistance  $R_{DS(on)}$
- Low profile (<0.7 mm)
- Low parasitic inductance
- Double.sided cooling
- Compatible with DirectFET® package MX footprint and outline
- 100% Rg Tested

### Applications

- On board power for server
- Power management for high performance computing
- Synchronous rectification
- High power density point of load converters



**Table 1 Key Performance Parameters**

Parameter	Value	Unit	Related Links
$V_{DS}$	40	V	<a href="#">IFX OptiMOS webpage</a> <a href="#">IFX OptiMOS product brief</a> <a href="#">IFX OptiMOS spice models</a> <a href="#">IFX Design tools</a>
$R_{DS(on),max}$	1.5	mΩ	
$I_D$	180	A	
$Q_{OSS}$	86	nC	
$Q_{g,typ}$	107		

Type	Package	Marking
BSB015N04NX3 G	MG-WDSO-2	0204

1) J-STD20 and JESD22

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	180	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				124		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				35		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}^1)$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	400		$T_C=25\text{ °C}$
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	-	40		
Avalanche energy, single pulse	$E_{AS}$	-	-	290	mJ	$I_D=40\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	
Power dissipation	$P_{tot}$	-	-	89	W	$T_C=25\text{ °C}$
				2.8		$T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55	150	56	Ncm	

1) J-STD20 and JESD22

2) See figure 3 for more detailed information

3) See figure 13 for more detailed information

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	1.0	-	°K/W	bottom
				1.4		top
Device on PCB	$R_{thJA}$	-	-	45		6 cm <sup>2</sup> cooling area <sup>1)</sup>

1) Device on 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air.

## 4 Electrical characteristics

Electrical characteristics, at  $T_J=25\text{ °C}$ , unless otherwise specified.

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	-	4		$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	10	$\mu\text{A}$	$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=25\text{ °C}$
		-	10	100		$V_{DS}=40\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.3	1.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
Gate resistance	$R_G$	0.2	0.5	1.0	$\Omega$	
Transconductance	$g_{fs}$	55	110		S	$ V_{DS} >2 I_{D} R_{DS(on)max}$ , $I_D=30\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	9000	12000	$\text{pF}$	$V_{GS}=0\text{ V}$ , $V_{DS}=20\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	2300	3100		
Reverse transfer capacitance	$C_{rss}$	-	91	-		
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	$V_{DD}=20\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	6.4	-		
Turn-off delay time	$t_{d(off)}$	-	36	-		
Fall time	$t_f$	-	7.6	-		

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	41	-	nC	$V_{DD}=20\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	26	-		
Gate to drain charge	$Q_{gd}$	-	13	-		
Switching charge	$Q_{sw}$	-	28	-		
Gate charge total	$Q_g$	-	107	142		
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	-	101	134		$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	86	-		$V_{DD}=20\text{ V}$ , $V_{GS}=0\text{ V}$

1) See figure 16 for gate charge parameter definition

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_s$			89	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{s,pulse}$			400		
Diode forward voltage	$V_{SD}$	-	0.81	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=30\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	-	50	nC	$V_R=15\text{ V}$ , $I_F=I_s$ , $di_F/dt=400\text{ A}/\mu\text{s}$

## 5 Electrical characteristics diagrams

Table 8

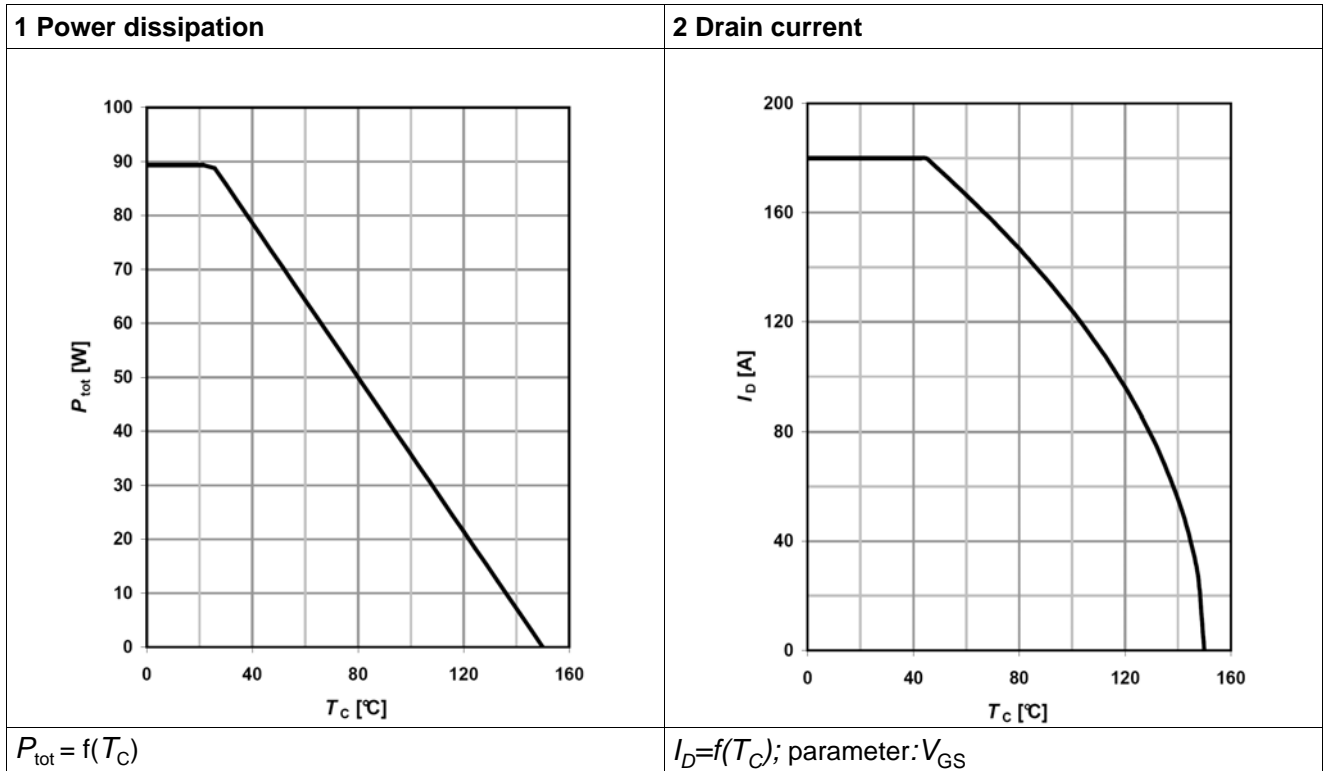


Table 9

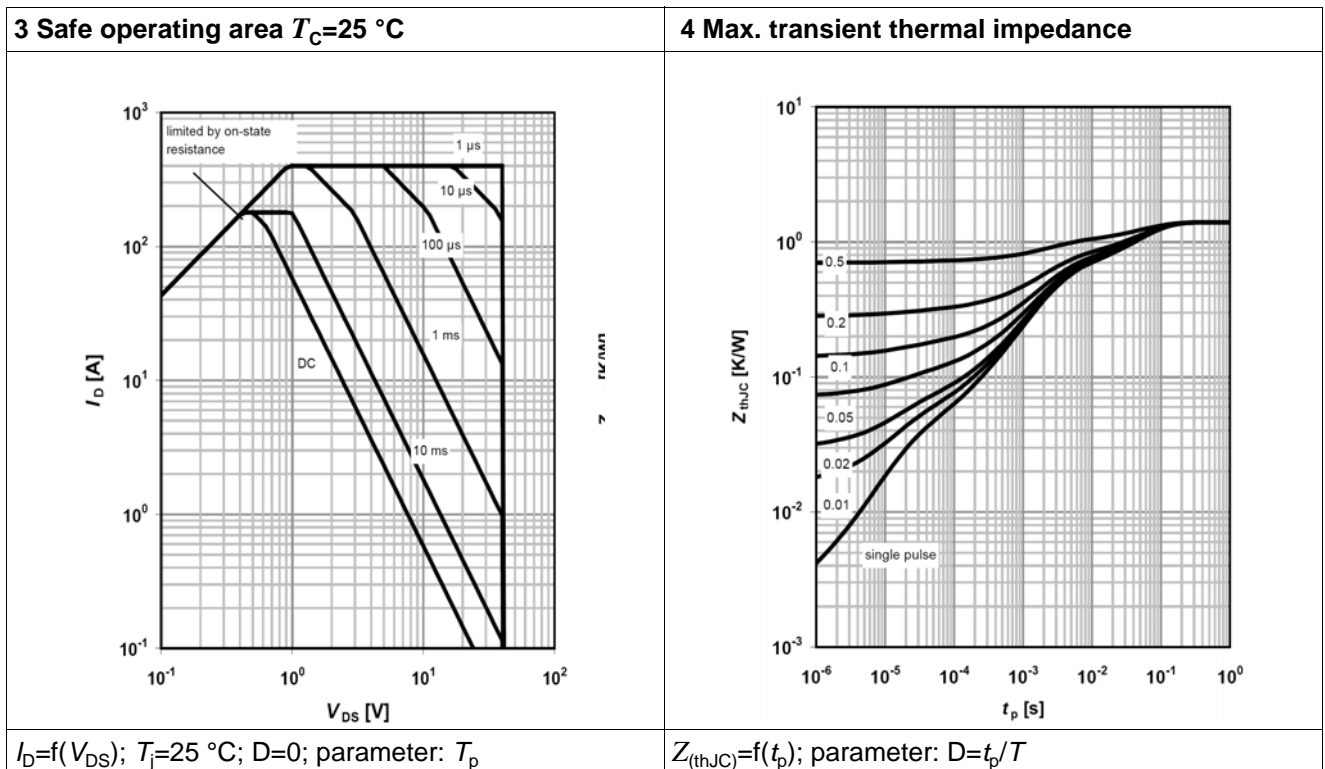




Table 10

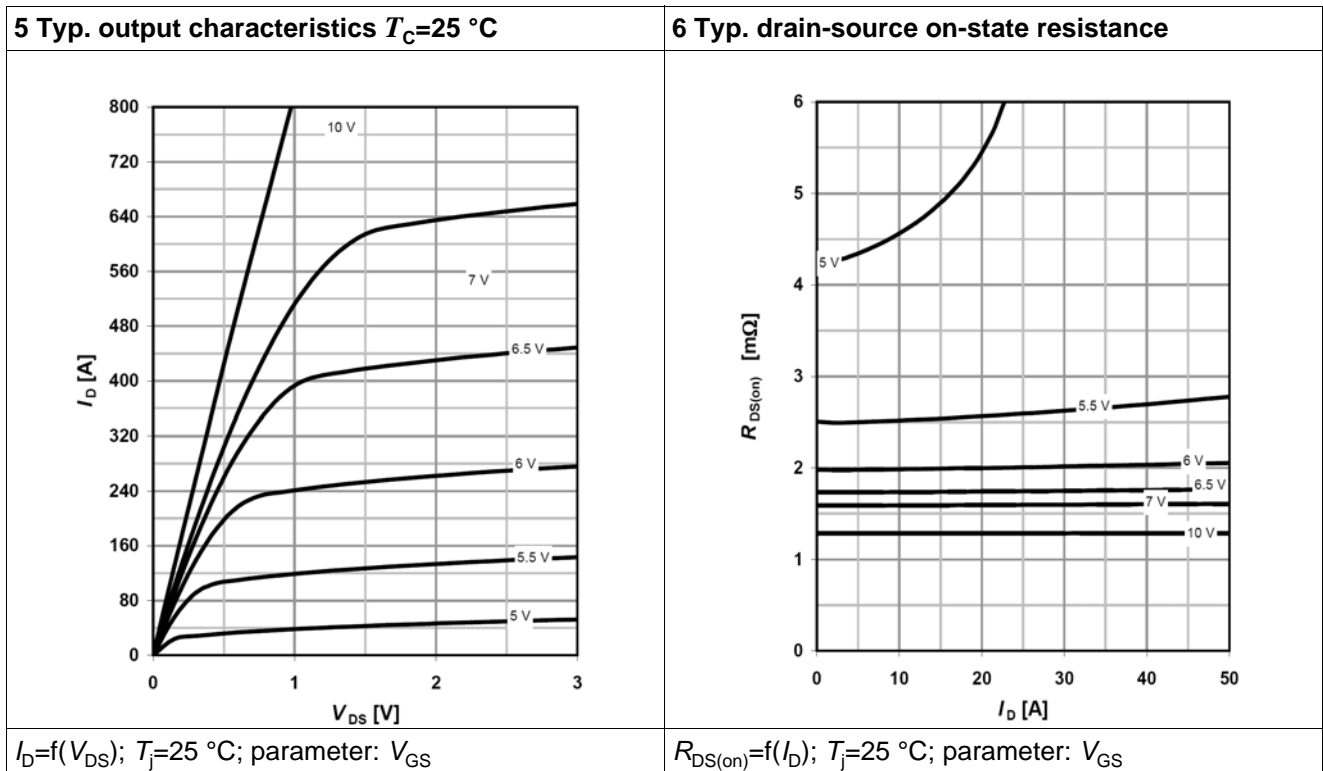


Table 11

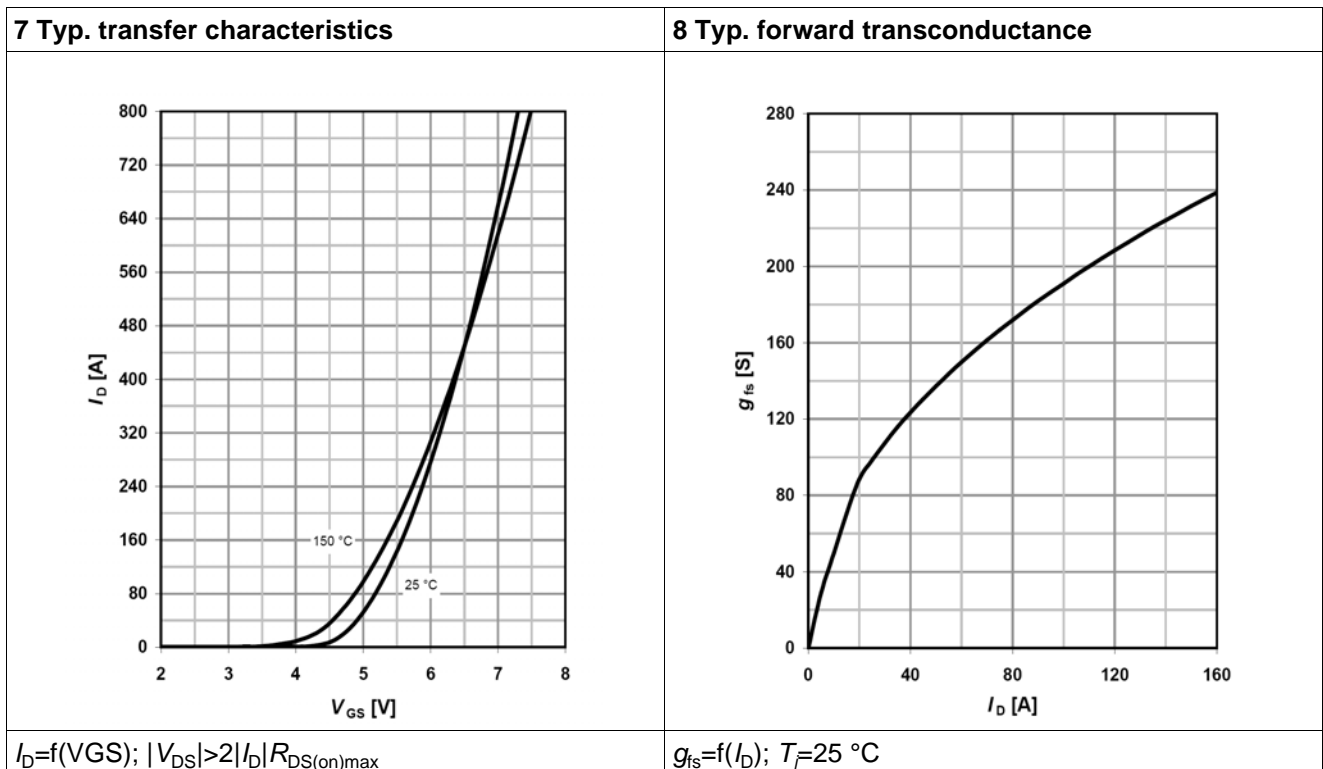


Table 12

<p><b>9 Drain-source on-state resistance</b></p> <p><math>R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}</math></p>	<p><b>10 Typ. gate threshold voltage</b></p> <p><math>V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=250\text{ }\mu\text{A}</math></p>
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Table 13

<p><b>11 Typ. capacitances</b></p> <p><math>C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}</math></p>	<p><b>12 Forward characteristics of reverse diode</b></p> <p><math>I_F=f(V_{SD}); \text{parameter: } T_j</math></p>
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Table 14

13 Avalanche characteristics	14 Typ. gate charge
$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega; \text{parameter: } T_{j(\text{start})}$	$V_{GS}=f(Q_{\text{gate}}); I_D=30\ \text{A pulsed}; \text{parameter: } V_{DD}$

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$	

## 6 Package outlines

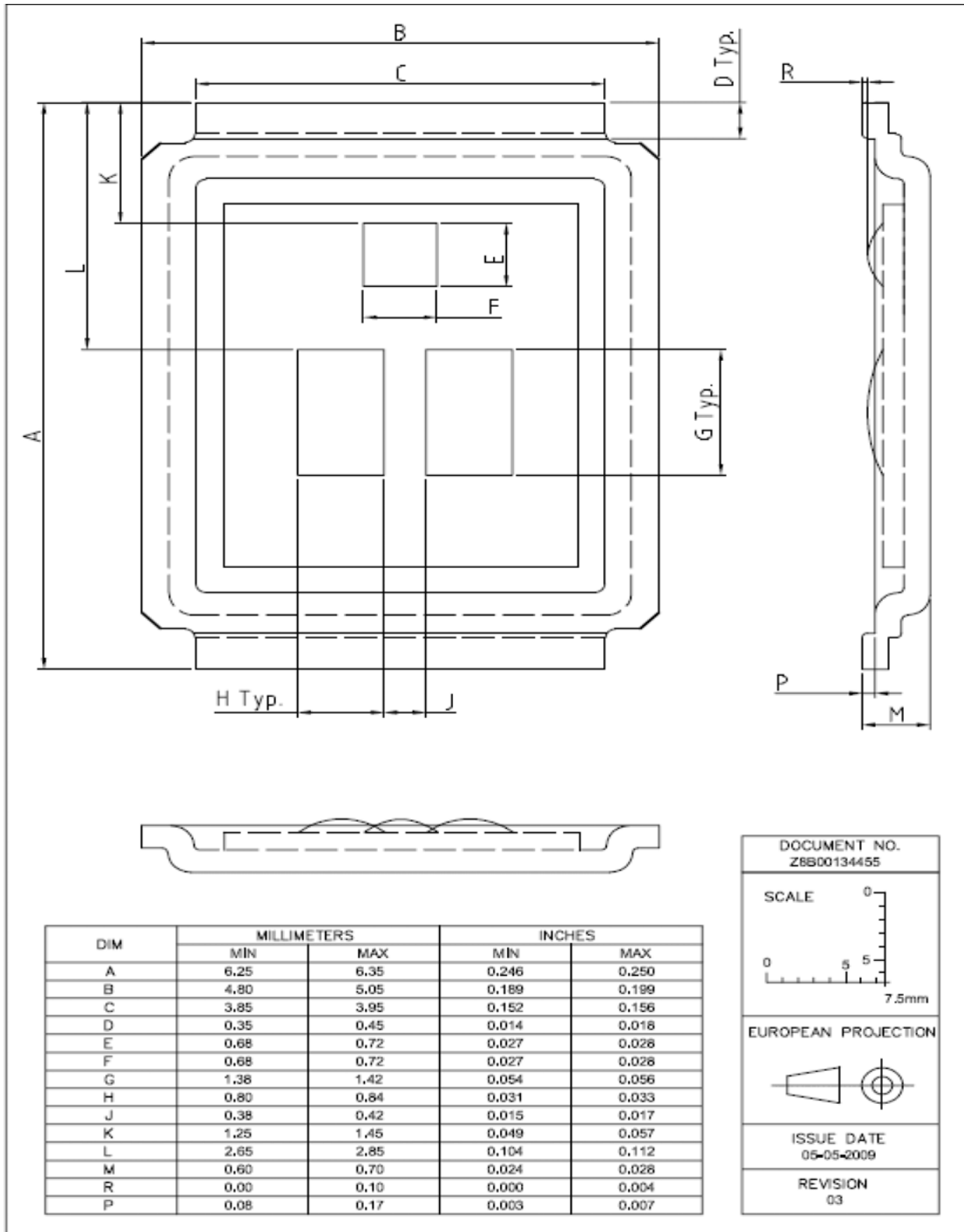


Figure 1 Outlines MG-WDSO-2, dimensions in mm/inches

7 Package outlines

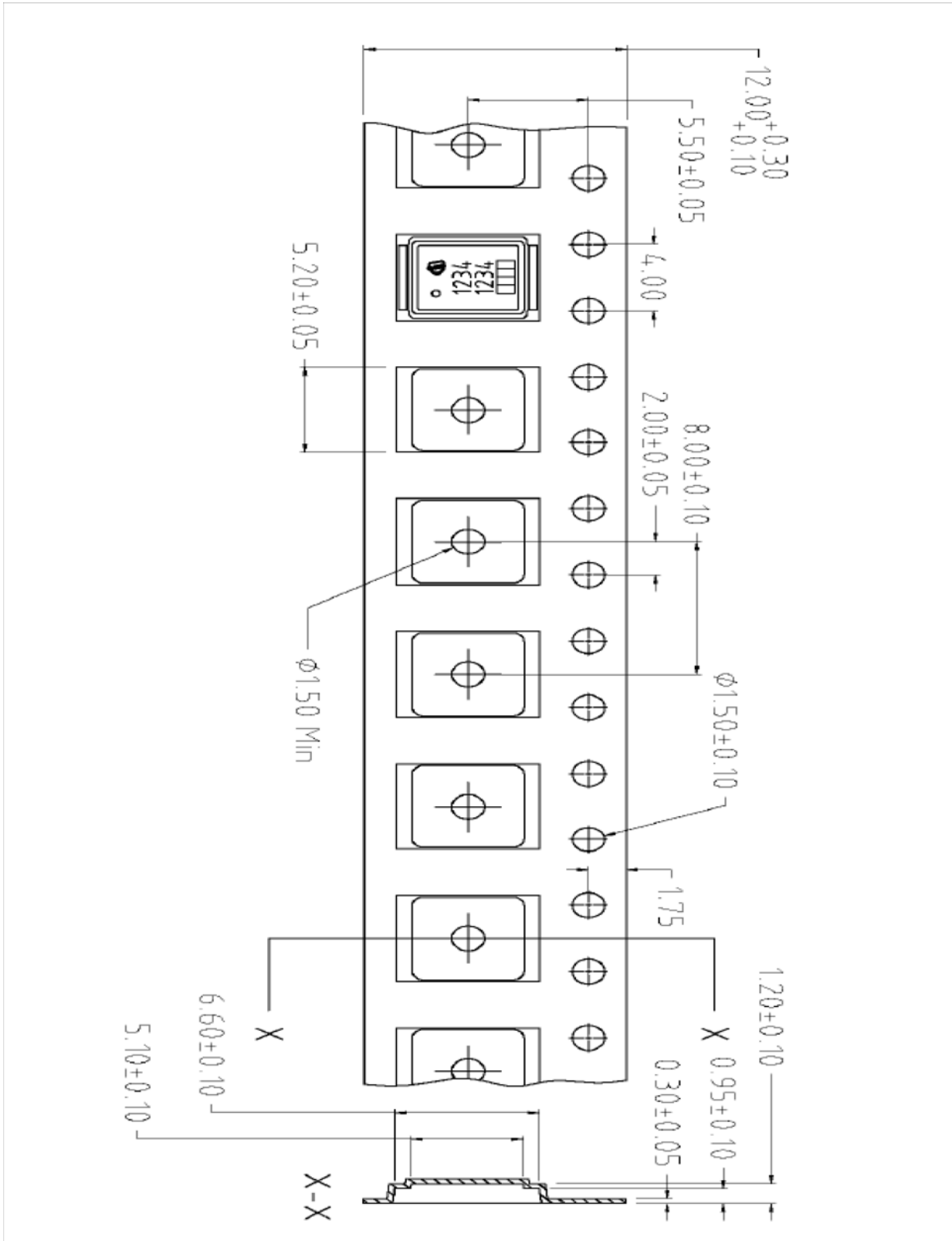


Figure 2 Outlines MG-WDSO-2, dimensions in mm/inches

## 8 Package outlines

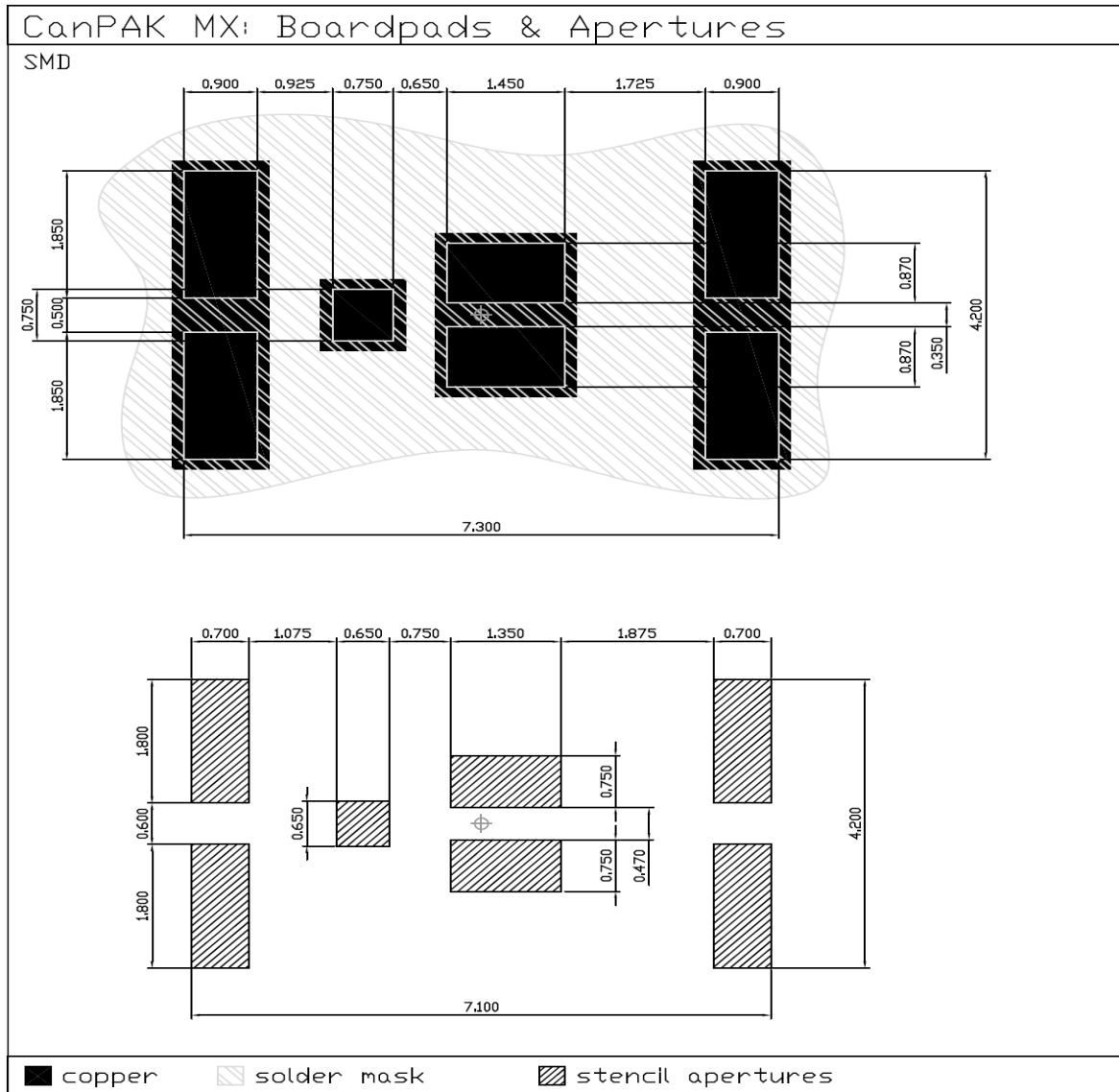
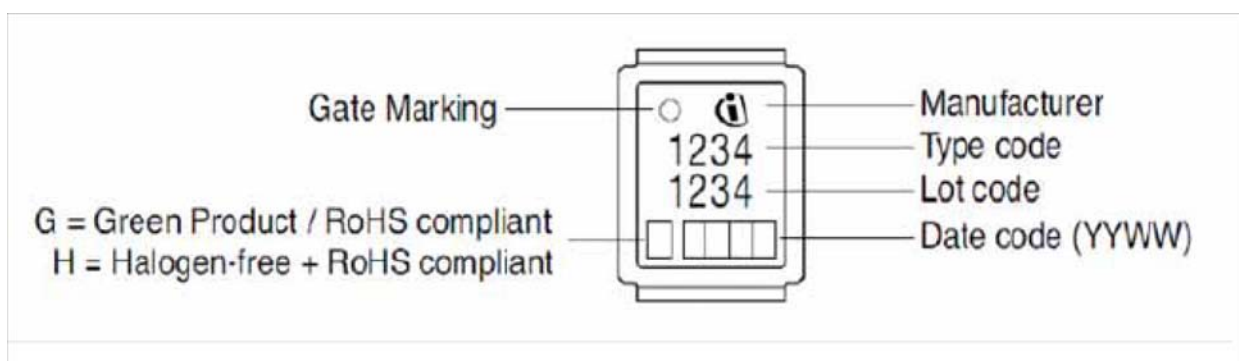


Figure 3 Outlines MG-WDSO-2, dimensions in mm/ Recommended stencil thickness 150µm

## 9 Marking layout



## 9 Revision History

Revision History: 2011-05-24, 2.4

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
2.0	Release Final version
2.3	DirectFET Disclaimer expired
2.4	Insert Marking layout

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