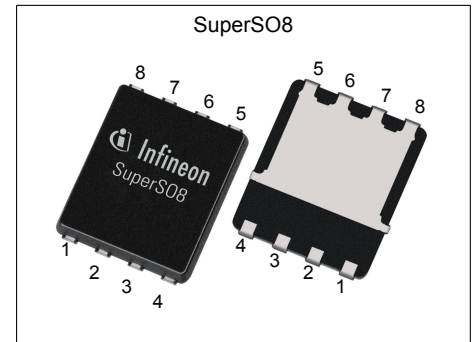


# MOSFET

## OptiMOS™5 Power-Transistor, 100 V

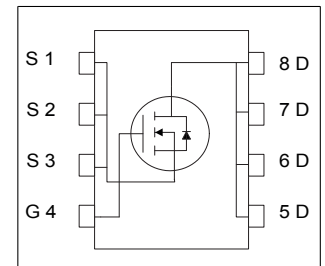
### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}$	7.0	m $\Omega$
$I_D$	80	A
$Q_{oss}$	41	nC
$Q_G(0V..10V)$	30	nC



Type / Ordering Code	Package	Marking	Related Links
BSC070N10NS5	PG-TDSON-8	070N10N5	-

<sup>1)</sup> J-STD20 and JESD22

## Table of Contents

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	80 51 14	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{K/W}^{(1)}$
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>(3)</sup>	$E_{AS}$	-	-	73	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	83 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^{(2)}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.9	1.5	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>(1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> See Diagram 3 for more detailed information

<sup>3)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$ , $I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.0 7.6	7.0 10.2	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=20\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.0	1.5	$\Omega$	-
Transconductance	$g_{fs}$	38	77	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=40\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	2100	2700	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	340	440	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	16	28	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Rise time	$t_r$	-	5	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	24	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$
Fall time	$t_f$	-	6	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=3\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	10	-	nC	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6	-	nC	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	6	10	nC	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	11	-	nC	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	30	38	nC	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=50\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	26	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	41	55	nC	$V_{DD}=50\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not Subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	76	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.1	V	$V_{GS}=0\text{ V}, I_F=40\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	53	106	ns	$V_R=50\text{ V}, I_F=40\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	89	179	nC	$V_R=50\text{ V}, I_F=40\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not Subject to production test.

### 4 Electrical characteristics diagrams

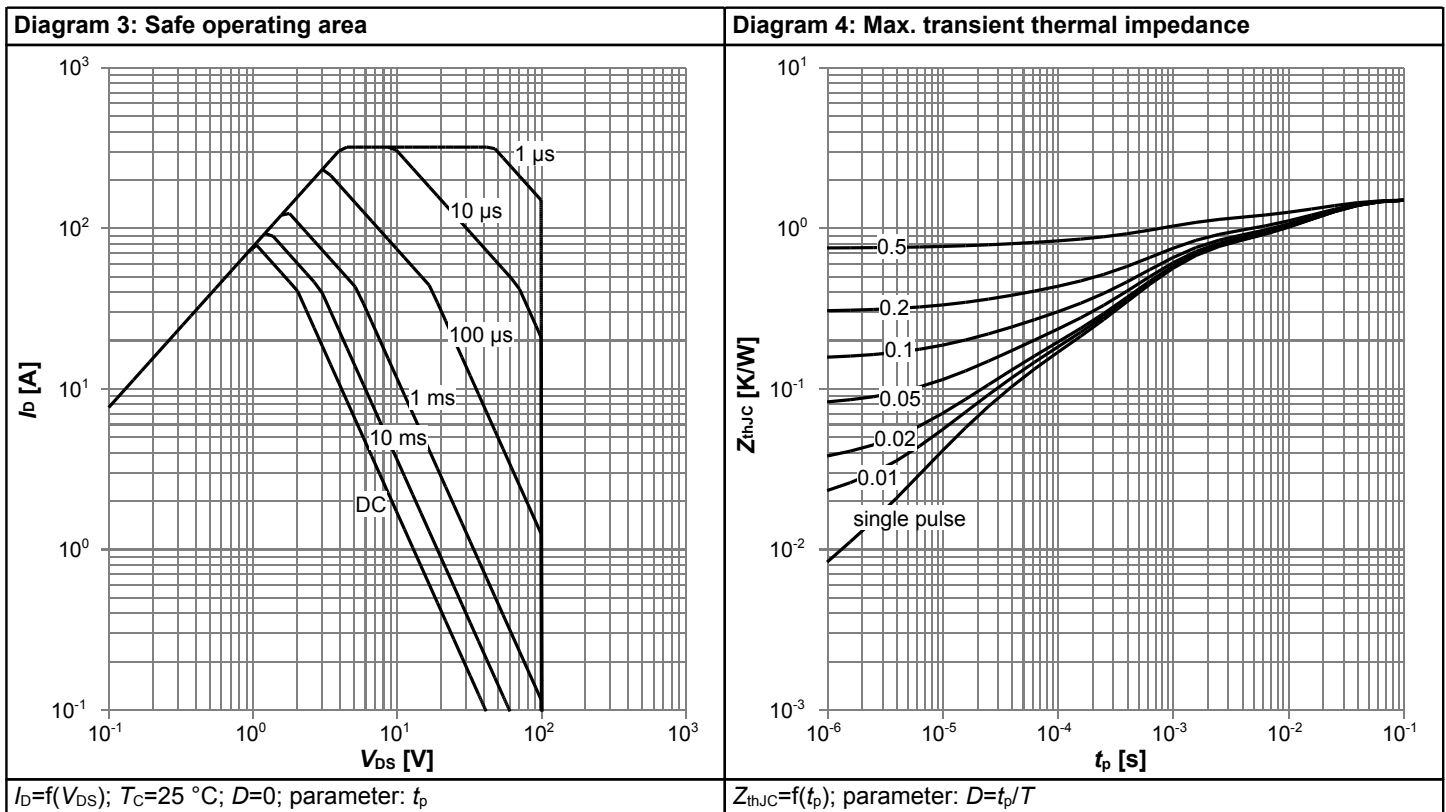
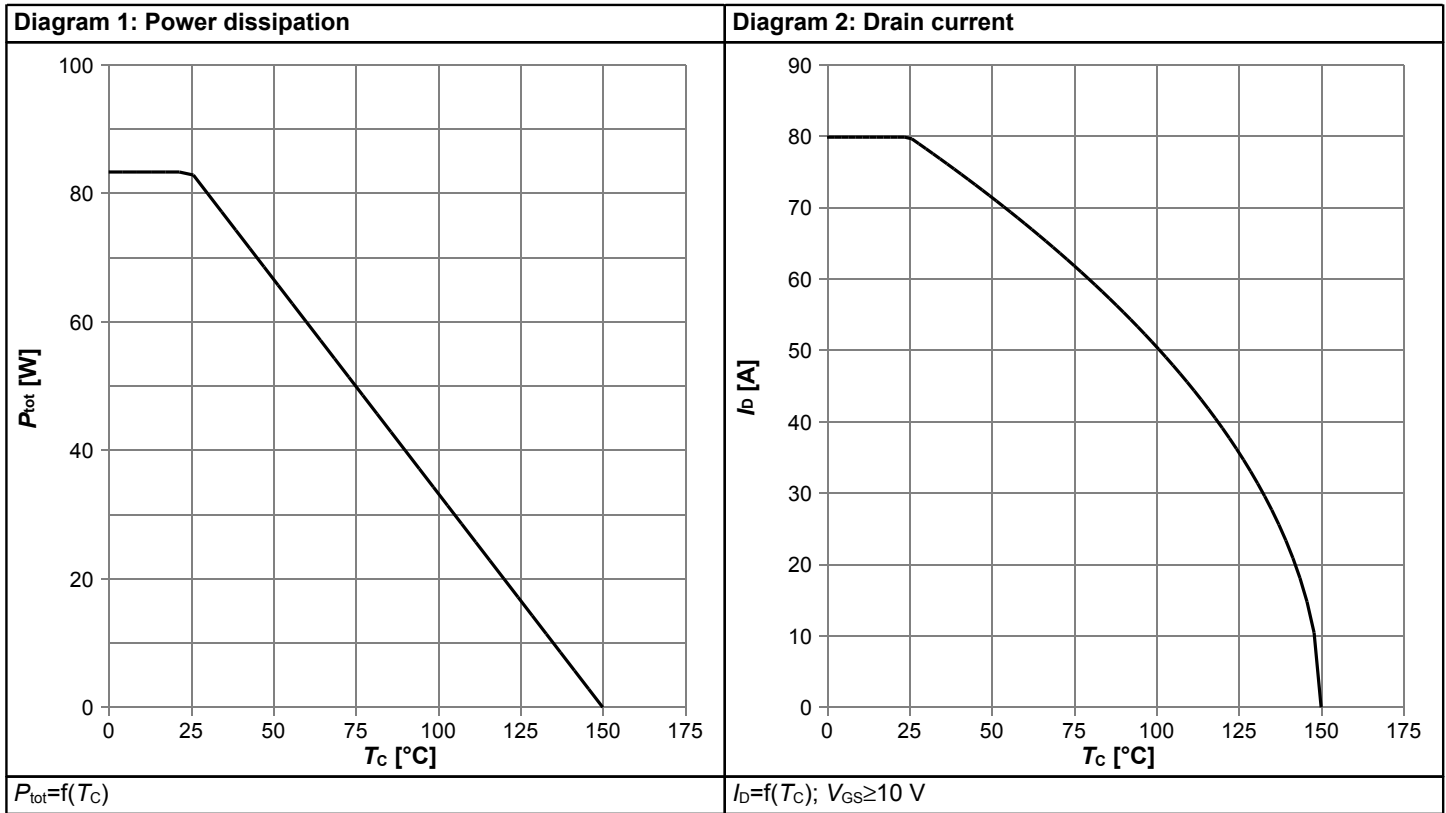
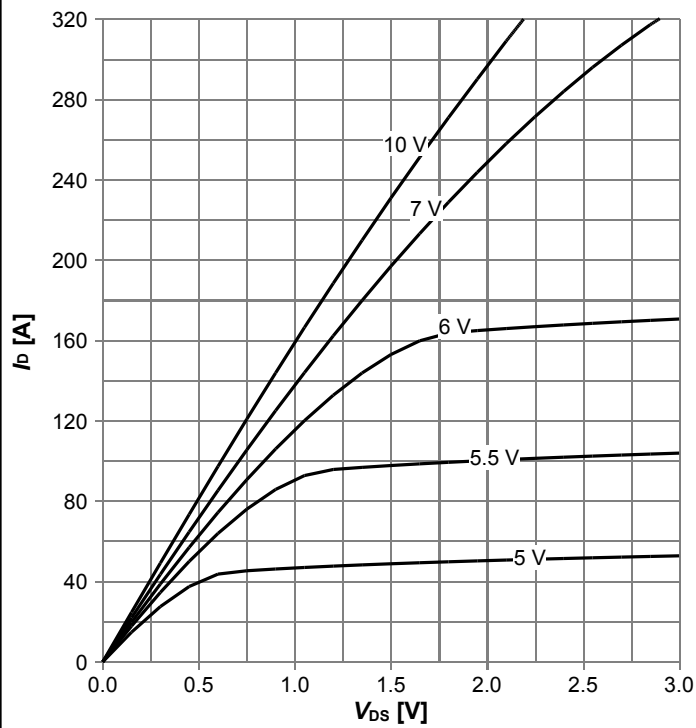
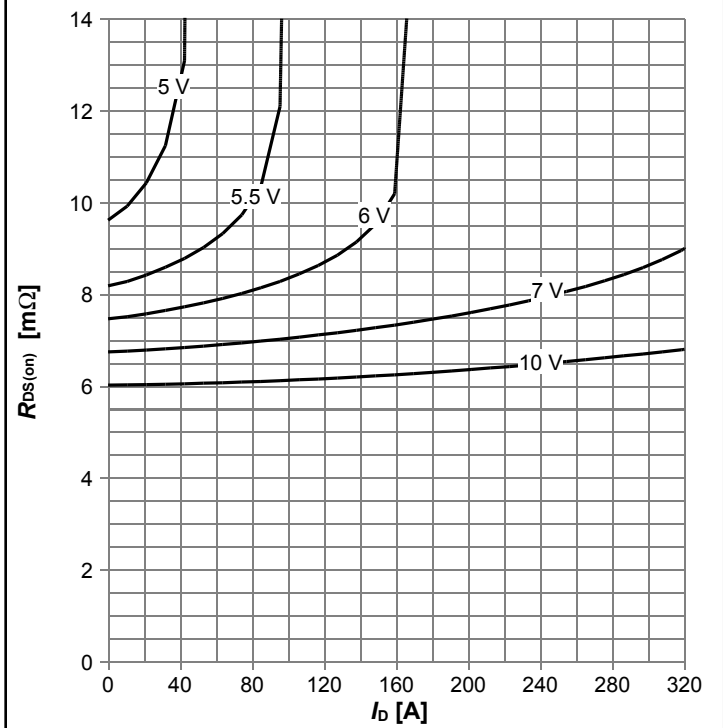


Diagram 5: Typ. output characteristics



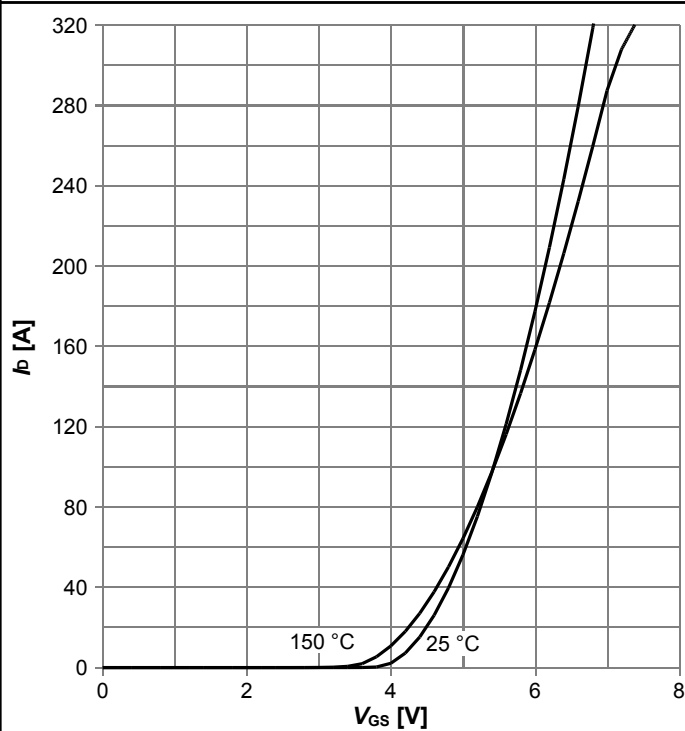
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



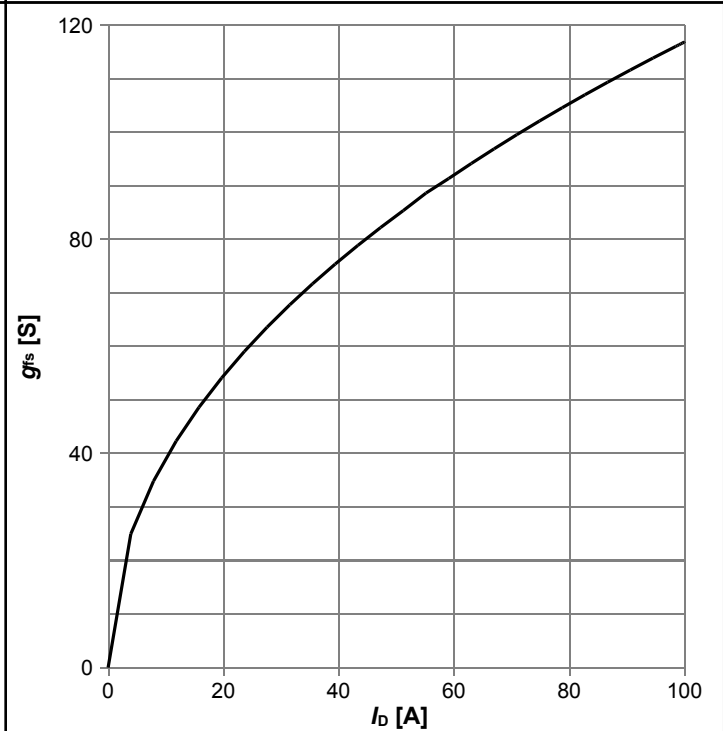
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



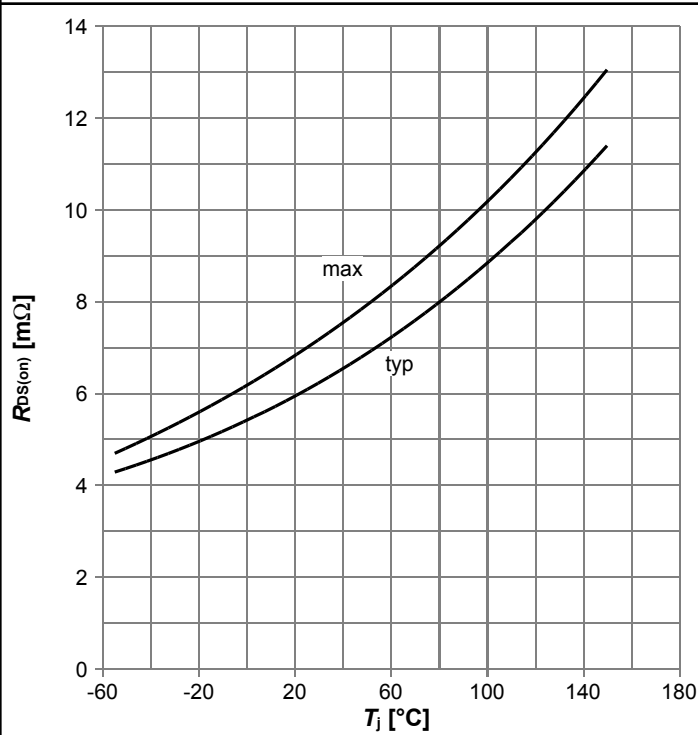
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



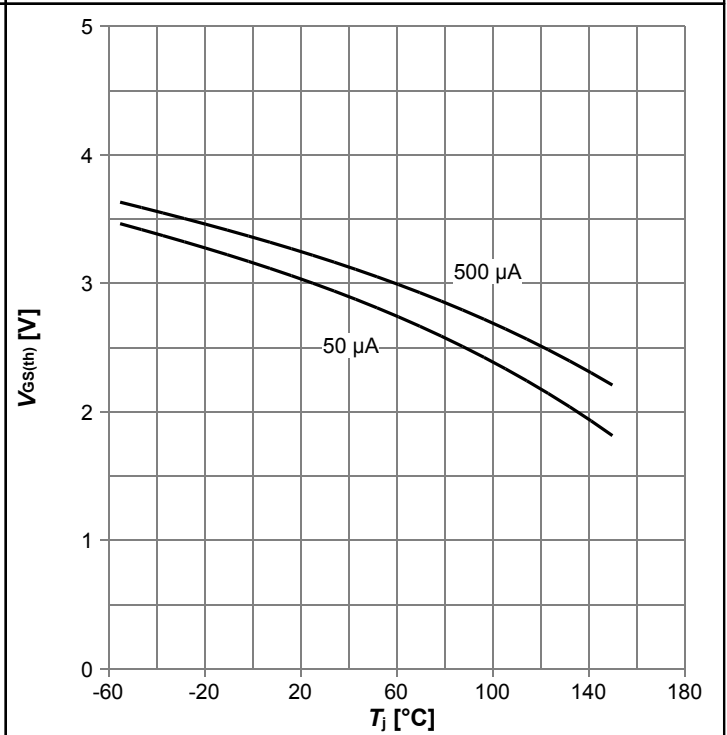
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



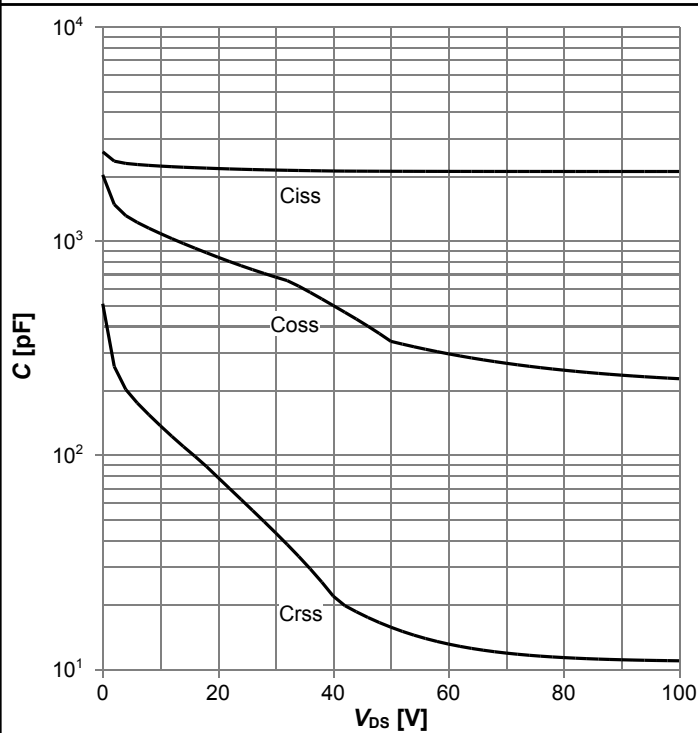
$R_{DS(on)}=f(T_j)$ ;  $I_D=40\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



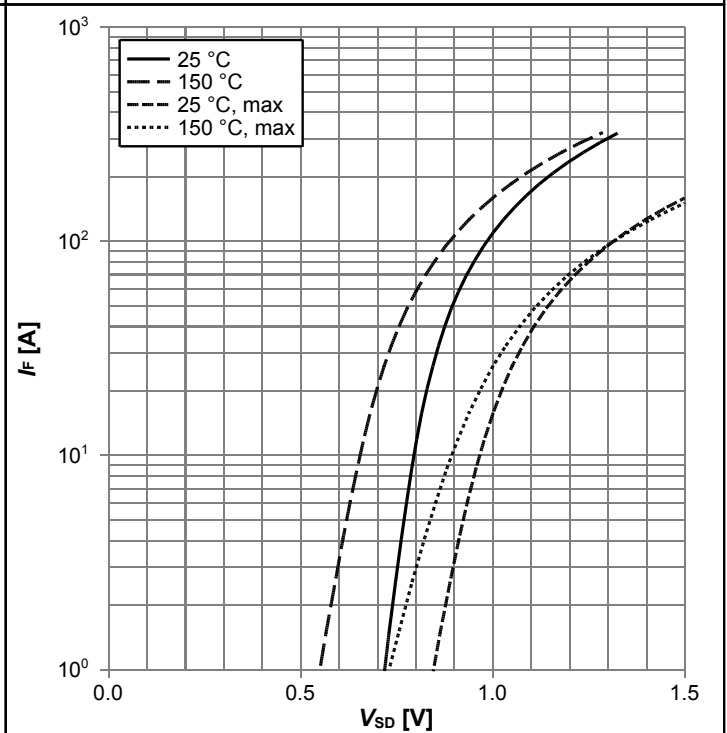
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

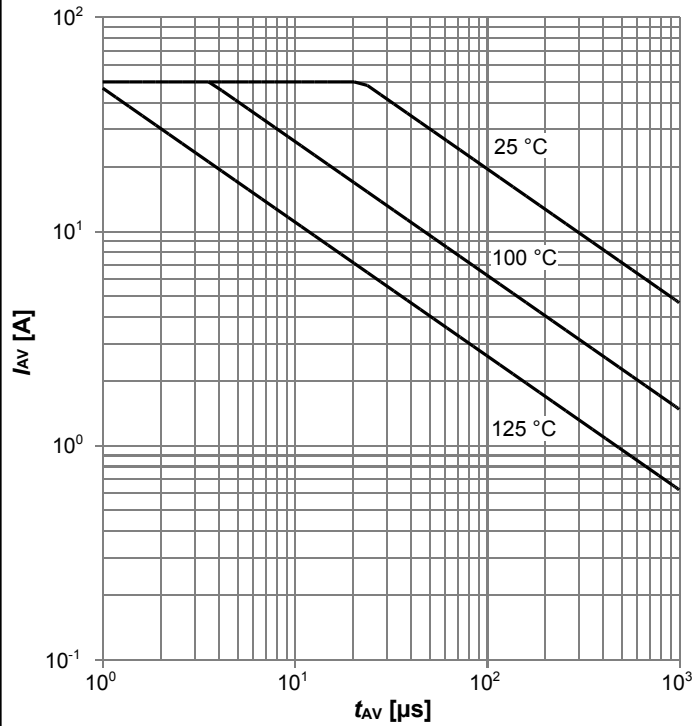
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

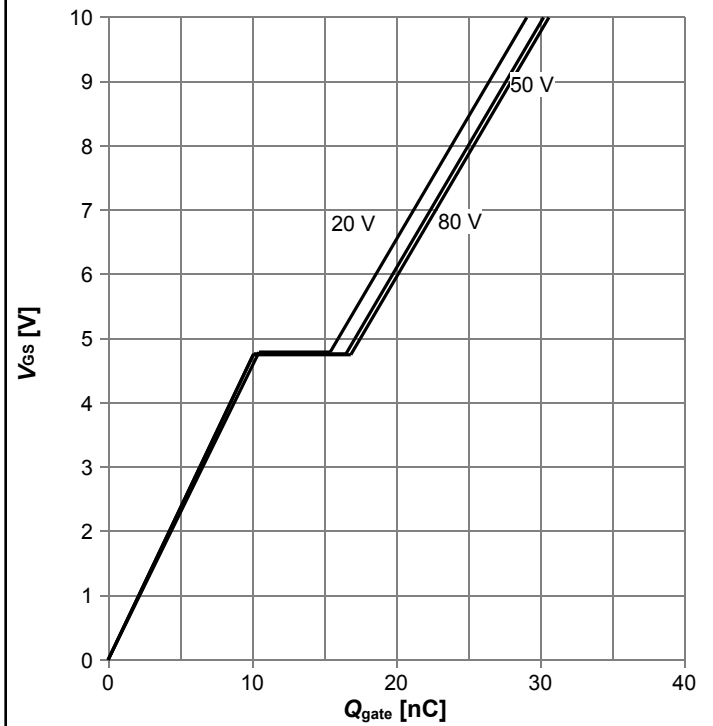


**Diagram 13: Avalanche characteristics**



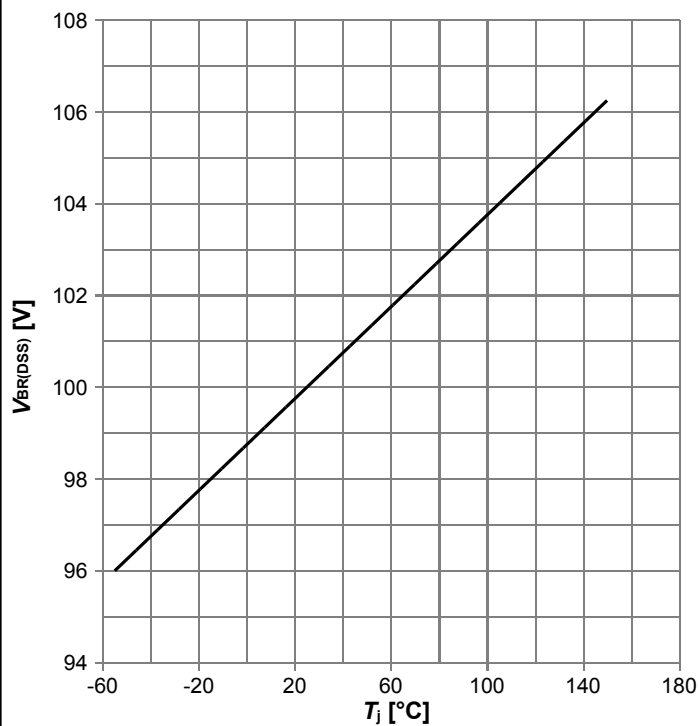
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



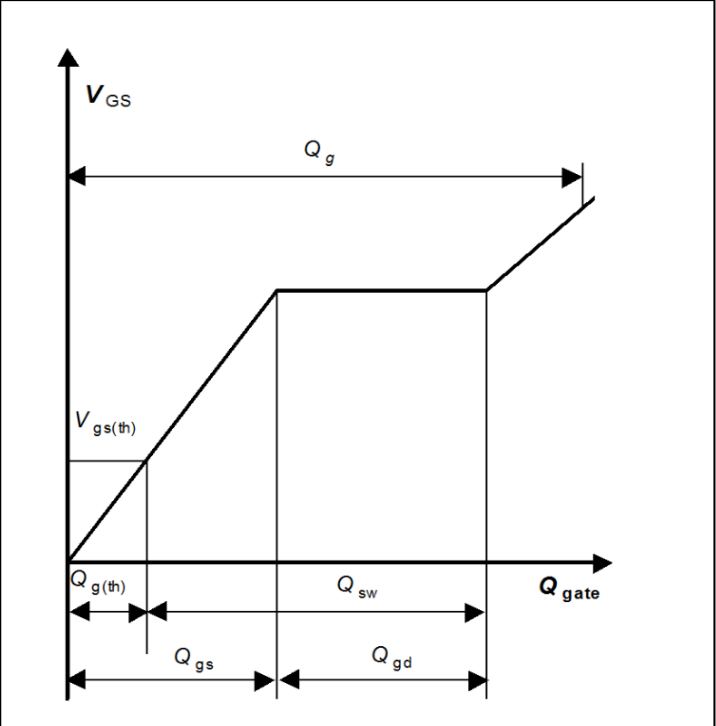
$V_{GS}=f(Q_{gate}); I_D=40$  A pulsed; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

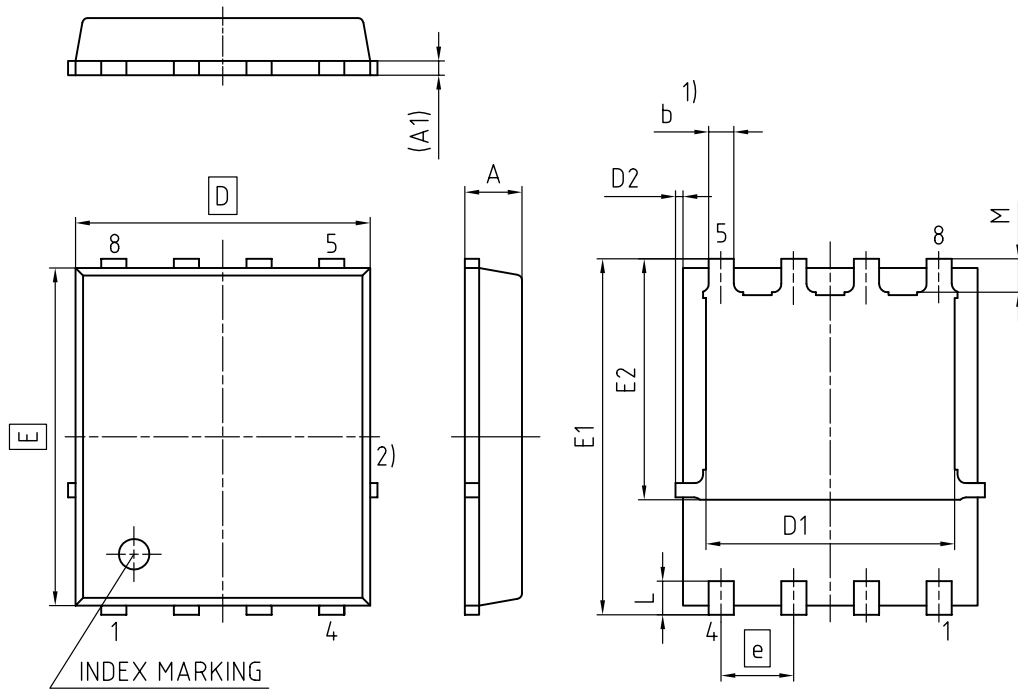


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

**Diagram Gate charge waveforms**



## 5 Package Outlines

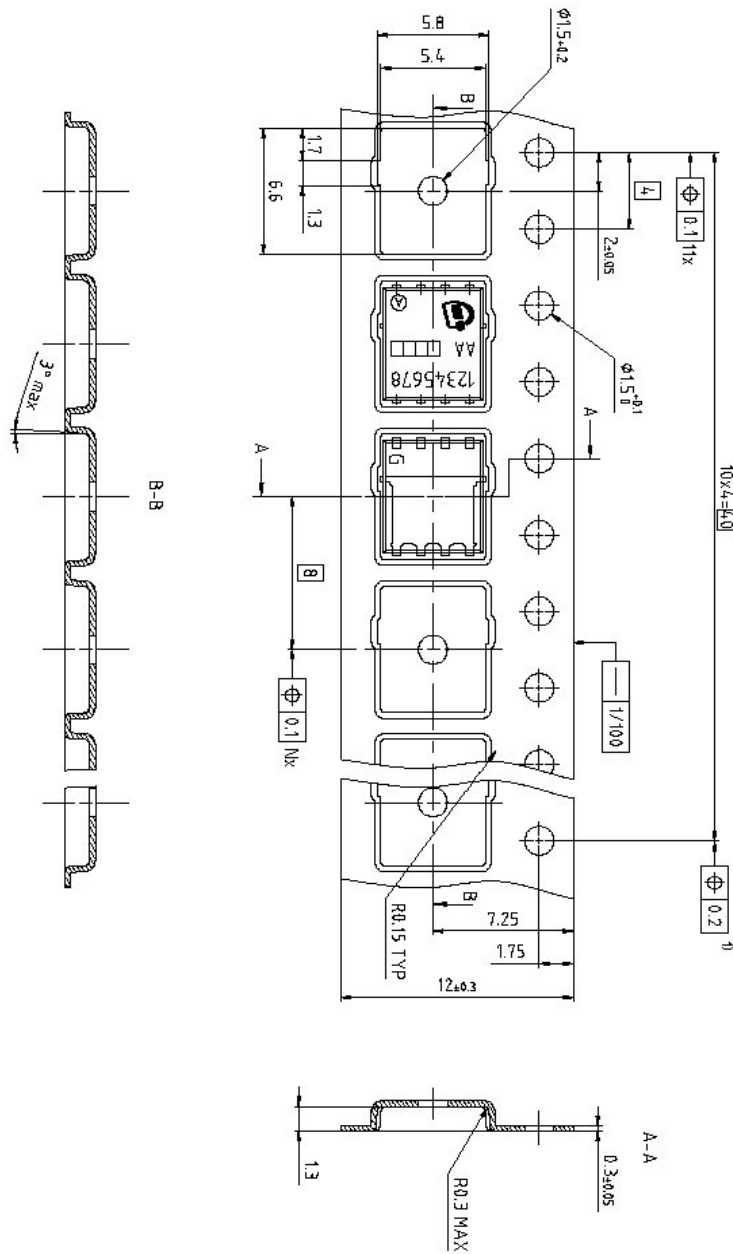


- 1) EXCLUDING MOLD FLASH  
 2) REMOVAL ON MOLD GATE  
 INTRUSION 0.1 MM  
 PROTRUSION 0.1 MM  
 LEAD LENGTH UP TO ANTI FLASH LINE  
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

<b>DOCUMENT NO.</b> Z8B00003332
<b>REVISION</b> 07
<b>SCALE 10:1</b> 0 1 2 3mm
<b>EUROPEAN PROJECTION</b> 
<b>ISSUE DATE</b> 06.06.2019

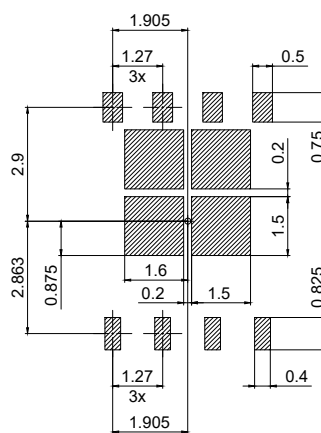
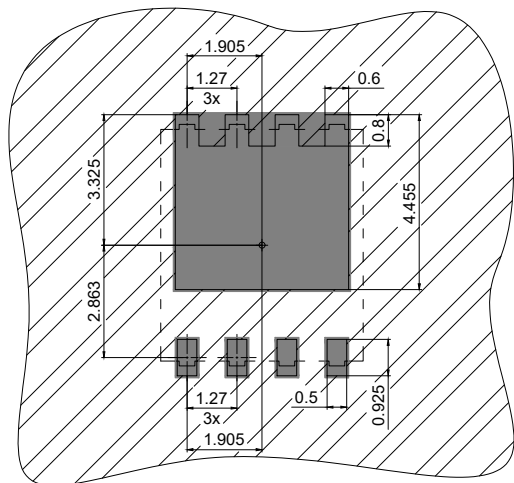
Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline Tape (TDSON-8)

PG-TDSON-8: Recommended Boardpads & Apertures



■ copper

▨ solder mask

▩ stencil apertures

all dimensions in mm

Figure 3 Outline Boardpads (TDSON-8), dimensions in mm

## Revision History

BSC070N10NS5

Revision: 2019-11-13, Rev. 2.3

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-11-26	Release of final version
2.1	2015-07-13	Update Marking
2.2	2016-09-07	Update Avalanche Energy
2.3	2019-11-13	Update package drawings

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[PJMF280N60E1\\_T0\\_00201](#) [PJMF600N65E1\\_T0\\_00201](#) [PJMF900N65E1\\_T0\\_00201](#) [PJMF900N60E1\\_T0\\_00201](#)