

# MOSFET

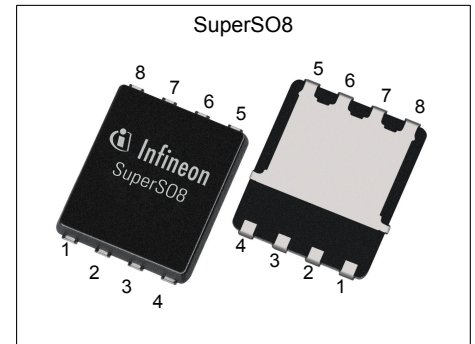
## OptiMOS™5 Power-Transistor, 150 V

### Features

- N-channel, logic level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

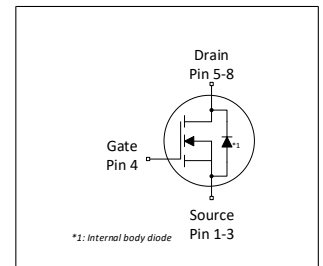
### Product validation

Fully qualified according to JEDEC for Industrial Applications



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	10.5	$m\Omega$
$I_D$	76	A
$Q_{oss}$	81	nC
$Q_G (0V...10V)$	34	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC105N15LS5	PG-TDSON-8	105N15LS	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	76 48 41 10.7	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	304	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	62	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	125 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	-

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	1.0	°C/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	50	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.3	1.8	2.3	V	$V_{DS}=V_{GS}$ , $I_D=91\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1.0 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	8.8 10.9	10.5 14	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$
Gate resistance	$R_G$	-	0.9	1.35	$\Omega$	-
Transconductance	$g_{fs}$	-	70	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=40\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	2300	3000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	580	750	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	17	30	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	2.3	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	17.8	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	3.4	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=40\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	7.5	-	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	4.1	-	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	6.9	10.4	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	10.3	-	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	18.1	23.0	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.3	-	V	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	34	43	nC	$V_{DD}=75\text{ V}$ , $I_D=40\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	81	108	nC	$V_{DS}=75\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

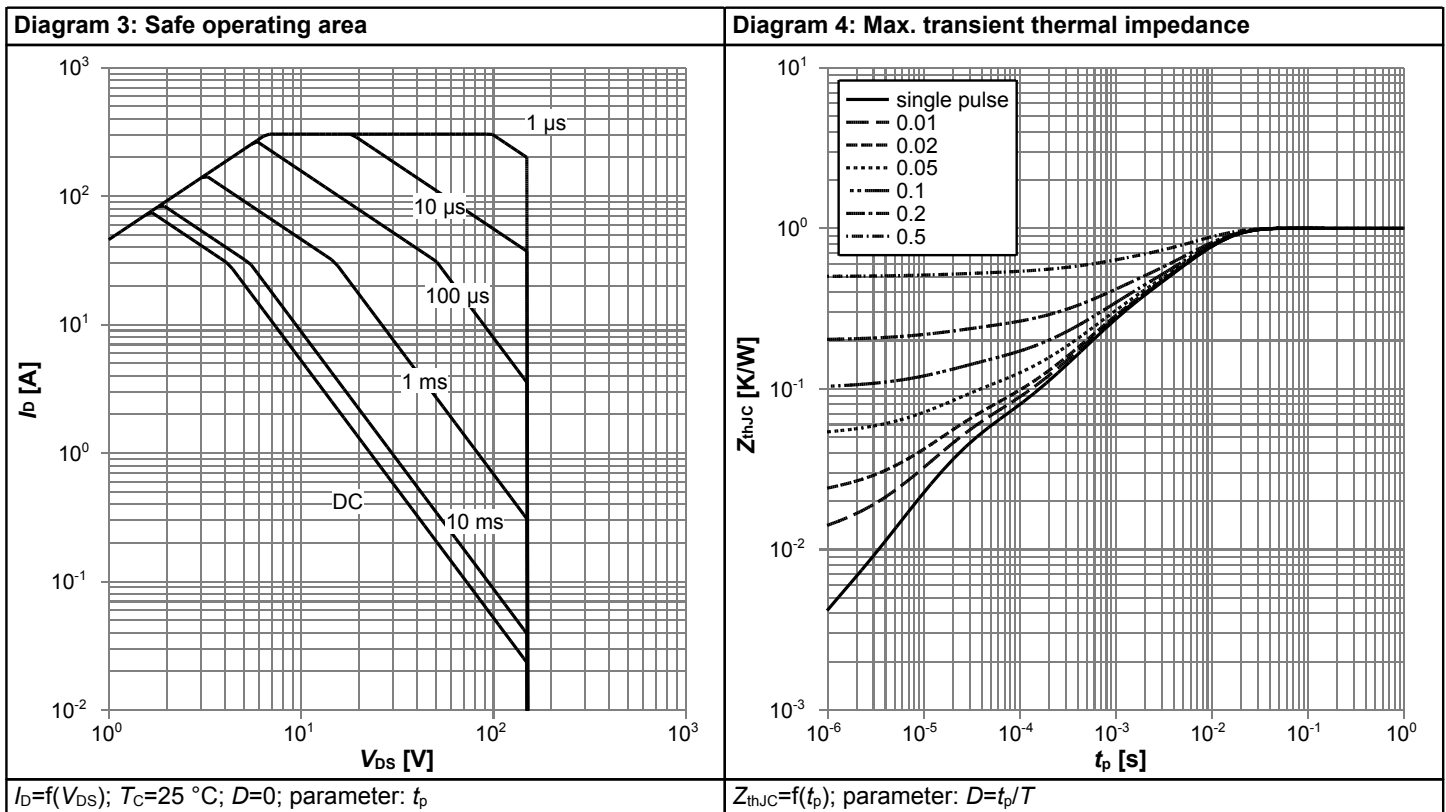
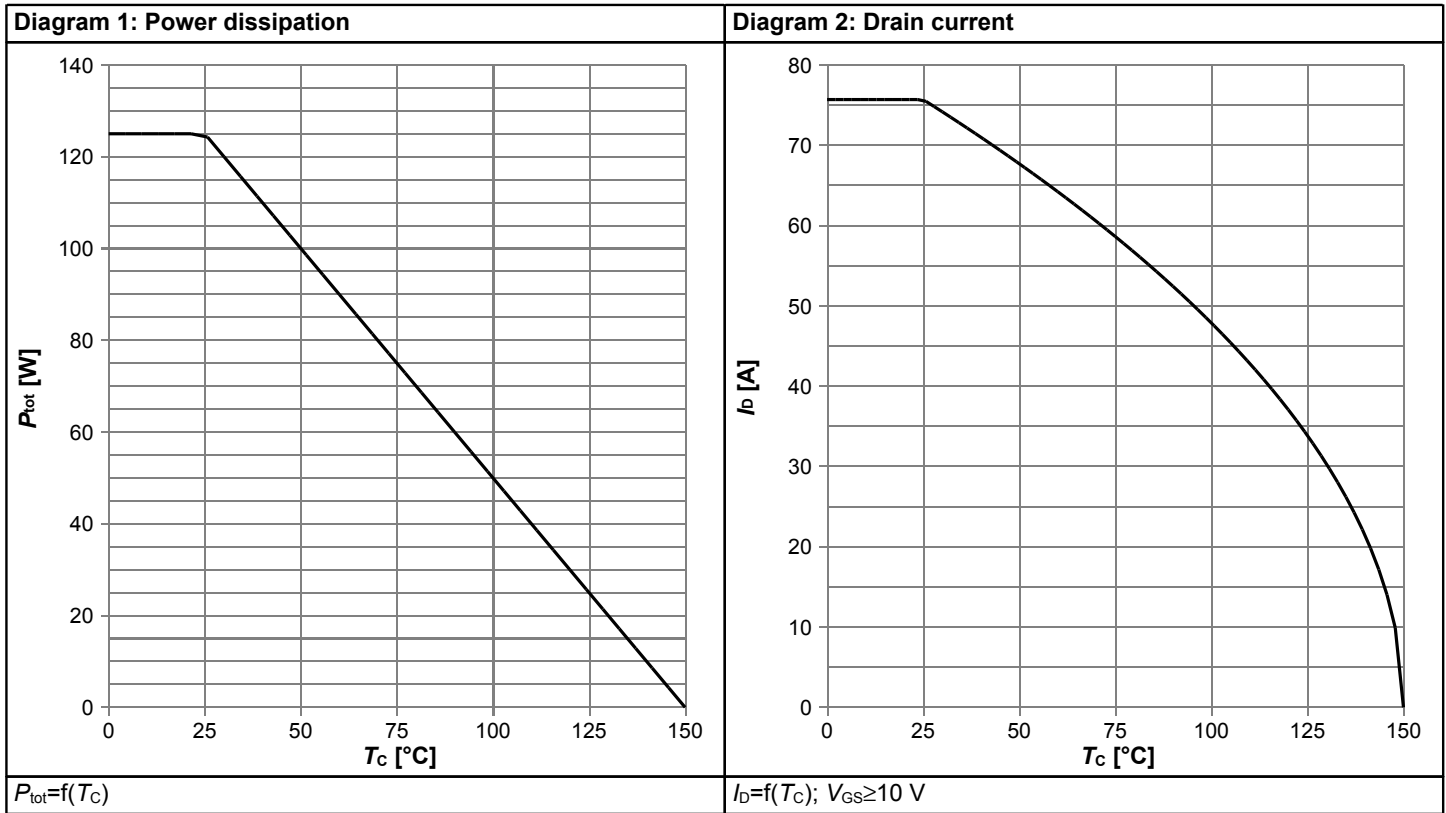
<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

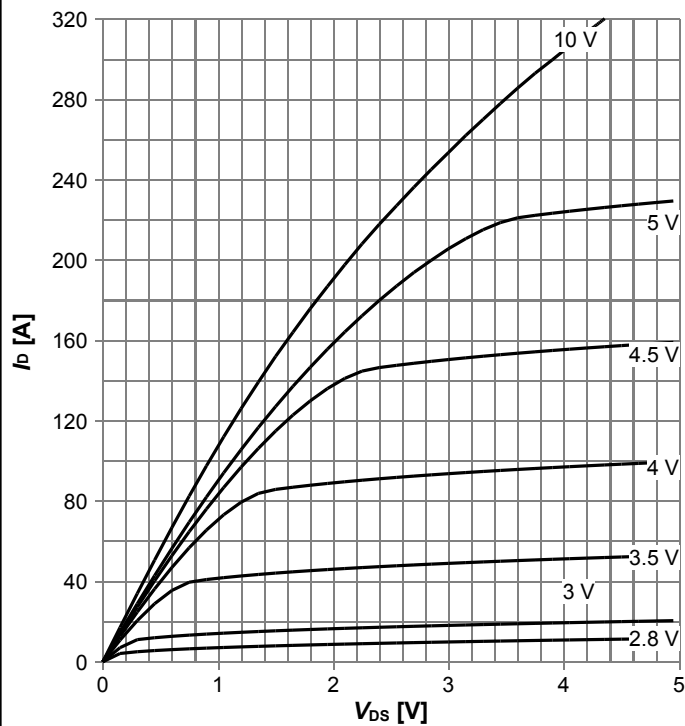
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	76	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	304	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.83	1.2	V	$V_{GS}=0\text{ V}, I_F=38\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	24.3	48.6	ns	$V_R=75\text{ V}, I_F=40\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	15.7	31.4	nC	$V_R=75\text{ V}, I_F=40\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

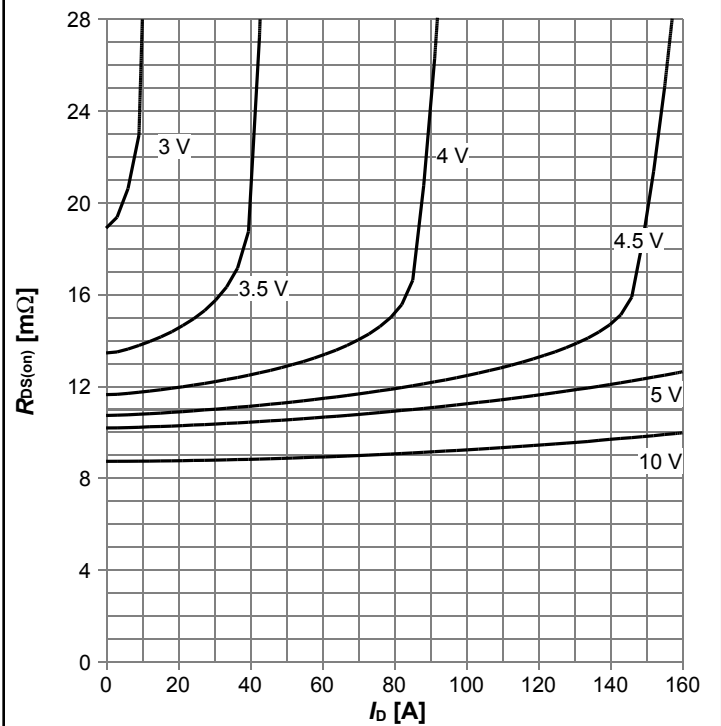


**Diagram 5: Typ. output characteristics**



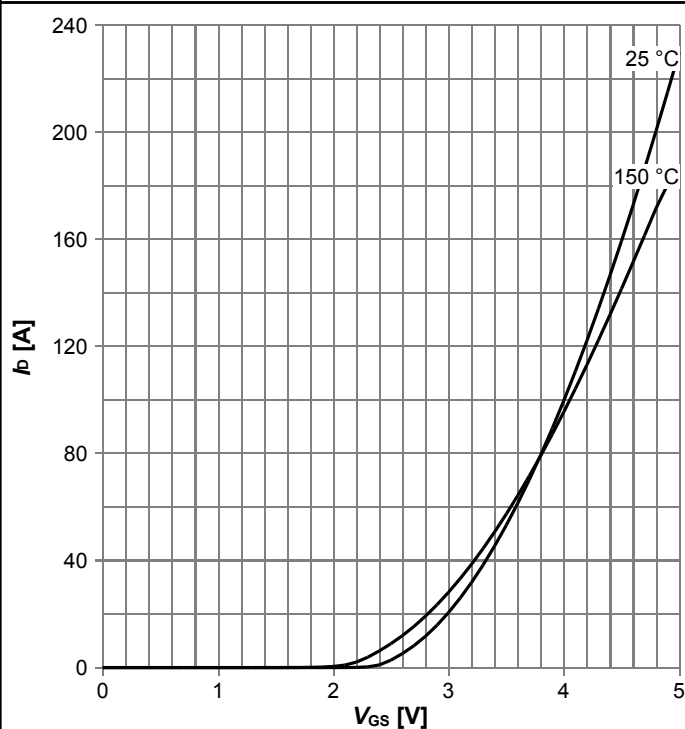
$I_D = f(V_{DS}), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



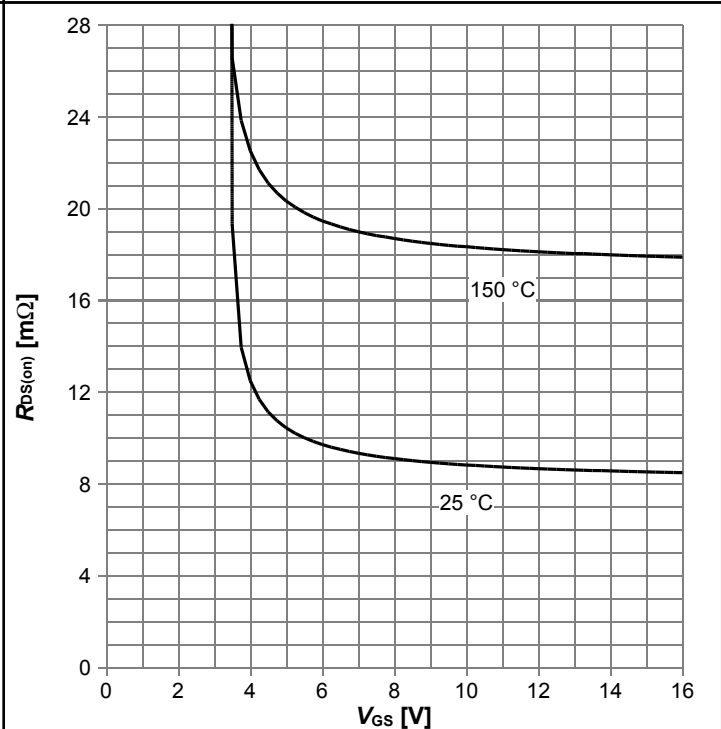
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



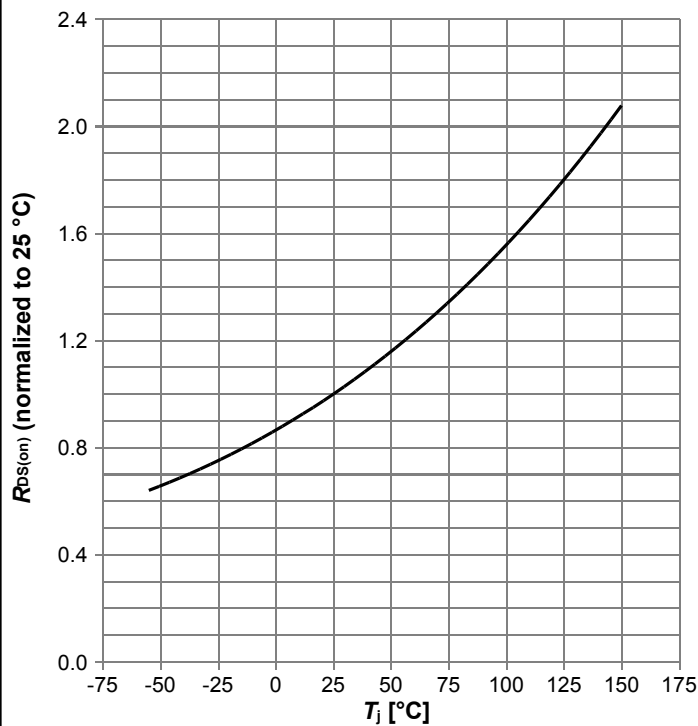
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

**Diagram 8: Typ. drain-source on resistance**



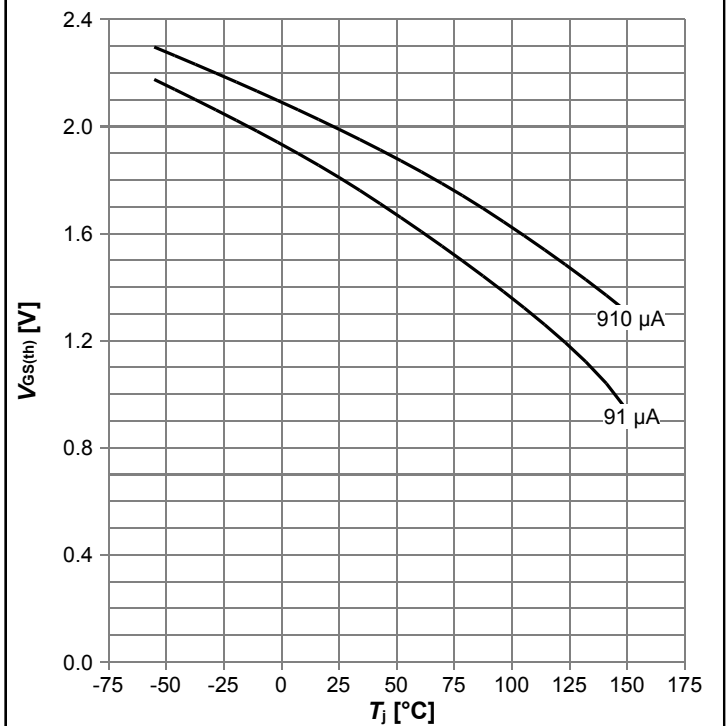
$R_{DS(on)} = f(V_{GS}), I_D = 40\text{ A};$  parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



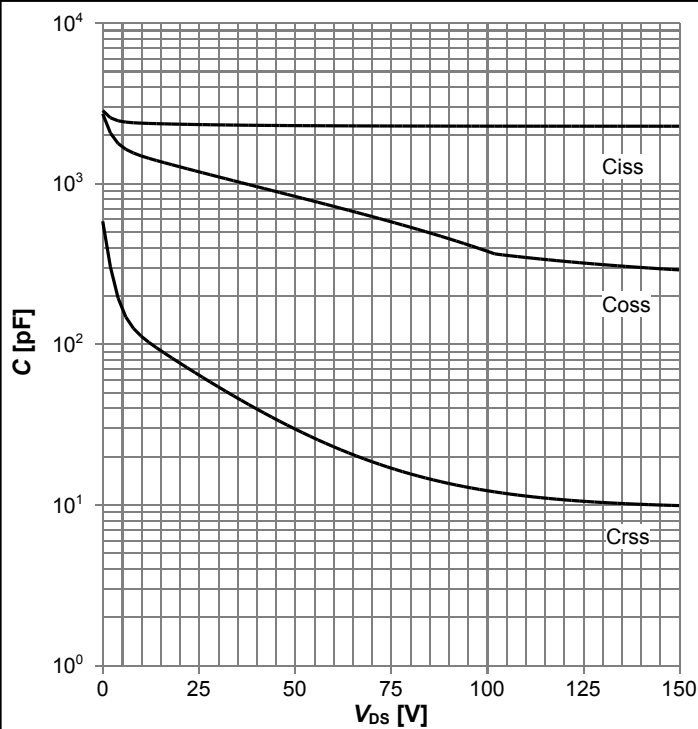
$R_{DS(on)}=f(T_j)$ ,  $I_D=40$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



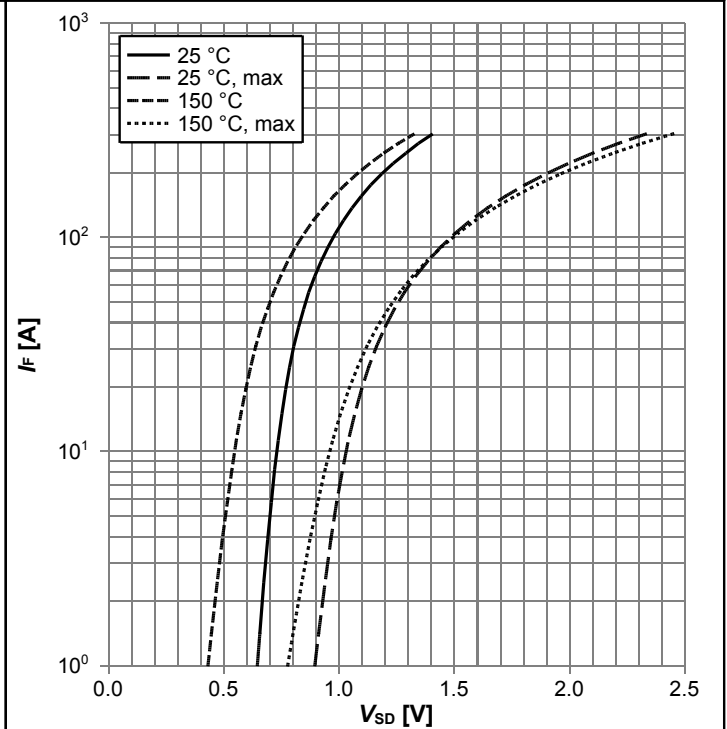
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

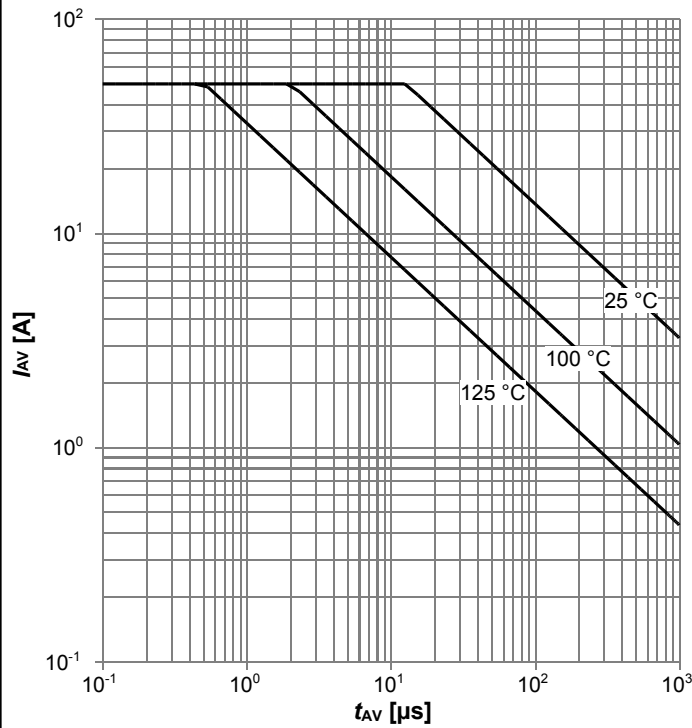
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

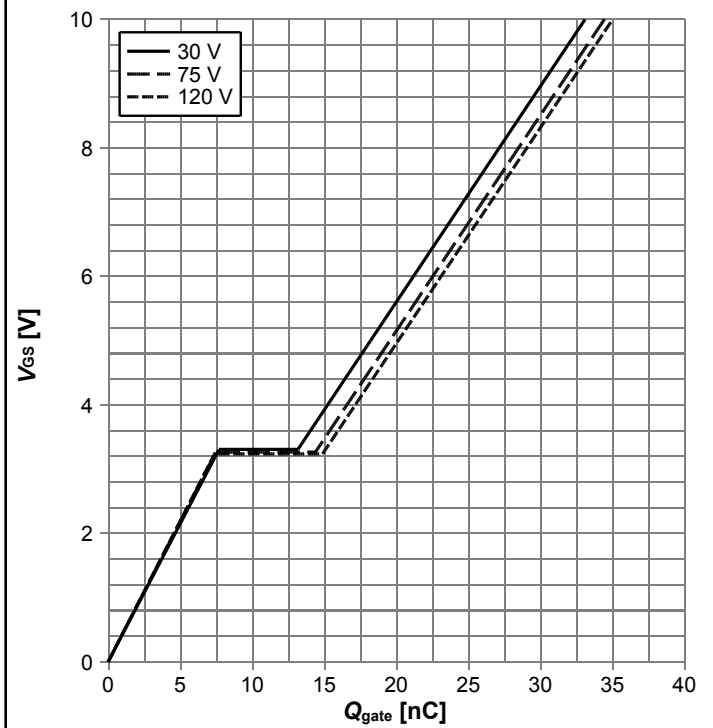


**Diagram 13: Avalanche characteristics**



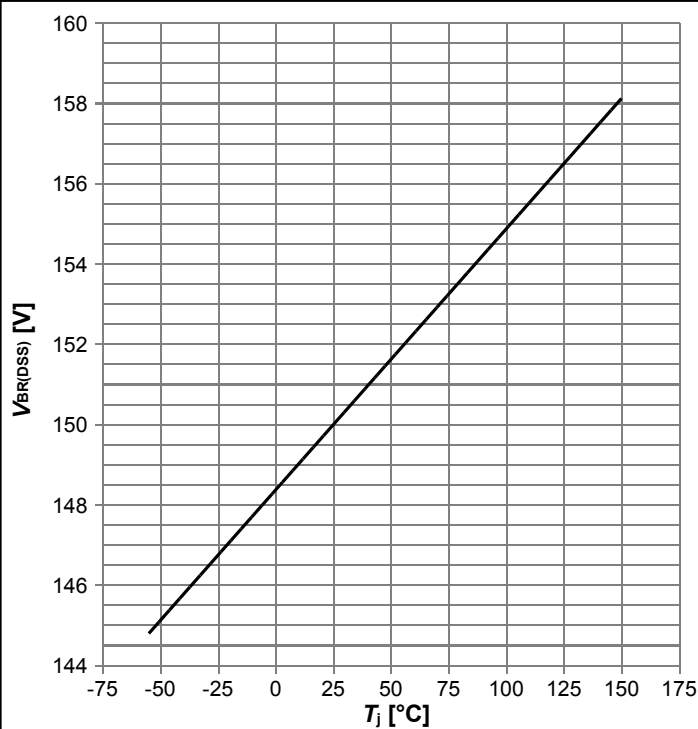
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

**Diagram 14: Typ. gate charge**



$V_{GS}=f(Q_{gate}), I_D=40$  A pulsed,  $T_j=25$  °C; parameter:  $V_{DD}$

**Diagram 15: Min. drain-source breakdown voltage**

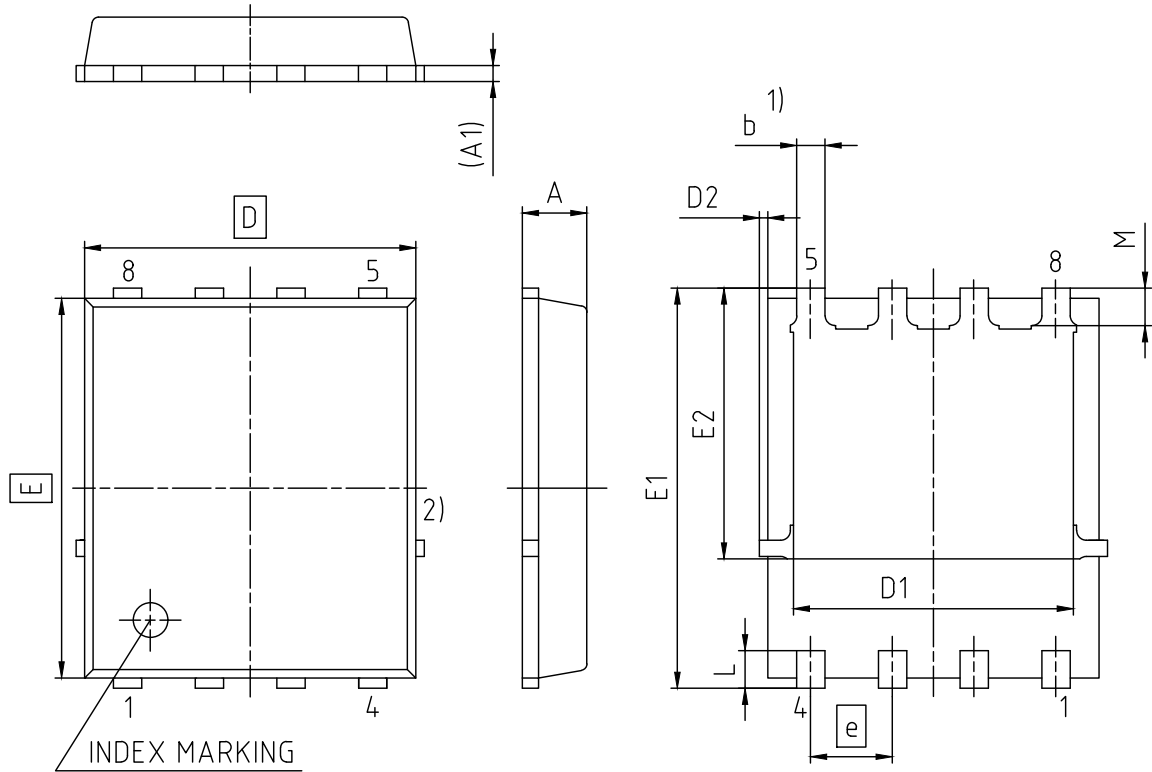


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

**Diagram Gate charge waveforms**



## 5 Package Outlines



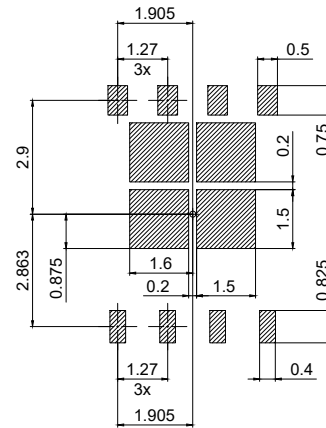
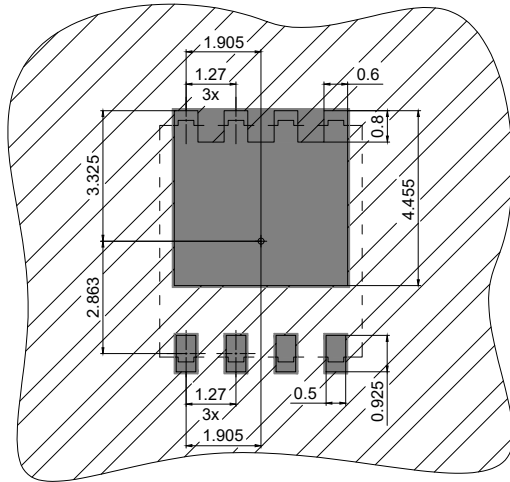
- 1) EXCLUDING MOLD FLASH  
 2) REMOVAL ON MOLD GATE  
 INTRUSION 0.1 MM  
 PROTRUSION 0.1 MM  
 LEAD LENGTH UP TO ANTI FLASH LINE  
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

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Figure 1 Outline PG-TDSON-8, dimensions in mm

PG-TDSON-8: Recommended Boardpads & Apertures



■ copper

▨ solder mask

▩ stencil apertures

all dimensions in mm

Figure 2 Outline Boardpads (TDSON-8), dimensions in mm

## Revision History

BSC105N15LS5

Revision: 2023-12-13, Rev. 2.0

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-13	Release of final version

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