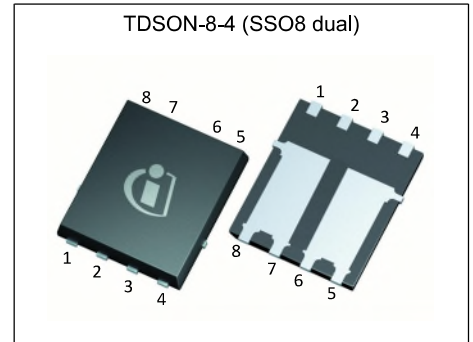


MOSFET

OptiMOS™-T2 Power Transistor, 60 V

Features

- Dual N-channel, Logic level
- Fast switching MOSFETs for SMPS
- Optimized technology for Synchronous Rectification
- Pb-free plating; RoHS compliant
- 100% Avalanche tested
- Superior Thermal Resistance
- Halogen-free according to IEC61249-2-21

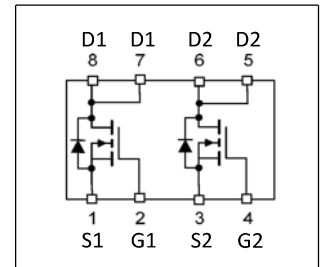


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	11.2	mΩ
I_D	57	A



Type / Ordering Code	Package	Marking	Related Links
BSC112N06LD	PG-TDSON-8-4	112N06LD	-

Table of Contents

Description	1
Maximum ratings	3
Thermal characteristics	3
Electrical characteristics	4
Electrical characteristics diagrams	6
Package Outlines	10
Revision History	11
Trademarks	11
Disclaimer	11

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified, one transistor active

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	57	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	228	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	80	mJ	$I_D=10\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	-	-	65	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	2.3	°C/W	-
Device on PCB, 6 cm ² cooling area ⁴⁾	R_{thJA}	-	-	60	°C/W	-
Device on PCB, minimal footprint ⁵⁾	R_{thJA}	-	-	100	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ device mounted on a minimum pad (one layer, 70 µm thick)

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.2	V	$V_{DS}=V_{GS}$, $I_D=28\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 5.0	1.0 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=16\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	9.5 12.5	11.2 15.8	m Ω	$V_{GS}=10\text{ V}$, $I_D=17\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	3090	4020	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	590	770	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	28	56	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=11\text{ }\Omega$
Rise time	t_r	-	3	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=11\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	51	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=11\text{ }\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=11\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	13	nC	$V_{DD}=30\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	3.4	6.7	nC	$V_{DD}=30\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	41	55	nC	$V_{DD}=30\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	$V_{DD}=30\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition. Defined by design, not subject to production test

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	38	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	228	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.88	1.1	V	$V_{GS}=0\text{ V}, I_F=17\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	35	-	ns	$V_R=30\text{ V}, I_F=9\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	35	-	nC	$V_R=30\text{ V}, I_F=9\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

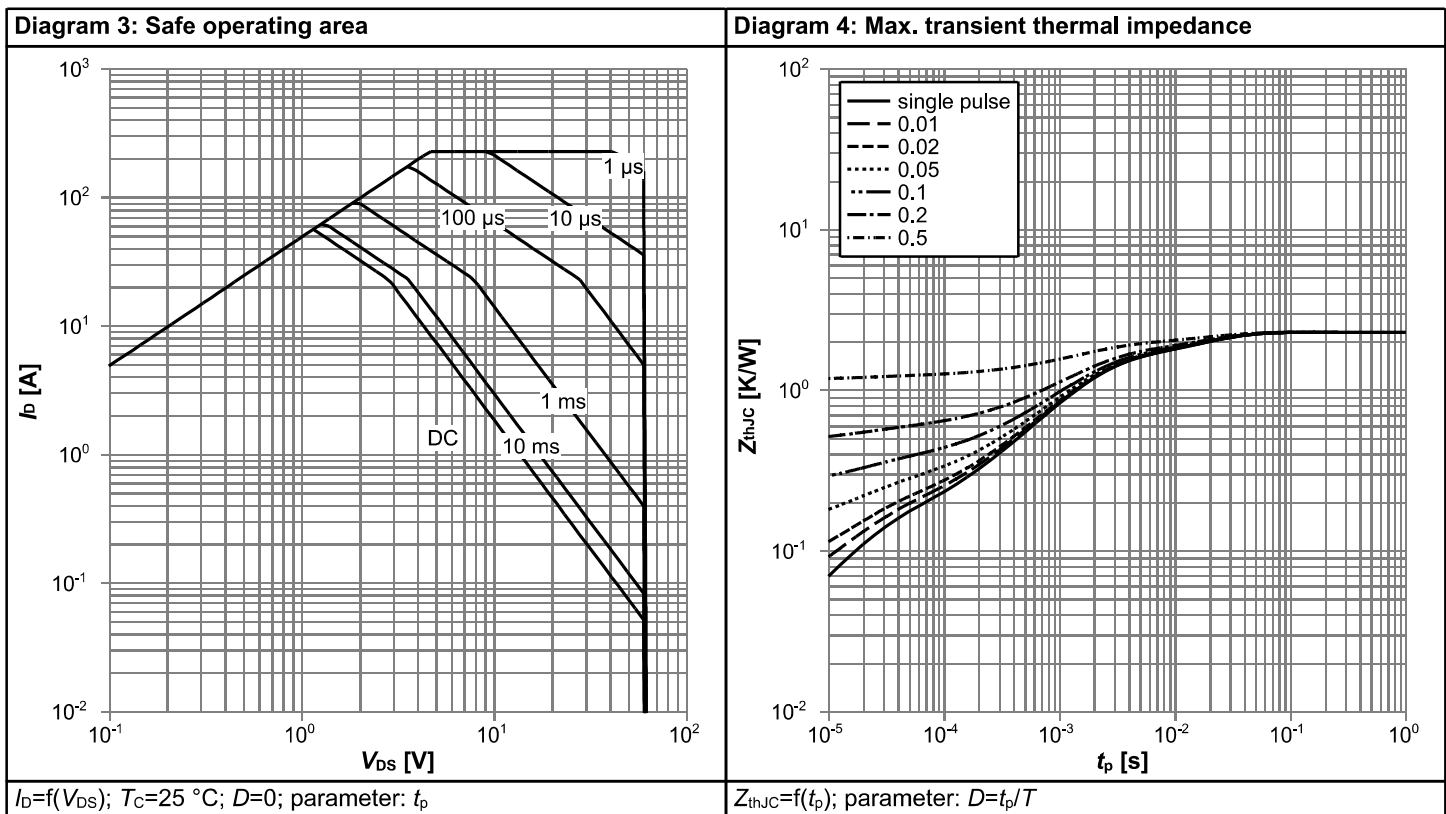
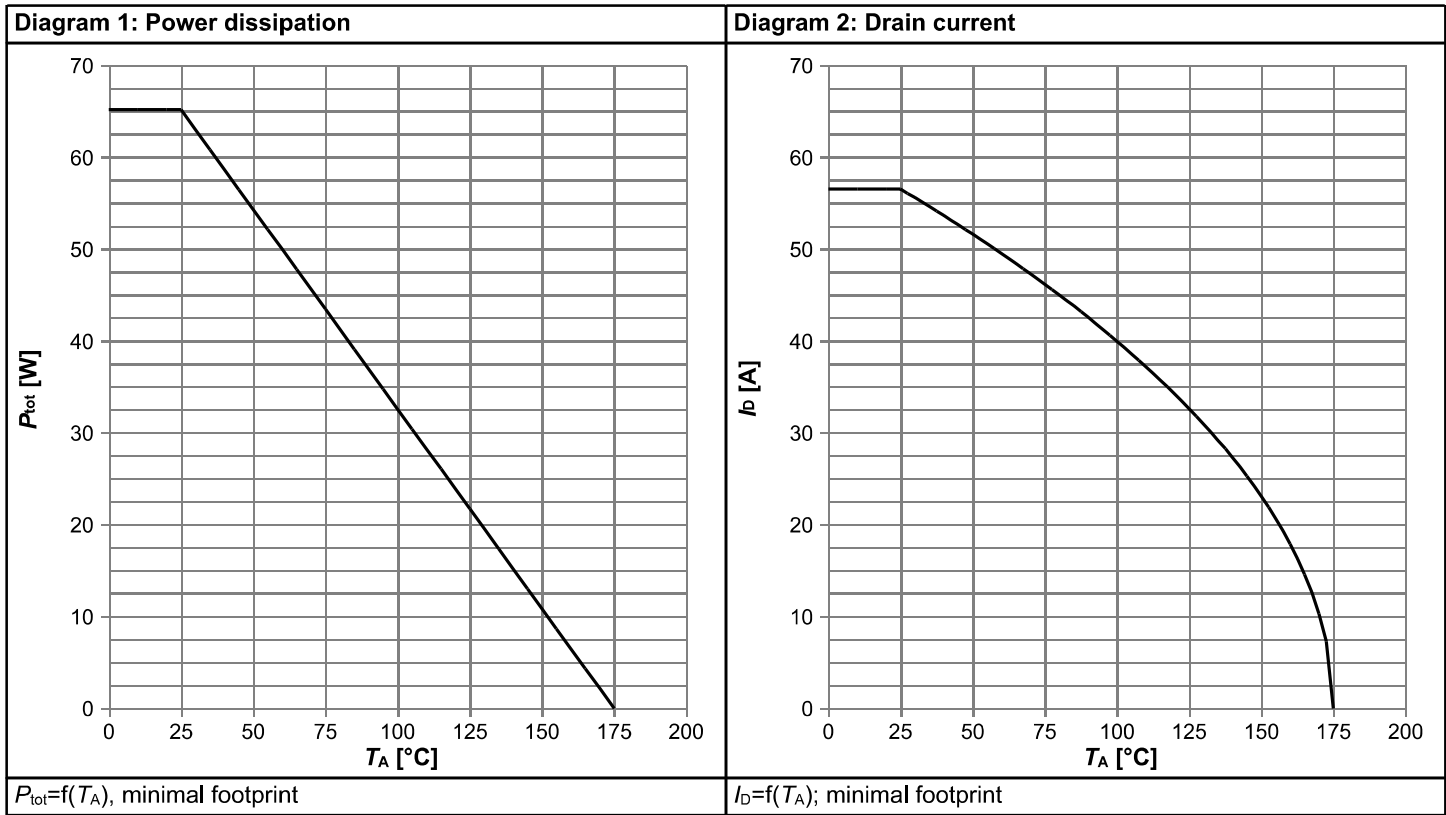
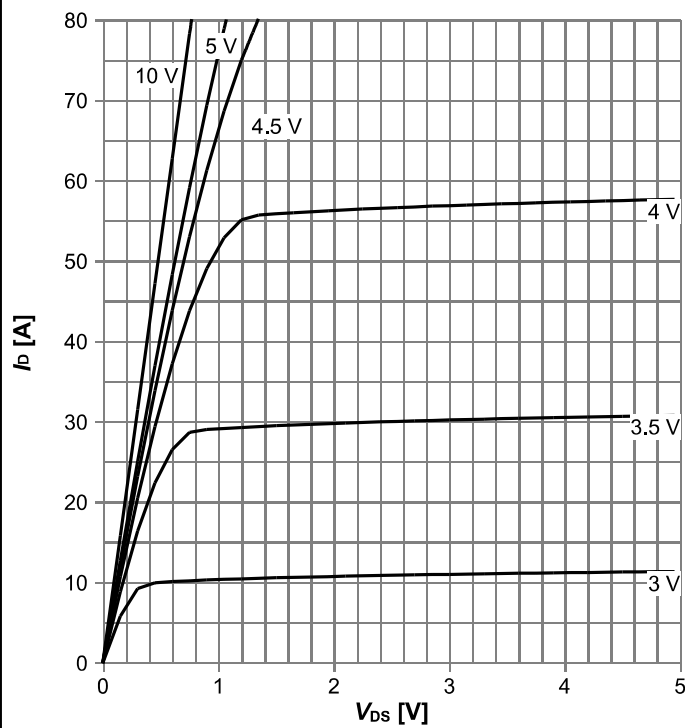
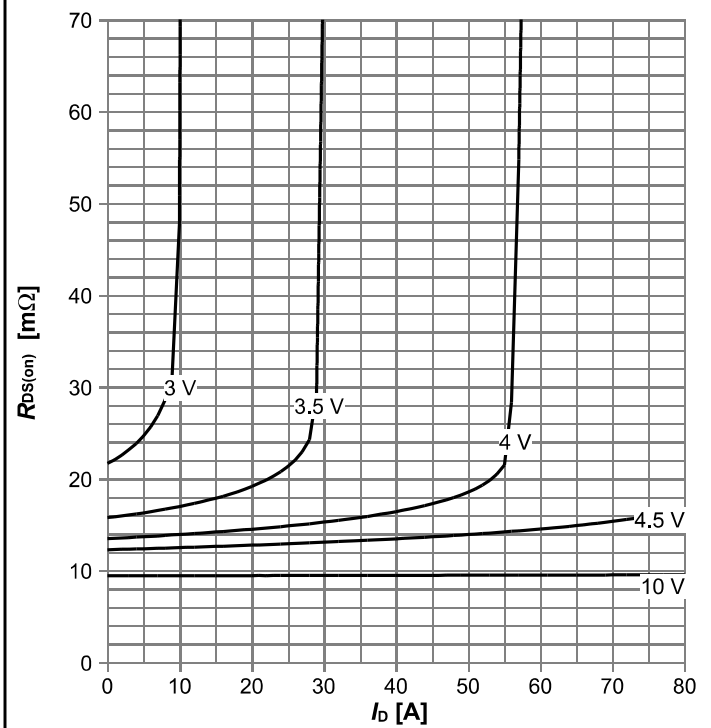


Diagram 5: Typ. output characteristics



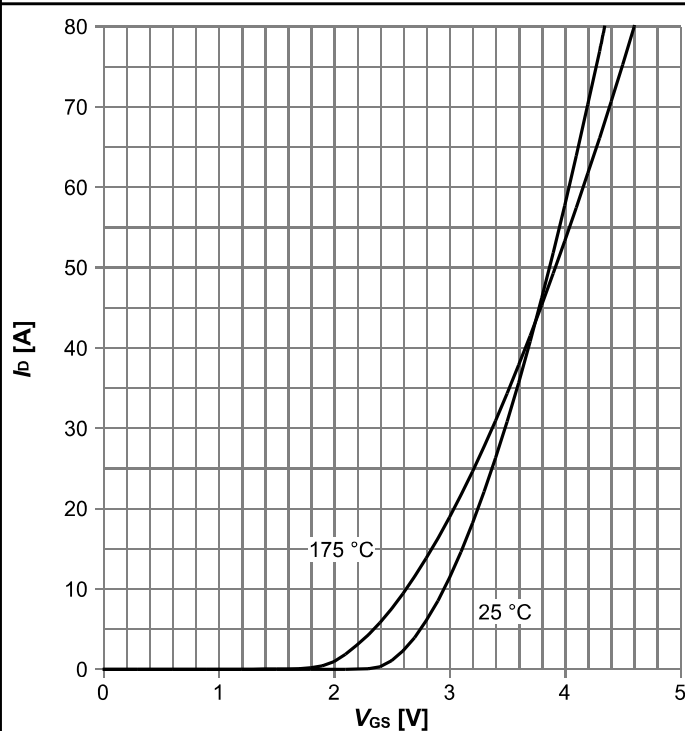
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



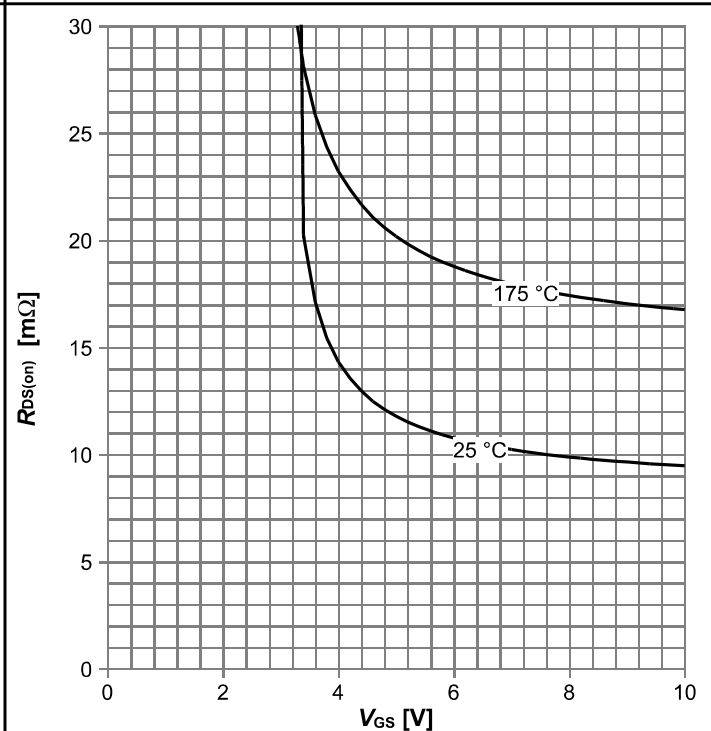
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



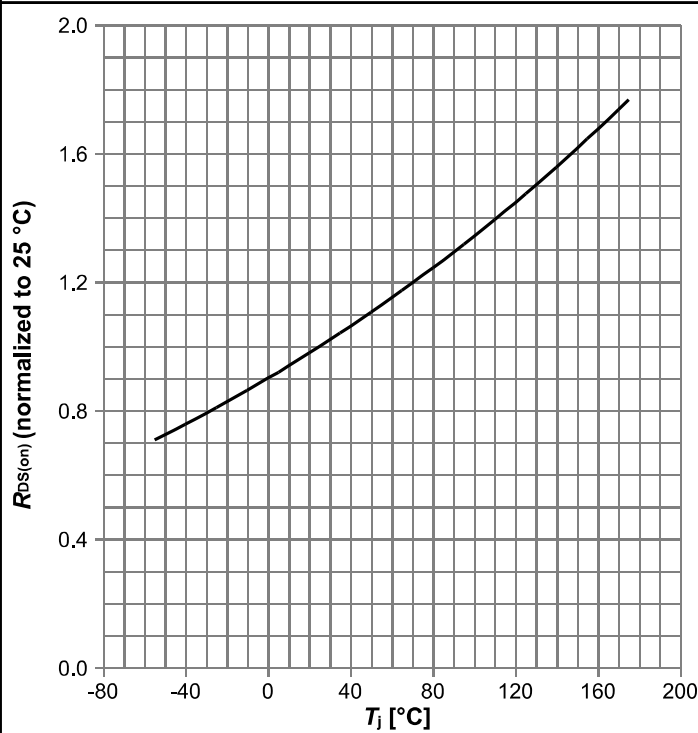
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



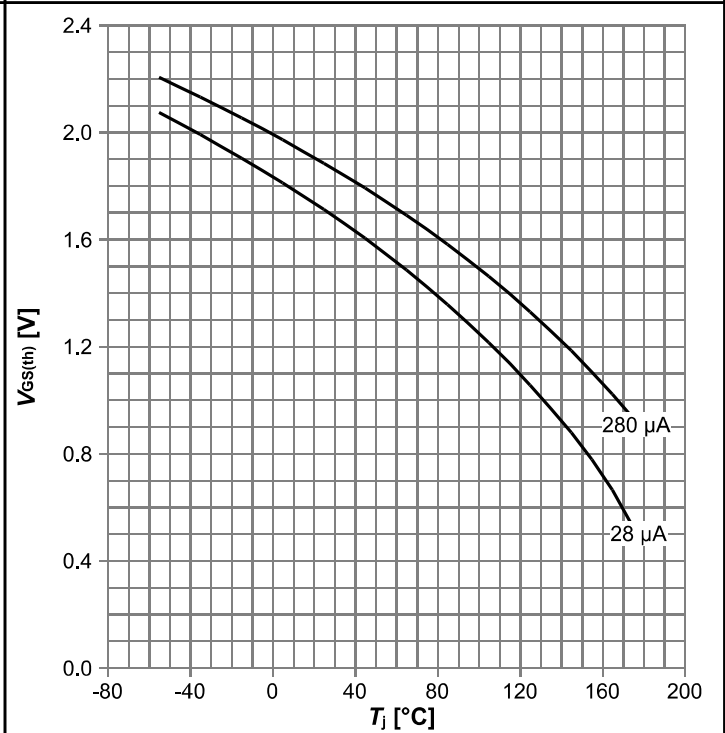
$R_{DS(on)} = f(V_{GS})$, $I_D = 17\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



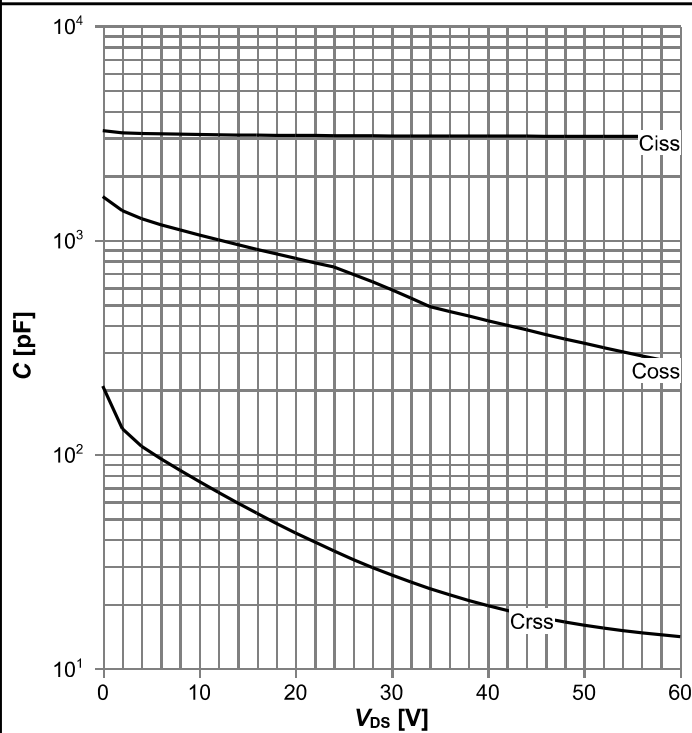
$R_{DS(on)}=f(T_j)$, $I_D=17$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



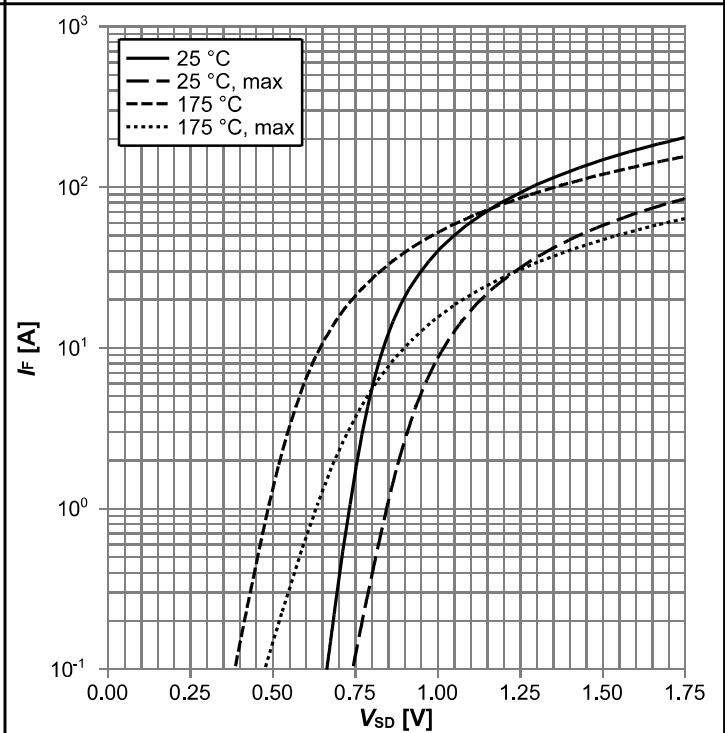
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



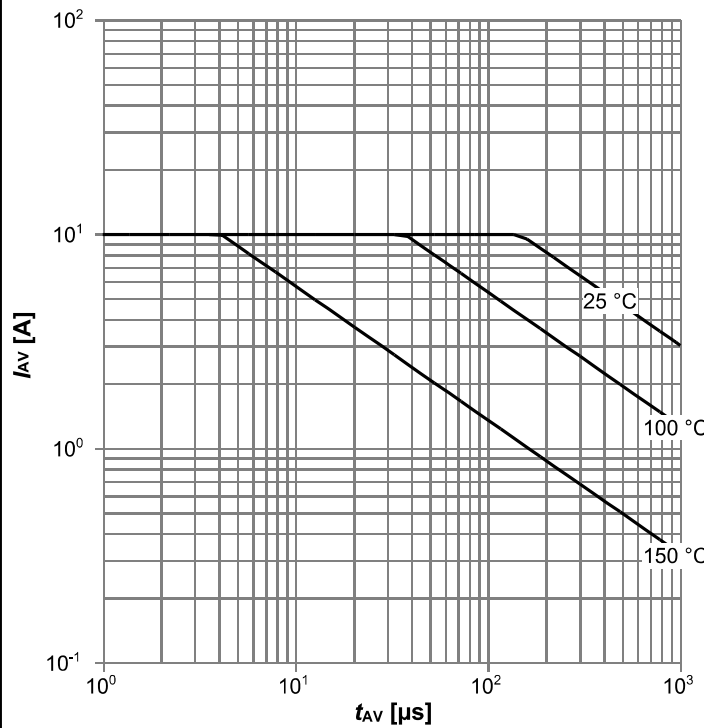
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



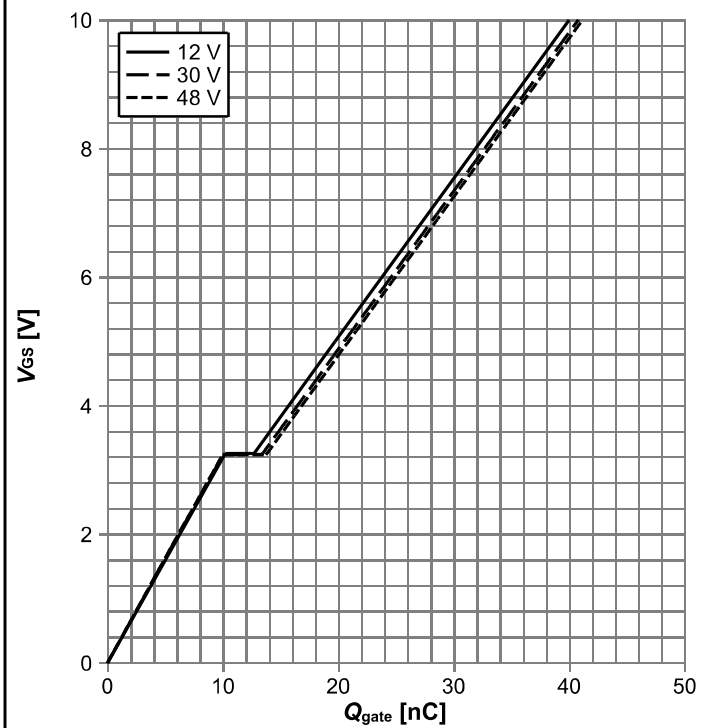
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



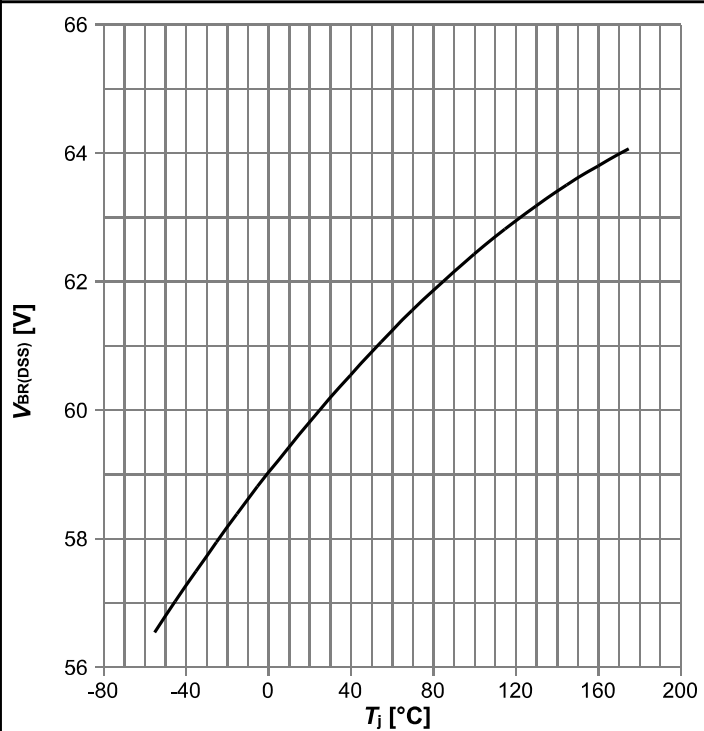
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega; \text{parameter: } T_{j,start}$

Diagram 14: Typ. gate charge



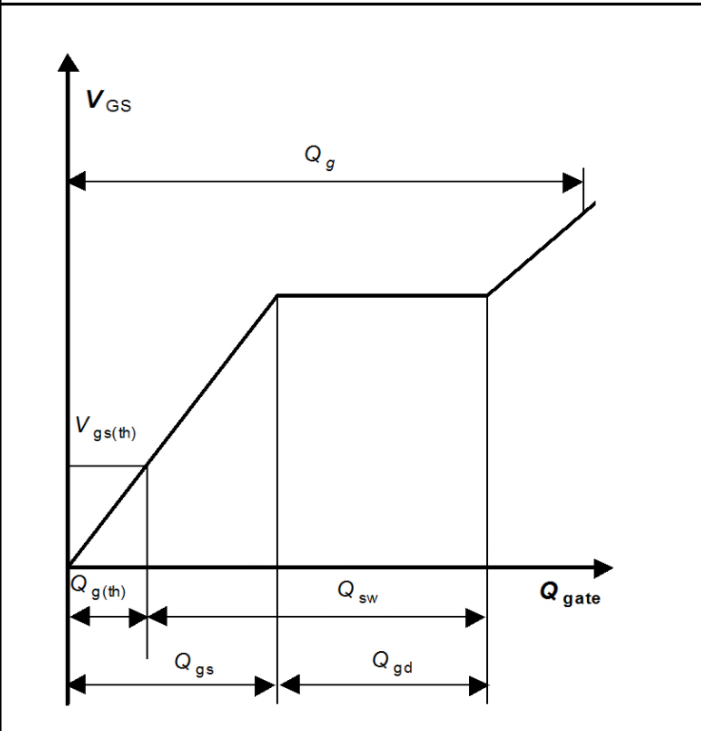
$V_{GS}=f(Q_{gate}), I_D=20 \text{ A pulsed}, T_j=25 \text{ °C}; \text{parameter: } V_{DD}$

Diagram 15: Drain-source breakdown voltage

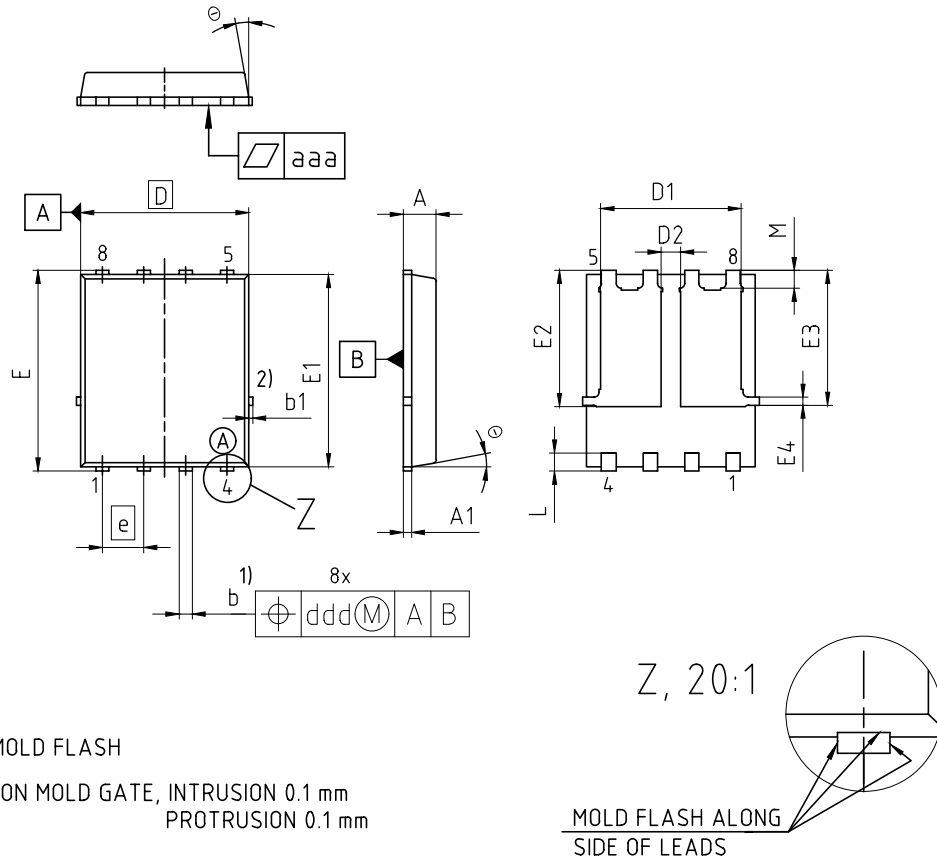


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



- 1) EXCLUDE MOLD FLASH
- 2) REMOVAL ON MOLD GATE, INTRUSION 0.1 mm
PROTRUSION 0.1 mm

ALL METAL SURFACES ARE PLATED EXCEPT AREA OF CUT

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
A1	0.15	0.35
b	0.34	0.54
b1	0.02	0.22
D	4.95	5.35
D1	4.20	4.40
D2	0.50	0.70
E	5.95	6.35
E1	5.70	6.10
E2	4.075	4.275
E3	4.035	4.235
E4	0.15	0.35
e	1.27	
L	0.45	0.65
M	0.45	0.65
ø	8.5°	11.5°
aaa	0.05	
ddd	0.10	

DOCUMENT NO. Z8B00189767
REVISION 01
SCALE 5:1 0 1 2 3 4mm
EUROPEAN PROJECTION
ISSUE DATE 31.07.2018

Figure 1 Outline PG-TDSON-8-4, dimensions in mm

Revision History

BSC112N06LD

Revision: 2021-06-28, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-12-11	Release of final version
2.1	2021-06-28	Update current rating, footnotes and Id Diagram 9

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