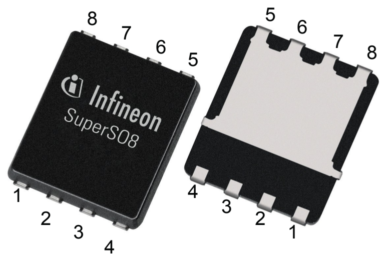
MOSFET

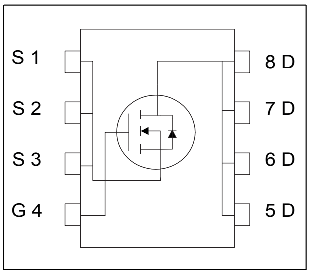
OptiMOS™ 2 Power-Transistor, 120 V

Features

- N-channel, logic level
- Excellent gate charge x RDS(on) product (FOM)
- Very low on-resistance RDS(on)
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

SuperSO8





Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	120	V
$R_{DS(on),max}$	12	mΩ
I_D	68	A
Q_{oss}	51	nC
Q_G(0V..10V)	51	nC

Type / Ordering Code	Package	Marking	Related Links
BSC120N12LS	PG-TDSON-8	120N12LS	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	68 53 10	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_A=25 °C, R_{THJA}=45 °C/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	274	A	T_A=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	155	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	114	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.64	1.1	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	18	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-
Thermal resistance, juntion - ambient, 6 cm² cooling area[2]	R_{thJA}	-	-	45	°C/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.85	2.4	V	V_{DS}=V_{GS}, I_D=72 µA
Zero gate voltage drain current	I_{DSS}	- -	0.01 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	9.8 11.7	12.0 14.2	mΩ	V_{GS}=10 V, I_D=34 A V_{GS}=4.5 V, I_D=17 A
Gate resistance[1]	R_G	-	0.7	-	Ω	-
Transconductance	g_{fs}	42	81	-	S	$\lvert V_{DS}\rvert \geq 2\lvert I_D\rvert R_{DS(on)max}$, I_D=34 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	3700	4900	pF	V_{GS}=0 V, V_{DS}=60 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	380	495	pF	V_{GS}=0 V, V_{DS}=60 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	19	25	pF	V_{GS}=0 V, V_{DS}=60 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	V_{DD}=60 V, V_{GS}=10 V, I_D=17 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	5	-	ns	V_{DD}=60 V, V_{GS}=10 V, I_D=17 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	22	-	ns	V_{DD}=60 V, V_{GS}=10 V, I_D=17 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	6	-	ns	V_{DD}=60 V, V_{GS}=10 V, I_D=17 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	11.4	-	nC	V_{DD}=60 V, I_D=17 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	8.4	-	nC	V_{DD}=60 V, I_D=17 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	13.1	-	nC	V_{DD}=60 V, I_D=17 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	51	-	nC	V_{DD}=60 V, I_D=17 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	V_{DD}=60 V, I_D=17 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	51	-	nC	V_{DS}=60 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

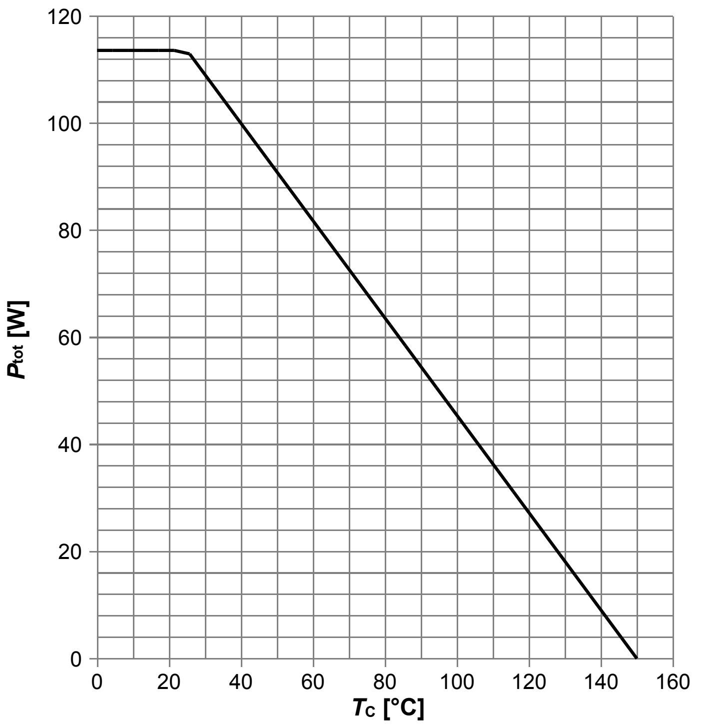
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	79	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	274	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.87	1.2	V	V_{GS}=0 V, I_F=34 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	85	-	ns	V_R=60 V, I_F=17 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	220	-	nC	V_R=60 V, I_F=17 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

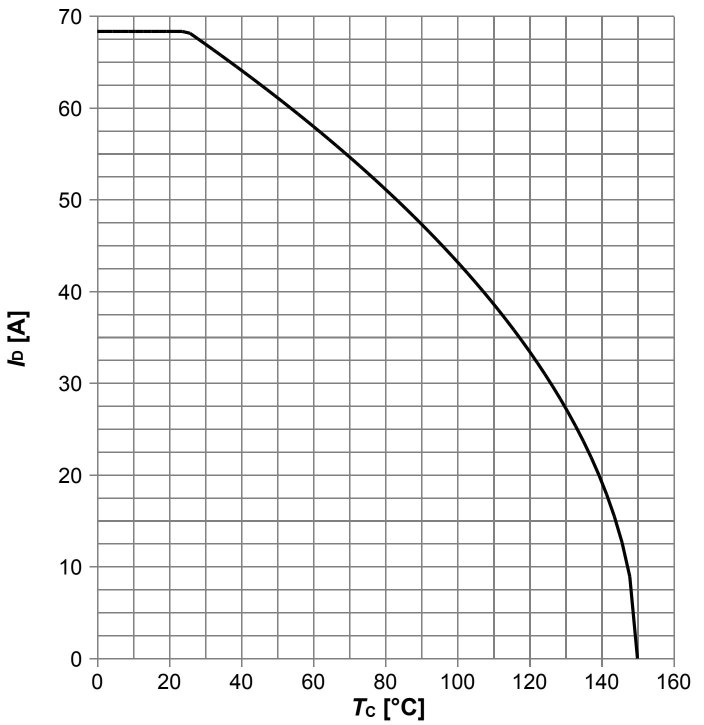
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



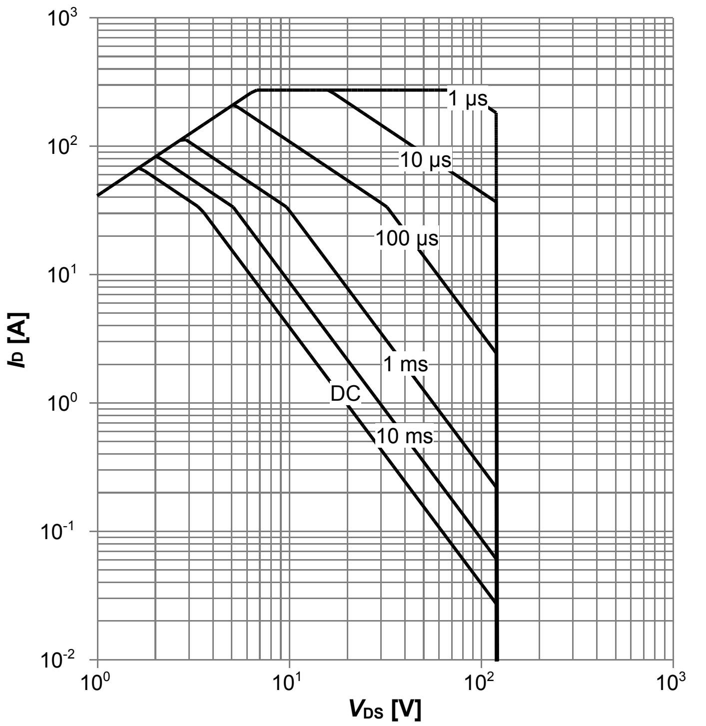
P_{tot}=f(T_C)

Diagram 2: Drain current



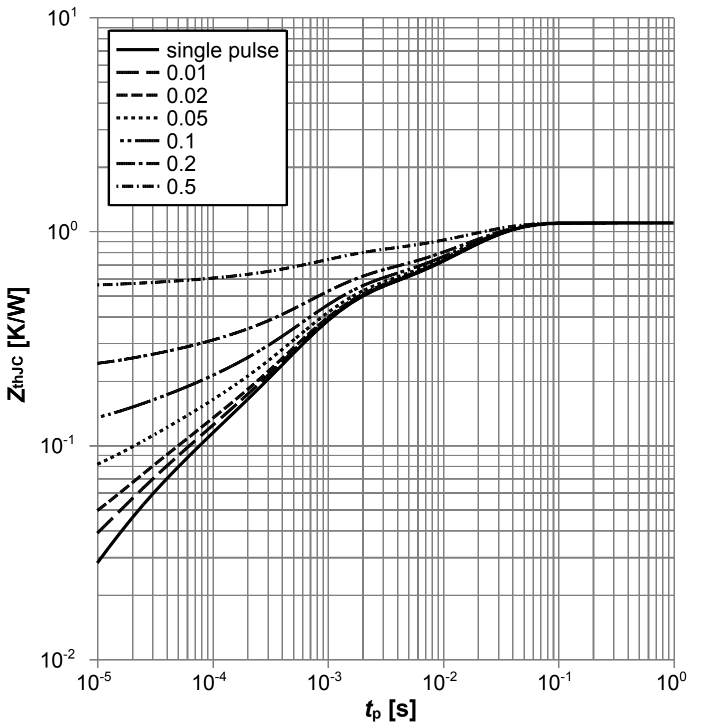
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



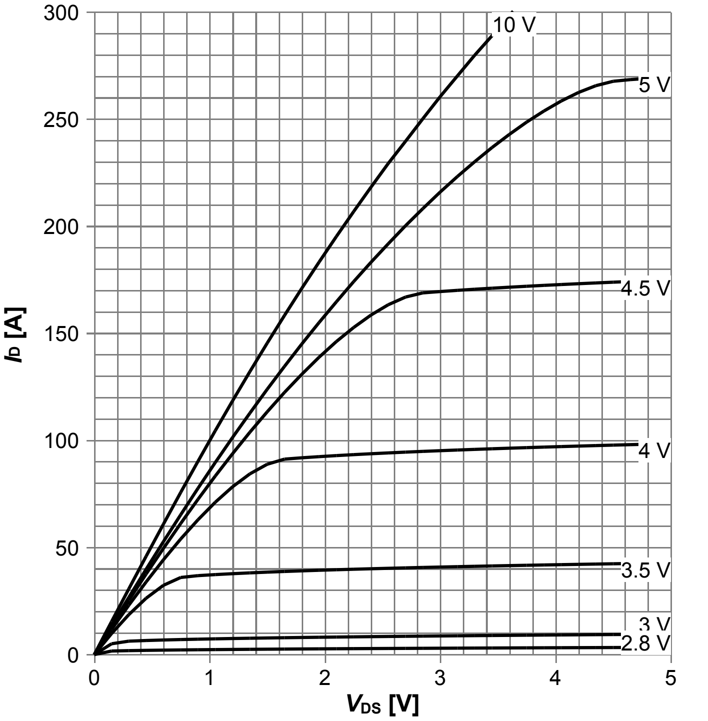
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



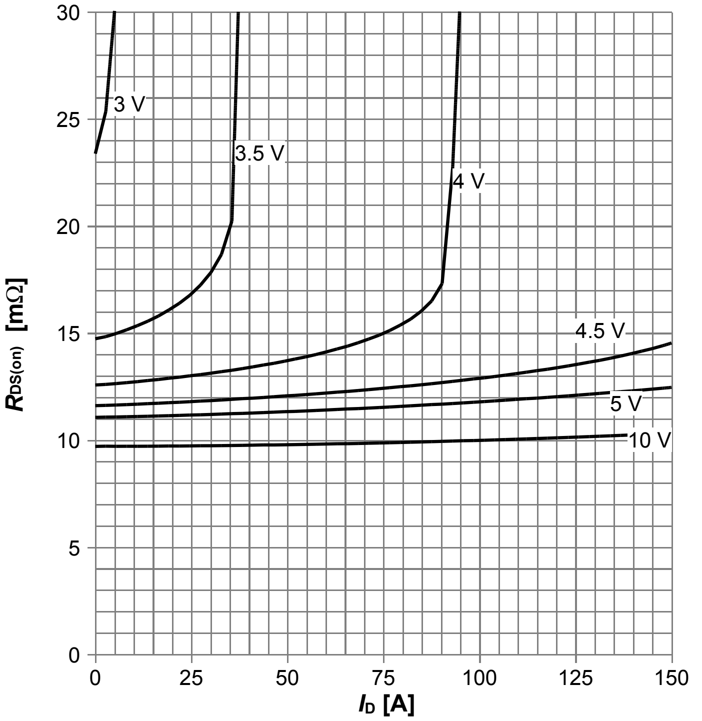
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



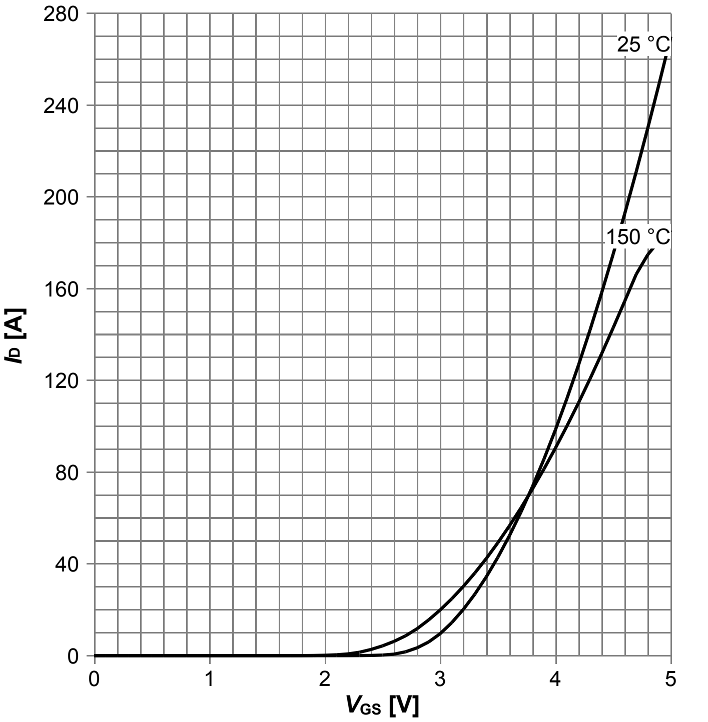
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



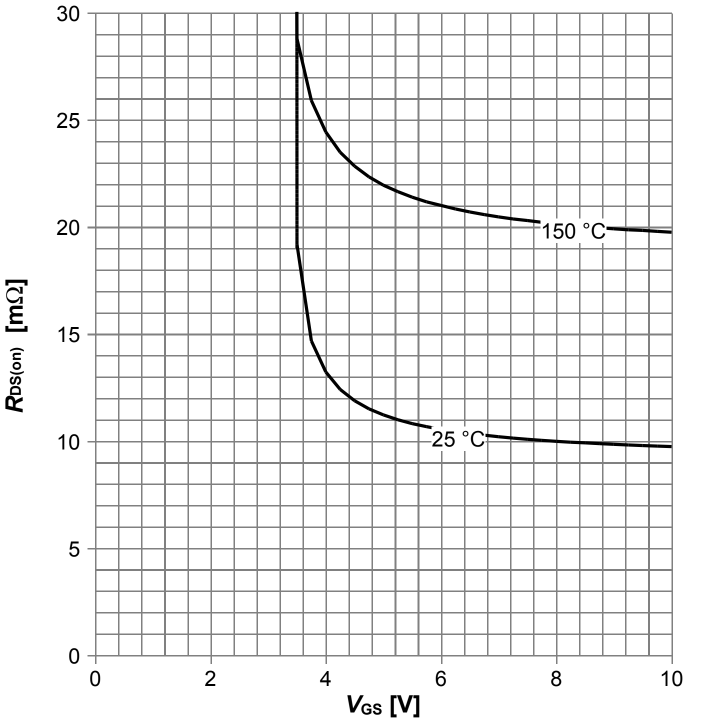
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



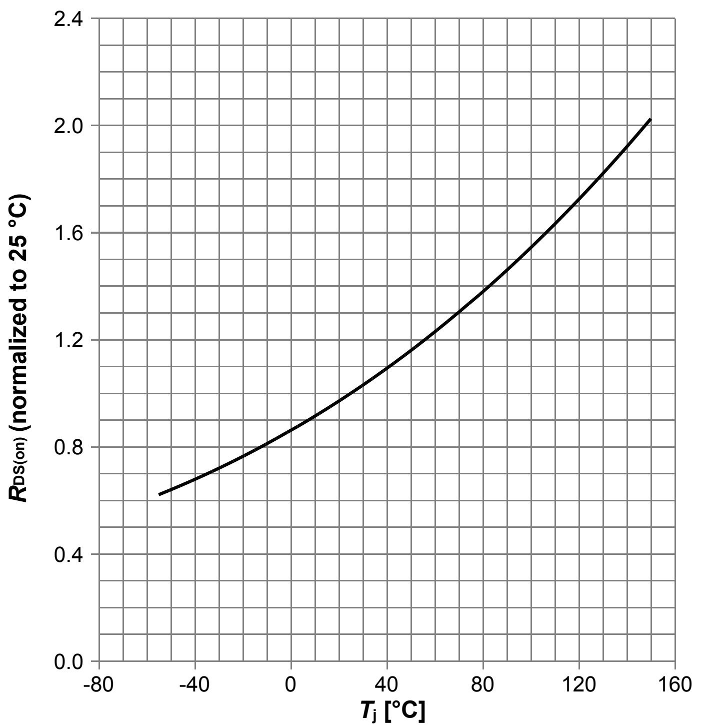
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



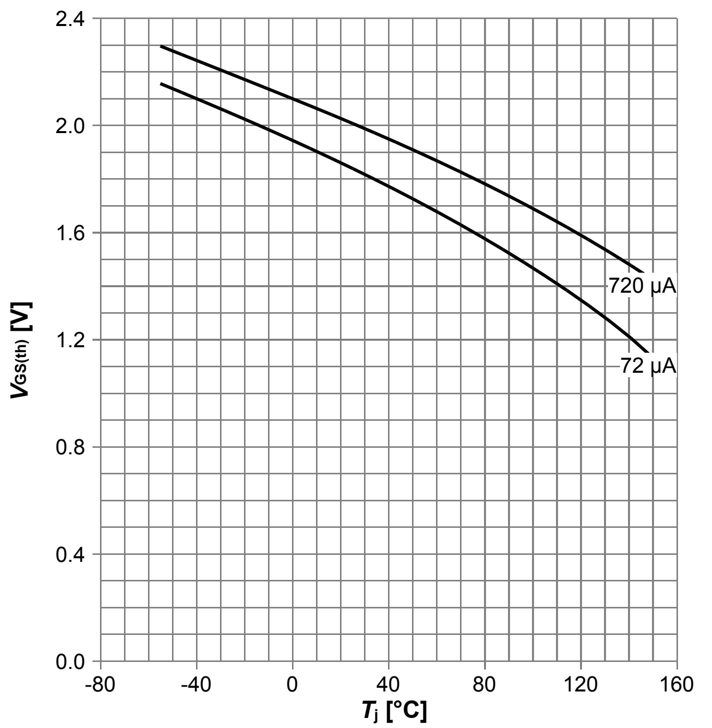
$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



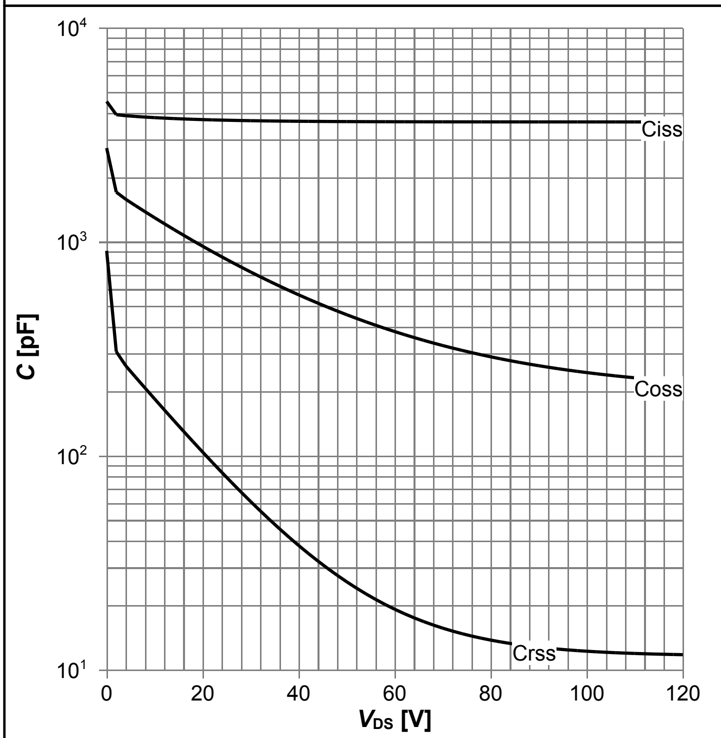
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



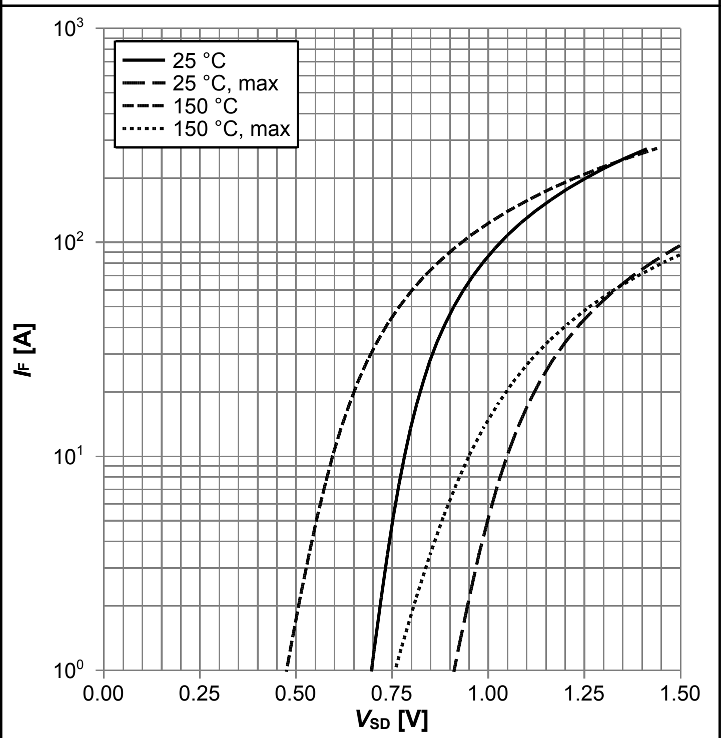
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



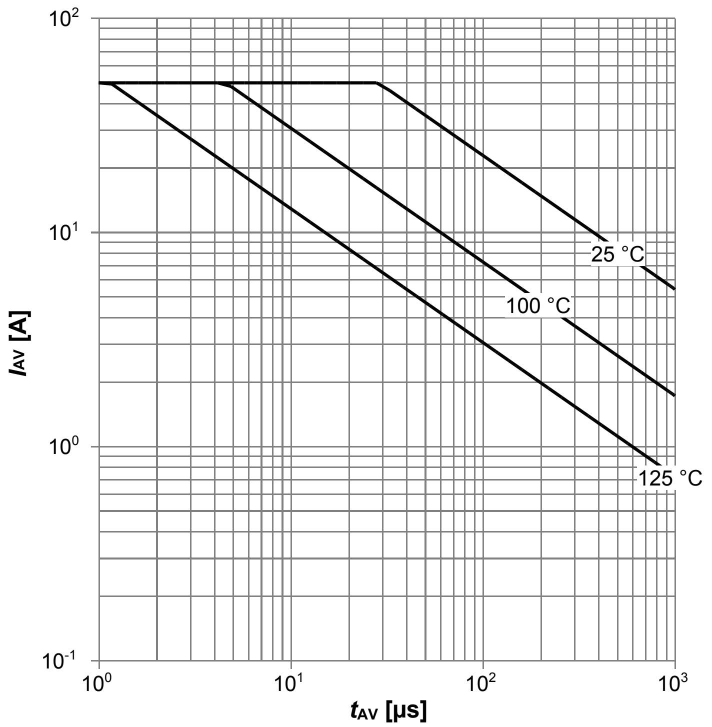
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



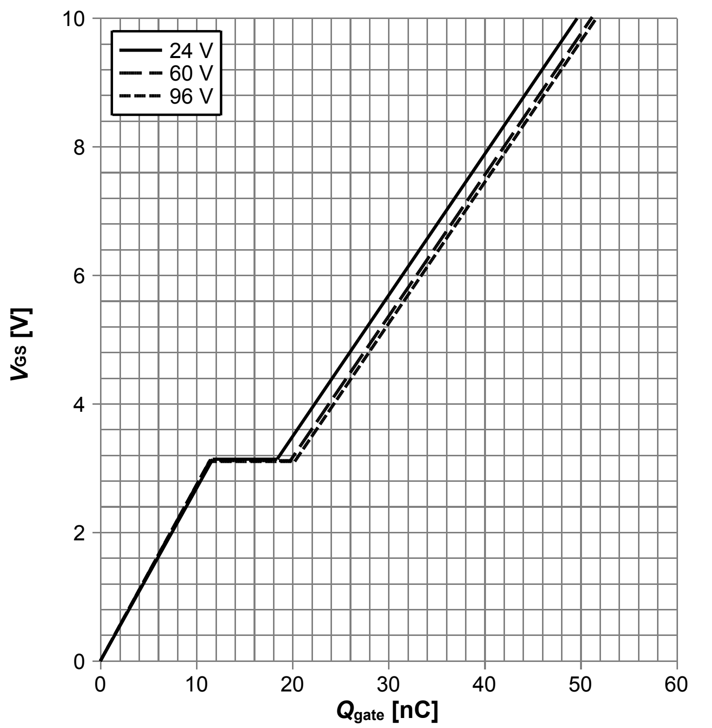
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



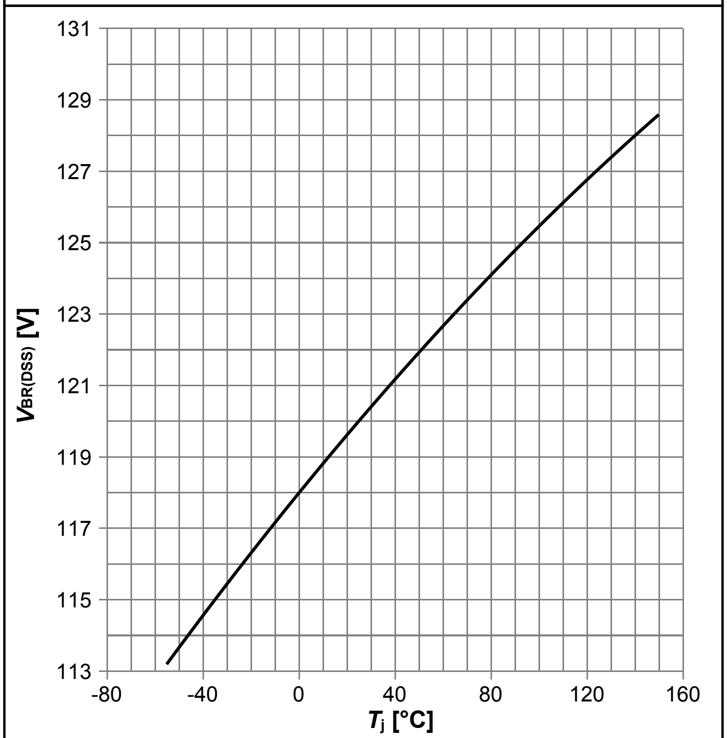
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



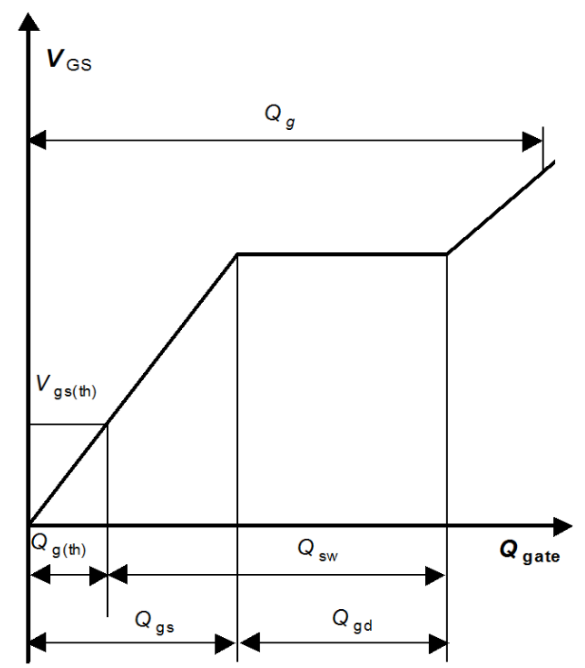
V_{GS}=f(Q_{gate}), I_D=25 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

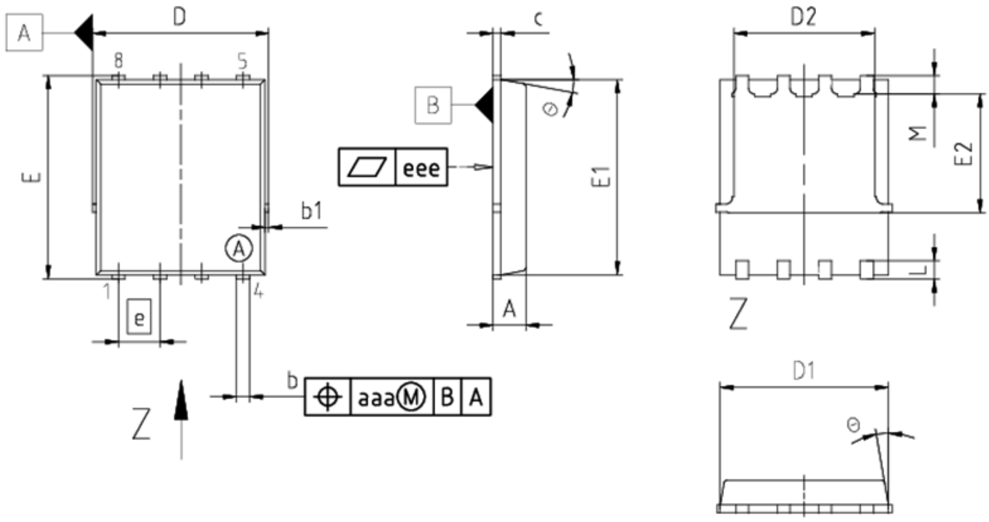


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
Θ	8.5°	12°
aaa	0.25	
eee	0.08	

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SCALE 0 2 4mm

EUROPEAN PROJECTION

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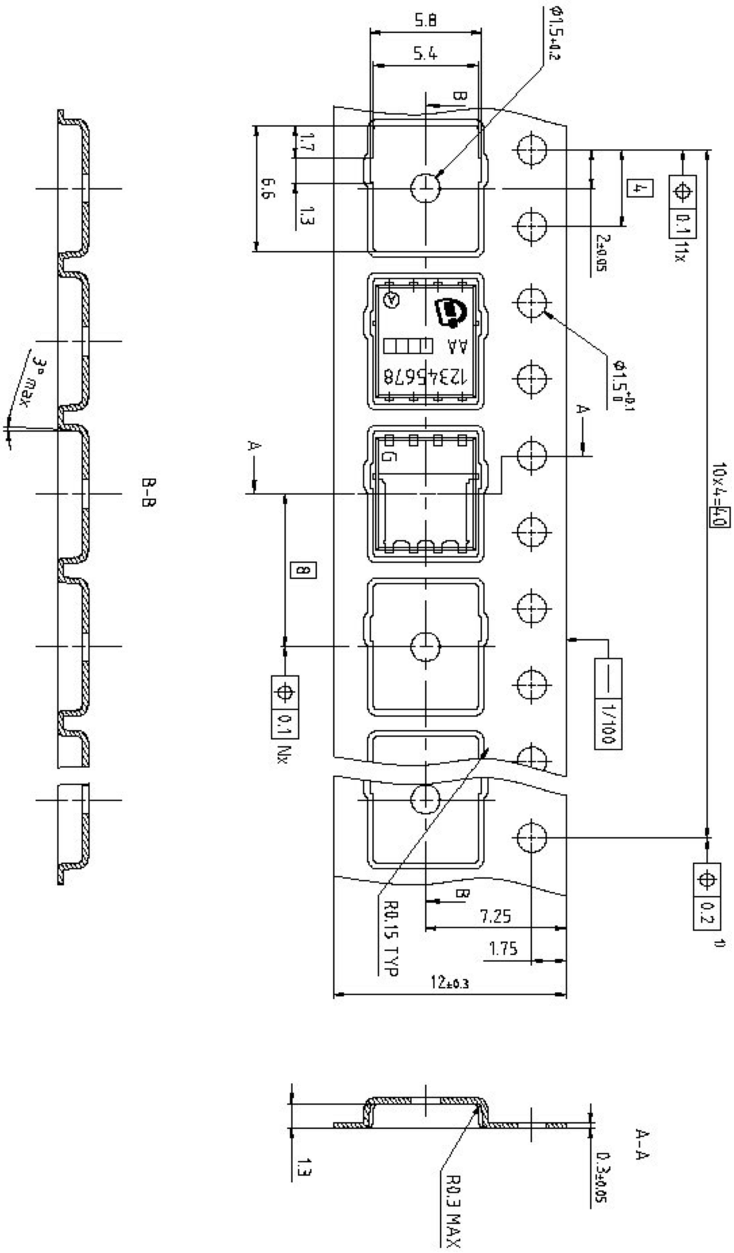
04

Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline Tape (TDSON-8)

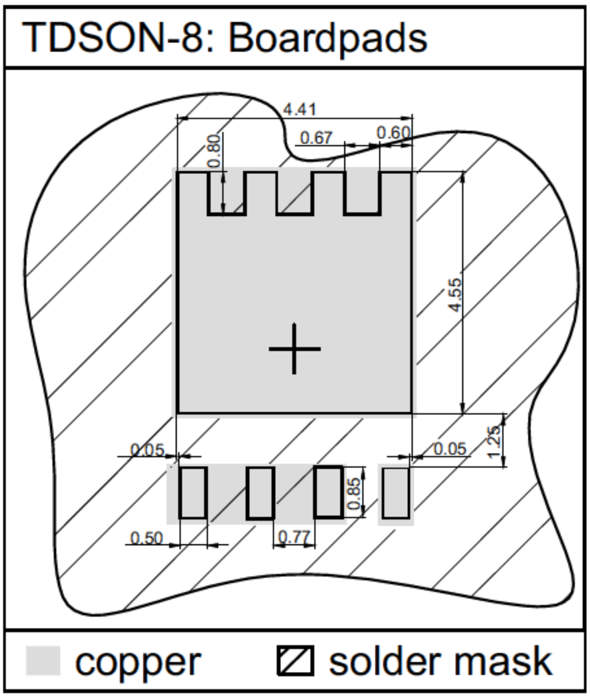


Figure 3 Outline Footprint (TDSON-8)

Revision History

BSC120N12LS

Revision: 2019-11-25, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-11-25	Release of final version

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