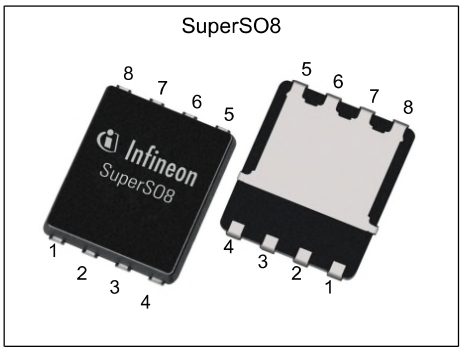
MOSFET

OptiMOS™ 5 Power-Transistor, 150 V



Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Very low reverse recovery charge (Qrr)
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Ideal for high-frequency switching and synchronous rectification

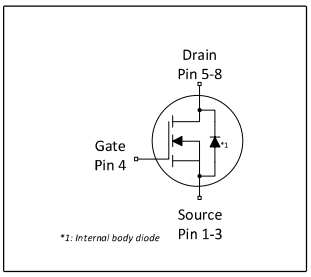


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	16	mΩ
I_D	56	A
Q_{rr}	25.7	nC

Type / Ordering Code	Package	Marking	Related Links
BSC160N15NS5	PG-TDSON-8	160N15NS	-

[1] J-STD20 and JESD22

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	56 36	A	T_C=25 °C T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	224	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	43	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	96	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.78	1.3	K/W	-
, 6 cm² cooling area[3]	R_{thJA}	-	-	50	K/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	V_{DS}=V_{GS}, I_D=60 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	13.7 15.1	16 18.5	mΩ	V_{GS}=10 V, I_D=28 A, V_{GS}=8 V, I_D=14 A
Gate resistance[4]	R_G	-	1	1.5	Ω	-
Transconductance	g_{fs}	20	40	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=28 A

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[4] Defined by design. Not subject to production test

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	1370	1820	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	341	454	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	9.6	17	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	9.6	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=28 A, $R_{G,ext}$=3 Ω
Rise time	t_r	-	3	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=28 A, $R_{G,ext}$=3 Ω
Turn-off delay time	$t_{d(off)}$	-	10.8	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=28 A, $R_{G,ext}$=3 Ω
Fall time	t_f	-	2.6	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=28 A, $R_{G,ext}$=3 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8	-	nC	V_{DD}=75 V, I_D=28 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	4	5.9	nC	V_{DD}=75 V, I_D=28 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	7.8	-	nC	V_{DD}=75 V, I_D=28 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	19	23.1	nC	V_{DD}=75 V, I_D=28 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	5.8	-	V	V_{DD}=75 V, I_D=28 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	51	68.2	nC	V_{DD}=75 V, V_{GS}=0 V

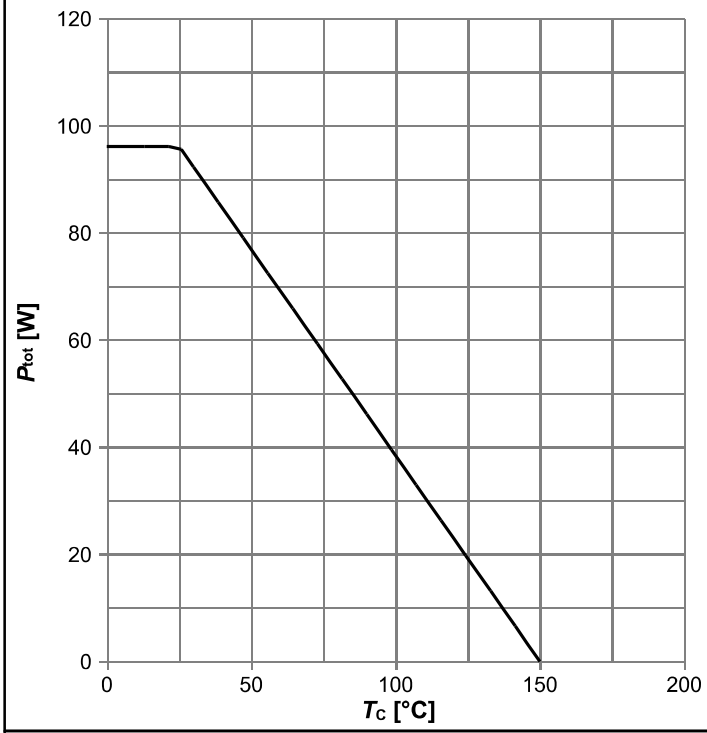
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	66	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	224	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.2	V	V_{GS}=0 V, I_F=28 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	30.5	61	ns	V_R=75 V, I_F=*28*, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	25.7	51.4	nC	V_R=75 V, I_F=*28*, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test
[2] See "Gate charge waveforms" for parameter definition

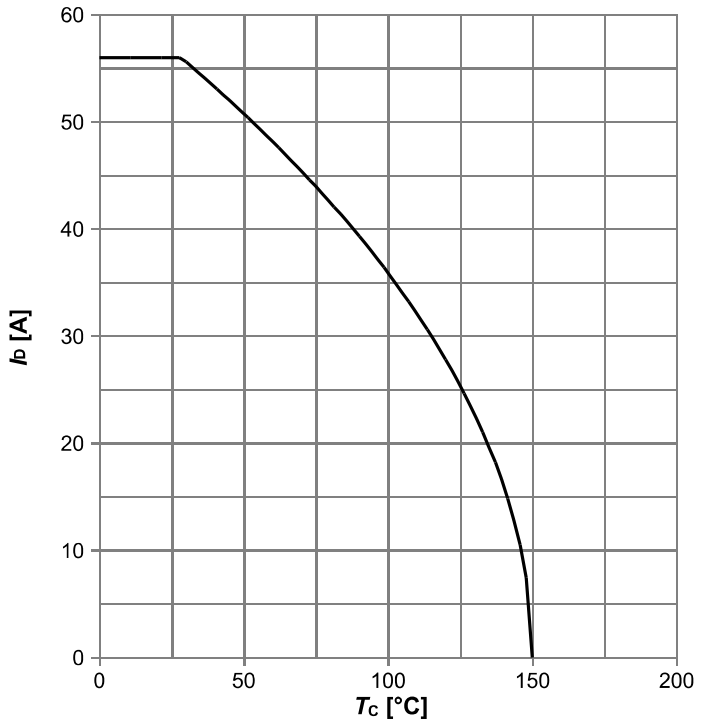
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



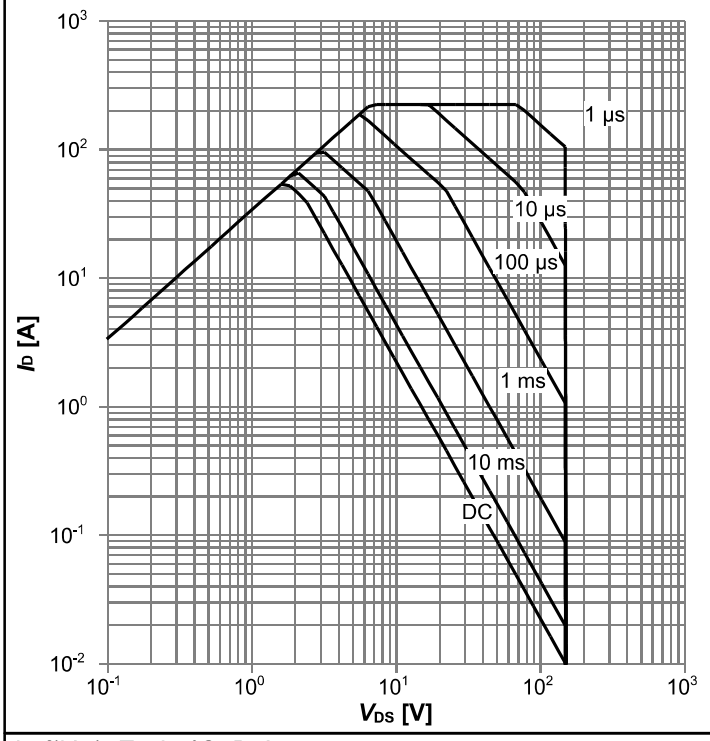
$P_{tot}=f(T_C)$

Diagram 2: Drain current



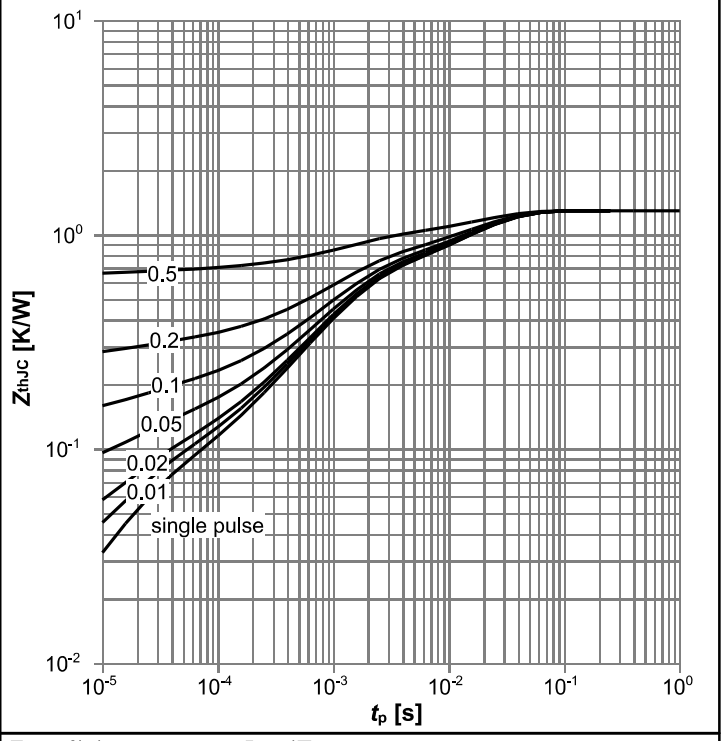
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



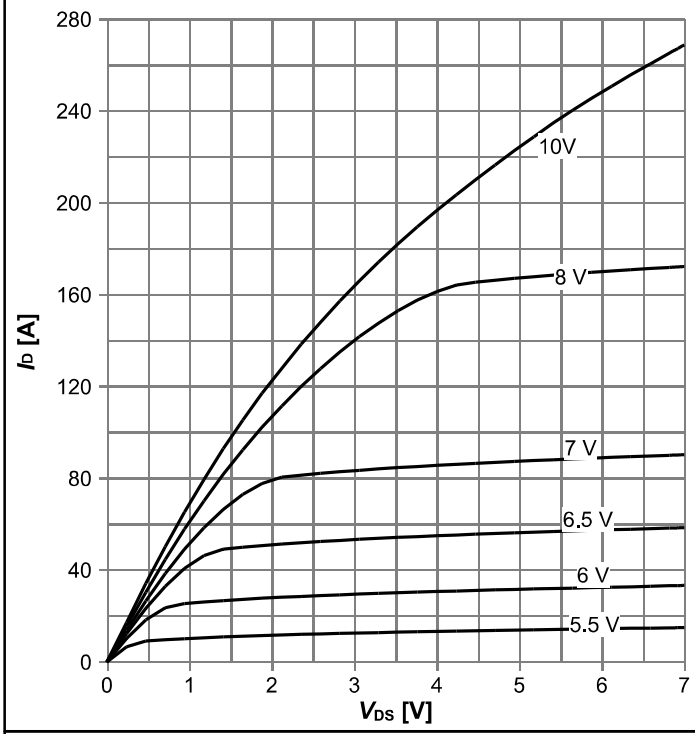
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



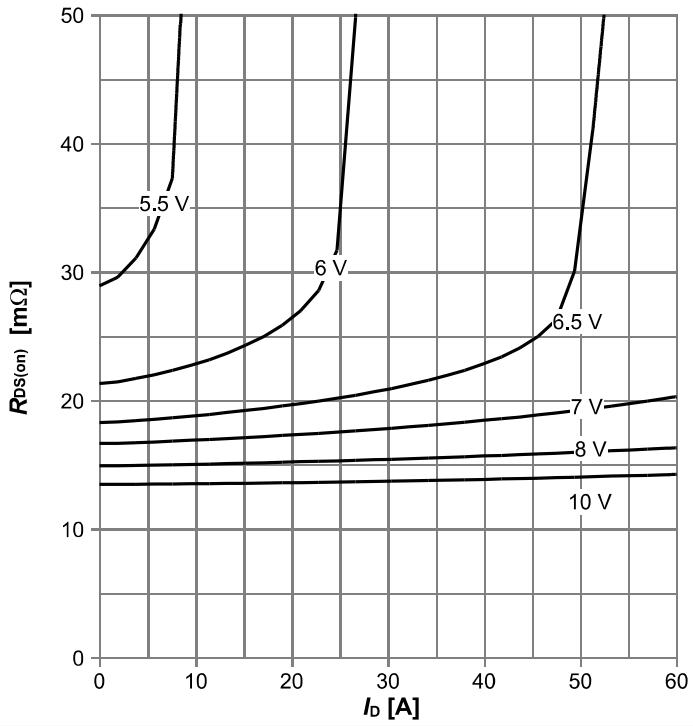
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



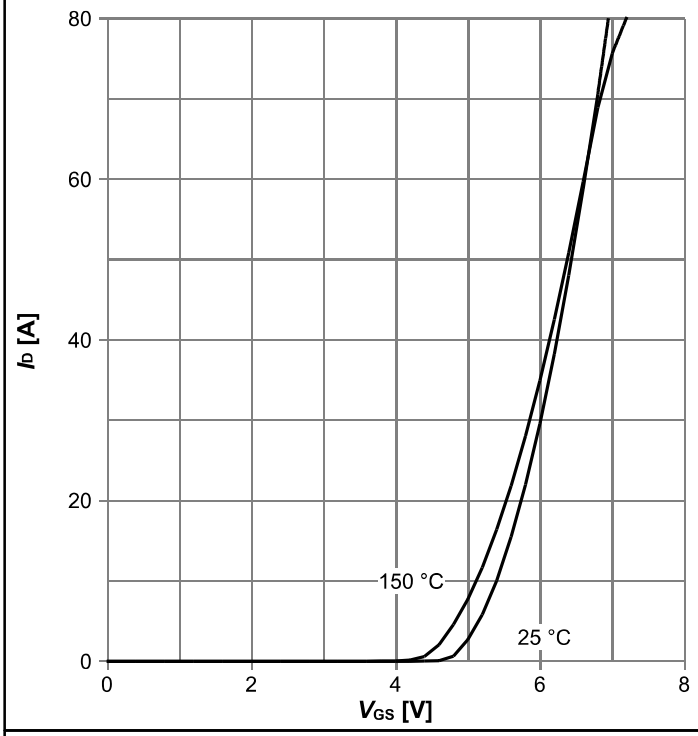
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



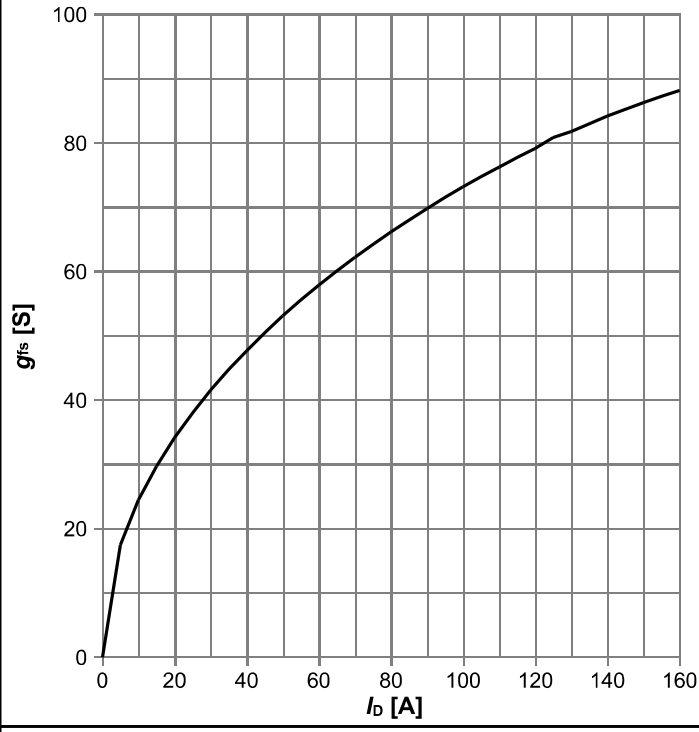
$R_{DS(on)}=f(I_D)$; $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



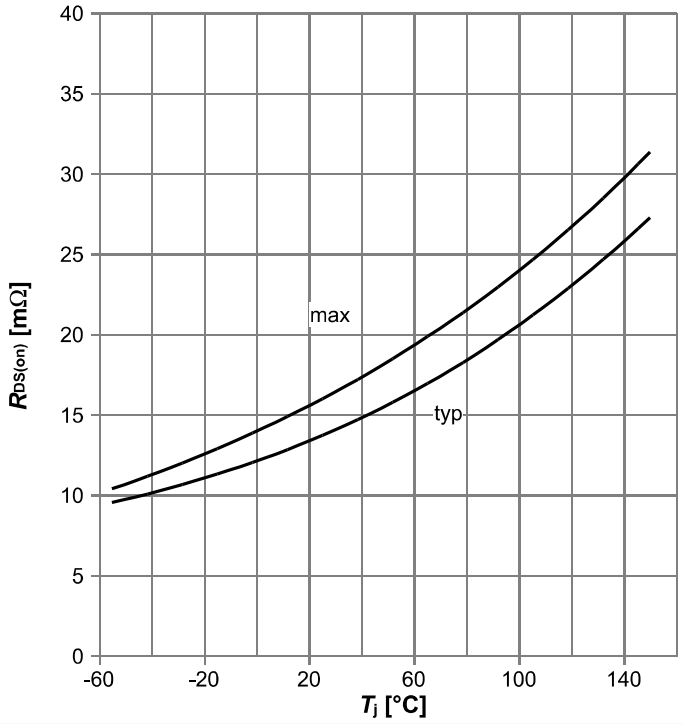
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



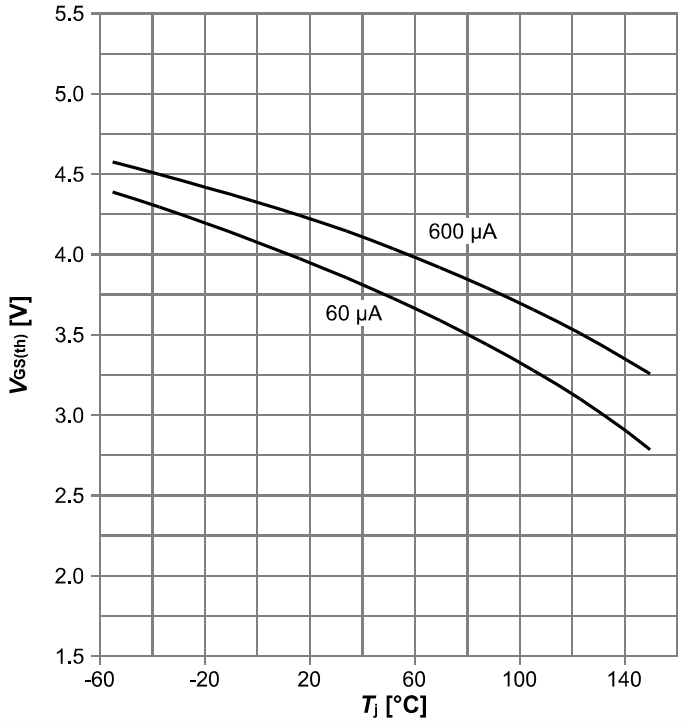
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on-state resistance



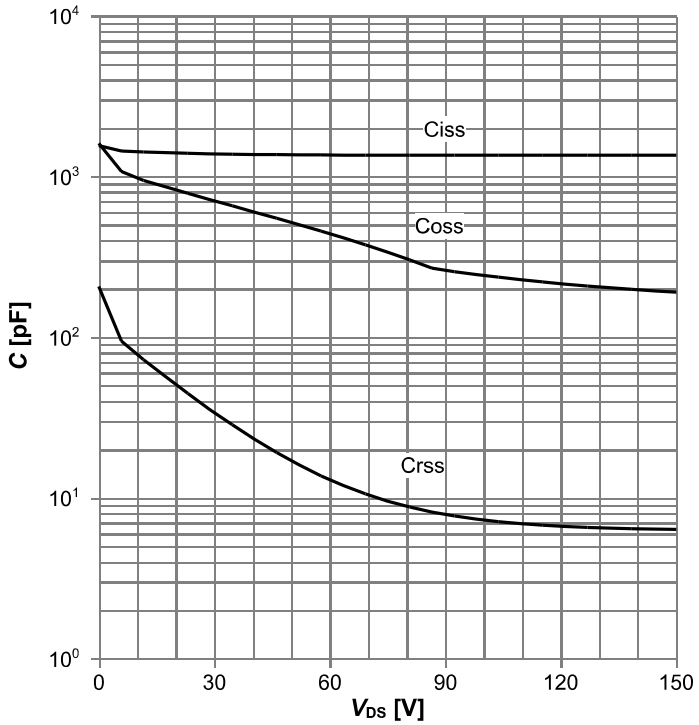
$R_{DS(on)}=f(T_j)$; I_D=28 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



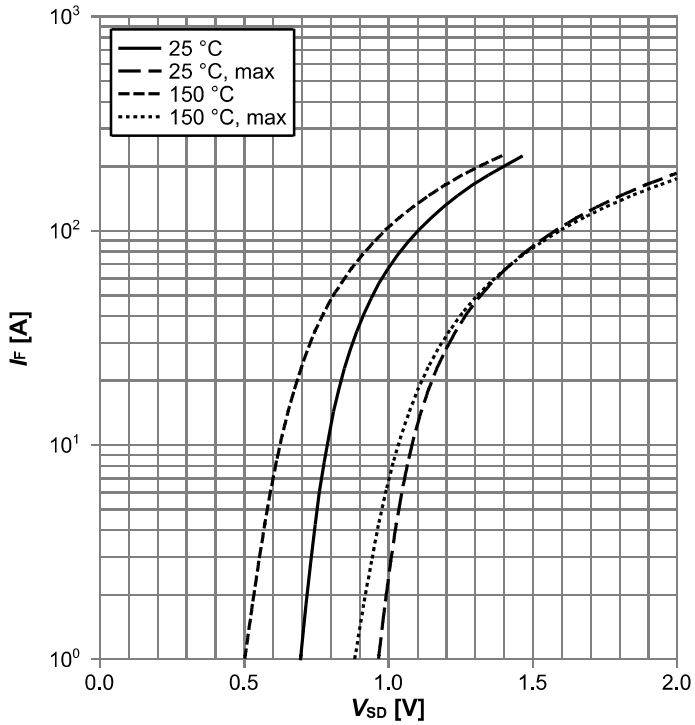
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



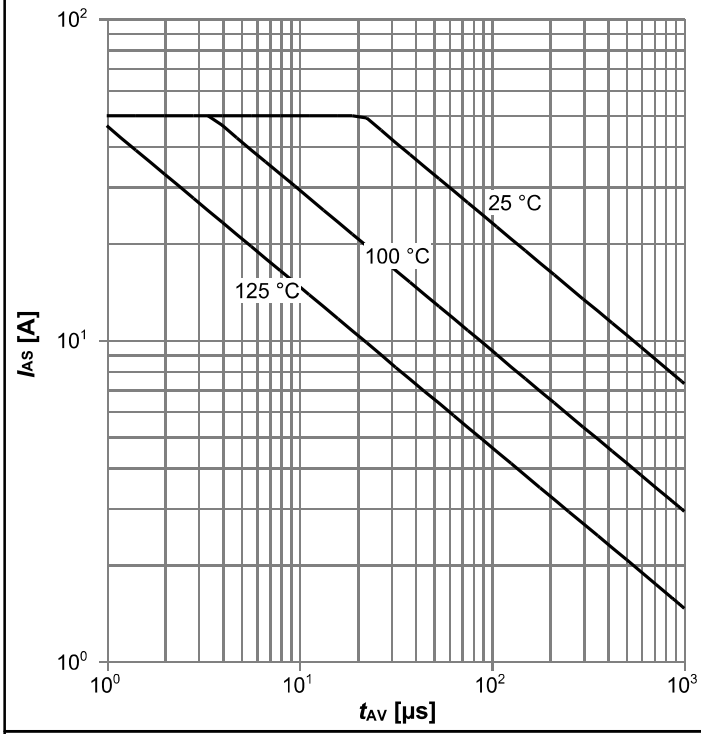
$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



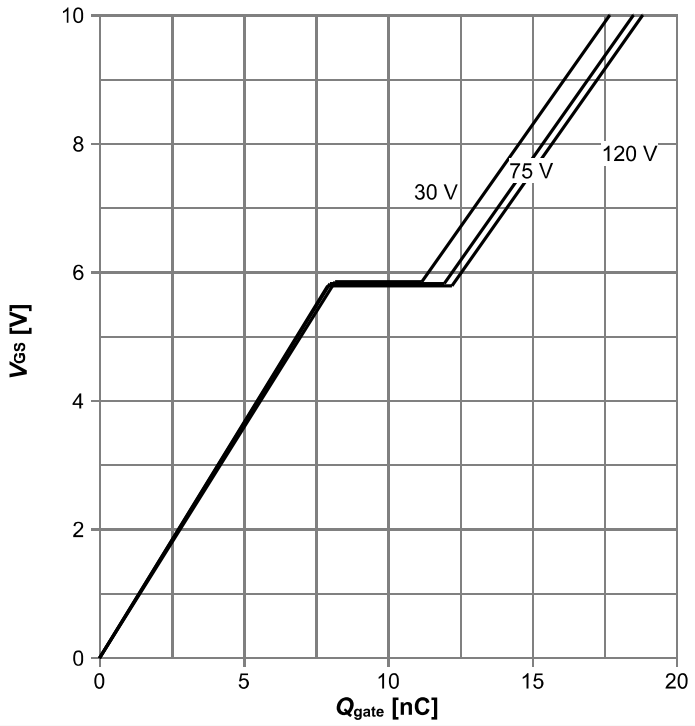
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



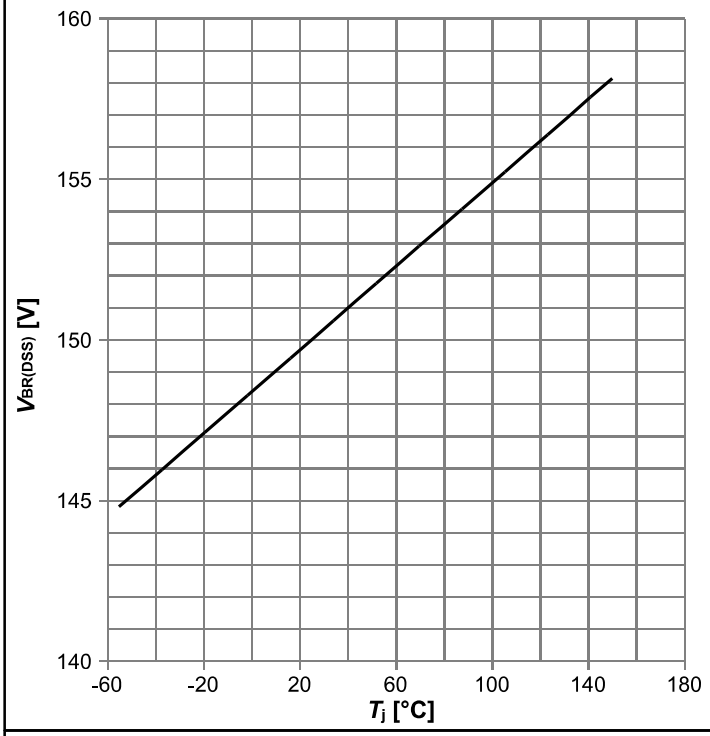
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



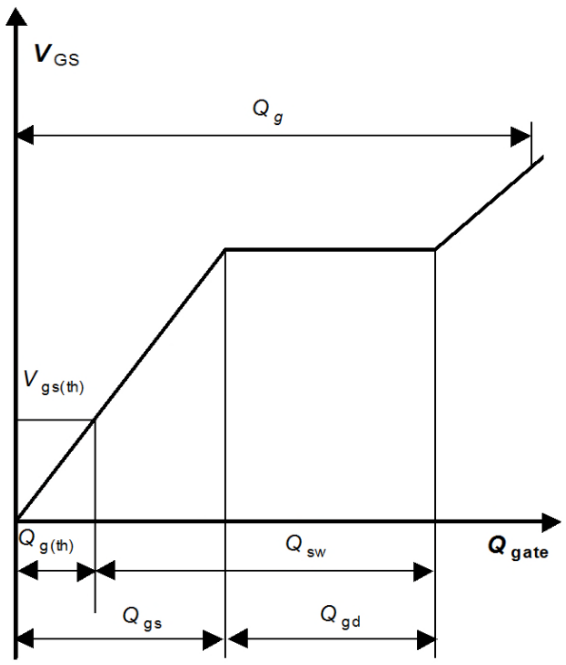
$V_{GS}=f(Q_{gate})$; $I_D=28A$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

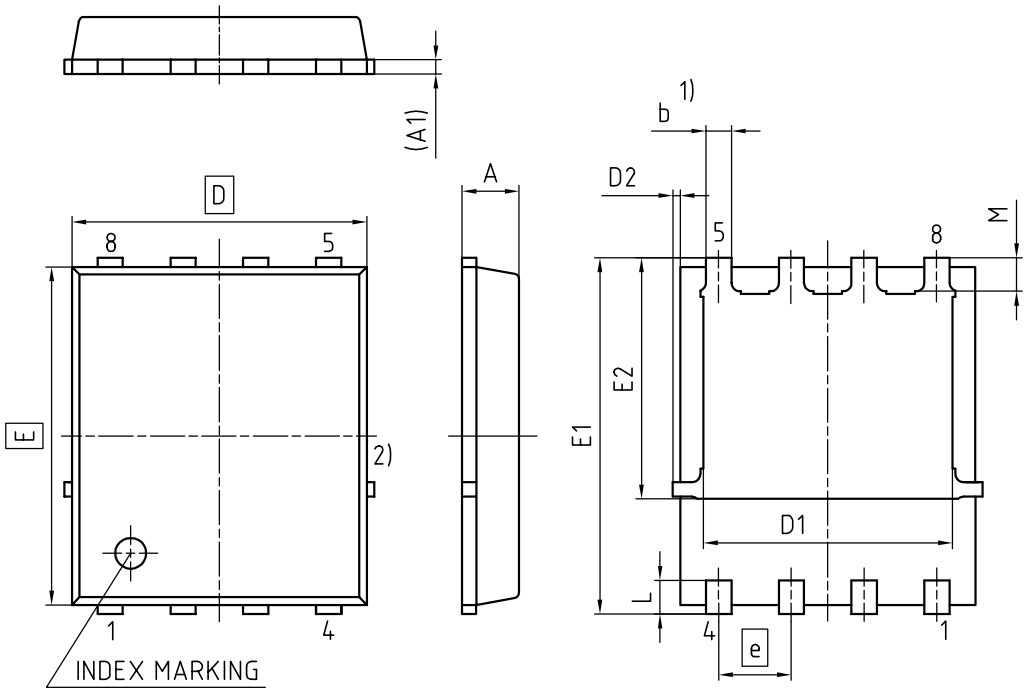


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO. Z8B00003332
REVISION 07
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE 06.06.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

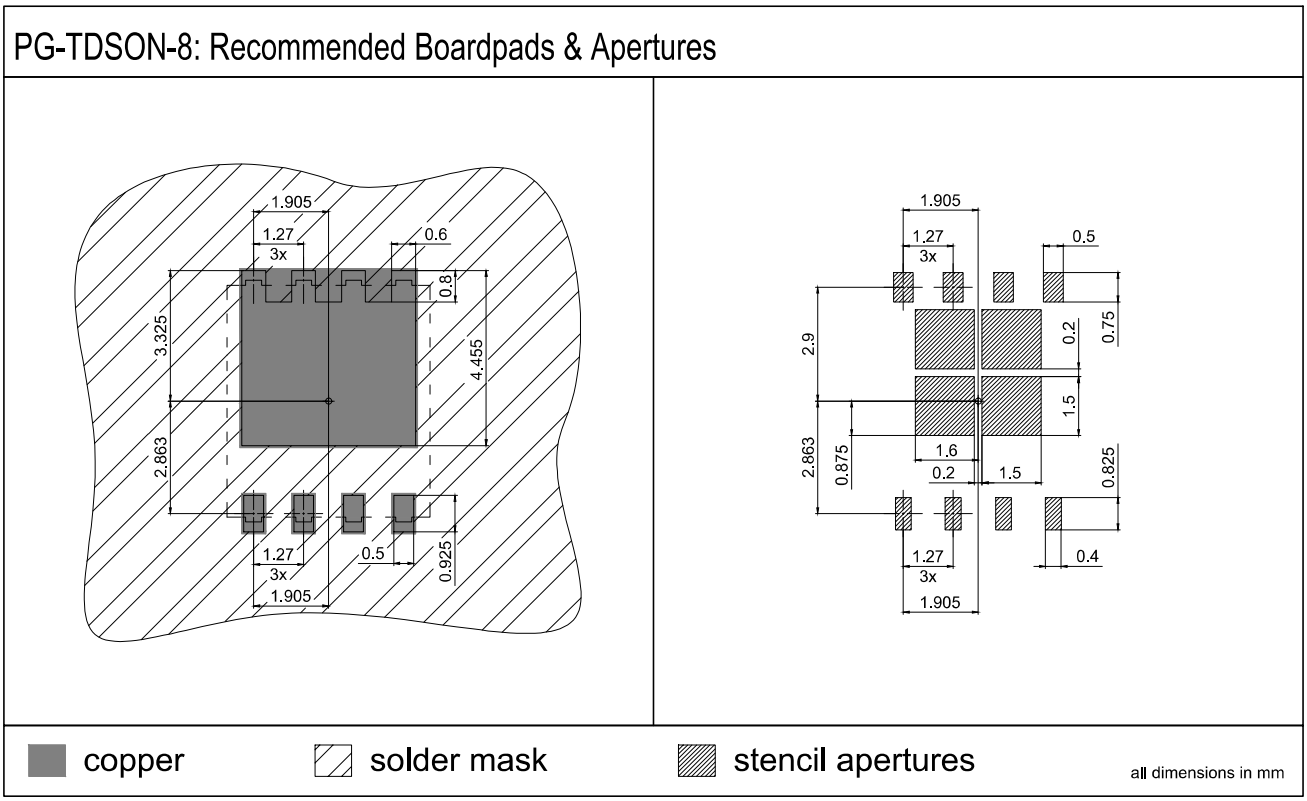
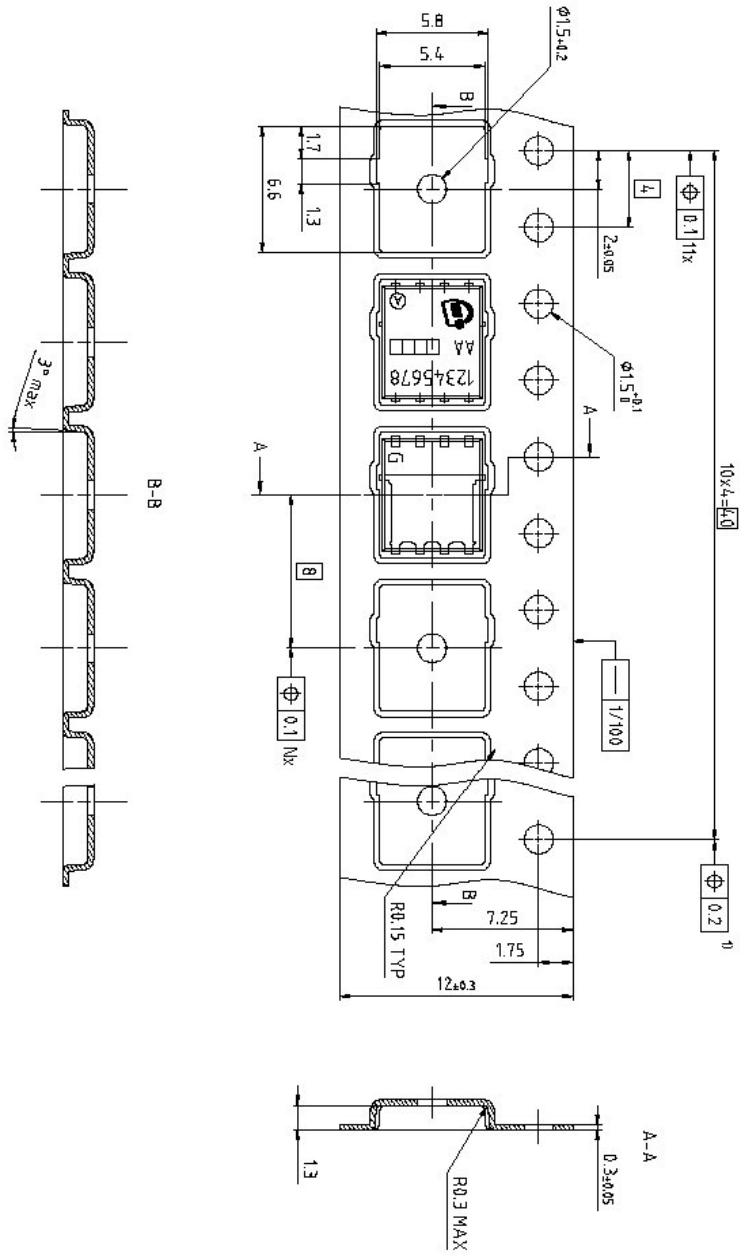


Figure 2 Outline Boardpads (TDSON-8), dimensions in mm



Dimension in mm

Figure 3 Outline Tape (TDSON-8)

Revision History

BSC160N15NS5

Revision: 2021-05-20, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-09-23	Release of final version
2.1	2015-10-12	Rev. 2.1
2.2	2016-01-22	Update Diagram 13
2.3	2020-02-19	Update package drawings
2.4	2021-05-20	Update Diagram 11 and forward current

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