

MOSFET

OptiMOS™3 Power-MOSFET, 75 V

Features

- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- Dual sided cooling
- Low parasitic inductance
- Low profile (<0.7mm)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Compatible with DirectFET® package ST footprint and outline

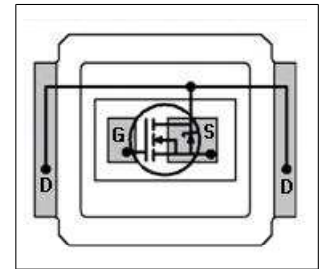


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	75	V
$R_{DS(on),max}$	45	mΩ
I_D	15	A

Type / Ordering Code	Package	Marking	Related Links
BSF450NE7NH3 G	MG-WDSON-2	0307	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	15	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ }^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ }^\circ\text{C}$, $R_{thJA}=58\text{ K/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	60	A	$T_C=25\text{ }^\circ\text{C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	17	mJ	$I_D=8\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	18 2.2	W	$T_C=25\text{ }^\circ\text{C}$ $T_A=25\text{ }^\circ\text{C}$, $R_{thJA}=58\text{ K/W}^{(1)}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	$^\circ\text{C}$	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	-	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	7	K/W	-
Device on PCB, 6 cm ² cooling area ⁽¹⁾	R_{thJA}	-	-	58	K/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See figure 3 for more detailed information

³⁾ See figure 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	75	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.8	V	$V_{DS}=V_{GS}$, $I_D=8\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	10 100	μA	$V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	37.6 46.5	45 62	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=8\text{ A}$ $V_{GS}=7\text{ V}$, $I_D=4\text{ A}$
Gate resistance	R_G	-	1.5	-	Ω	-
Transconductance	g_{fs}	5.5	11	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=8\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	390	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	110	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	22	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8.0	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	11.3	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	11	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	3.2	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=8\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	2	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	3	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	6	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	$V_{DD}=37.5\text{ V}$, $I_D=8\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	7	-	nC	$V_{DD}=37.5\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	15	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	60	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=8\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	24	-	ns	$V_R=37.5\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	87	-	nC	$V_R=37.5\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

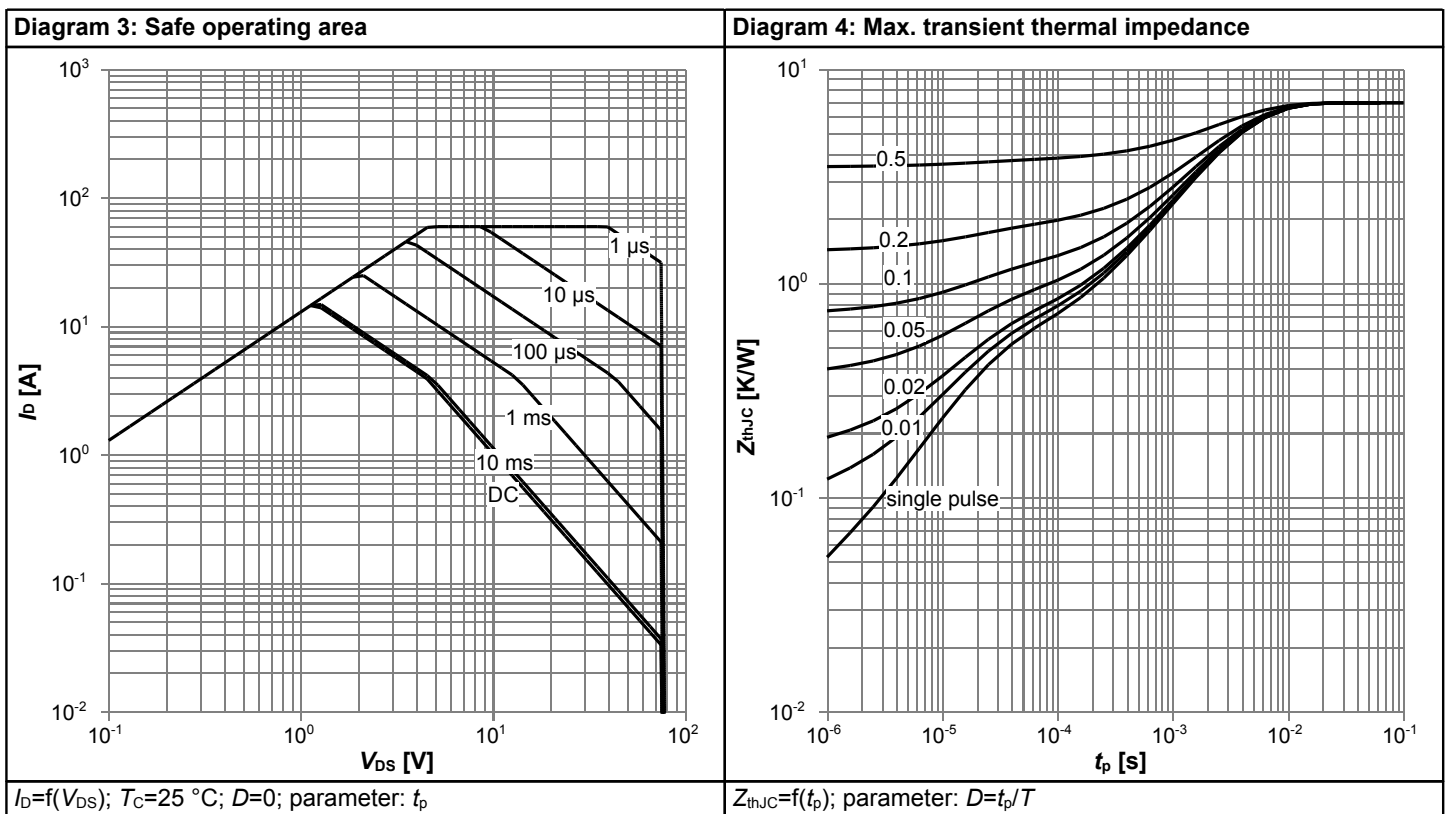
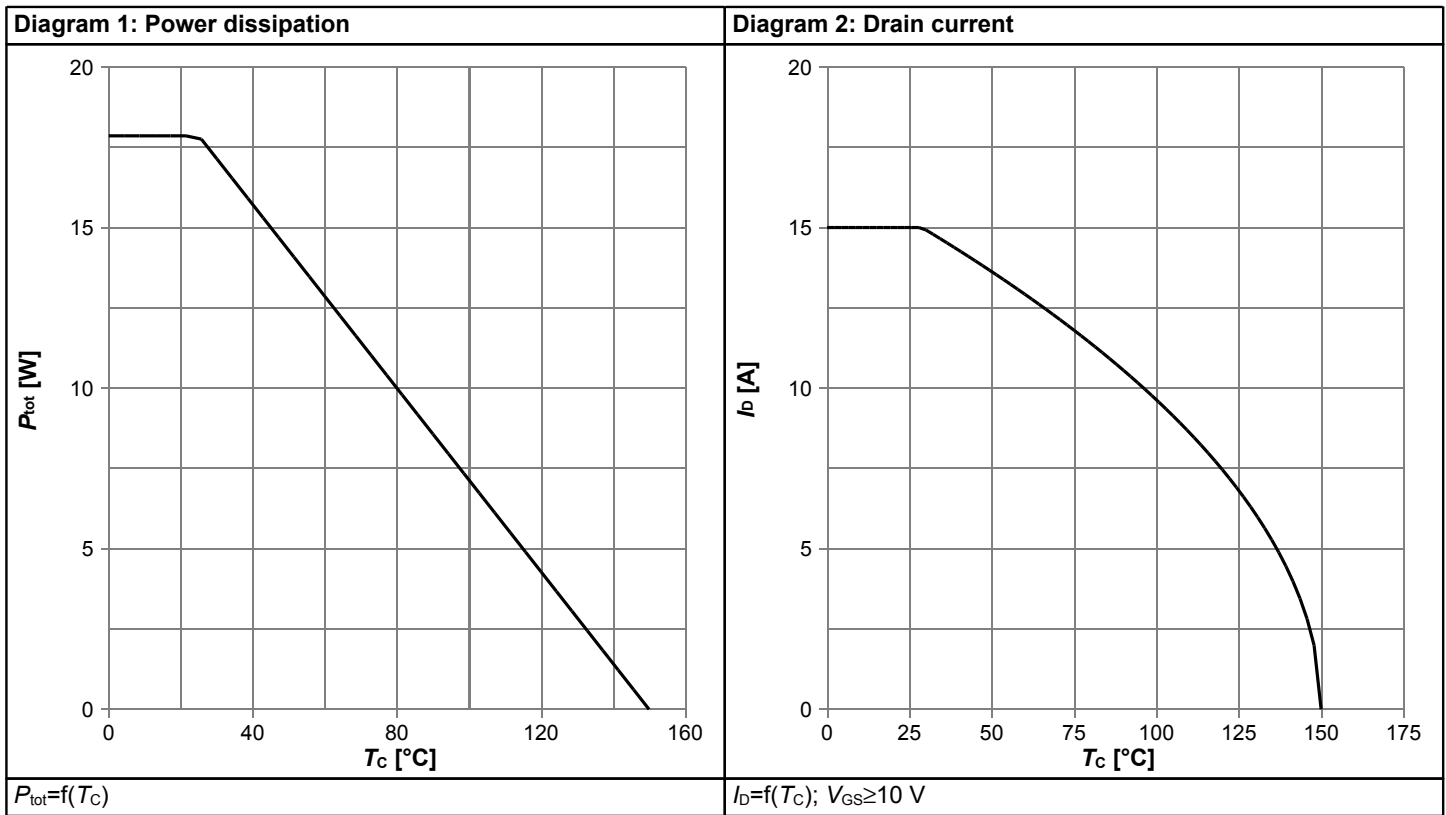
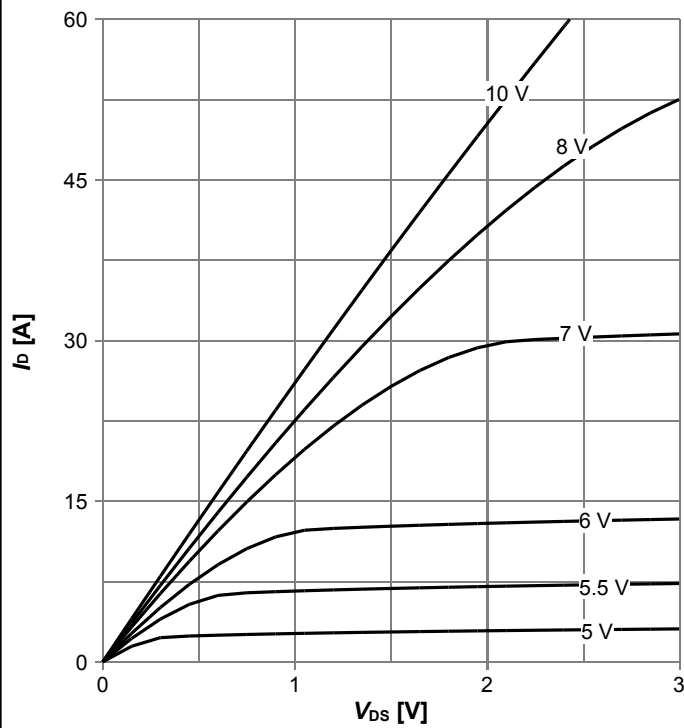
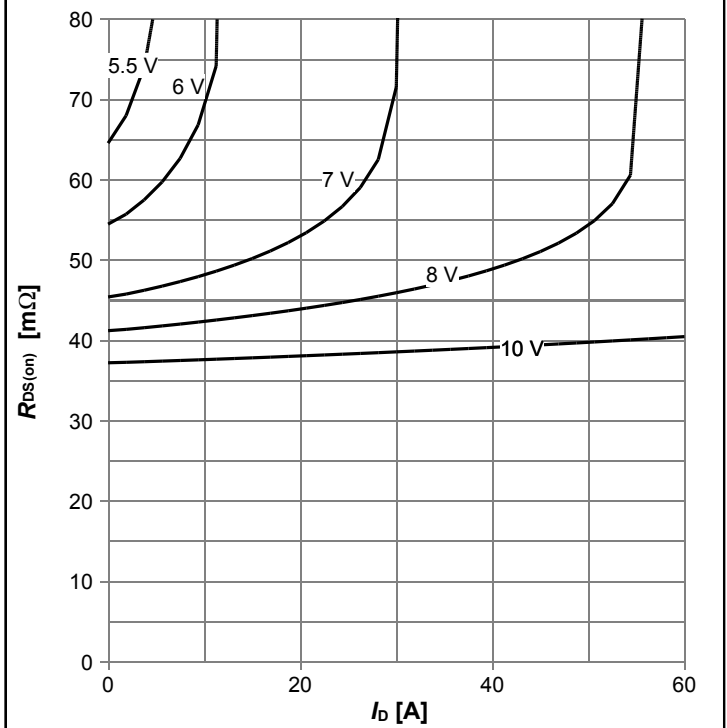


Diagram 5: Typ. output characteristics



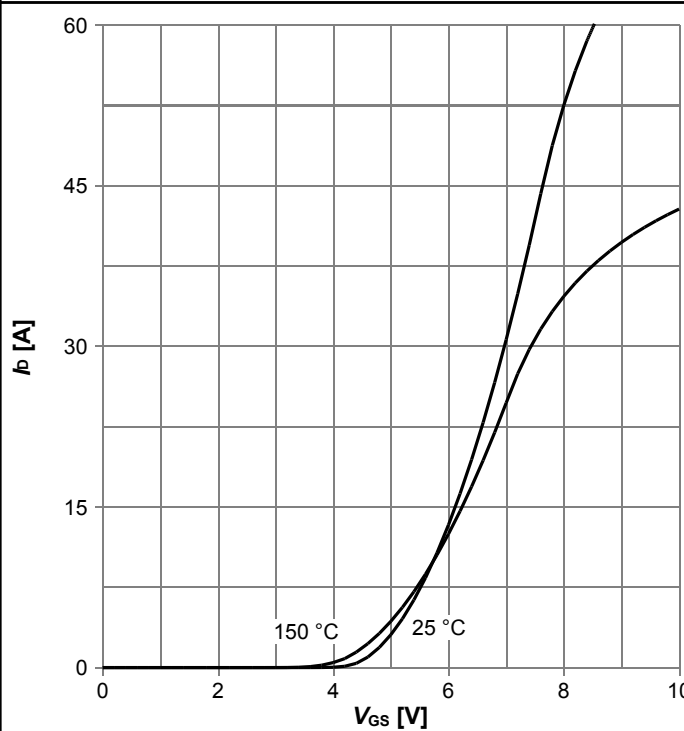
$I_D = f(V_{DS}); T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



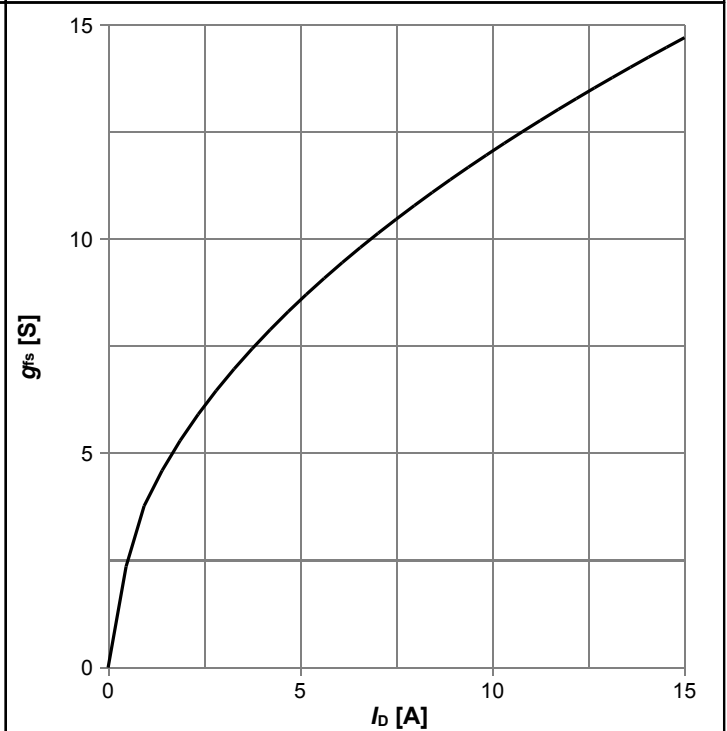
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



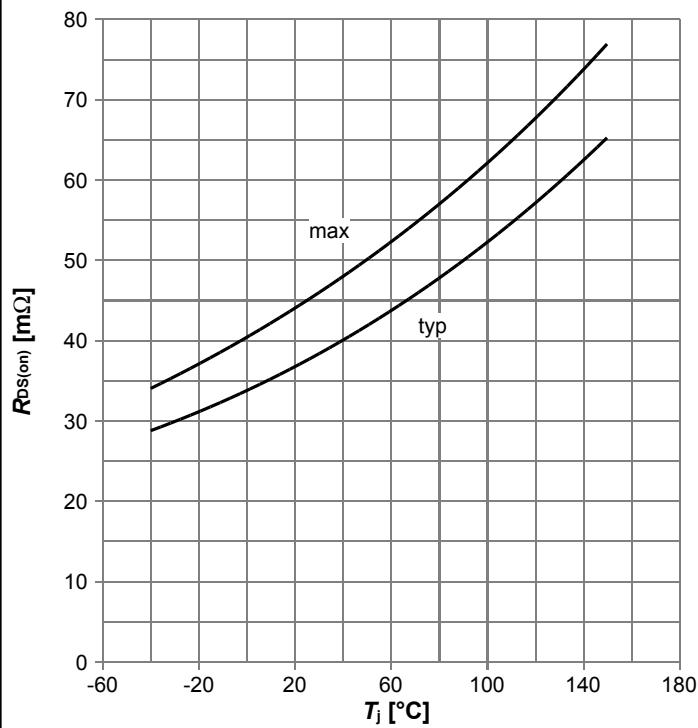
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. forward transconductance



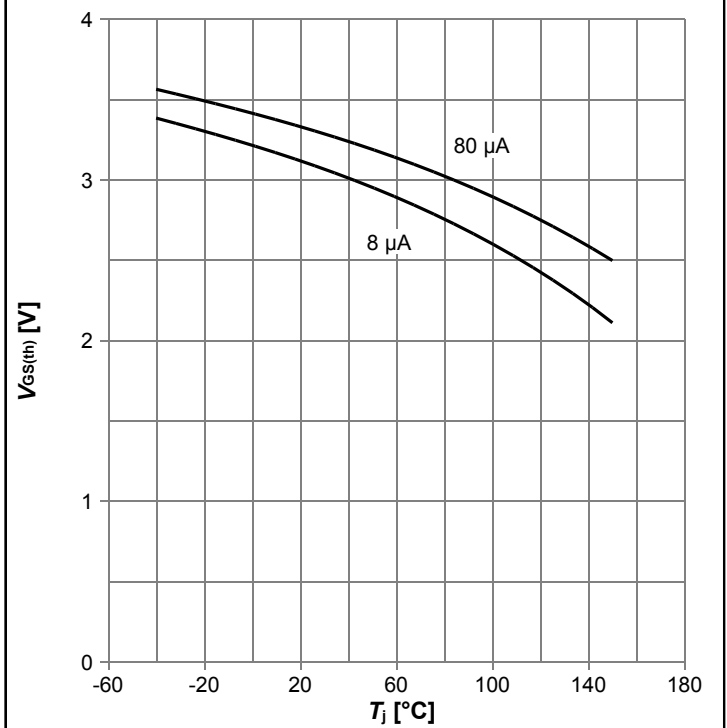
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



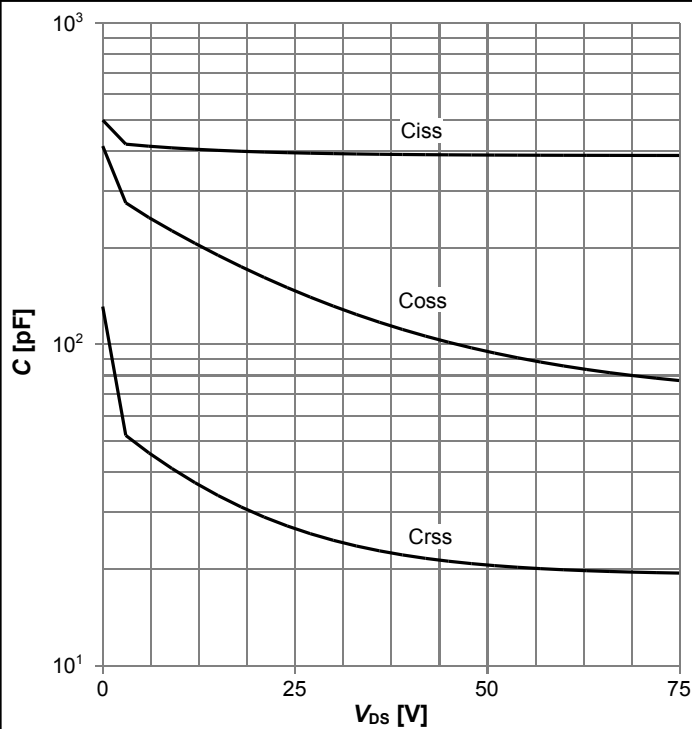
$R_{DS(on)}=f(T_j)$; $I_D=8$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



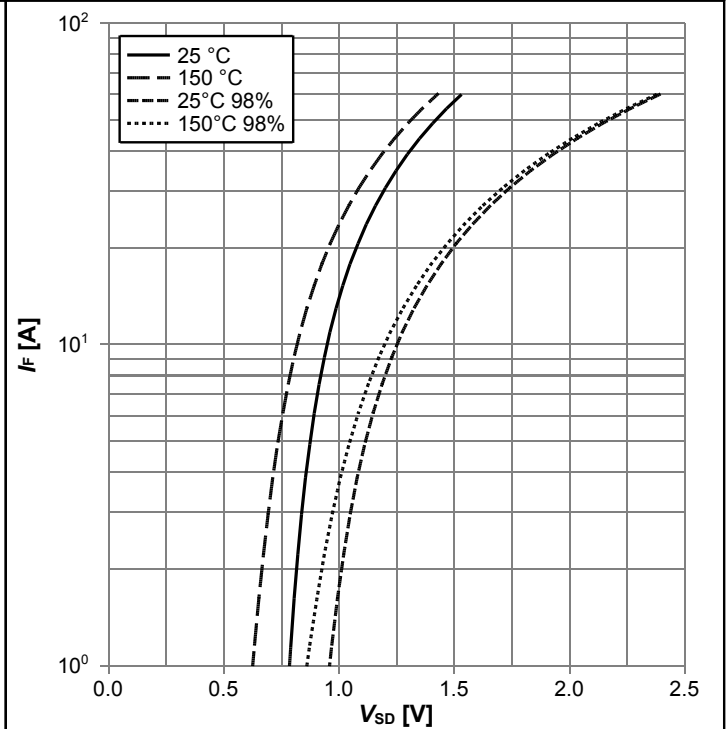
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



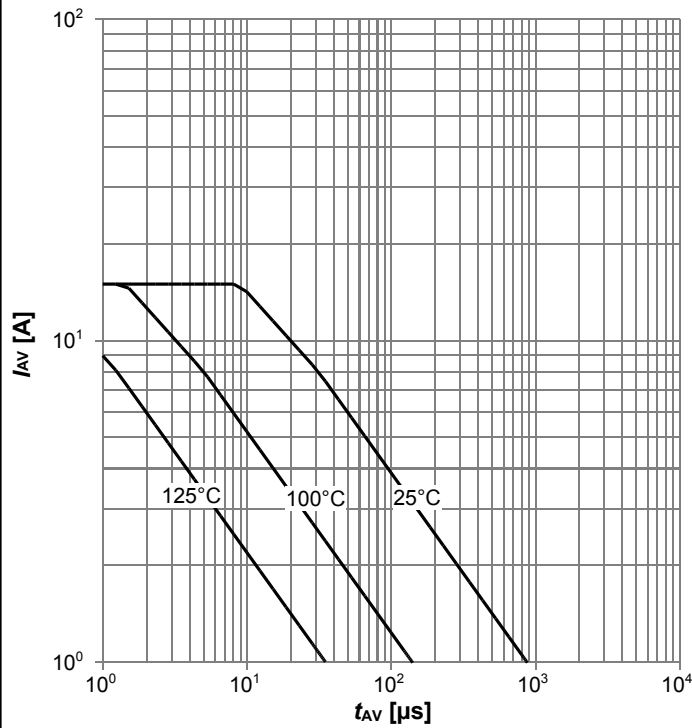
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



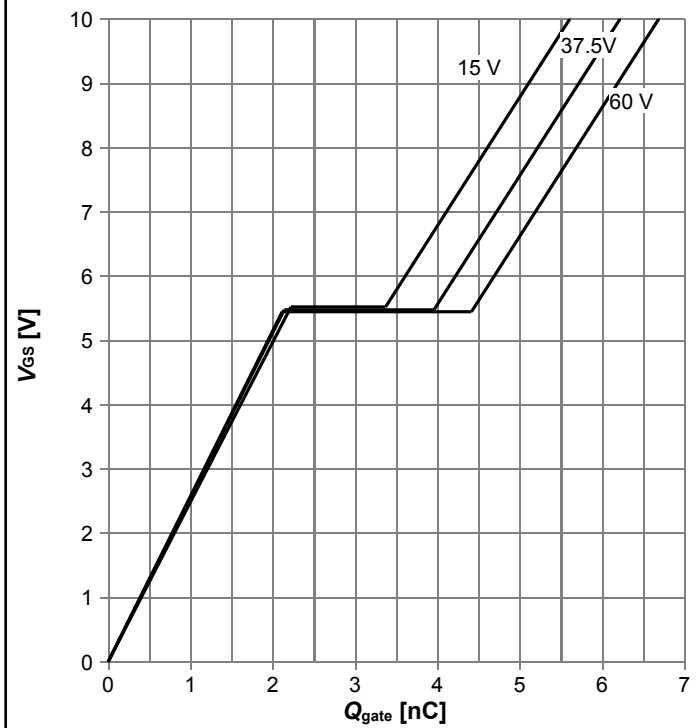
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



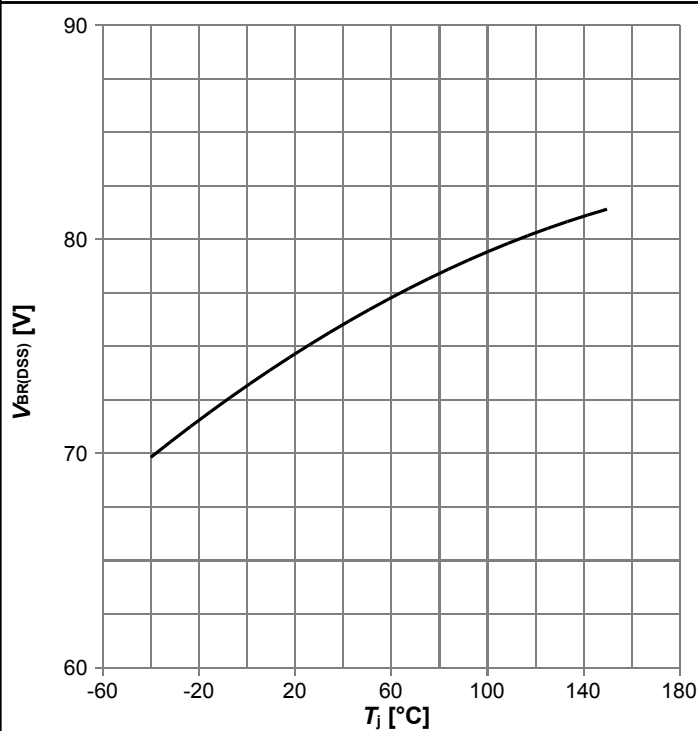
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



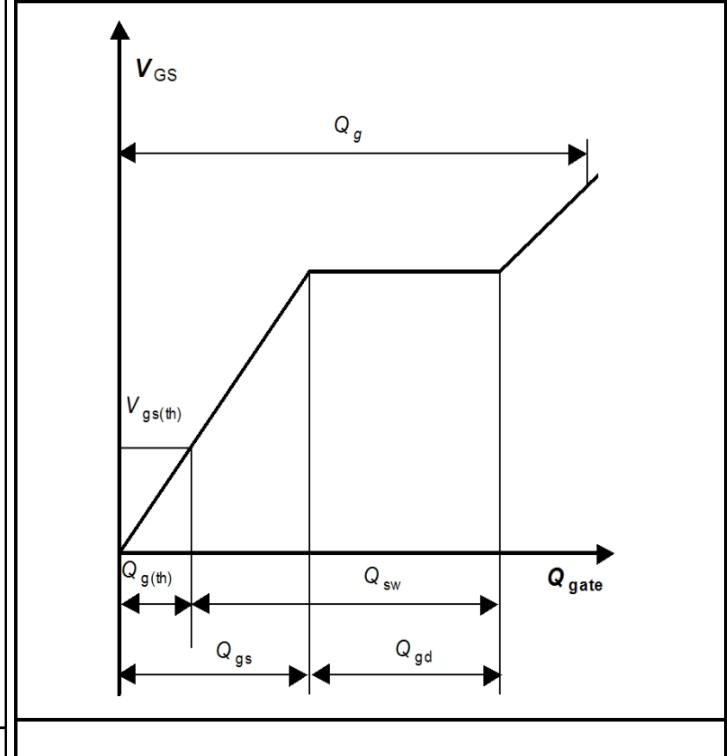
$V_{GS}=f(Q_{gate}); I_D=8 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



5 Package Outlines

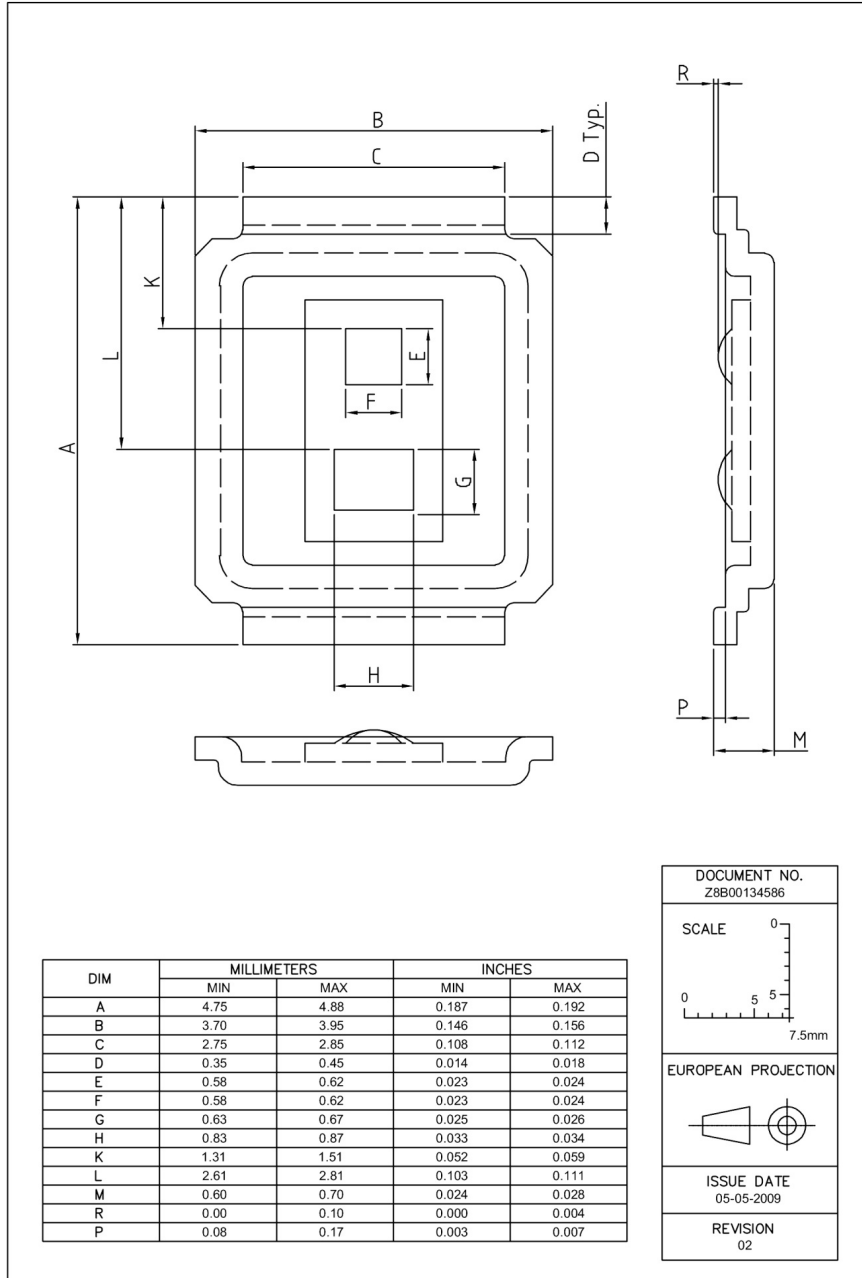


Figure 1 Outline MG-WDSO-2, dimensions in mm/inches

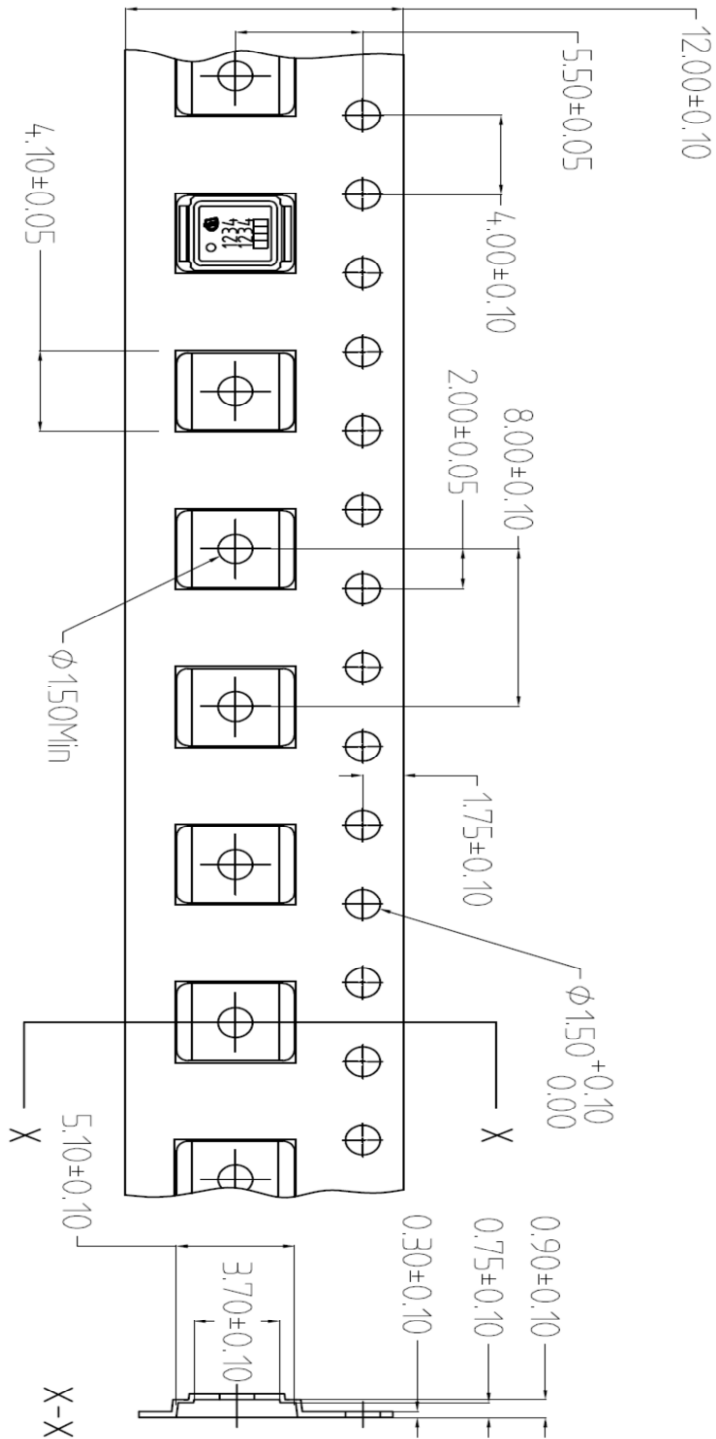
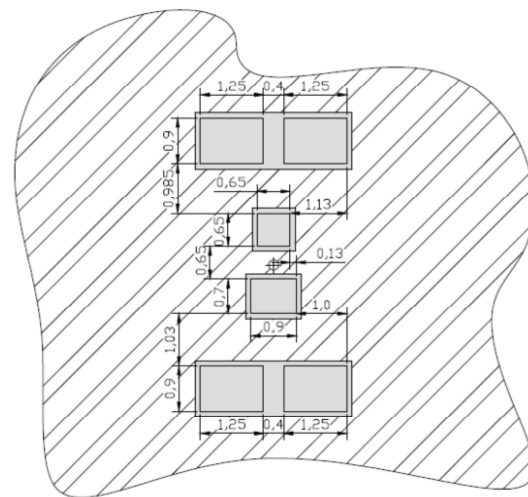
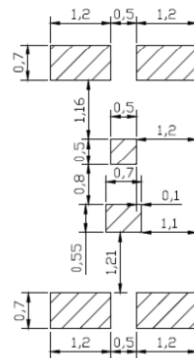


Figure 2 Outline Tape (MG-WDSO-2)



■ copper ▨ solder mask



▨ stencil apertures

Figure 3 Outline Boardpad (MG-WDSO-2)

Revision History

BSF450NE7NH3 G

Revision: 2017-06-19, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2015-03-30	Release of Final version
2.3	2017-06-19	Change of VGS(th) max value to 3.8V

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