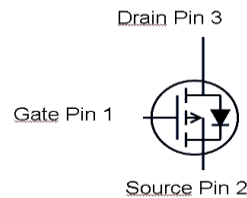
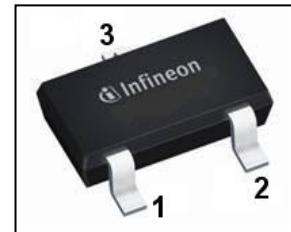


SIPMOS[®] Small-Signal-Transistor
Features

- P-Channel
- Enhancement mode / Logic level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Footprint compatible to SOT23
- Qualified according to AEC Q101
- Halogen free according to IEC61249-2-21

Product Summary

V_{DS}	-100	V
$R_{DS(on),max}$	1.8	Ω
I_D	-0.36	A


PG-SC59


Type	Package	Tape and Reel Information	Marking	Halogen-free	Packing
BSR316P	PG-SC59	H6327 = 3000 pcs. / reel	LC	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
			steady state	
Continuous drain current	I_D	$T_A=25\text{ °C}$	-0.36	A
		$T_A=70\text{ °C}$	-0.29	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-1.44	
Avalanche energy, single pulse	E_{AS}	$I_D=-0.36\text{ A}$, $R_{GS}=25\ \Omega$	25	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	0.5	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^{\circ}\text{C}$
ESD class		JESD22-A114-HBM	1A (250V to 500V)	
Soldering temperature			260 $^{\circ}\text{C}$	
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	250	K/W
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Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$	-	-	-100	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-170\text{ }\mu\text{A}$	-2	-1.5	-1	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$	-	-0.1	-1	μA
		$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}$, $I_D=-0.33\text{ A}$	-	1.8	2.2	Ω
		$V_{GS}=-10\text{ V}$, $I_D=-0.36\text{ A}$	-	1.3	1.8	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=-0.29\text{ A}$	0.3	0.5	-	S

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics³⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	124	165	pF
Output capacitance	C_{oss}		-	25	33	
Reverse transfer capacitance	C_{rss}		-	13	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-50\text{ V},$ $V_{GS}=-10\text{ V},$ $I_D=-0.36\text{ A}, R_{G,ext}=6\ \Omega$	-	5	8	ns
Rise time	t_r		-	6	9	
Turn-off delay time	$t_{d(off)}$		-	71	106	
Fall time	t_f		-	26	39	

Gate Charge Characteristics^{2), 3)}

Gate to source charge	Q_{gs}	$V_{DD}=-80\text{ V},$ $I_D=-0.36\text{ A}, V_{GS}=0\text{ to }-10\text{ V}$	-	0.3	0.4	nC
Gate to drain charge	Q_{gd}		-	1.6	2.4	
Gate charge total	Q_g		-	5.3	7.0	
Gate plateau voltage	$V_{plateau}$		-	-2.7	-	V

Reverse Diode

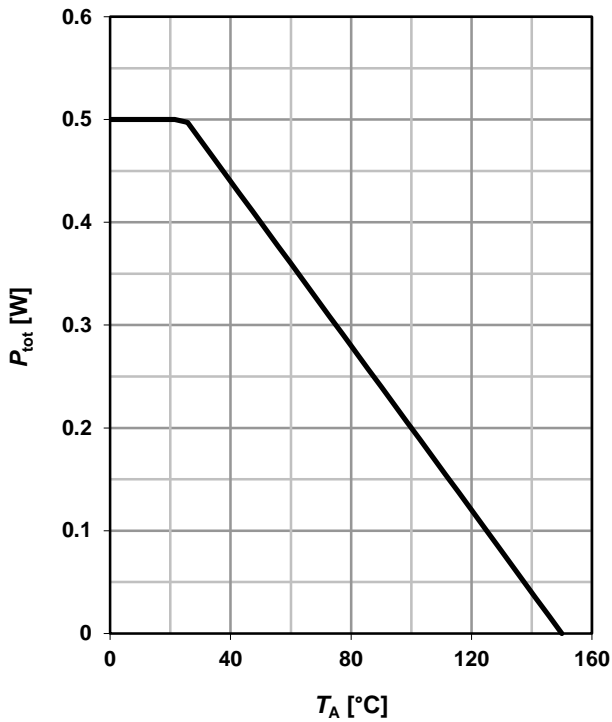
Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	-0.36	A
Diode pulse current	$I_{S,pulse}$		-	-	-1.44	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=0.36\text{ A},$ $T_j=25\text{ °C}$	-	-0.8	-1.1	V
Reverse recovery time ³⁾	t_{rr}	$V_R=-50\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	40.6	-	ns
Reverse recovery charge ³⁾	Q_{rr}		-	46.4	-	nC

²⁾ See figure 16 for gate charge parameter definition

³⁾ Defined by design. Not subjected to production test

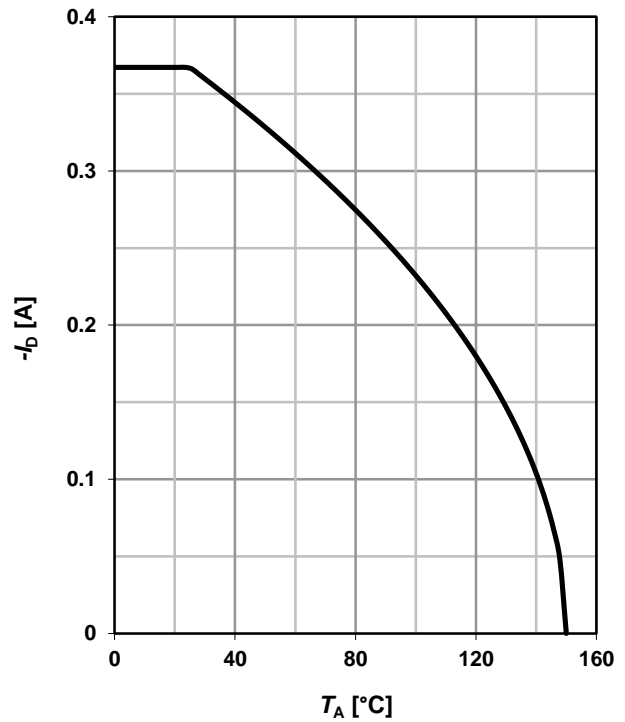
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

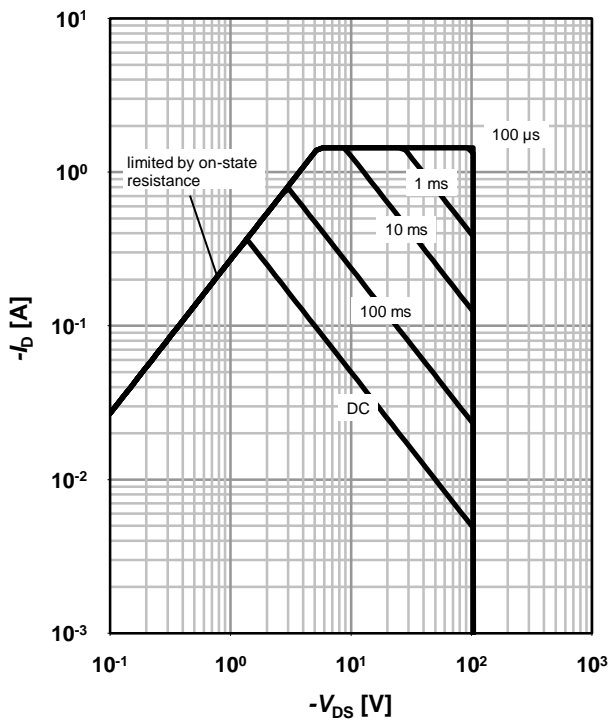
$I_D=f(T_C); |V_{GS}|\geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

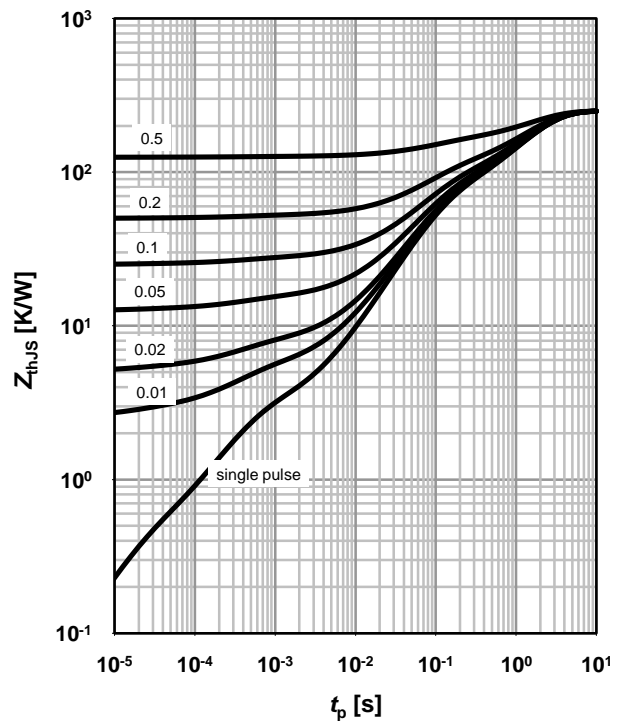
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

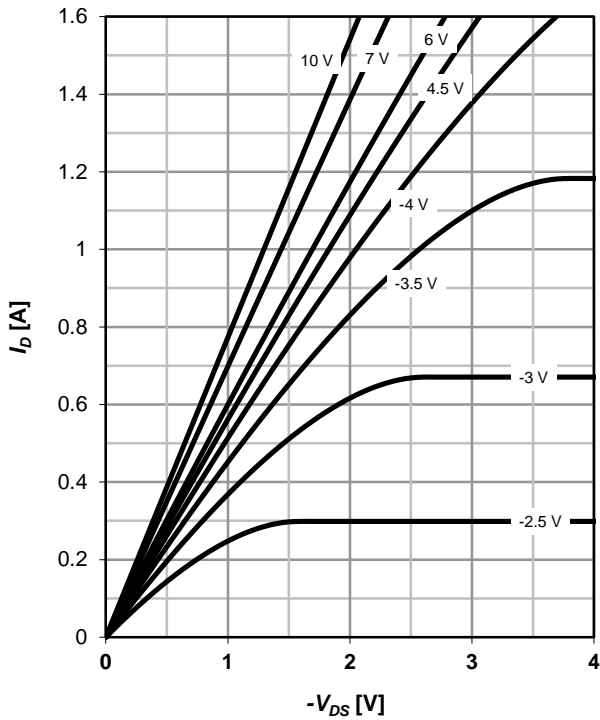
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

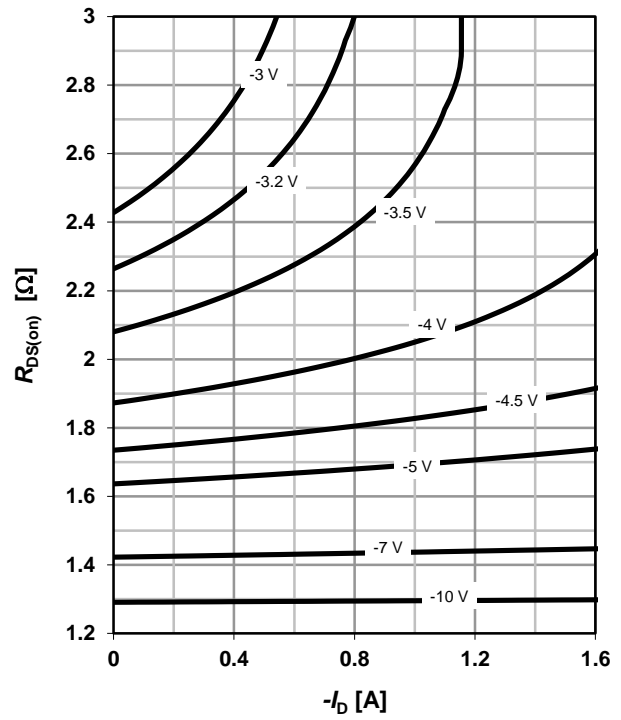
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

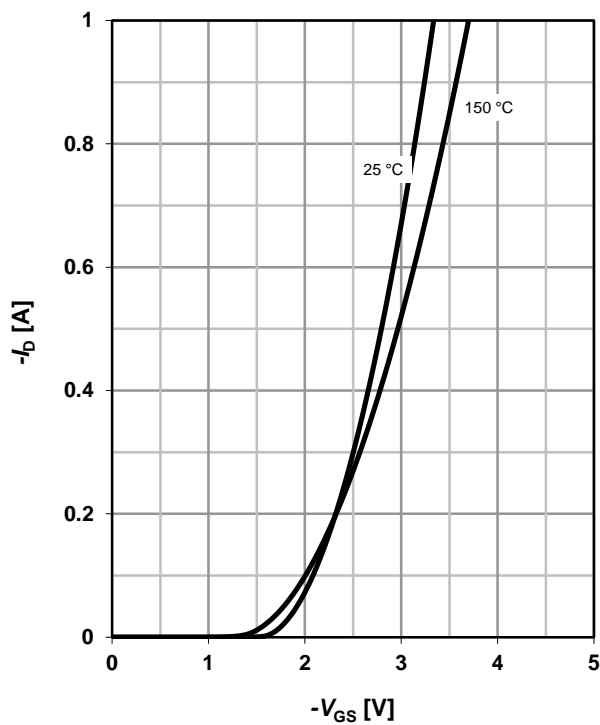
parameter: V_{GS}



7 Typ. transfer characteristics

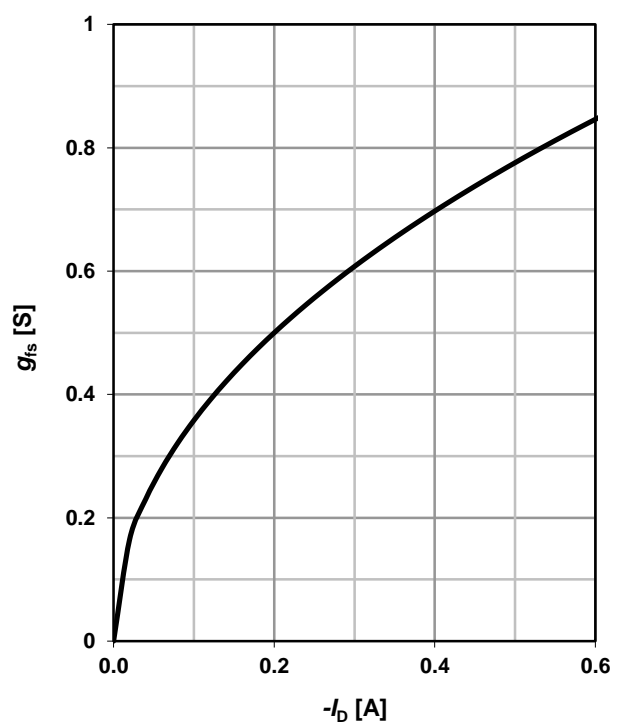
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



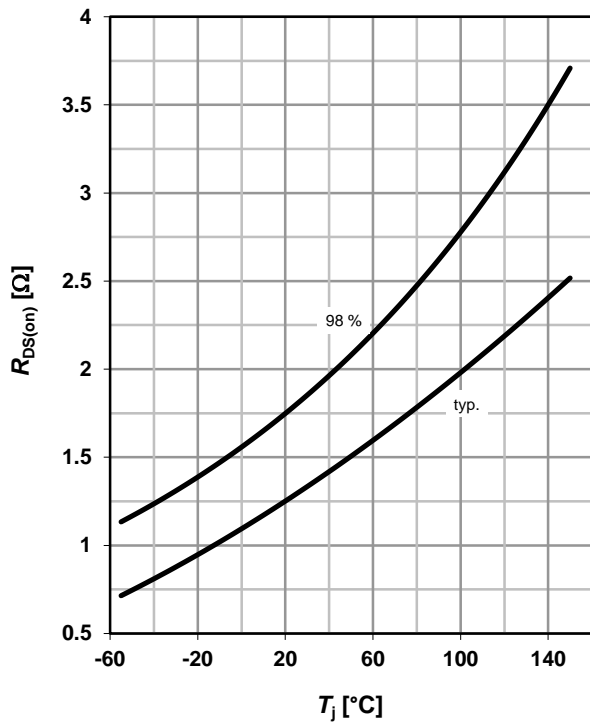
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



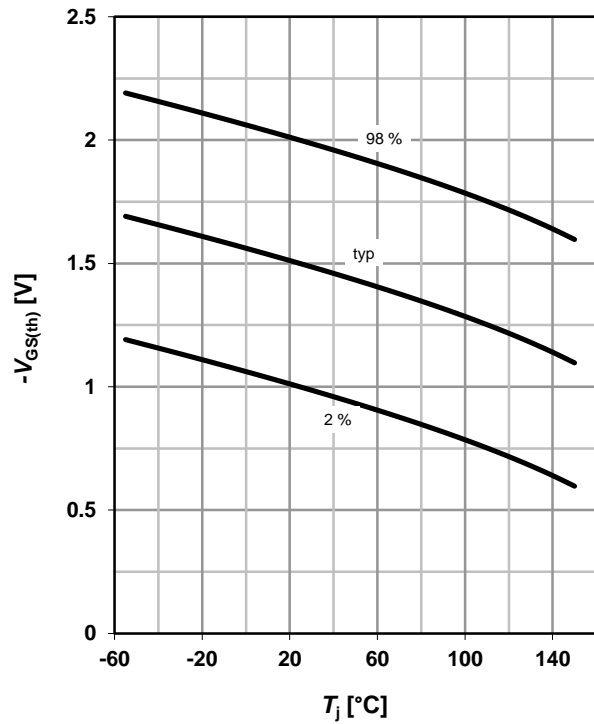
9 Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; $I_D=-0.36\text{ A}$; $V_{GS}=-10\text{ V}$



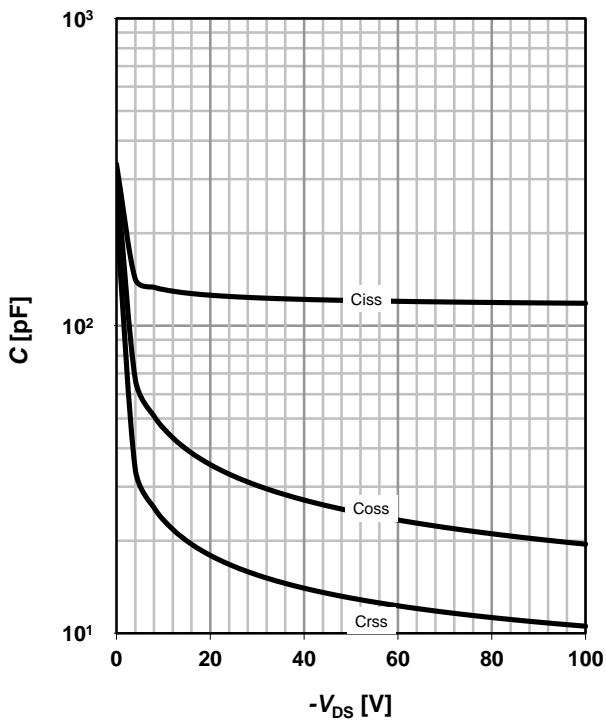
10 Typ. gate threshold voltage

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=-170\text{ }\mu\text{A}$



11 Typ. capacitances

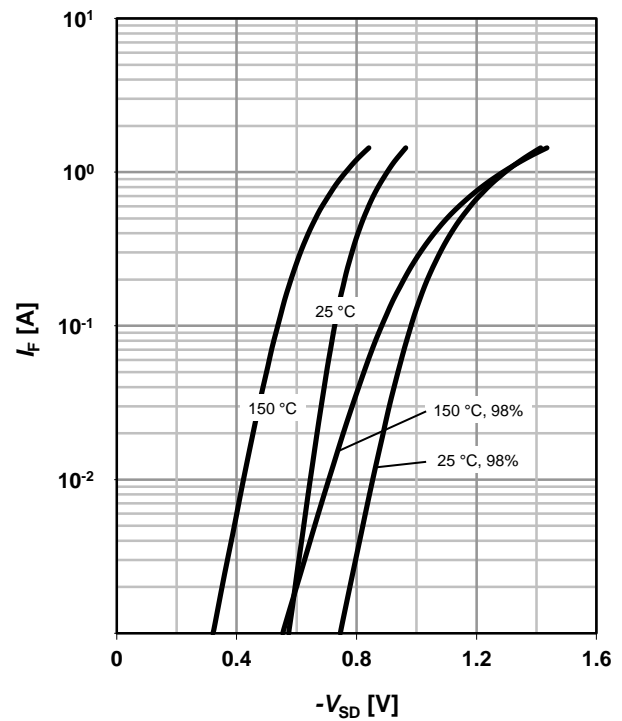
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$



12 Forward characteristics of reverse diode

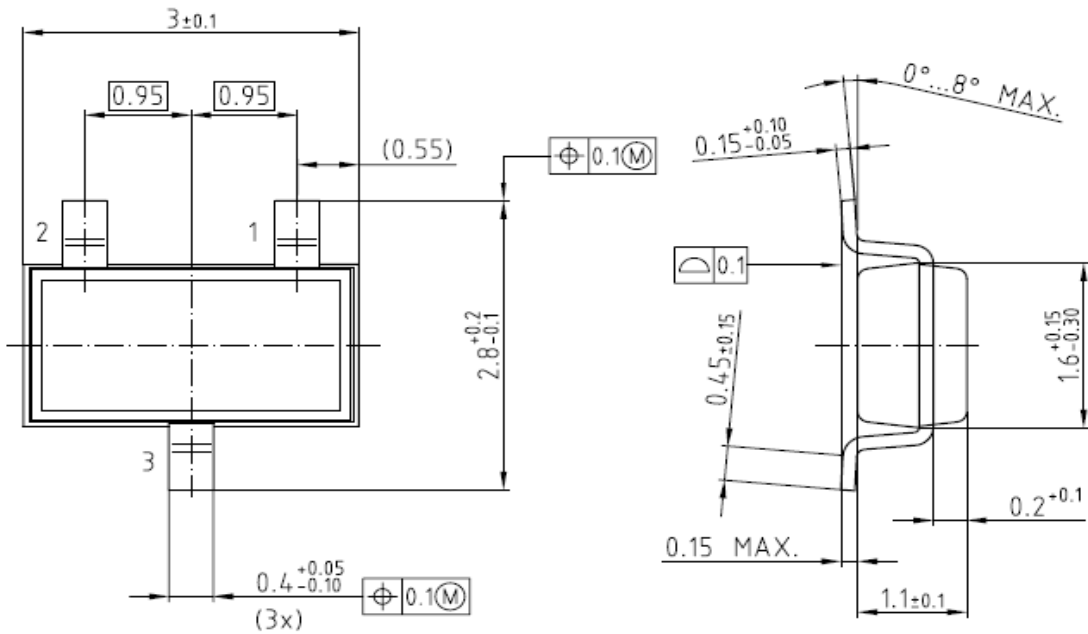
$I_F=f(V_{SD})$

parameter: T_j

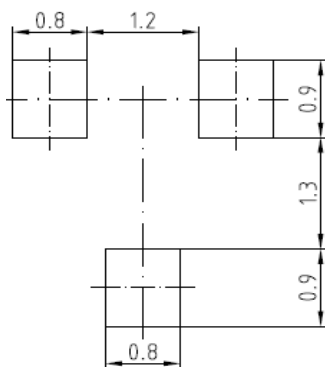


Package Outline

SC-59: Outline

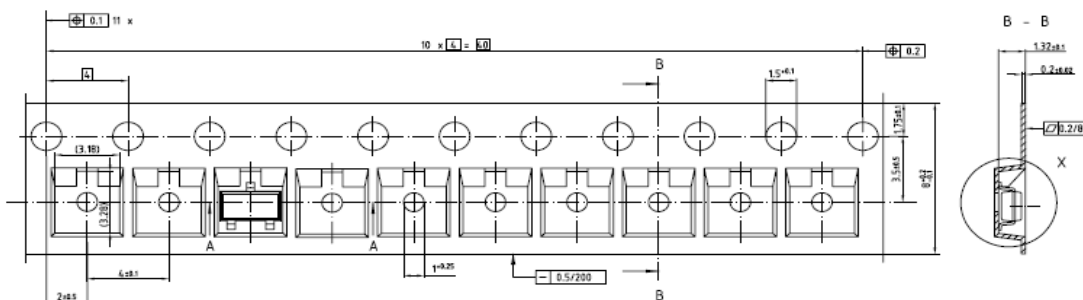


Footprint



Packaging

Tape

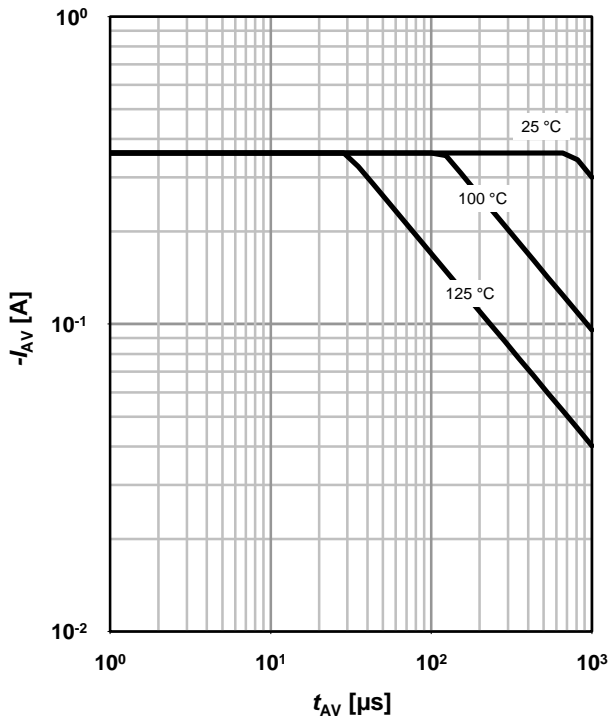


Dimensions in mm

13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

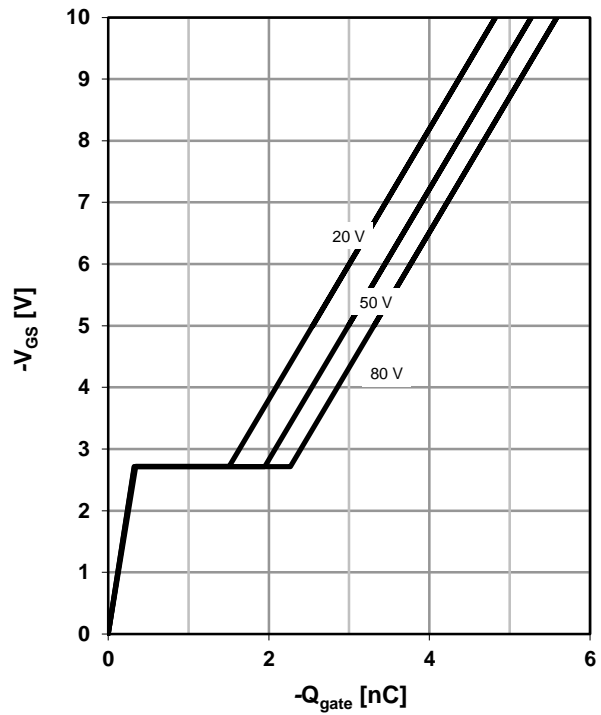
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

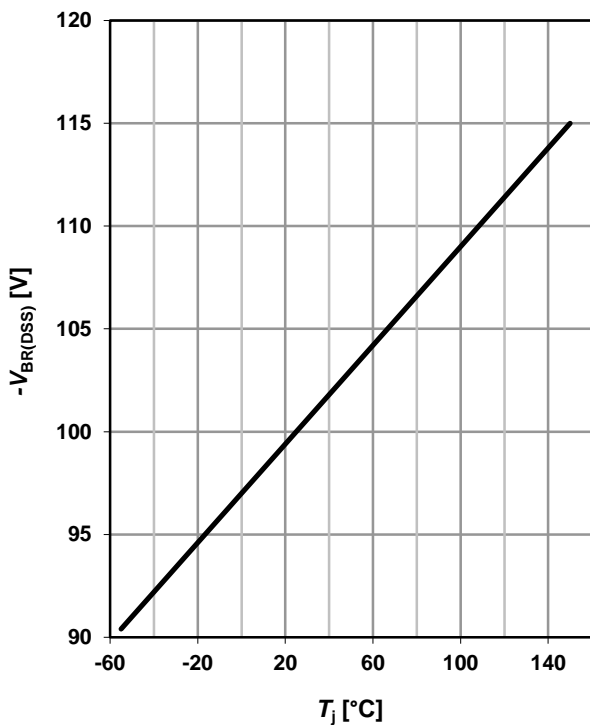
$V_{GS}=f(Q_{\text{gate}}); I_D=-0.36 \text{ A pulsed}$

parameter: V_{DD}

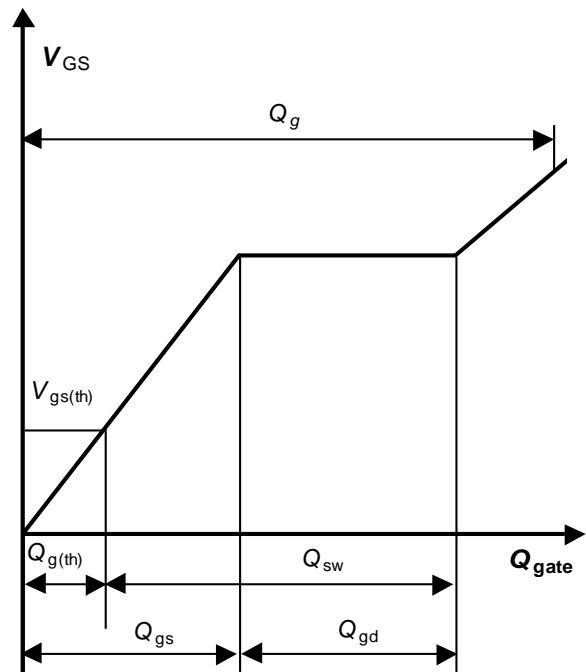


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=-250 \mu\text{A}$



16 Gate charge waveforms



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