

# MOSFET

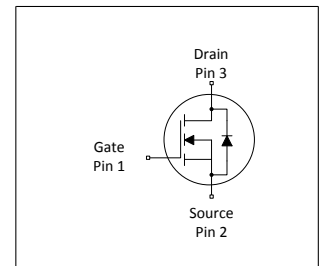
## OptiMOS™ Small-Signal-Transistor, 100 V

### Features

- N-channel
- Enhancement mode
- Logic level (4.5V rated)
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Fully qualified according to JEDEC for Industrial Applications



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}, V_{GS}=10\text{ V}$	6	$\Omega$
$R_{DS(on),max}, V_{GS}=4.5\text{ V}$	10	$\Omega$
$I_D$	0.19	A
ESD Sensitivity, JESD22-A114 (HBM)	class 0 (<250V)	



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSS123I	PG-SOT23	Als	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	0.19 0.15	A	$V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ $V_{GS}=4.5\text{ V}$ , $T_A=70\text{ °C}$
Pulsed drain current	$I_{D,pulse}$	-	-	0.77	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	2.0	mJ	$I_D=0.19\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Reverse diode $dv/dt$	$dv/dt$	-	-	6	kV/ $\mu$ s	$I_D=0.19\text{ A}$ , $V_{DS}=80\text{ V}$ , $di/dt=200\text{ A}/\mu\text{s}$ , $T_{j,max}=150\text{ °C}$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation <sup>1)</sup>	$P_{tot}$	-	-	0.5	W	$T_A=25\text{ °C}$ , $R_{THJA}=250\text{ °C/W}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - ambient, minimum footprint <sup>1)</sup>	$R_{thJA}$	-	-	250	K/W	-

## 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	0.8	1.4	1.8	V	$V_{DS}=V_{GS}$ , $I_D=13\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-	0.01 5	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-	10	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4 2.7	6 10	$\Omega$	$V_{GS}=10\text{ V}$ , $I_D=0.19\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=0.15\text{ A}$
Transconductance	$g_{fs}$	-	0.41	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=0.15\text{ A}$

<sup>1)</sup> Performed on 40mm<sup>2</sup> FR4 PCB. The traces are 1mm wide, 70 $\mu$ m thick and 20mm long; they are present on both sides of the PCB

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	15	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	2.5	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	1.6	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	2.3	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=0.19\text{ A}$ , $R_{G,ext}=6\ \Omega$
Rise time	$t_r$	-	3.2	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=0.19\text{ A}$ , $R_{G,ext}=6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	7.4	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=0.19\text{ A}$ , $R_{G,ext}=6\ \Omega$
Fall time	$t_f$	-	22	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=0.19\text{ A}$ , $R_{G,ext}=6\ \Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	0.04	-	nC	$V_{DD}=50\text{ V}$ , $I_D=0.19\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	0.23	-	nC	$V_{DD}=50\text{ V}$ , $I_D=0.19\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	0.63	-	nC	$V_{DD}=50\text{ V}$ , $I_D=0.19\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	$V_{DD}=50\text{ V}$ , $I_D=0.19\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	0.19	A	$T_A=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	0.77	A	$T_A=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.86	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=0.19\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	12	18	ns	$V_R=50\text{ V}$ , $I_F=0.19\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	4.3	6.5	nC	$V_R=50\text{ V}$ , $I_F=0.19\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

### 4 Electrical characteristics diagrams

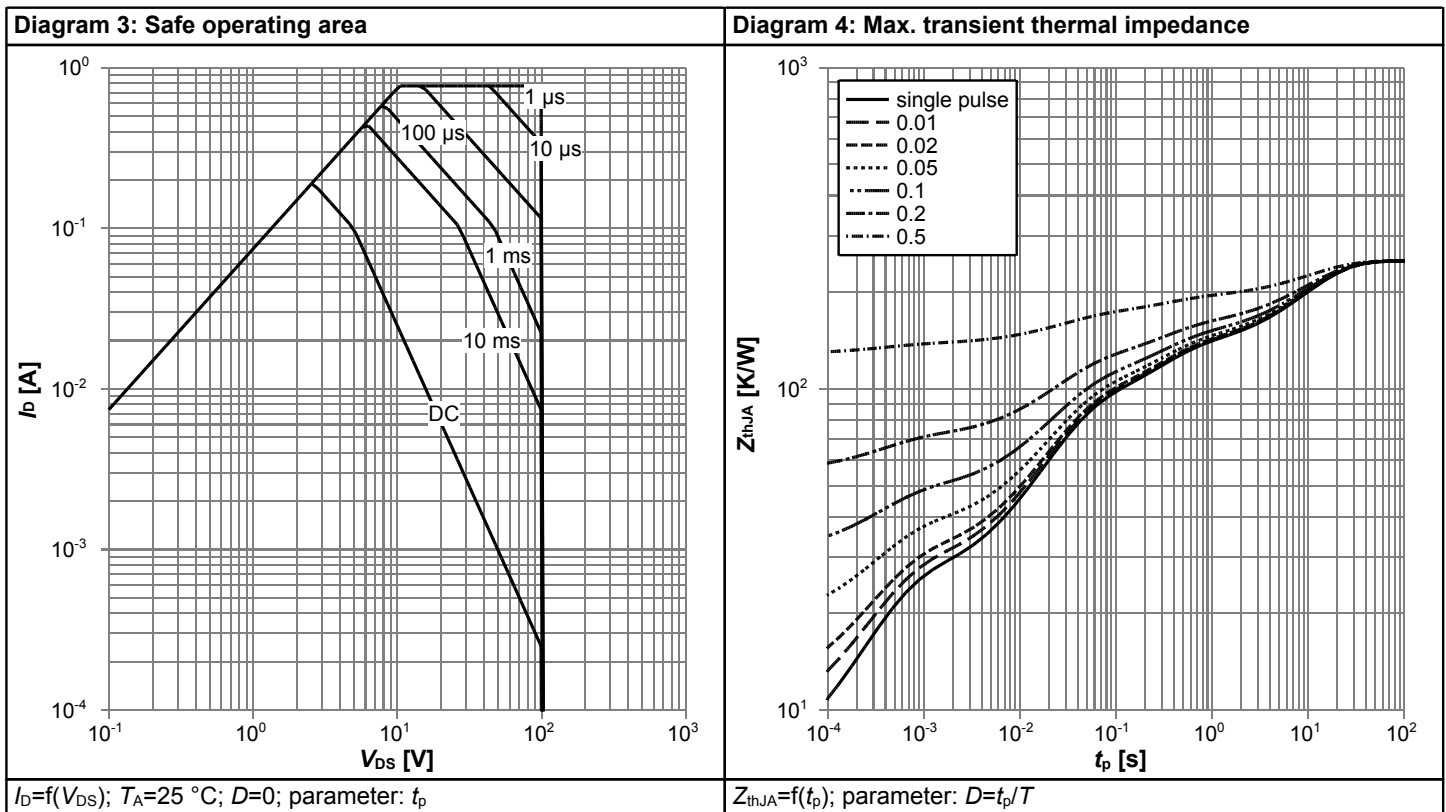
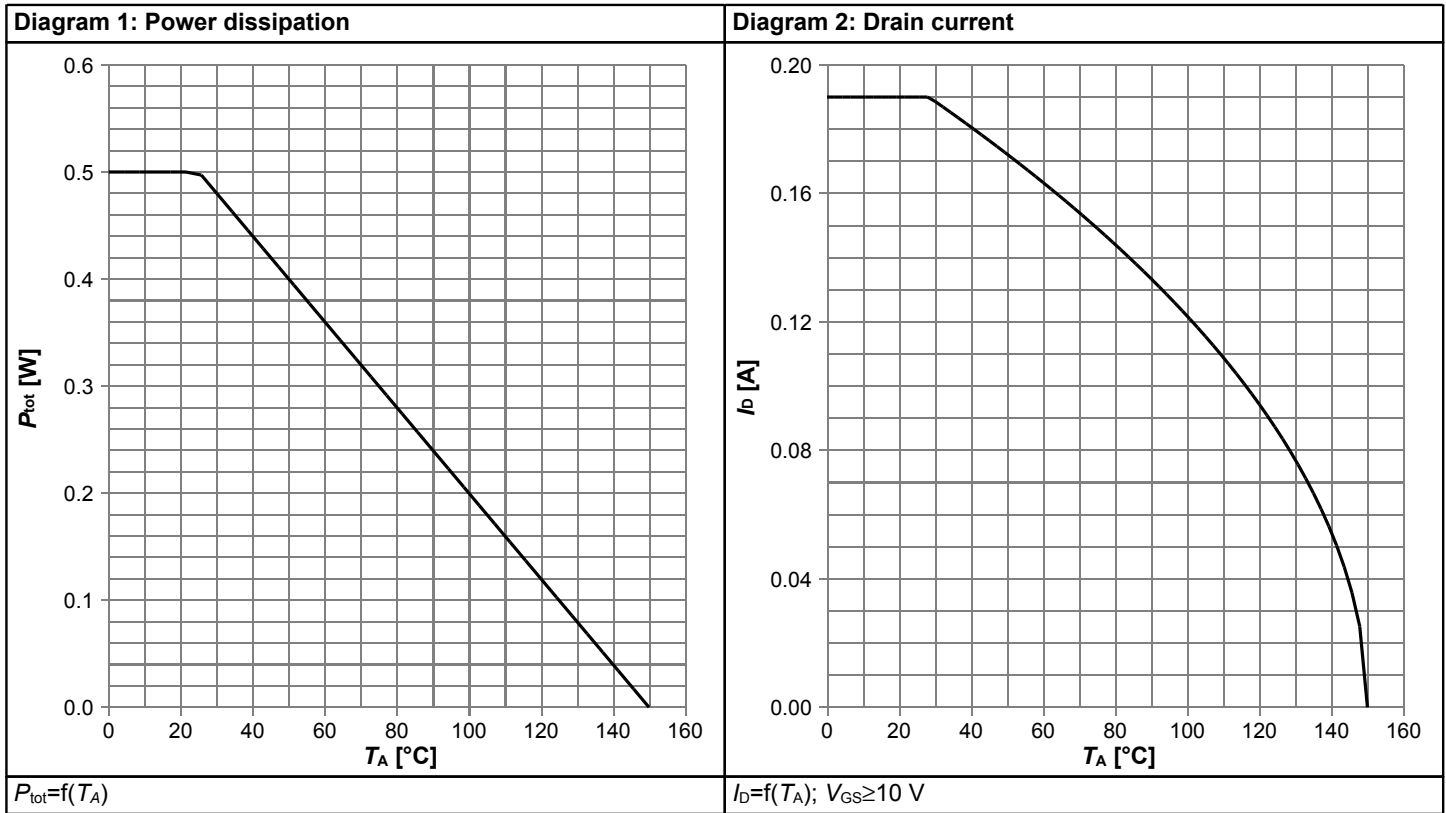
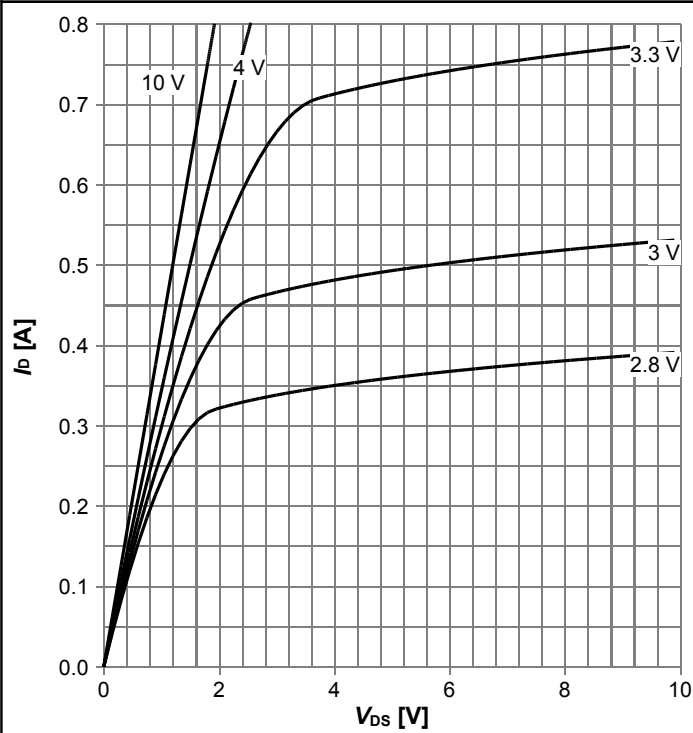
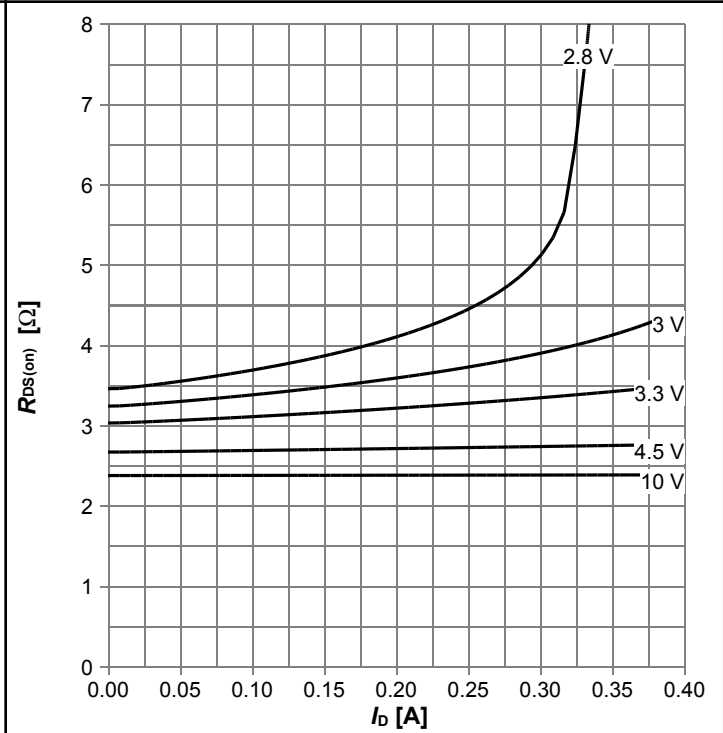


Diagram 5: Typ. output characteristics



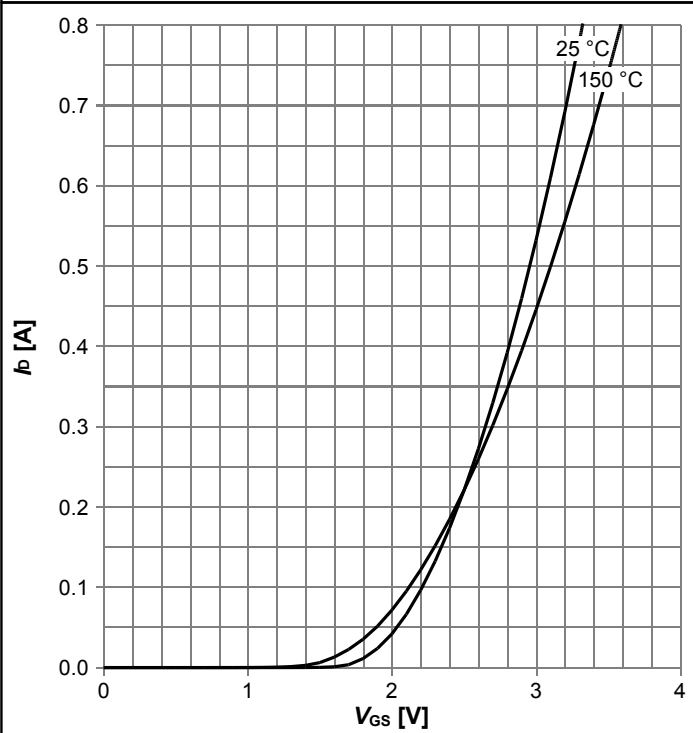
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



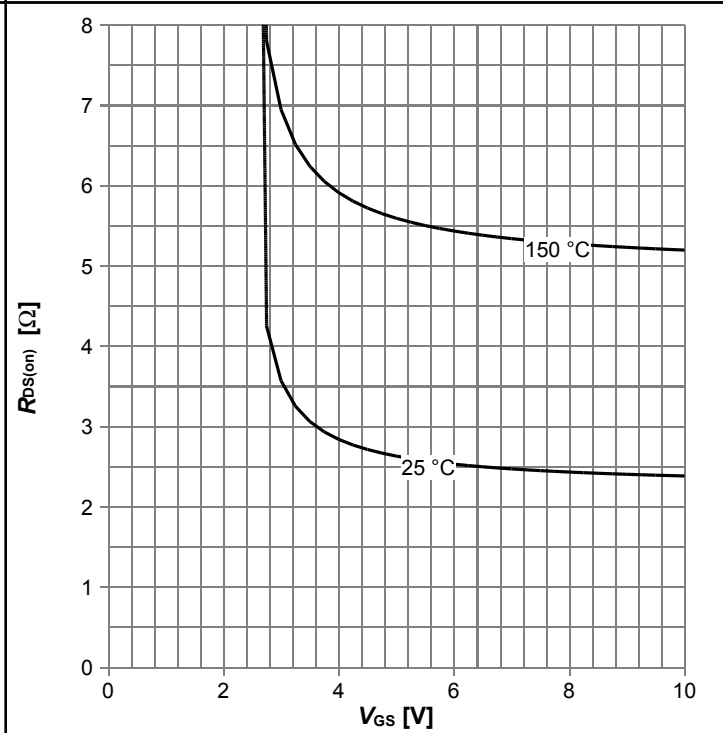
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



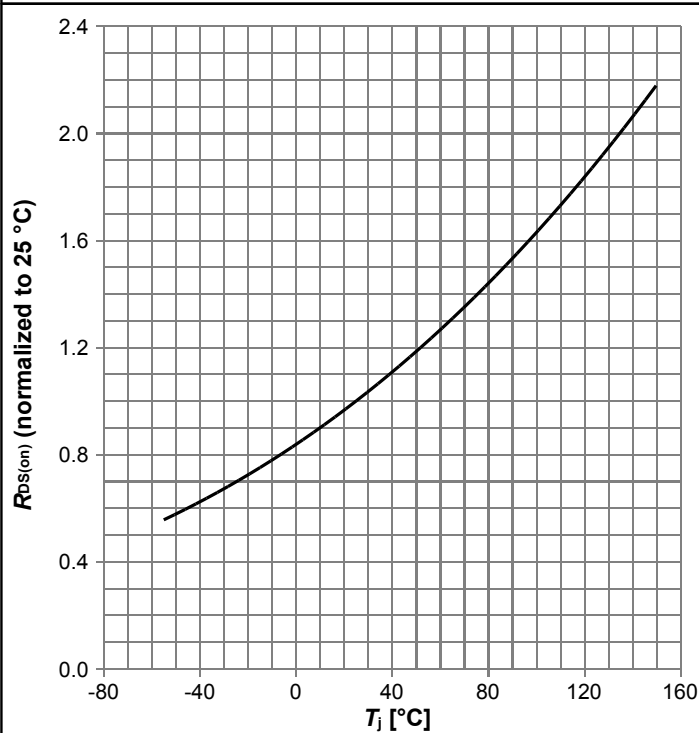
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



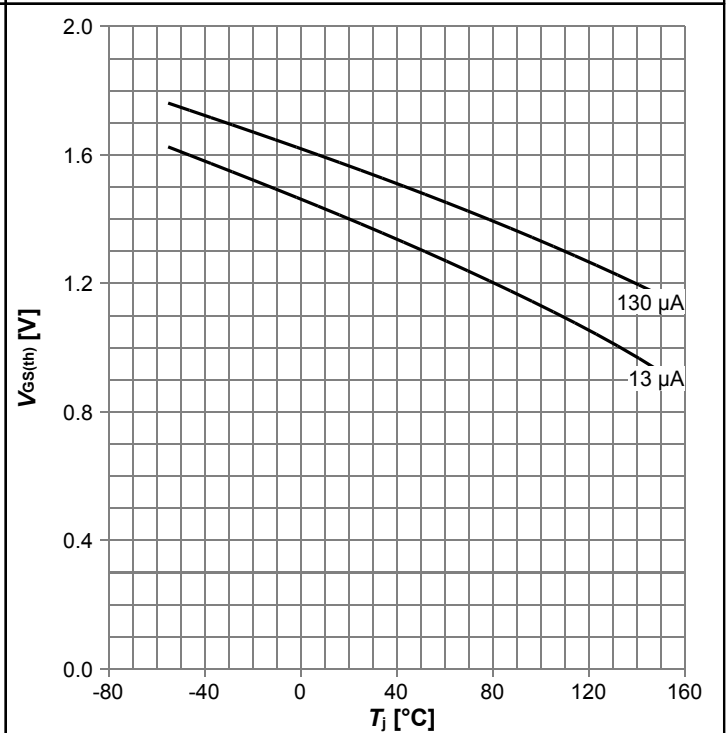
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 0.19\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



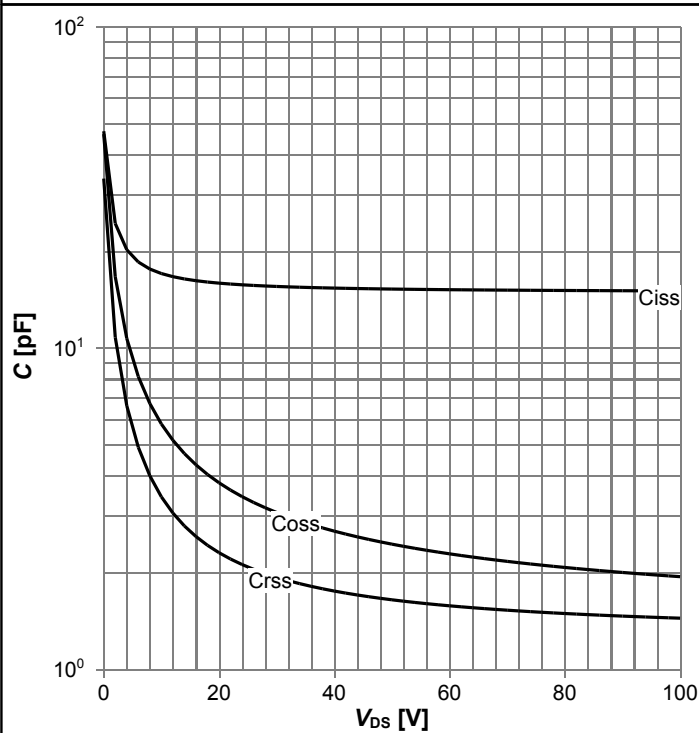
$R_{DS(on)}=f(T_j)$ ,  $I_D=0.19$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



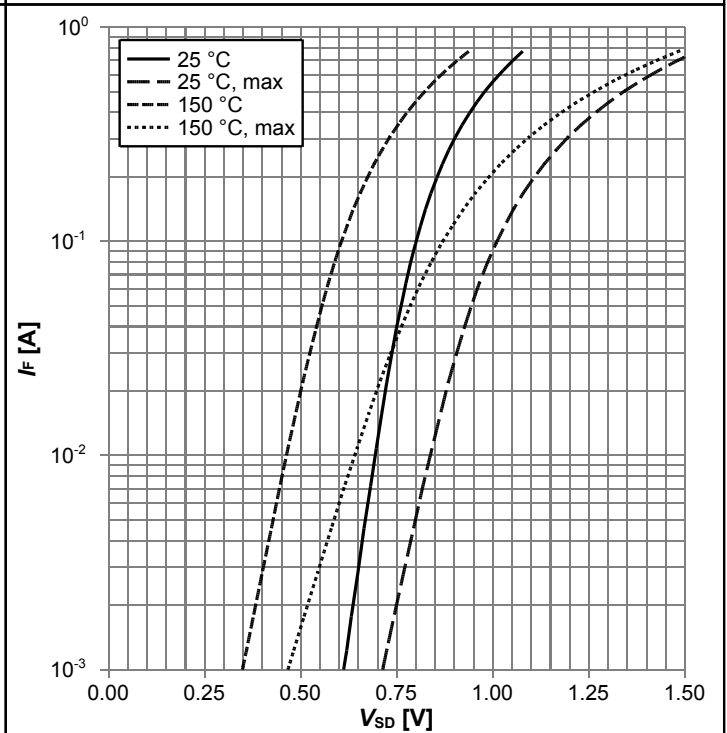
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



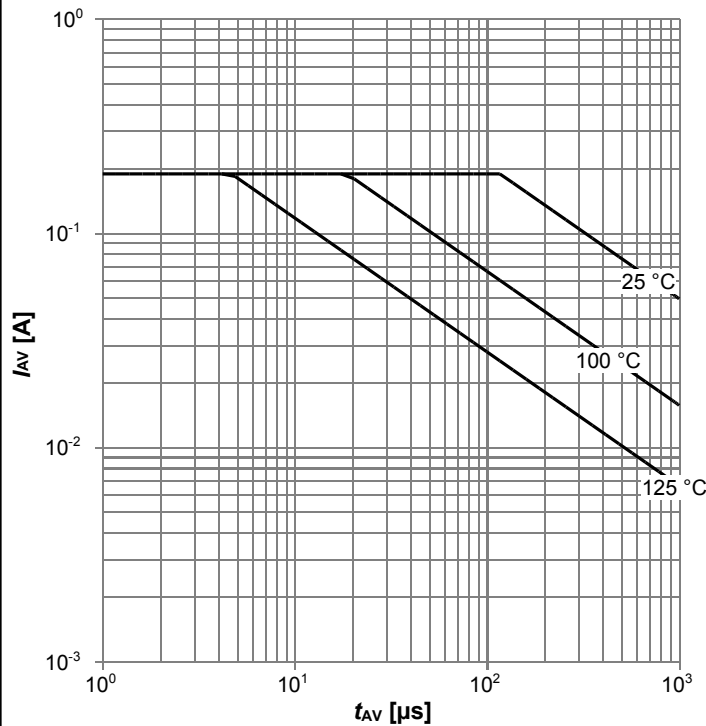
$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

Diagram 12: Forward characteristics of reverse diode



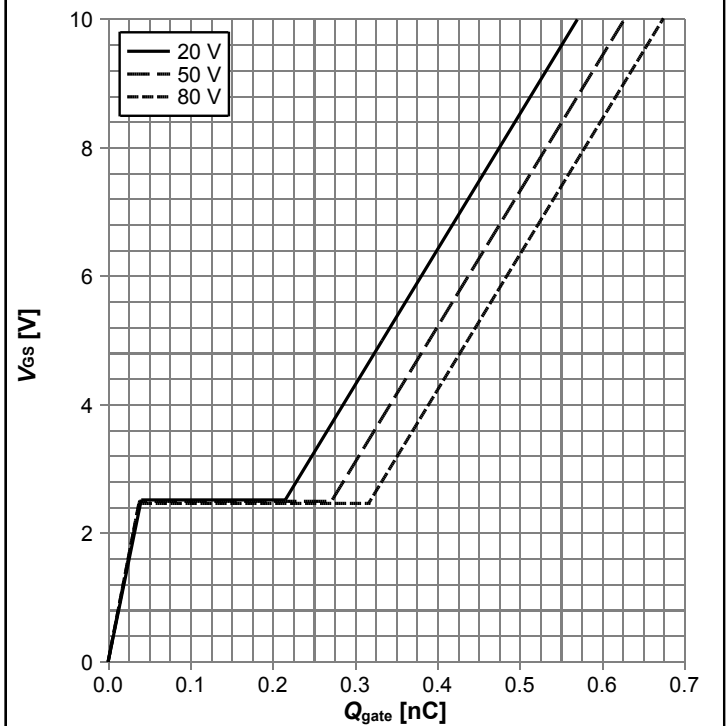
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



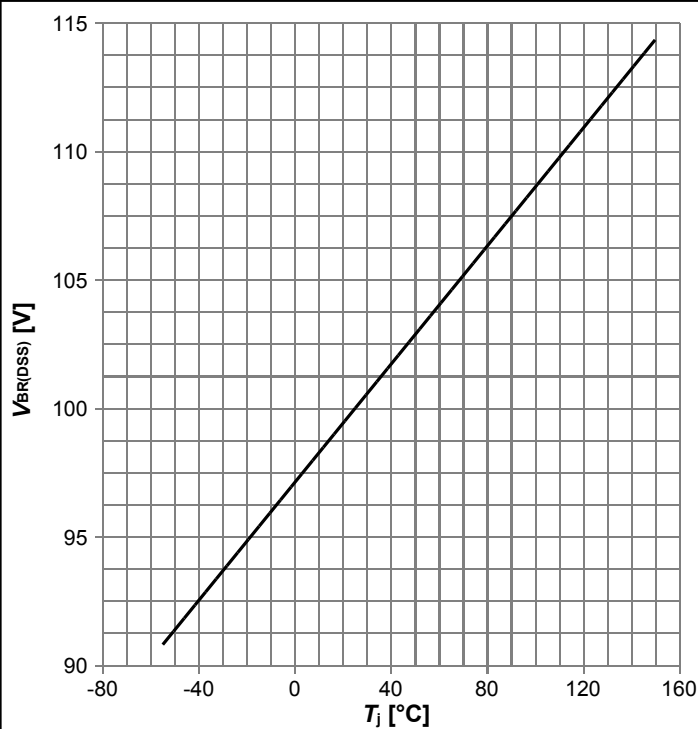
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



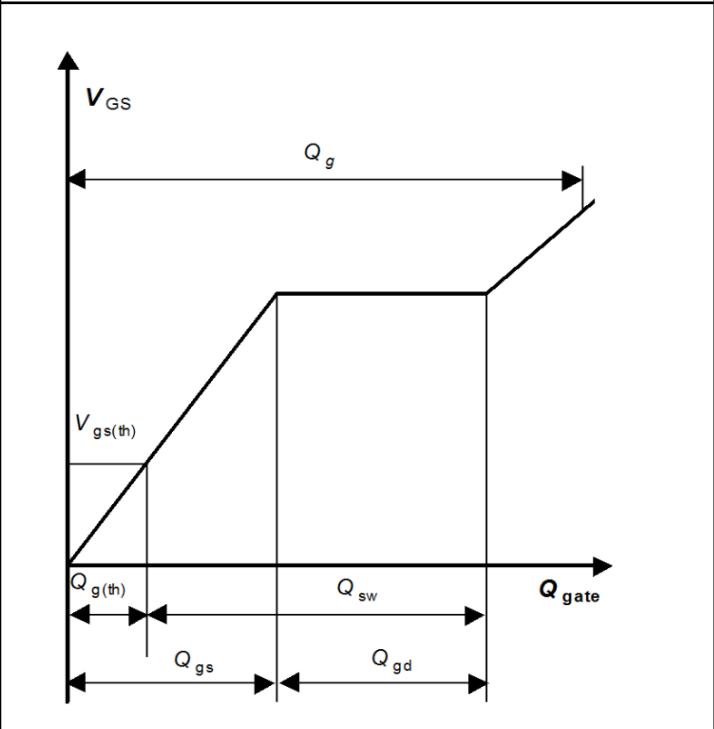
$V_{GS}=f(Q_{gate}), I_D=0.19 \text{ A pulsed}, T_j=25 \text{ °C}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



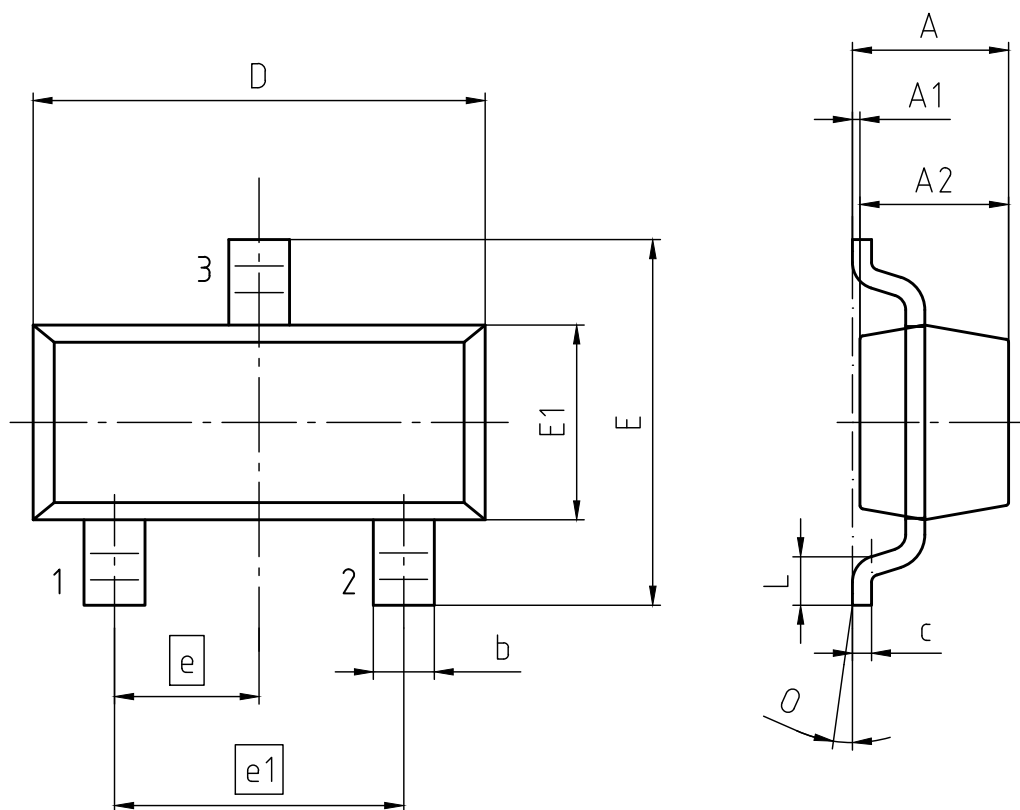
$V_{BR(DSS)}=f(T_j); I_D=250 \mu\text{A}$

Diagram Gate charge waveforms





## 5 Package Outlines



PACKAGE - GROUP NUMBER:		<b>PG-SOT23-3-U01</b>	
REVISION: 01		DATE: 09.12.2020	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	0.89	1.12	
A1	0.01	0.10	
A2	0.88	1.02	
b	0.30	0.50	
c	0.08	0.20	
D	2.80	3.04	
E	2.10	2.64	
E1	1.20	1.40	
e	0.95		
e1	1.90		
L	0.15	0.60	
O	0°	8°	

Figure 1 Outline PG-SOT23, dimensions in mm

## Revision History

BSS123I

**Revision: 2021-02-01, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-01-26	Release of final version
2.1	2021-02-01	Update format

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