



**Overview**

**Basic Features**

- High-Side Switch with Diagnosis and Embedded Protection
- Part of PROFET™+2 12V Family
- ReverseON for low power dissipation in Reverse Polarity
- Green Product (RoHS compliant)

**Protection Features**

- Absolute and dynamic temperature limitation with controlled reactivation
- Overcurrent protection (tripping) with Intelligent Latch
- Undervoltage shutdown
- Overvoltage protection with external components (as shown in [Figure 37](#))

**Diagnostic Features**

- Proportional load current sense
- Open Load in ON and OFF state
- Short circuit to ground and battery

**Product Validation**

Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.

**Description**

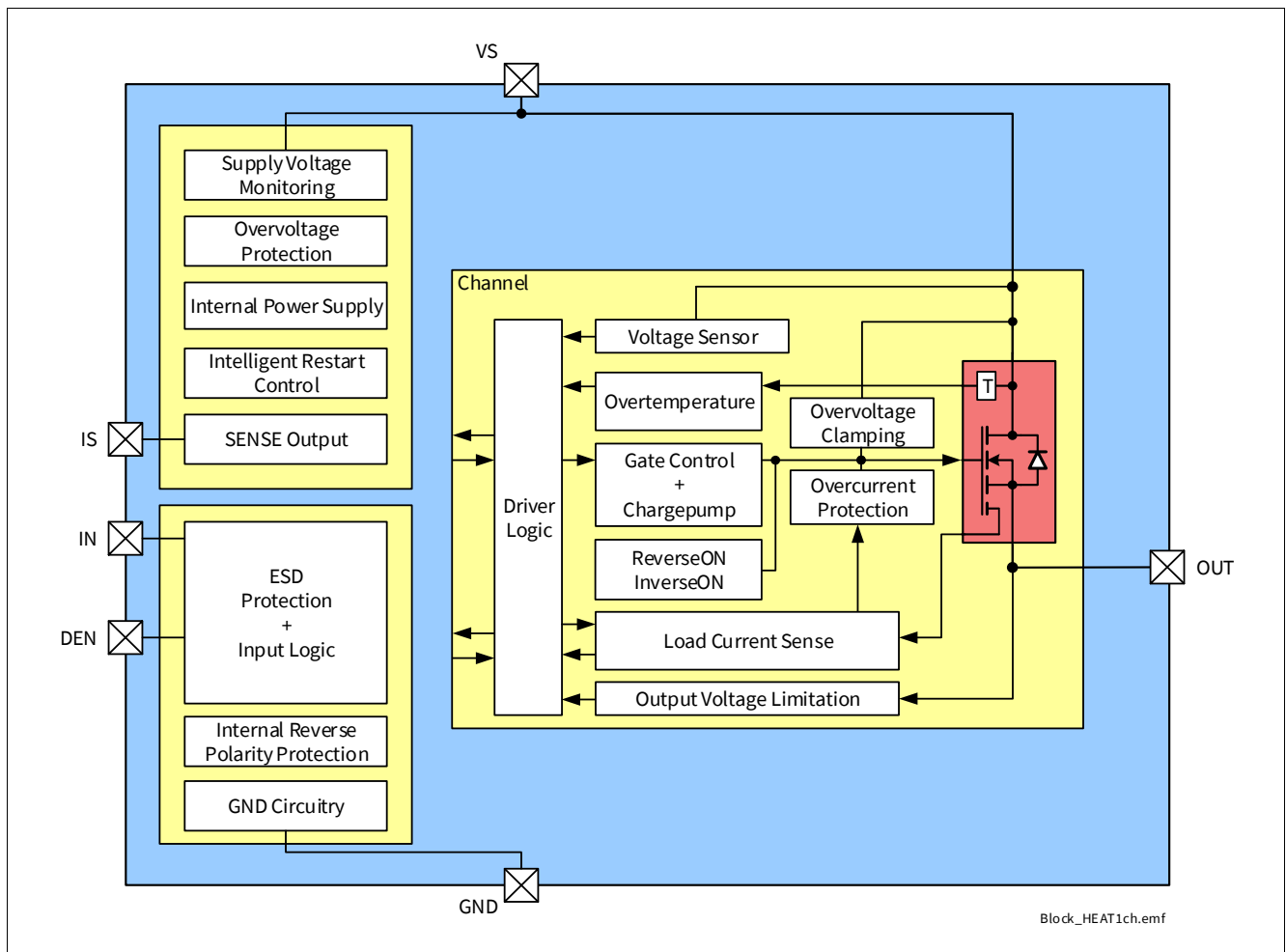
The BTS7002-1EPP is a Smart High-Side Power Switch, providing protection functions and diagnosis.

**Table 1 Product Summary**

Parameter	Symbol	Values
Minimum Operating voltage	$V_{S(OP)}$	4.1 V
Minimum Operating voltage (cranking)	$V_{S(UV)}$	3.1 V
Maximum Operating voltage	$V_S$	28 V
Minimum Overvoltage protection ( $T_J \geq 25\text{ °C}$ )	$V_{DS(CLAMP)_25}$	35 V
Maximum current in OFF mode ( $T_J \leq 85\text{ °C}$ )	$I_{VS(OFF)_85}$	0.9 $\mu$ A
Maximum operative current	$I_{GND(ON\_D)}$	3 mA
Typical ON-state resistance ( $T_J = 25\text{ °C}$ )	$R_{DS(ON)_25}$	2.6 m $\Omega$
Maximum ON-state resistance ( $T_J = 150\text{ °C}$ )	$R_{DS(ON)_150}$	4.8 m $\Omega$
Nominal load current ( $T_A = 85\text{ °C}$ )	$I_{L(NOM)}$	21 A
Minimum overload detection current	$I_{L(OVLO)\_40}$	120 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	$k_{ILIS}$	22700

## 2 Block Diagram and Terms

### 2.1 Block Diagram

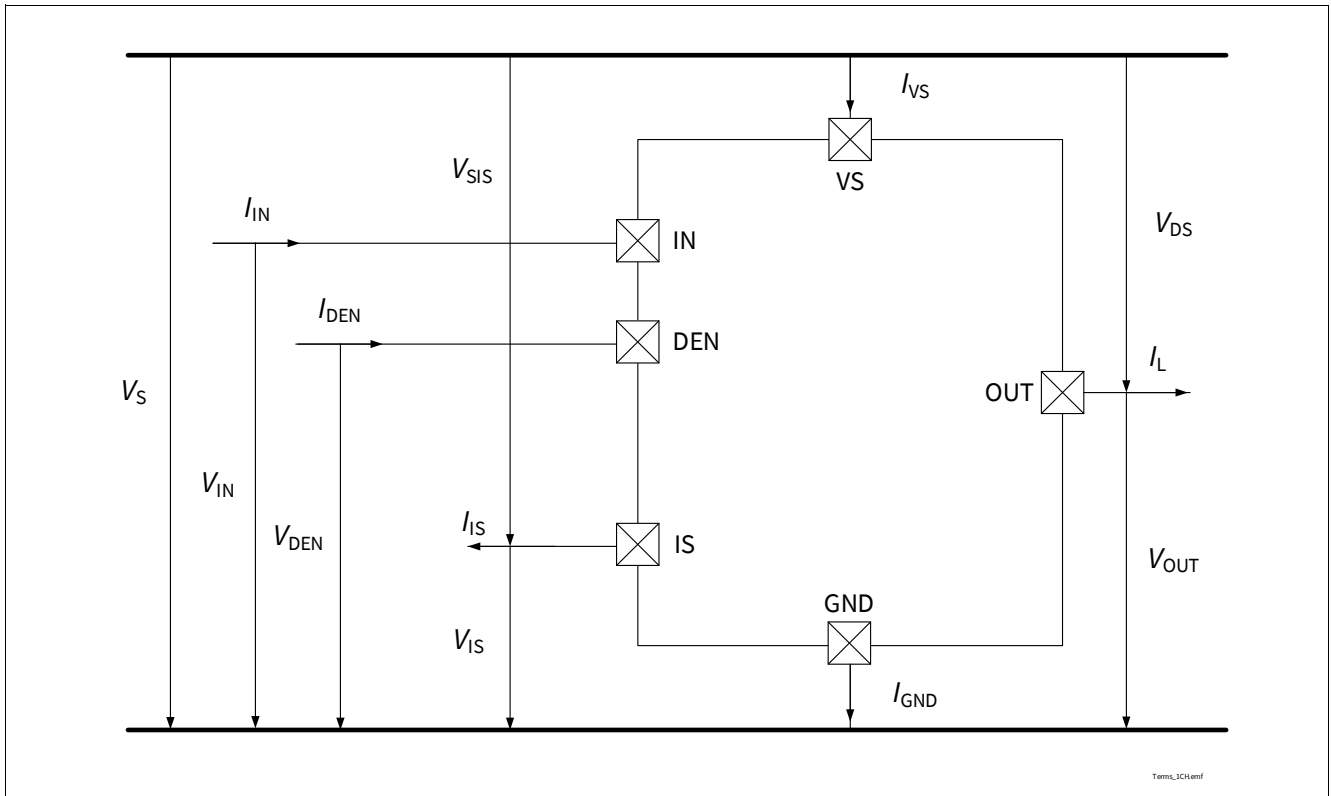


**Figure 2 Block Diagram of BTS7002-1EPP**

**Block Diagram and Terms**

**2.2 Terms**

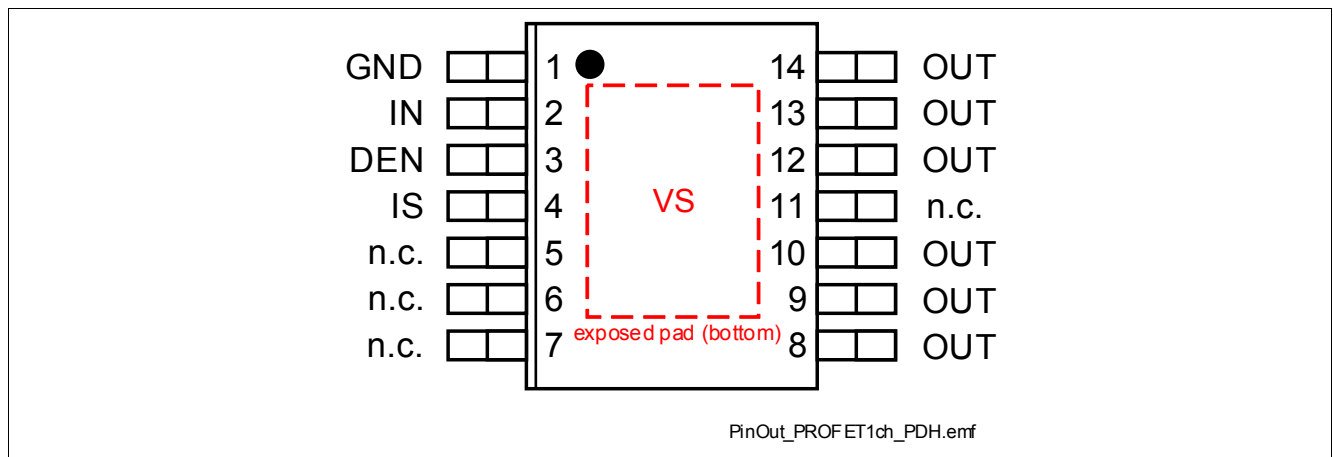
**Figure 3** shows all terms used in this data sheet, with associated convention for positive values.



**Figure 3 Voltage and Current Convention**

### **3 Pin Configuration**

#### **3.1 Pin Assignment**



**Figure 4 Pin Configuration**

**Pin Configuration**

**3.2 Pin Definitions and Functions**

**Table 2 Pin Definition**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
EP	VS (exposed pad)	<b>Supply Voltage</b> Battery voltage
1	GND	<b>Ground</b> Signal ground
2	IN	<b>Input Channel</b> Digital signal to switch ON the channel (“high” active) If not used: connect to GND pin or to module ground with resistor $R_{IN} = 4.7 \text{ k}\Omega$
3	DEN	<b>Diagnostic Enable</b> Digital signal to enable device diagnosis (“high” active) and to clear the protection latch of channel If not used: connect to GND pin or to module ground with resistor $R_{DEN} = 4.7 \text{ k}\Omega$
4	IS	<b>SENSE current output</b> Analog/digital signal for diagnosis If not used: left open
5-7, 11	n.c.	Not connected, internally not bonded
8-10, 12-14	OUT	<b>Output</b> Protected high-side power output channel <sup>1)</sup>

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

**General Product Characteristics**

**4 General Product Characteristics**

**4.1 Absolute Maximum Ratings - General**

**Table 3 Absolute Maximum Ratings<sup>1)</sup>**

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply pins</b>							
Power Supply Voltage	$V_S$	-0.3	–	28	V	–	P_4.1.0.1
Load Dump Voltage	$V_{BAT(LD)}$	–	–	35	V	suppressed Load Dump acc. to ISO16750-2 (2010). $R_f = 2\ \Omega$	P_4.1.0.3
Supply Voltage for Short Circuit Protection	$V_{BAT(SC)}$	0	–	24	V	Setup acc. to AEC-Q100-012	P_4.1.0.25
Reverse Polarity Voltage	$-V_{BAT(REV)}$	–	–	16	V	$t \leq 2\text{ min}$ $T_A = +25\text{ °C}$ Setup as described in <a href="#">Chapter 10</a>	P_4.1.0.5
Current through GND Pin	$I_{GND}$	-50	–	50	mA	$R_{GND}$ according to <a href="#">Chapter 10</a>	P_4.1.0.9

**Logic & control pins (Digital Input = DI)**

**DI = IN, DEN**

Current through DI Pin	$I_{DI}$	-1	–	2	mA	<sup>2)</sup>	P_4.1.0.14
Current through DI Pin Reverse Battery Condition	$I_{DI(REV)}$	-1	–	10	mA	<sup>2)</sup> $t \leq 2\text{ min}$	P_4.1.0.36

**IS pin**

Voltage at IS Pin	$V_{IS}$	-1.5	–	$V_S$	V	$I_{IS} = 10\ \mu\text{A}$	P_4.1.0.16
Current through IS Pin	$I_{IS}$	-25	–	$I_{IS(SAT),M}$ AX	mA	–	P_4.1.0.18

**Temperatures**

Junction Temperature	$T_J$	-40	–	150	°C	–	P_4.1.0.19
Storage Temperature	$T_{STG}$	-55	–	150	°C	–	P_4.1.0.20

**General Product Characteristics**

**Table 3 Absolute Maximum Ratings<sup>1)</sup>** (continued)

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>ESD Susceptibility</b>							
ESD Susceptibility all Pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM <sup>3)</sup>	P_4.1.0.21
ESD Susceptibility OUT vs GND and VS connected (HBM)	$V_{ESD(HBM)_{OU T}}$	-4	–	4	kV	HBM <sup>3)</sup>	P_4.1.0.22
ESD Susceptibility all Pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	CDM <sup>4)</sup>	P_4.1.0.23
ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	$V_{ESD(CDM)_{CR N}}$	-750	–	750	V	CDM <sup>4)</sup>	P_4.1.0.24

- 1) Not subject to production test - specified by design.
- 2) Maximum  $V_{DI}$  to be considered for Latch-Up tests: 5.5 V.
- 3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.
- 4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**4.2 Absolute Maximum Ratings - Power Stages**

**4.2.1 Power Stage - 2 mΩ**

**Table 4 Absolute Maximum Ratings<sup>1)</sup>**

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Single Pulse	$E_{AS}$	–	–	315	mJ	$I_L = 2 * I_{L(NOM)}$ $T_{J(0)} = 150\text{ °C}$ $V_S = 28\text{ V}$	P_4.2.10.1



**General Product Characteristics**

**Table 4 Absolute Maximum Ratings<sup>1)</sup>** (continued)

$T_J = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Repetitive Pulse	$E_{AR}$	–	–	74	mJ	$I_L = I_{L(NOM)}$ $T_{J(0)} = 85\text{ °C}$ $V_S = 13.5\text{ V}$ 1M cycles	P_4.2.10.2
Load Current	$ I_L $	–	–	$I_{L(OVL0), MAX}$	A	–	P_4.2.10.3

1) Not subject to production test - specified by design.

**4.3 Functional Range**

**Table 5 Functional Range - Supply Voltage and Temperature<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	6	13.5	18	V	–	P_4.3.0.1
Lower Extended Supply Voltage Range for Operation	$V_{S(EXT,LOW)}$	3.1	–	6	V	<sup>2)3)</sup> (parameter deviations possible)	P_4.3.0.2
Supply Voltage Range reached after Overload Protection activation leading to “Undervoltage on $V_S$ ” condition	$V_{S(EXT,CVG)}$	–	–	3.1	V	$C_{VSGND}$ is required when the Overload Protection is triggered (see <a href="#">Chapter 8.2</a> ) and the observed number of retries is different from what specified in <a href="#">Chapter 8.3.1</a>	P_4.3.0.7
Upper Extended Supply Voltage Range for Operation	$V_{S(EXT,UP)}$	18	–	28	V	<sup>3)</sup> (parameter deviations possible)	P_4.3.0.3
Junction Temperature	$T_J$	-40	–	150	°C	–	P_4.3.0.5

1) Not subject to production test - specified by design.

2) In case of  $V_S$  voltage decreasing:  $V_{S(EXT,LOW),MIN} = 3.1\text{ V}$ . In case of  $V_S$  voltage increasing:  $V_{S(EXT,LOW),MIN} = 4.1\text{ V}$ .

3) Protection functions still operative.

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics tables.

**General Product Characteristics**

**4.4 Thermal Resistance**

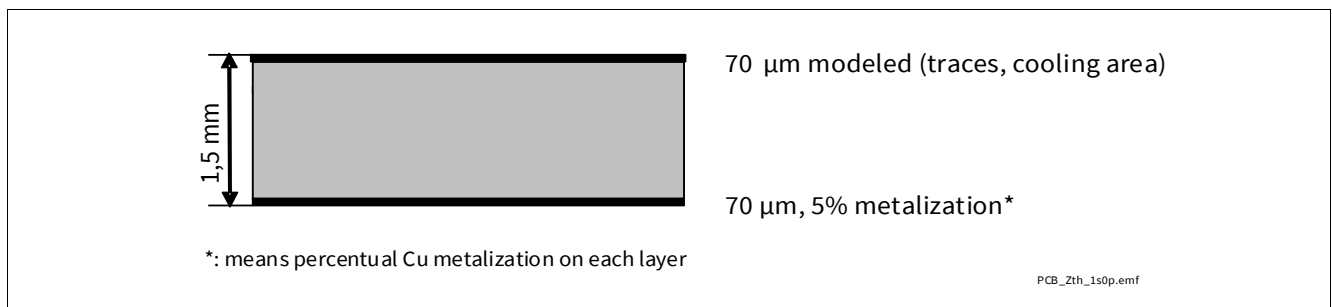
Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 6 Thermal Resistance<sup>1)</sup>**

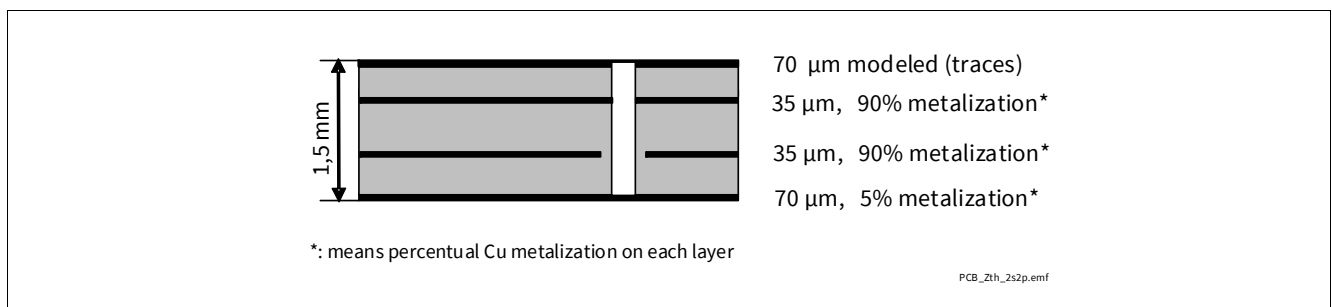
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Characterization Parameter Junction-Top	$\Psi_{JTOP}$	–	3	5	K/W	<sup>2)</sup>	P_4.4.0.1
Thermal Resistance Junction-to-Case	$R_{thJC}$	–	0.78	1.3	K/W	<sup>2)</sup> simulated at exposed pad	P_4.4.0.2
Thermal Resistance Junction-to-Ambient	$R_{thJA}$	–	30.7	–	K/W	<sup>2)</sup>	P_4.4.0.3

- 1) Not subject to production test - specified by design.
- 2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at  $T_A = 105^\circ\text{C}$ ,  $P_{DISSIPATION} = 1\text{ W}$ .

**4.4.1 PCB Setup**

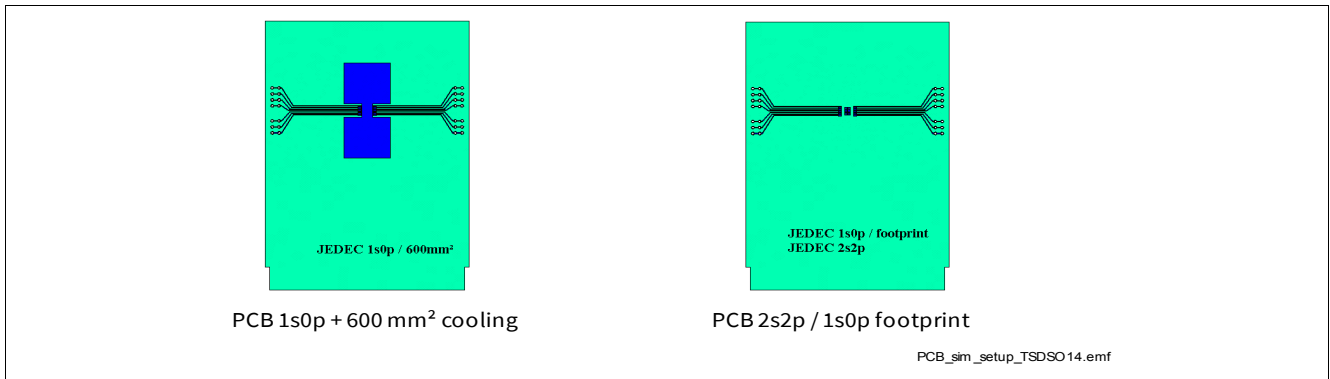


**Figure 5 1s0p PCB Cross Section**

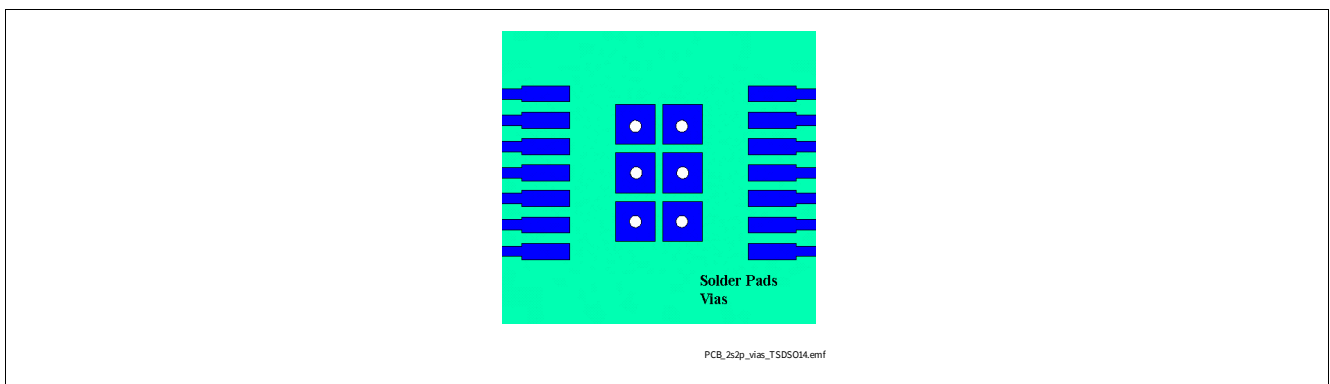


**Figure 6 2s2p PCB Cross Section**

**General Product Characteristics**



**Figure 7 PCB setup for thermal simulations**

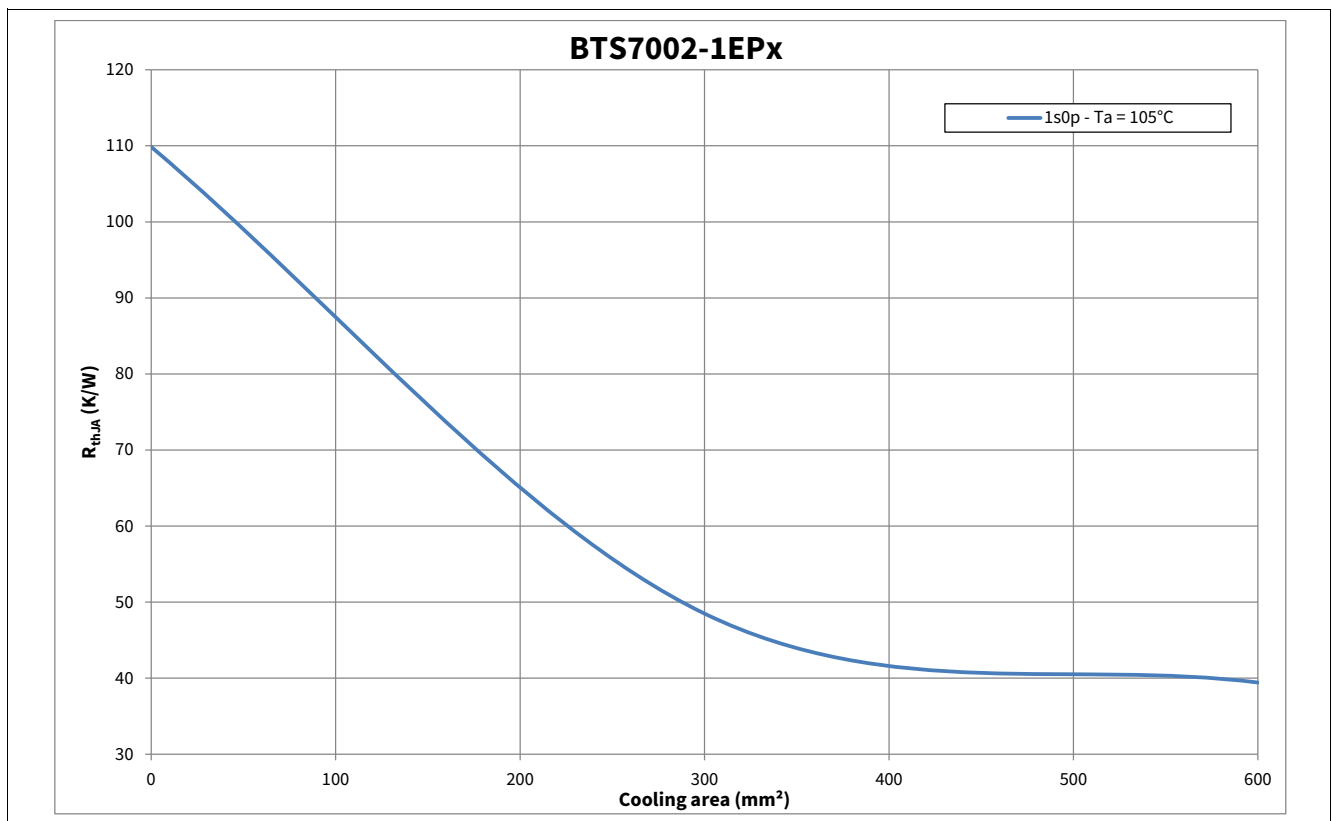


**Figure 8 Thermal vias on PCB for 2s2p PCB setup**

### 4.4.2 Thermal Impedance



**Figure 9** Typical Thermal Impedance. PCB setup according [Chapter 4.4.1](#)



**Figure 10** Thermal Resistance on 1s0p PCB with various cooling surfaces

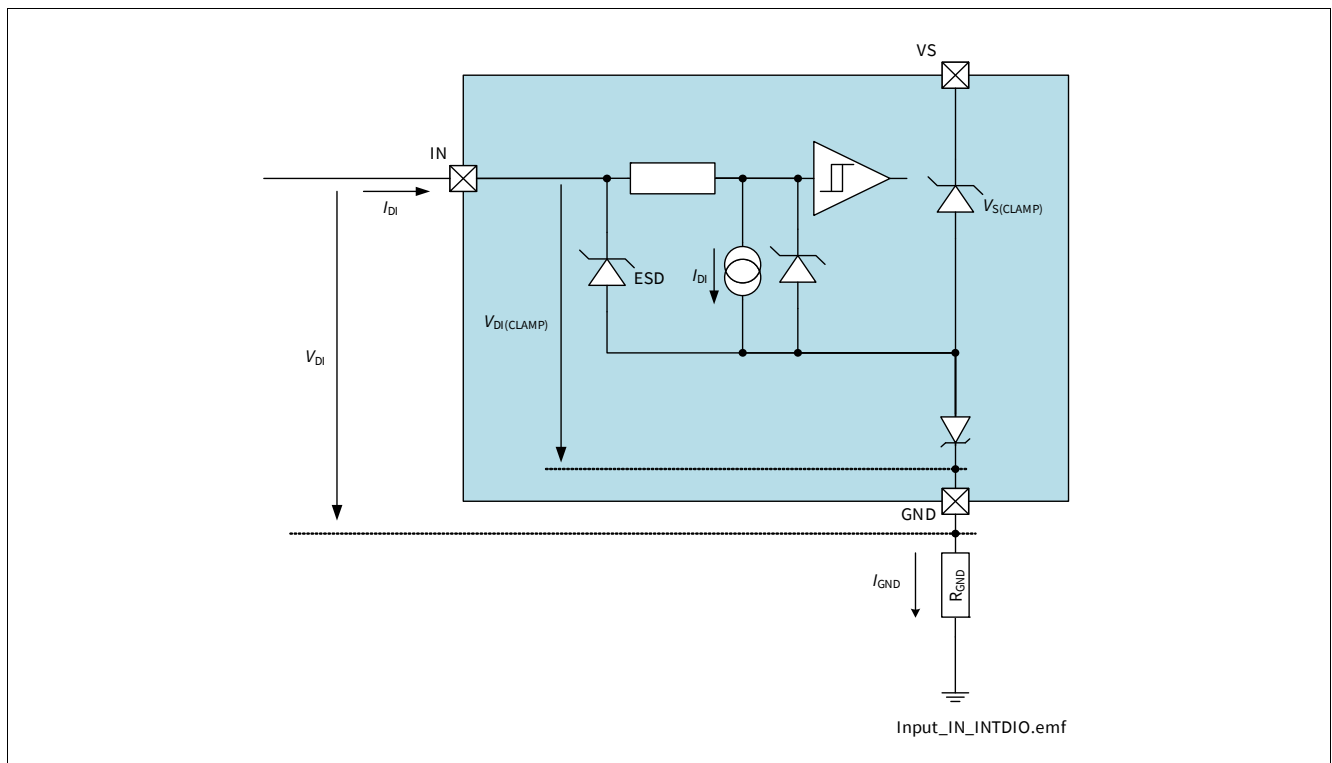
**Logic Pins**

**5 Logic Pins**

The device has 2 digital pins.

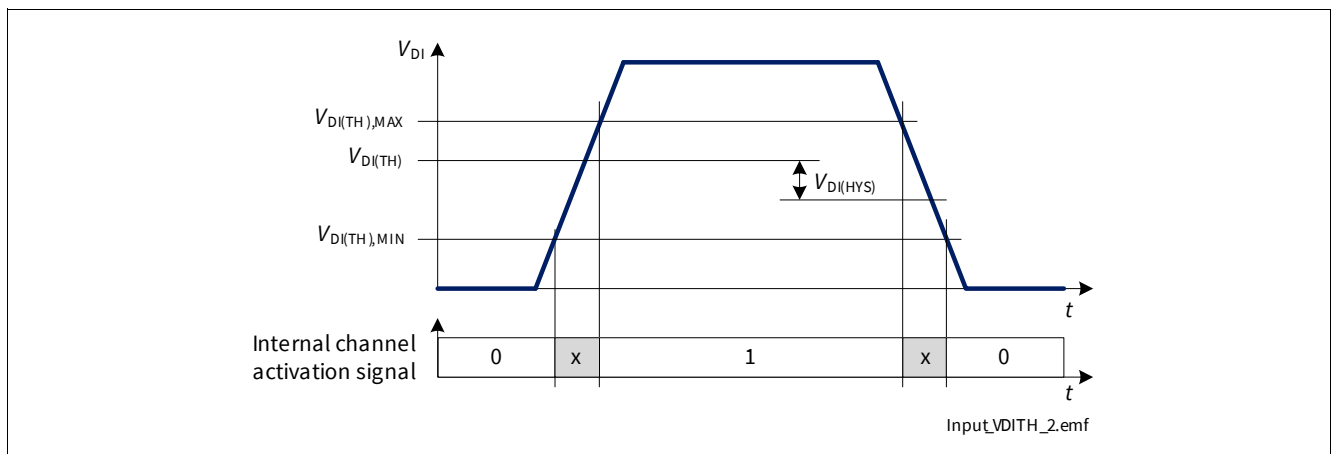
**5.1 Input Pin (IN)**

The input pin IN activates the output channel. The input circuitry is compatible with 3.3V and 5V microcontroller (see [Chapter 10](#) for the complete application setup overview). The electrical equivalent of the input circuitry is shown in [Figure 11](#). In case the pin is not used, it should be pulled to module GND or device GND pin via  $R_{IN} = 4.7\text{ k}\Omega$ .



**Figure 11 Input circuitry**

The logic thresholds for “low” and “high” states are defined by parameters  $V_{DI(TH)}$  and  $V_{DI(HYS)}$ . The relationship between these two values is shown in [Figure 12](#). The voltage  $V_{IN}$  needed to ensure a “high” state is always higher than the voltage needed to ensure a “low” state.



**Figure 12 Input Threshold voltages and hysteresis**

**Logic Pins**

**5.2 Diagnosis Pin**

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and can be used to reset the latched protection (Protection circuitry not disabled by DEN). When DEN pin is set to “high”, the diagnosis is enabled (see [Chapter 9.2](#) for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance).

The transition from “high” to “low” of DEN pin clears the protection latch of the channel depending on the logic state of IN pin and DEN pulse length (see [Chapter 8.3](#) for more details). The internal structure of diagnosis pins is the same as the one of input pins. See [Figure 11](#) for more details.

**5.3 Electrical Characteristics Logic Pins**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Digital Input (DI) pins = IN, DEN

**Table 7 Electrical Characteristics: Logic Pins - General**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Voltage Threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.1
Digital Input Clamping Voltage	$V_{DI(CLAMP1)}$	–	7	–	V	<sup>1)</sup> $I_{DI} = 1\text{ mA}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.2
Digital Input Clamping Voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	$I_{DI} = 2\text{ mA}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.3
Digital Input Hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	<sup>1)</sup> See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.4
Digital Input Current (“high”)	$I_{DI(H)}$	2	10	25	μA	$V_{DI} = 2\text{ V}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.5
Digital Input Current (“low”)	$I_{DI(L)}$	2	10	25	μA	$V_{DI} = 0.8\text{ V}$ See <a href="#">Figure 11</a> and <a href="#">Figure 12</a>	P_5.4.0.6

1) Not subject to production test - specified by design.

**Power Supply**

## 6 Power Supply

The BTS7002-1EPP is supplied by  $V_S$ , which is used for the internal logic as well as supply for the power output stage.  $V_S$  has an undervoltage detection circuit, which prevents the activation of the power output stage and diagnosis in case the applied voltage is below the undervoltage threshold ( $V_S < V_{S(OP)}$ ). During power up, the internal power on signal is set when supply voltage ( $V_S$ ) exceeds the minimum operating voltage ( $V_S > V_{S(OP)}$ ).

### 6.1 Operation Modes

BTS7002-1EPP has the following operation modes in case of  $V_S > V_{S(OP)}$ :

- OFF mode
- ON mode
- Diagnosis in ON mode
- Diagnosis in OFF mode
- Fault

The transition between operation modes is determined according to these variables:

- Logic level at IN pin
- Logic level at DEN pin
- Internal latch
- Sense current  $I_{IS}$  level

The truth table in case of  $V_S > V_{S(OP)}$  is shown in **Table 8**. The behavior of BTS7002-1EPP as well as some parameters may change in dependence on the operation mode of the device.

There are three parameters describing each operation mode of BTS7002-1EPP:

- Status of the output channel
- Status of the diagnosis
- Current consumption at VS pin (measured by  $I_{VS}$  in OFF mode,  $I_{GND}$  in all other operative modes)

**Table 8 Operation Mode truth table**

IN	DEN	Internal latch	$I_{IS}$	Operative Mode	Comment
L	L	L	leakage	OFF	DMOS channel is OFF
L	L	H	leakage	OFF	DMOS channel is OFF
L	H	L	leakage	OFF_DIAG	Diagnostic in OFF-mode
			open load		Diagnostic in OFF-mode
			fault		Diagnostic in OFF-mode
L	H	H	fault		Diagnostic in OFF-mode
H	L	L	leakage	ON	DMOS channel is ON, no diagnostic
H	L	H	leakage	fault	DMOS channel is switched OFF due to failure
H	H	L	$I_{IS}$	ON_DIAG	DMOS channel is ON and diagnostic
H	H	H	fault	fault	DMOS channel is switched OFF due to failure

## Power Supply

### 6.1.1 OFF mode

When BTS7002-1EPP is in OFF mode, the output channel is OFF. The current consumption is minimum (see parameter  $I_{VS(OFF)}$ ). No Overtemperature, Overload protection mechanism and no diagnosis function is active when the device is in OFF mode.

### 6.1.2 ON mode

ON (IN = High; DEN = Low) mode is the normal operation mode of BTS7002-1EPP. Device current consumption is specified with  $I_{GND(ON\_D)} + I_{IS(OFF)}$  (measured at GND pin because the current at VS pin includes the load current). Overcurrent and Overtemperature protections are active. No diagnosis function is active.

### 6.1.3 OFF\_Diag mode

The device is in OFF\_Diag mode as long as DEN pin is set to “high” and IN pin is set to “low”. The output channel is OFF. If an open load case happens, an Open Load in OFF current  $I_{IS(OLOFF)}$  may be present at IS pin. In such situation, the current consumption of the device is increased.

### 6.1.4 ON\_Diag mode

The device is in normal ON mode with current sense function.  $I_{IS}$  or  $I_{IS(FAULT)}$  will be present at IS pin. Device current consumption is specified with  $I_{GND(ON\_D)}$ . Depending on the load condition, either a fault current  $I_{IS(FAULT)}$  or  $I_{IS}$  current may be present at IS pin.

### 6.1.5 Fault mode

The device is in Fault mode as soon as a protection event happens which affects that the device switches off due to its protection function. In Fault mode, a  $I_{IS(FAULT)}$  signal is presenting at IS pin during the DEN signal is “high”.

## 6.2 Undervoltage on $V_S$

Between  $V_{S(OP)}$  and  $V_{S(UV)}$  the undervoltage mechanism is triggered. If the device is operative (in ON mode) and the supply voltage drops below the undervoltage threshold  $V_{S(UV)}$ , the internal logic switches OFF the output channel.

As soon as the supply voltage  $V_S$  is above the operative threshold  $V_{S(OP)}$ , the channel is switched ON again. The restart is delayed with a time  $t_{DELAY(UV)}$  which protects the device in case the undervoltage condition is caused by a short circuit event (according to AEC-Q100-012), as shown in [Figure 13](#).

If the device is in OFF mode and the input is set to “high”, the channel will be switched ON if  $V_S > V_{S(OP)}$  without waiting for  $t_{DELAY(UV)}$ .



Power Supply

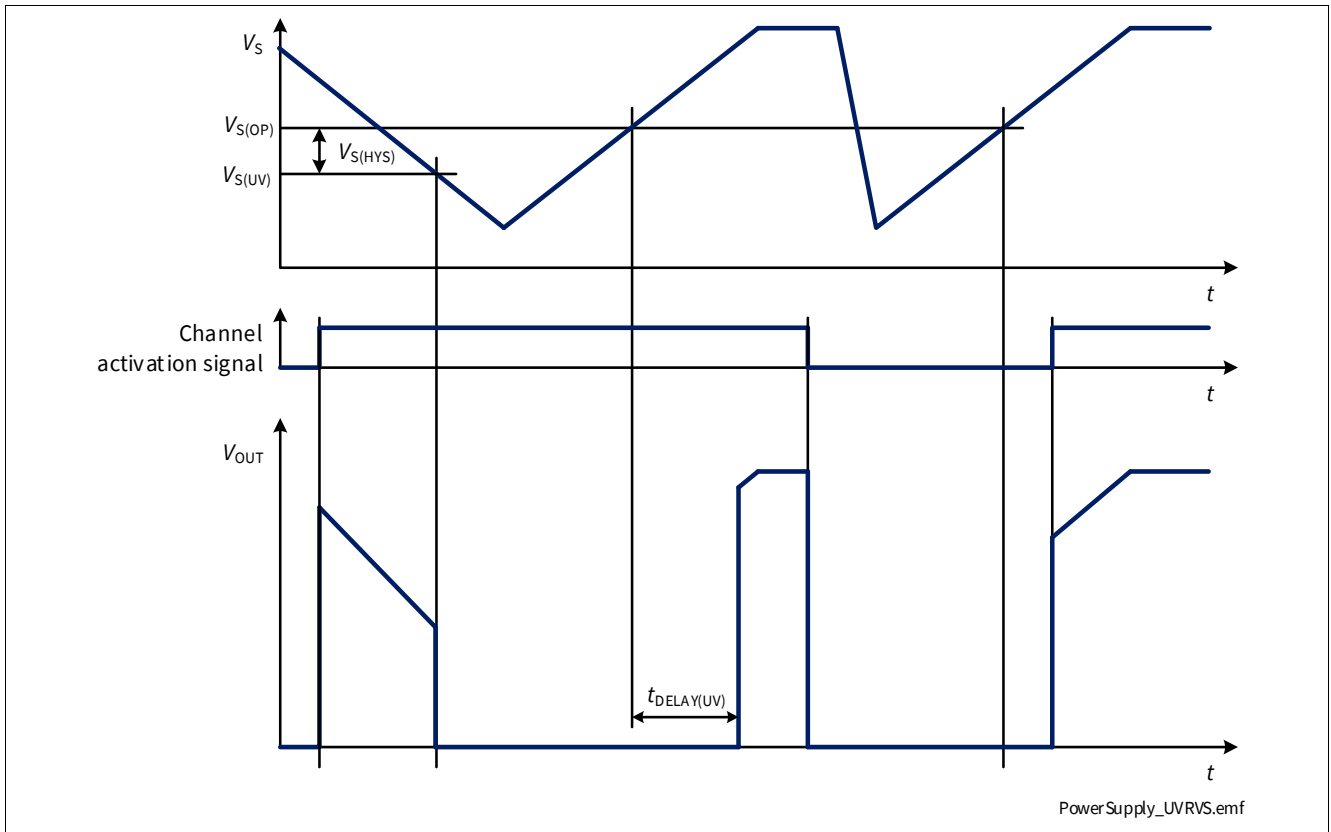


Figure 13  $V_S$  undervoltage behavior

**Power Supply**

**6.3 Electrical Characteristics Power Supply**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**Table 9 Electrical Characteristics: Power Supply - General**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>VS pin</b>							
Power Supply Undervoltage Shutdown	$V_{S(UV)}$	1.8	2.3	3.1	V	$V_S$ decreasing IN = "high" From $V_{DS} \leq 0.5\text{ V}$ to $V_{DS} = V_S$ See <a href="#">Figure 13</a>	P_6.4.0.1
Power Supply Minimum Operating Voltage	$V_{S(OP)}$	2.0	3.0	4.1	V	$V_S$ increasing IN = "high" From $V_{DS} = V_S$ to $V_{DS} \leq 0.5\text{ V}$ See <a href="#">Figure 13</a>	P_6.4.0.3
Power Supply Undervoltage Shutdown Hysteresis	$V_{S(HYS)}$	–	0.7	–	V	<sup>1)</sup> $V_{S(OP)} - V_{S(UV)}$ See <a href="#">Figure 13</a>	P_6.4.0.6
Power Supply Undervoltage Recovery Time	$t_{DELAY(UV)}$	2.5	5	7.5	ms	$dV_S/dt \leq 0.5\text{ V}/\mu\text{s}$ $V_S \geq -1\text{ V}$ See <a href="#">Figure 13</a>	P_6.4.0.7
Breakdown Voltage between GND and VS Pins in Reverse Battery	$-V_{S(REV)}$	16	–	30	V	<sup>1)</sup> $I_{GND(REV)} = 7\text{ mA}$ $T_J = 150\text{ °C}$	P_6.4.0.9

1) Not subject to production test - specified by design.

**Power Supply**

**6.4 Electrical Characteristics Power Supply - Product Specific**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**6.4.1 BTS7002-1EPP**

**Table 10 Electrical Characteristics: Power Supply BTS7002-1EPP**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Current Consumption in OFF Mode with Loads	$I_{VS(OFF)_85}$	–	0.1	0.9	$\mu\text{A}$	1) $V_S = 18\text{ V}$ $V_{OUT} = 0\text{ V}$ IN = DEN = “low” $T_J \leq 85\text{ °C}$	P_6.5.20.1
Supply Current Consumption in OFF Mode with Loads	$I_{VS(OFF)_150}$	–	1	27	$\mu\text{A}$	$V_S = 18\text{ V}$ $V_{OUT} = 0\text{ V}$ IN = DEN = “low” $T_J = 150\text{ °C}$	P_6.5.20.2
Operating Current in ON_Diag Mode (Channel ON)	$I_{GND(ON\_D)}$	–	2	3	mA	$V_S = 18\text{ V}$ IN = DEN = “high”	P_6.5.20.3
Operating Current in OFF_Diag Mode	$I_{GND(OFF\_D)}$	–	1.2	1.8	mA	$V_S = 18\text{ V}$ IN = “low”; DEN = “high”	P_6.5.20.5

1) Not subject to production test - specified by design.

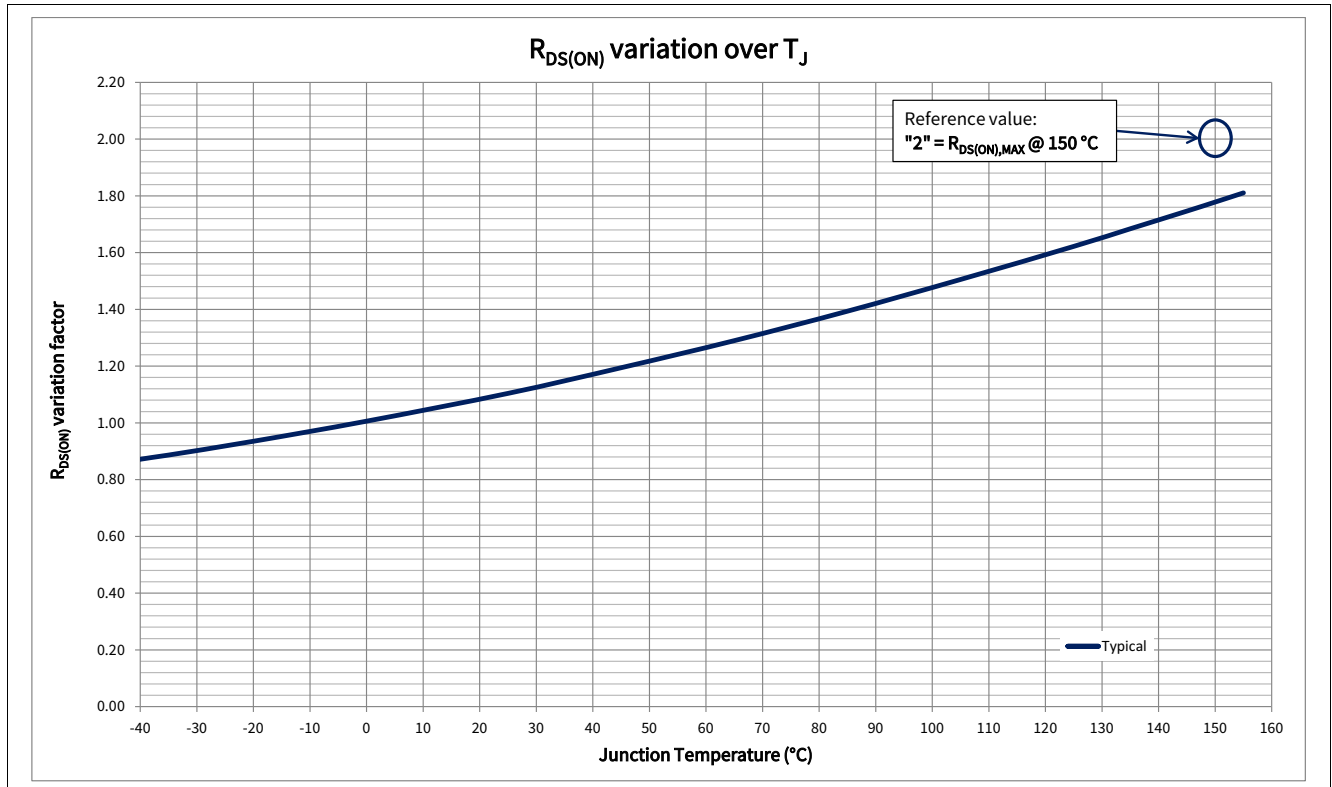
Power Stages

## 7 Power Stages

The high-side power stage is built using a N-channel vertical Power MOSFET with charge pump.

### 7.1 Output ON-State Resistance

The ON-state resistance  $R_{DS(ON)}$  depends mainly on junction temperature  $T_J$ . **Figure 14** shows the variation of  $R_{DS(ON)}$  across the whole  $T_J$  range. The value “2” on the y-axis corresponds to the maximum  $R_{DS(ON)}$  measured at  $T_J = 150\text{ °C}$ .



**Figure 14**  $R_{DS(ON)}$  variation factor

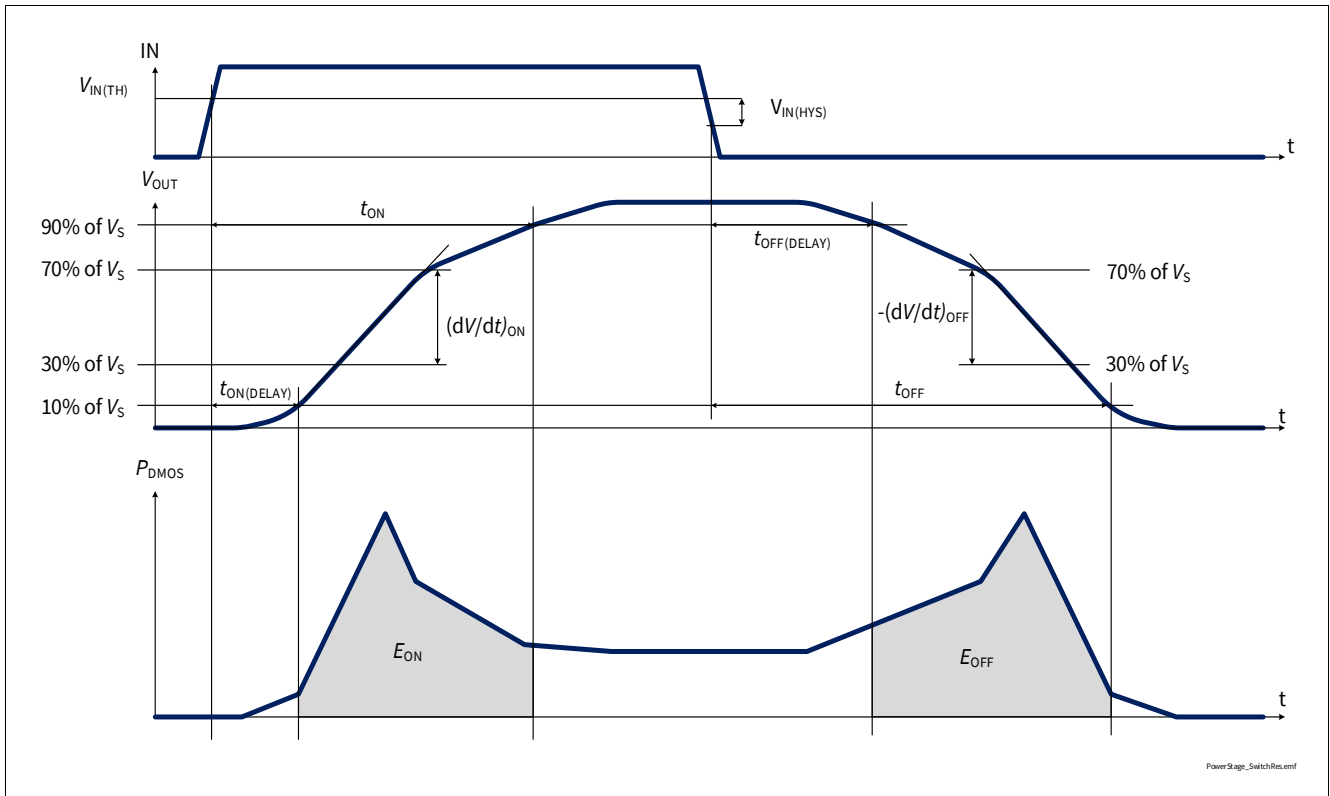
The behavior in Reverse Polarity is described in [Chapter 8.4.1](#).

### 7.2 Switching loads

#### 7.2.1 Switching Resistive Loads

When switching resistive loads, the switching times and slew rates shown in **Figure 15** can be considered. The switch energy values  $E_{ON}$  and  $E_{OFF}$  are proportional to load resistance and times  $t_{ON}$  and  $t_{OFF}$ .

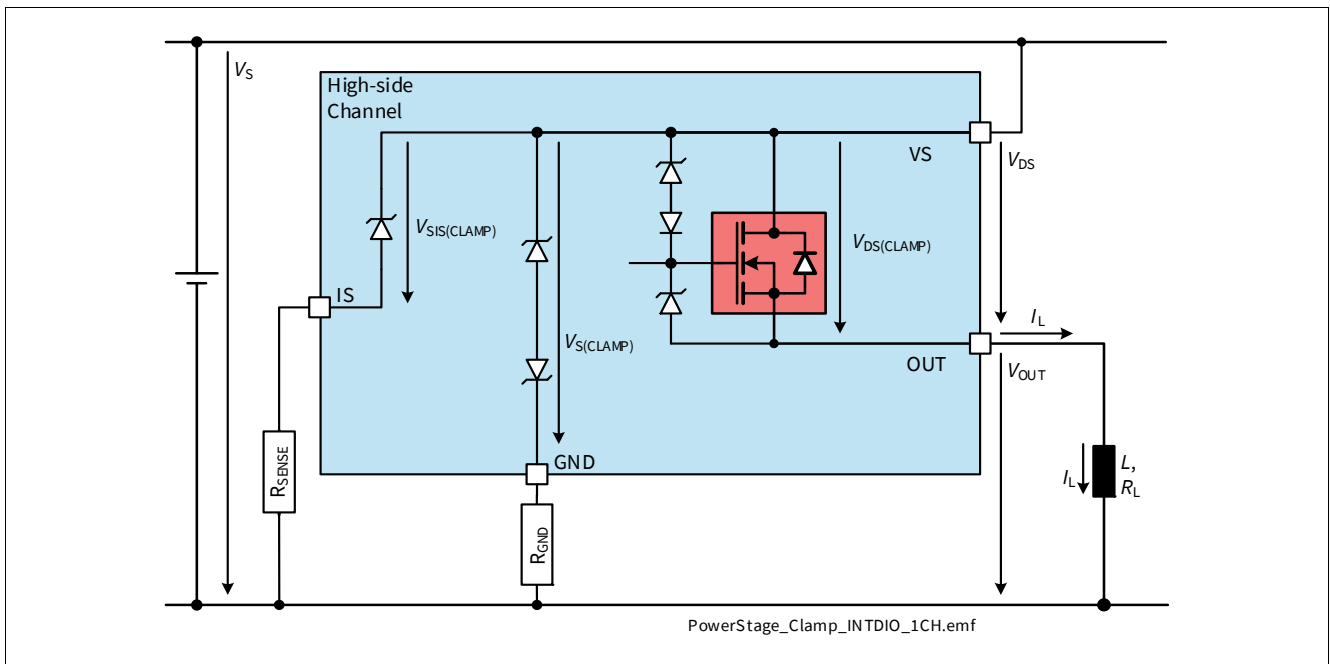
**Power Stages**



**Figure 15 Switching a Resistive Load**

**7.2.2 Switching Inductive Loads**

When switching OFF inductive loads with high-side switches, the voltage  $V_{OUT}$  drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the negative output voltage so that  $V_{DS} = V_{DS(CLAMP)}$ . **Figure 16** shows a concept drawing of the implementation. The clamping structure is available in all operation modes listed in **Chapter 6.1**.



**Figure 16 Output Clamp concept**

## Power Stages

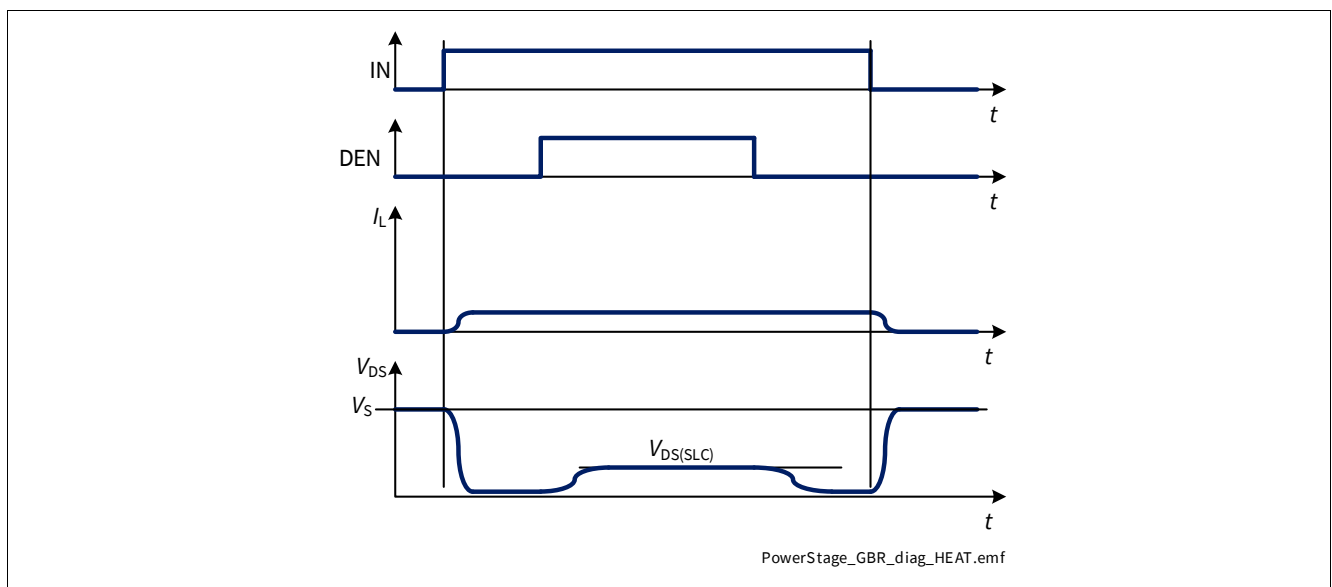
During demagnetization of inductive loads, energy has to be dissipated in BTS7002-1EPP. The energy can be calculated with **Equation (7.1)**:

$$E = V_{DS(CLAMP)} \cdot \left[ \frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (7.1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Please refer to **Chapter 4.2** for the maximum allowed values of  $E_{AS}$  (single pulse energy) and  $E_{AR}$  (repetitive energy).

### 7.2.3 Output Voltage Limitation

To increase the current sense accuracy,  $V_{DS}$  voltage is monitored. When the output current  $I_L$  decreases while the channel is diagnosed (DEN pin set to “high” - see **Figure 17**) bringing  $V_{DS}$  equal or lower than  $V_{DS(SLC)}$ , the output DMOS gate is partially discharged. This increases the output resistance so that  $V_{DS} = V_{DS(SLC)}$  even for very small output currents. The  $V_{DS}$  increase allows the current sensing circuitry to work more efficiently, providing better  $k_{ILIS}$  accuracy for output current in the low range.



**Figure 17** Output Voltage Limitation activation during diagnosis

## 7.3 Advanced Switching Characteristics

### 7.3.1 Inverse Current behavior

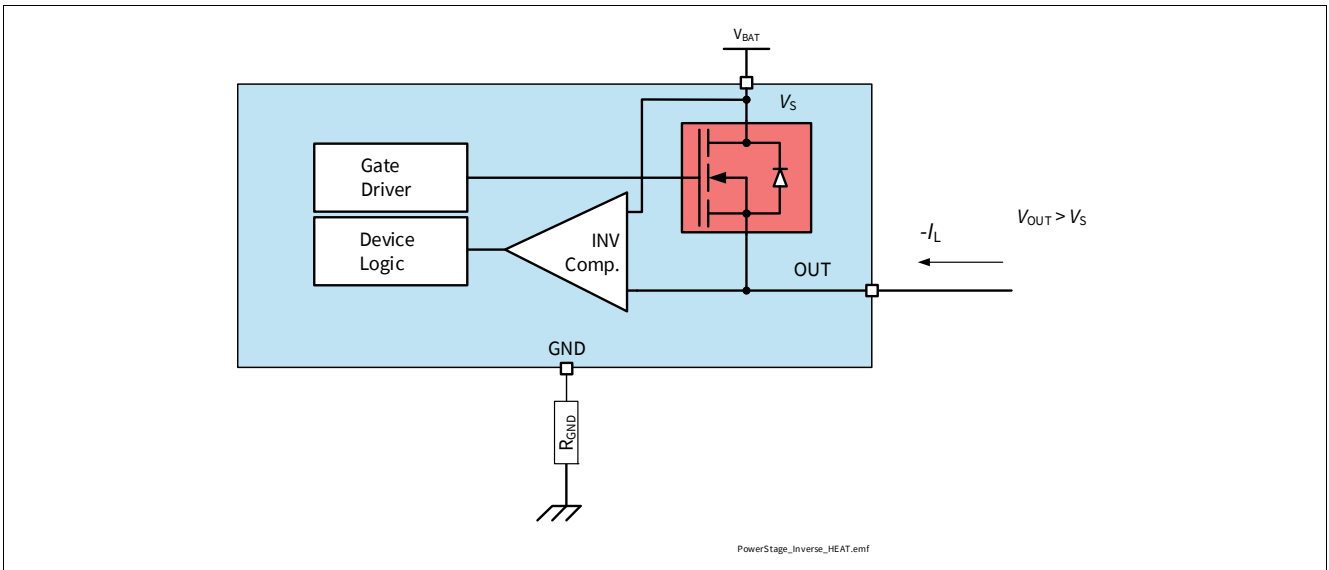
When  $V_{OUT} > V_S$ , a current  $I_{INV}$  flows into the power output transistor (see **Figure 18**). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. If the channel is in ON state,  $R_{DS(INV)}$  can be expected and power dissipation in the output stage is comparable to normal operation in  $R_{DS(ON)}$ .

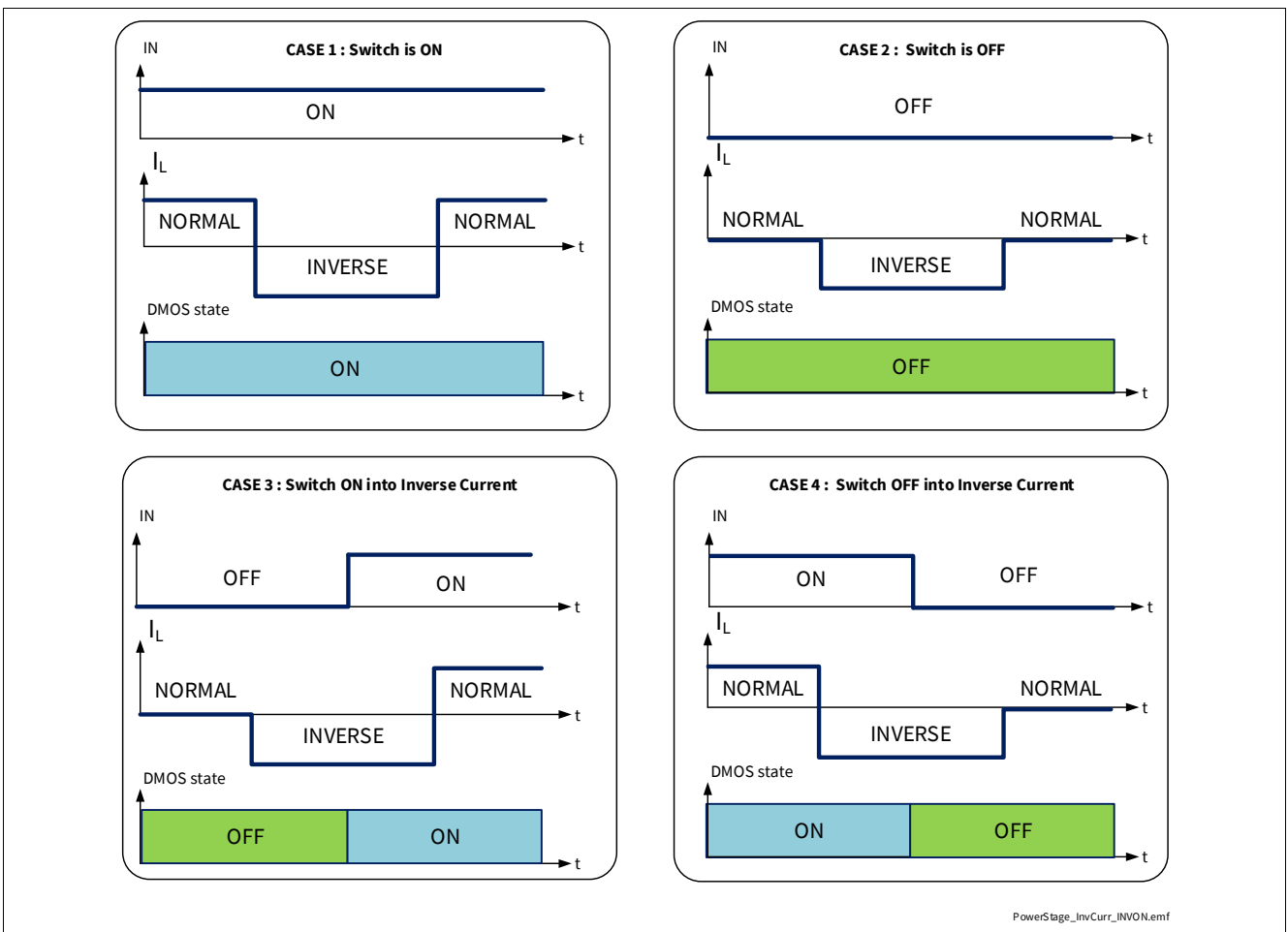
During Inverse Current condition, the channel remains in ON or OFF state as long as  $|I_L| < |I_{L(INV)}|$ .

With InverseON, it is possible to switch ON the channel during Inverse Current condition as long as  $|I_L| < |I_{L(INV)}|$  (see **Figure 19**).

**Power Stages**



**Figure 18 Inverse Current Circuitry**



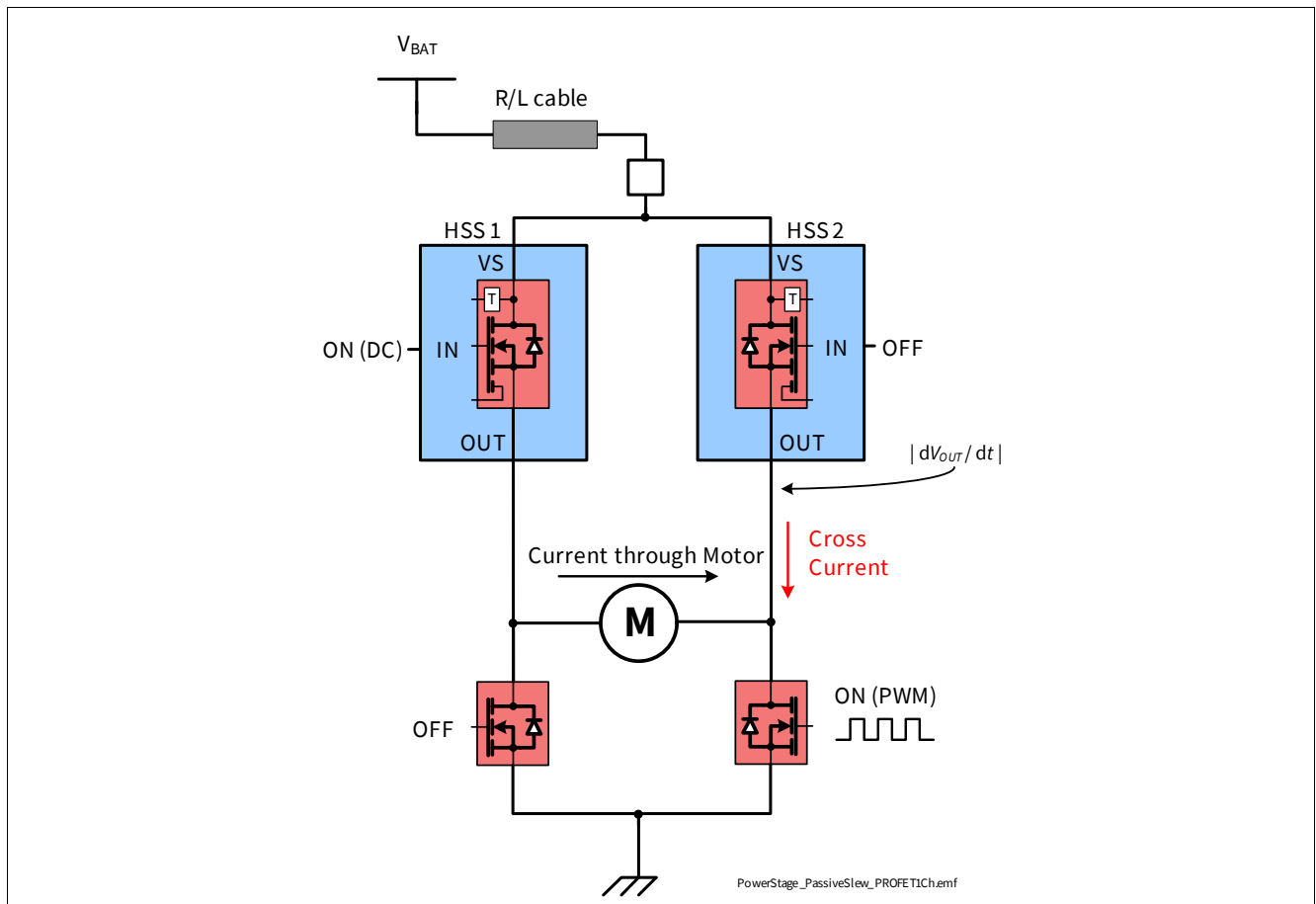
**Figure 19 InverseON - Channel behavior in case of applied Inverse Current**

*Note: No protection mechanism like Overtemperature or Overload protection is active during applied Inverse Currents.*

**Power Stages**

**7.3.2 Cross Current robustness with H-Bridge configuration**

When BTS7002-1EPP is used as high-side switch e.g. in a bridge configuration (therefore paired with a low-side switch as shown in **Figure 20**), the maximum slew rate applied to the output by the low-side switch must be lower than  $|dV_{OUT} / dt|$ . Otherwise the output stage may turn ON in linear mode (not in  $R_{DS(ON)}$ ) while the low-side switch is commutating. This creates an unprotected overheating for the DMOS due to the cross-conduction current.



**Figure 20 High-Side switch used in Bridge configuration**



**Power Stages**

**7.4 Electrical Characteristics Power Stages**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**Table 11 Electrical Characteristics: Power Stages - General**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Drain to Source Clamping Voltage at $T_J = -40\text{ °C}$	$V_{DS(CLAMP)_{-40}}$	33	36.5	42	V	$I_L = 5\text{ mA}$ $T_J = -40\text{ °C}$ See <a href="#">Figure 16</a>	P_7.4.0.1
Drain to Source Clamping Voltage at $T_J \geq 25\text{ °C}$	$V_{DS(CLAMP)_{25}}$	35	38	44	V	<sup>1)</sup> $I_L = 5\text{ mA}$ $T_J \geq 25\text{ °C}$ See <a href="#">Figure 16</a>	P_7.4.0.2

1) Tested at  $T_J = 150\text{ °C}$ .

**7.4.1 Electrical Characteristics Power Stages**

**Table 12 Electrical Characteristics: Power Stages**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Timings</b>							
Switch-ON Delay	$t_{ON(Delay)}$	10	70	130	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 10\% V_S$	P_7.4.5.1
Switch-OFF Delay	$t_{OFF(Delay)}$	10	50	160	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 90\% V_S$	P_7.4.5.2
Switch-ON Time	$t_{ON}$	50	130	210	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 90\% V_S$	P_7.4.5.3
Switch-OFF Time	$t_{OFF}$	30	100	220	$\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 10\% V_S$	P_7.4.5.4
Switch-ON/OFF Matching $t_{ON} - t_{OFF}$	$\Delta t_{SW}$	-60	25	90	$\mu\text{s}$	$V_S = 13.5\text{ V}$	P_7.4.5.5
<b>Voltage Slope</b>							
Switch-ON Slew Rate	$(dV/dt)_{ON}$	0.16	0.27	0.39	V/ $\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 30\% \text{ to } 70\%$ of $V_S$	P_7.4.5.6
Switch-OFF Slew Rate	$-(dV/dt)_{OFF}$	0.16	0.27	0.39	V/ $\mu\text{s}$	$V_S = 13.5\text{ V}$ $V_{OUT} = 70\% \text{ to } 30\%$ of $V_S$	P_7.4.5.7

**Power Stages**

**Table 12 Electrical Characteristics: Power Stages** (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Slew Rate Matching (dV/dt) <sub>ON</sub> - (dV/dt) <sub>OFF</sub>	$\Delta(dV/dt)_{SW}$	-0.15	0	+0.15	V/ $\mu$ s	$V_S = 13.5$ V	P_7.4.5.8
<b>Voltages</b>							
Output Voltage Drop Limitation at Small Load Currents	$V_{DS(SLC)}$	2	10	20	mV	<sup>1)</sup> $I_{OUT} = I_{OUT(OL)} = 20$ mA	P_7.4.5.9

1) Not subject to production test - specified by design

**7.5 Electrical Characteristics - Power Output Stages**

$V_S = 6$  V to 18 V,  $T_J = -40$  °C to +150 °C

Typical values:  $V_S = 13.5$  V,  $T_J = 25$  °C

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1$   $\Omega$

**7.5.1 Power Output Stage - 2 m $\Omega$**

**Table 13 Electrical Characteristics: Power Stages - 2 m $\Omega$**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output characteristics</b>							
ON-State Resistance at $T_J = 25$ °C	$R_{DS(ON)_25}$	-	2.6	-	m $\Omega$	<sup>1)</sup> $T_J = 25$ °C	P_7.5.10.1
ON-State Resistance at $T_J = 150$ °C	$R_{DS(ON)_150}$	-	-	4.8	m $\Omega$	$T_J = 150$ °C	P_7.5.10.2
ON-State Resistance in Cranking	$R_{DS(ON)_CRAN}$ K	-	-	6	m $\Omega$	$T_J = 150$ °C $V_S = 3.1$ V	P_7.5.10.3
ON-State Resistance in Inverse Current at $T_J = 25$ °C	$R_{DS(INV)_25}$	-	2.7	-	m $\Omega$	<sup>1)</sup> $T_J = 25$ °C $V_S = 13.5$ V $I_L = -4$ A DEN = "low" see <a href="#">Figure 18</a>	P_7.5.10.4
ON-State Resistance in Inverse Current at $T_J = 150$ °C	$R_{DS(INV)_150}$	-	-	6	m $\Omega$	$T_J = 150$ °C $V_S = 13.5$ V $I_L = -4$ A DEN = "low" see <a href="#">Figure 18</a>	P_7.5.10.5

**Power Stages**

**Table 13 Electrical Characteristics: Power Stages - 2 mΩ (continued)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-State Resistance in Reverse Polarity at $T_J = 25\text{ °C}$	$R_{DS(REV)_25}$	–	5.7	–	mΩ	1) $T_J = 25\text{ °C}$ $V_S = -13.5\text{ V}$ $I_L = -4\text{ A}$ see <a href="#">Figure 29</a>	P_7.5.10.6
ON-State Resistance in Reverse Polarity at $T_J = 150\text{ °C}$	$R_{DS(REV)_150}$	–	–	9.6	mΩ	$T_J = 150\text{ °C}$ $V_S = -13.5\text{ V}$ $I_L = -4\text{ A}$	P_7.5.10.7
Nominal Load Current	$I_{L(NOM)}$	–	21	–	A	1) $T_A = 85\text{ °C}$ $T_J \leq 150\text{ °C}$	P_7.5.10.8
Output Leakage Current at $T_J \leq 85\text{ °C}$	$I_{L(OFF)_85}$	–	0.1	0.9	μA	1) $V_{OUT} = 0\text{ V}$ $V_{IN} = \text{“low”}$ $T_A \leq 85\text{ °C}$	P_7.5.10.9
Output Leakage Current at $T_J = 150\text{ °C}$	$I_{L(OFF)_150}$	–	–	27	μA	$V_{OUT} = 0\text{ V}$ $V_{IN} = \text{“low”}$ $T_A = 150\text{ °C}$	P_7.5.10.10
Inverse Current Capability	$I_{L(INV)}$	–	-21	–	A	1) $V_S < V_{OUT}$ IN = “high” see <a href="#">Figure 18</a>	P_7.5.10.11

**Voltage Slope**

Passive Slew Rate (e.g. for Half Bridge Configuration)	$ dV_{OUT} / dt $	–	–	10	V/μs	1) $V_S = 13.5\text{ V}$ see <a href="#">Figure 20</a>	P_7.5.10.12
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**Voltages**

Drain Source Diode Voltage	$ V_{DS(DIODE)} $	–	550	700	mV	$I_L = -190\text{ mA}$ $T_J = 150\text{ °C}$	P_7.5.10.13
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**Switching Energy**

Switch-ON Energy	$E_{ON}$	–	1.5	–	mJ	1) $V_S = 18\text{ V}$ see <a href="#">Figure 15</a>	P_7.5.10.14
Switch-OFF Energy	$E_{OFF}$	–	1.65	–	mJ	1) $V_S = 18\text{ V}$ see <a href="#">Figure 15</a>	P_7.5.10.15

1) Not subject to production test - specified by design.

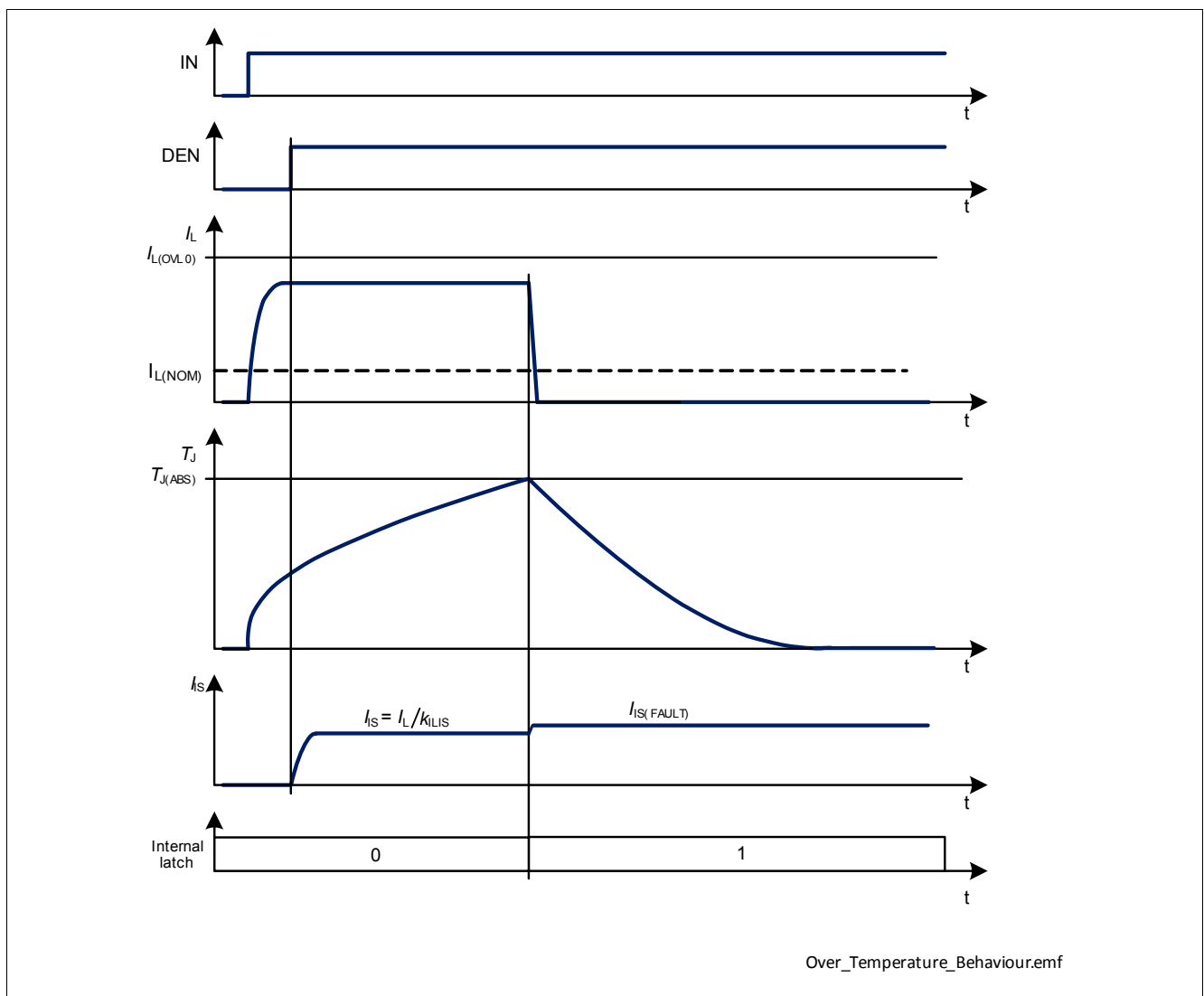
**Protection**

**8 Protection**

The BTS7002-1EPP is protected against Overtemperature, Overload, Reverse Battery (with ReverseON) and Overvoltage. Overtemperature and Overload protections are working when the device is in ON or ON\_Diag mode but not during InverseON and ReverseON function. Overvoltage protection works in all operation modes. Reverse Battery protection works when the GND and VS pins are reverse supplied.

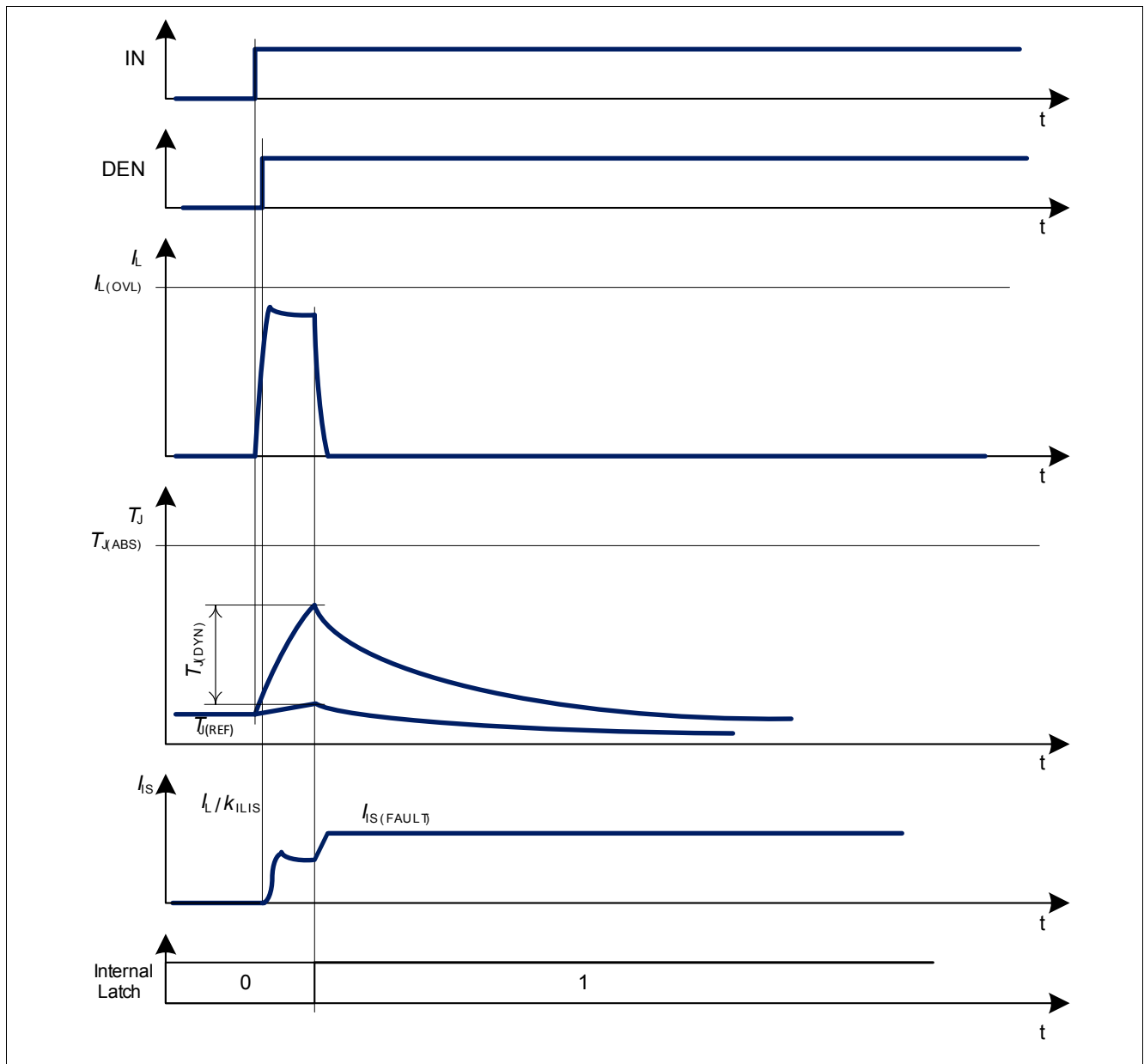
**8.1 Overtemperature Protection**

The device incorporates both an absolute ( $T_{J(ABS)}$ ) and a dynamic ( $T_{J(DYN)}$ ) temperature protection circuitry for the channel. An increase of junction temperature  $T_J$  above either one of the two thresholds ( $T_{J(ABS)}$  or  $T_{J(DYN)}$ ) switches OFF the overheated channel to prevent destruction. The channel remains switched OFF until junction temperature has reached the “Reactivation” condition described in **Table 14**. The behavior is shown in **Figure 21** (absolute Overtemperature Protection) and **Figure 22** (dynamic Overtemperature Protection).  $T_{J(REF)}$  is the reference temperature used for dynamic temperature protection.



**Figure 21 Overtemperature Protection (Absolute)**

**Protection**



**Figure 22 Overtemperature Protection (Dynamic)**

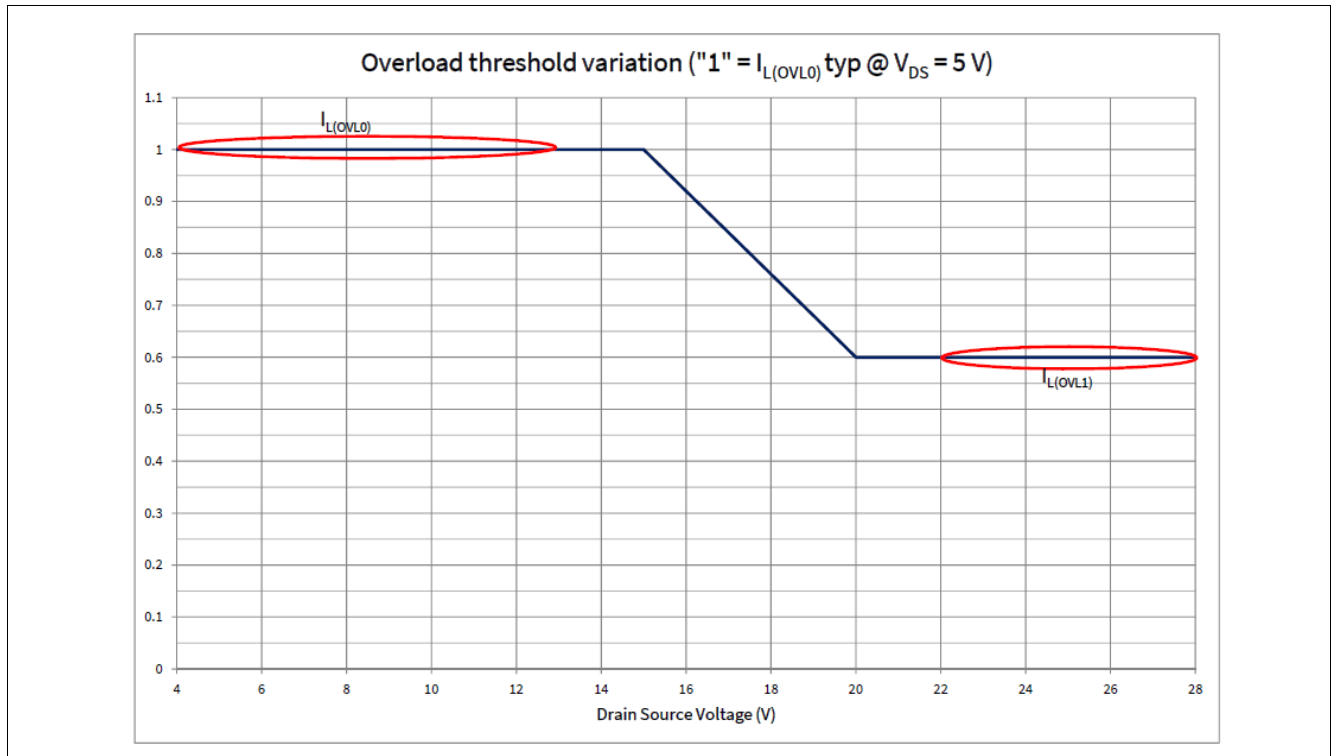
When the Overtemperature protection circuitry allows the channel to be switched ON again, the Intelligent Latch strategy described in [Chapter 8.3](#) is followed.

**8.2 Overload Protection**

The BTS7002-1EPP is protected in case of Overload or short circuit to ground. Two Overload thresholds are defined (see [Figure 23](#)) and selected automatically depending on the voltage  $V_{DS}$  across the power DMOS:

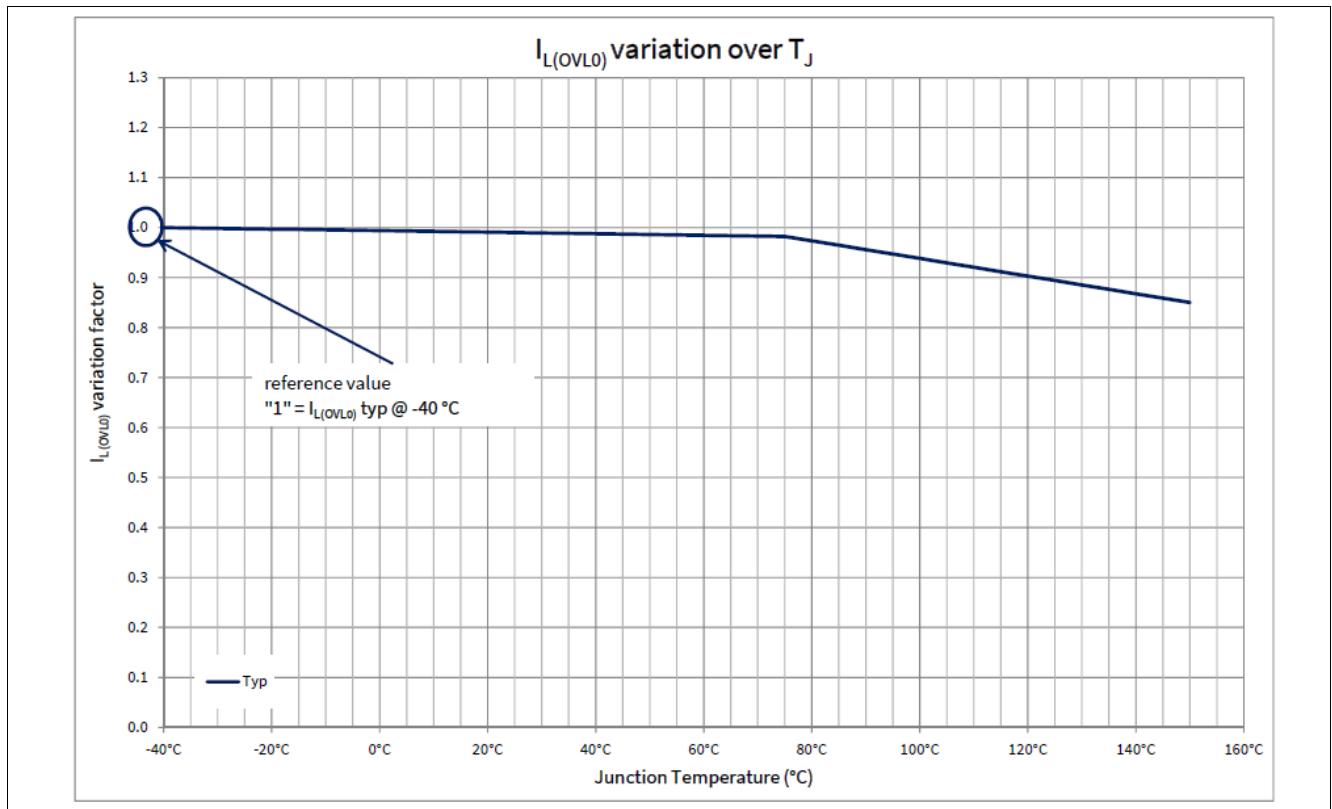
- $I_{L(OVL0)}$  when  $V_{DS} < 13\text{ V}$
- $I_{L(OVL1)}$  when  $V_{DS} > 22\text{ V}$

Protection



**Figure 23 Overload Current Thresholds**

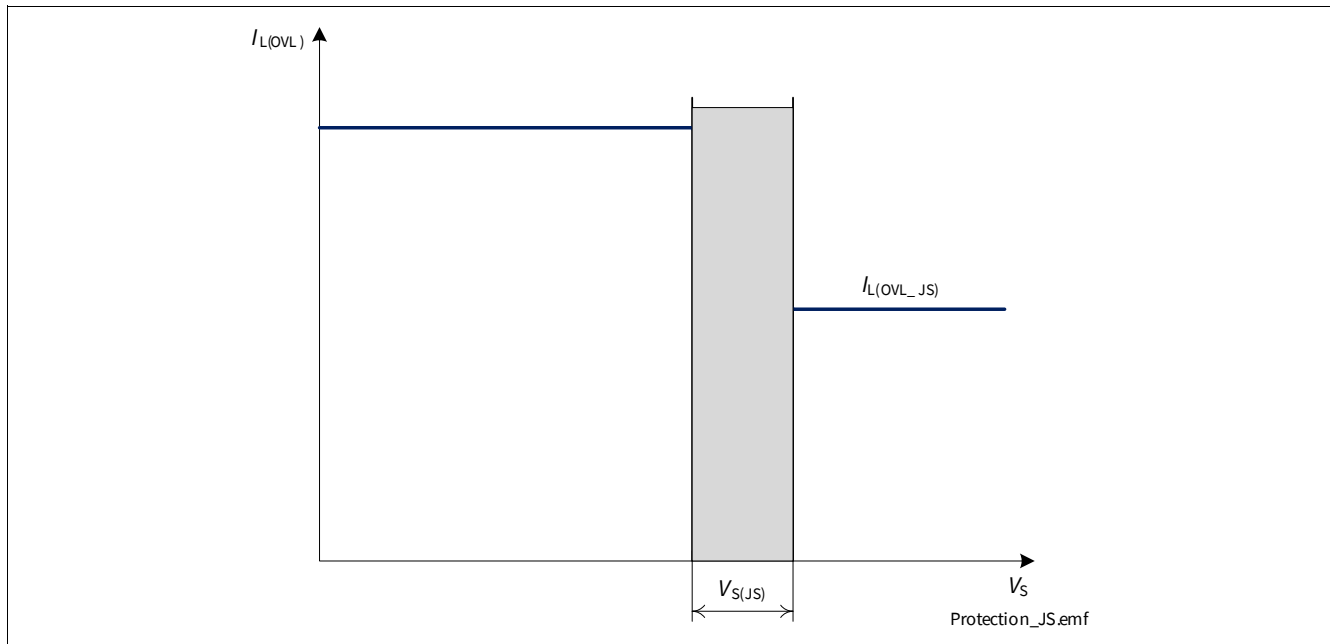
In order to allow a higher load inrush at low ambient temperature, Overload threshold is maximum at low temperature and decreases when  $T_J$  increases (see [Figure 24](#)).  $I_{L(OVL0)}$  typical value remains constant up to a junction temperature of +75 °C.



**Figure 24 Overload Current Thresholds variation with  $T_J$**

**Protection**

Power supply voltage  $V_S$  can increase above 18 V for short time, for instance in Load Dump or in Jump Start condition. Whenever  $V_S \geq V_{S(JS)}$ , the overload detection current is set to  $I_{L(OVL\_JS)}$  as shown in **Figure 25**.



**Figure 25** Overload Detection Current variation with  $V_S$  voltage

When  $I_L \geq I_{L(OVL)}$  (either  $I_{L(OVL0)}$  or  $I_{L(OVL1)}$ ) the channel is switched OFF. The channel is allowed to be reactivated according to the intelligent latch strategy described in **Chapter 8.3**.

**8.3 Protection and Diagnosis in case of Fault**

Any event that triggers a protection mechanism (either Overtemperature or Overload) has 2 consequences:

- The channel switches OFF and the internal latch is set to “1”
- If the diagnosis is active for the channel, a current  $I_{IS(FAULT)}$  is provided by IS pin (see **Chapter 9.2.2** for further details)

The channel can be switched ON again if all the protection mechanisms fulfill the “reactivation” conditions described in **Table 14**. Furthermore, the device has the intelligent latch to protect itself against unwanted repetitive reactivation in fault condition.

**Table 14** Protection “Reactivation” Condition

Fault condition	Switch OFF event	“Reactivation” condition
Overtemperature	$T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$	$T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis)
Overload	$I_L \geq I_{L(OVL)}$	Device is OFF

**8.3.1 Intelligent Latch Strategy**

At normal condition, when IN is set to “high”, the channel is switched ON. In case of fault condition the output stage latches OFF. There are two ways to de-latch the switch.

With IN pin:

It is necessary to set the input pin to “low” for a time longer than  $t_{DELAY(LR)}$  (“latch reset delay” time) to de-latch the channel. The channel can be allowed to restart only if the “latch” conditions for the protection mechanisms are fulfilled (see **Table 14**).

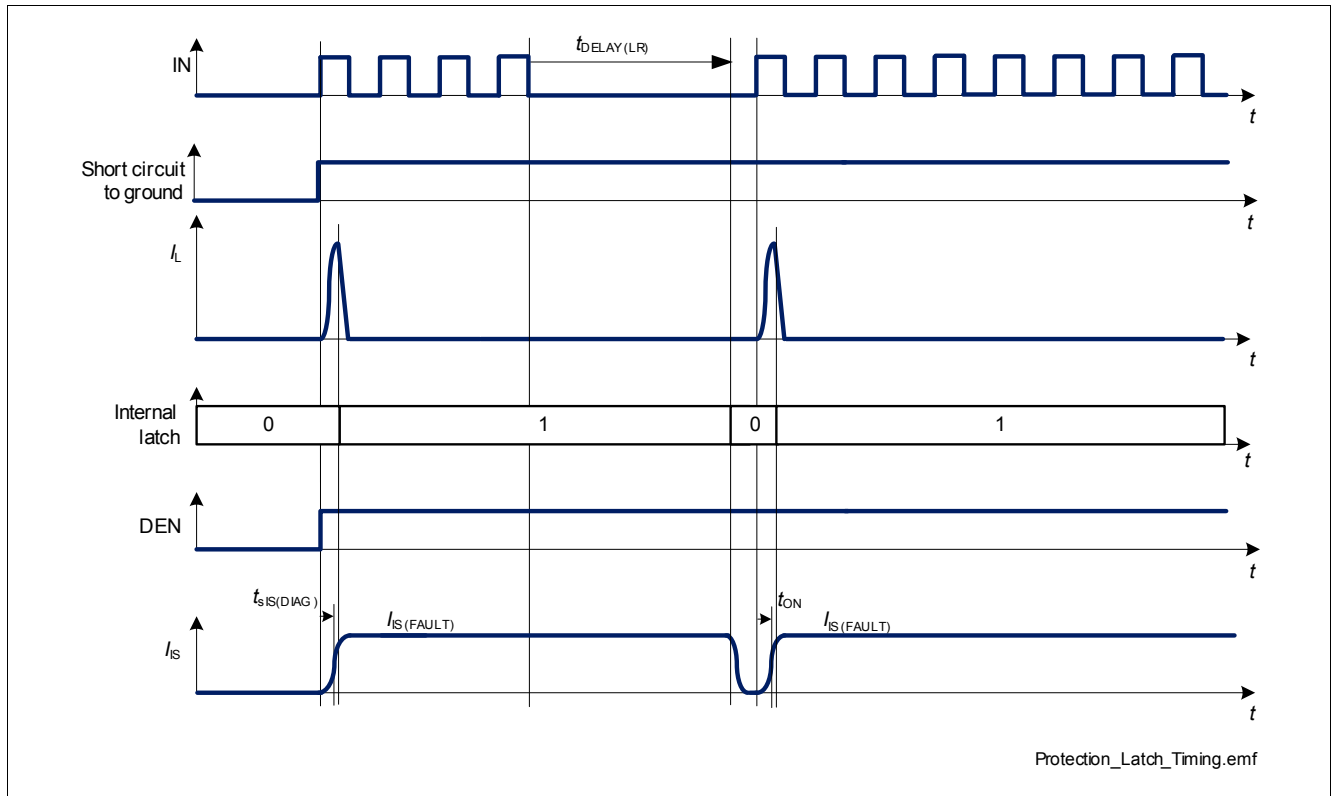
**Protection**

During the “latch reset delay” time, if the input is set to “high” the channel remains switched OFF and the timer  $t_{\text{DELAY(LR)}}$  is reset. The timer  $t_{\text{DELAY(LR)}}$  restarts as soon as the input pin is set to “low” again. The intelligent latch strategy is shown in **Figure 28** (flowchart) and **Figure 26** (timing diagram).

With DEN pin:

It is possible to “force” a reset of the internal latch without waiting for  $t_{\text{DELAY(LR)}}$  by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than  $t_{\text{DEN(LR)}}$  to ensure a reset of the internal latch.

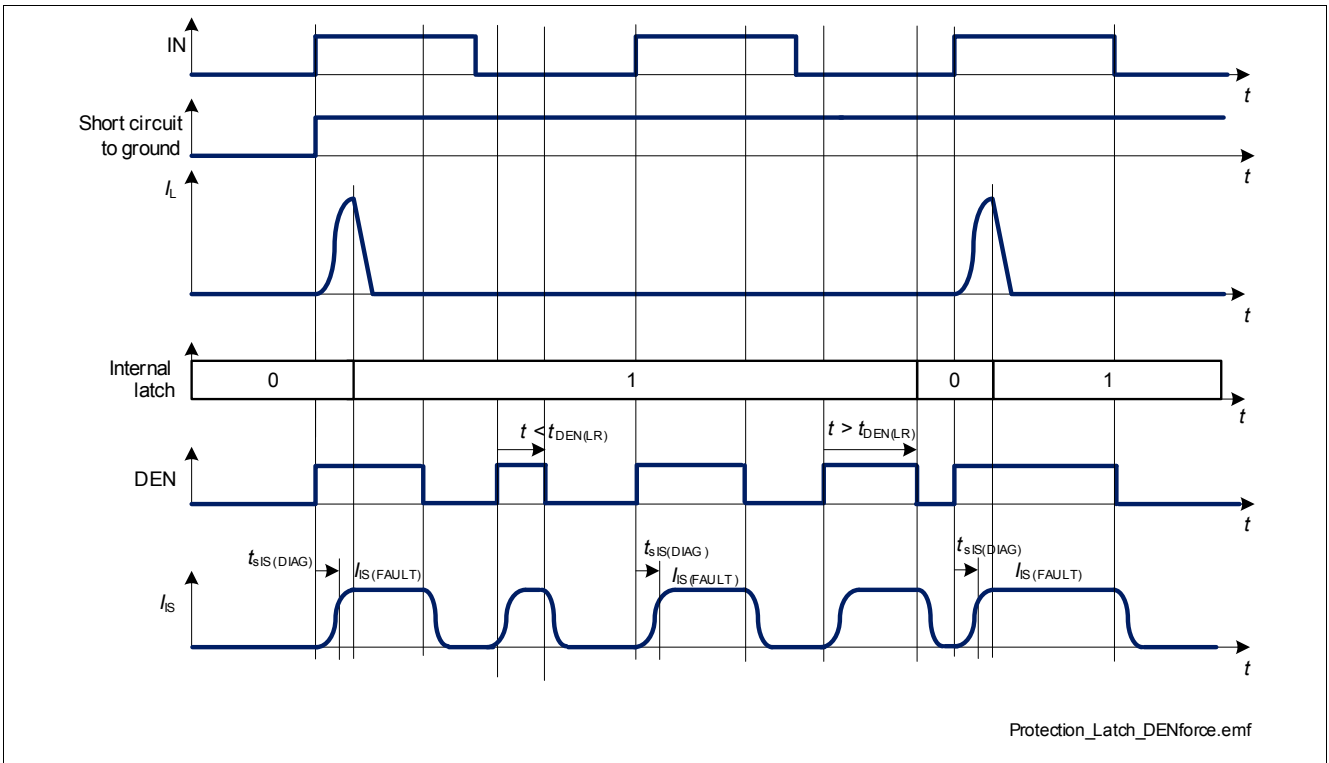
The timing is shown in **Figure 27**.



**Figure 26 Intelligent Latch Timing Diagram**



**Protection**



**Figure 27 Intelligent Latch Timing Diagram with Forced Reset**

Protection

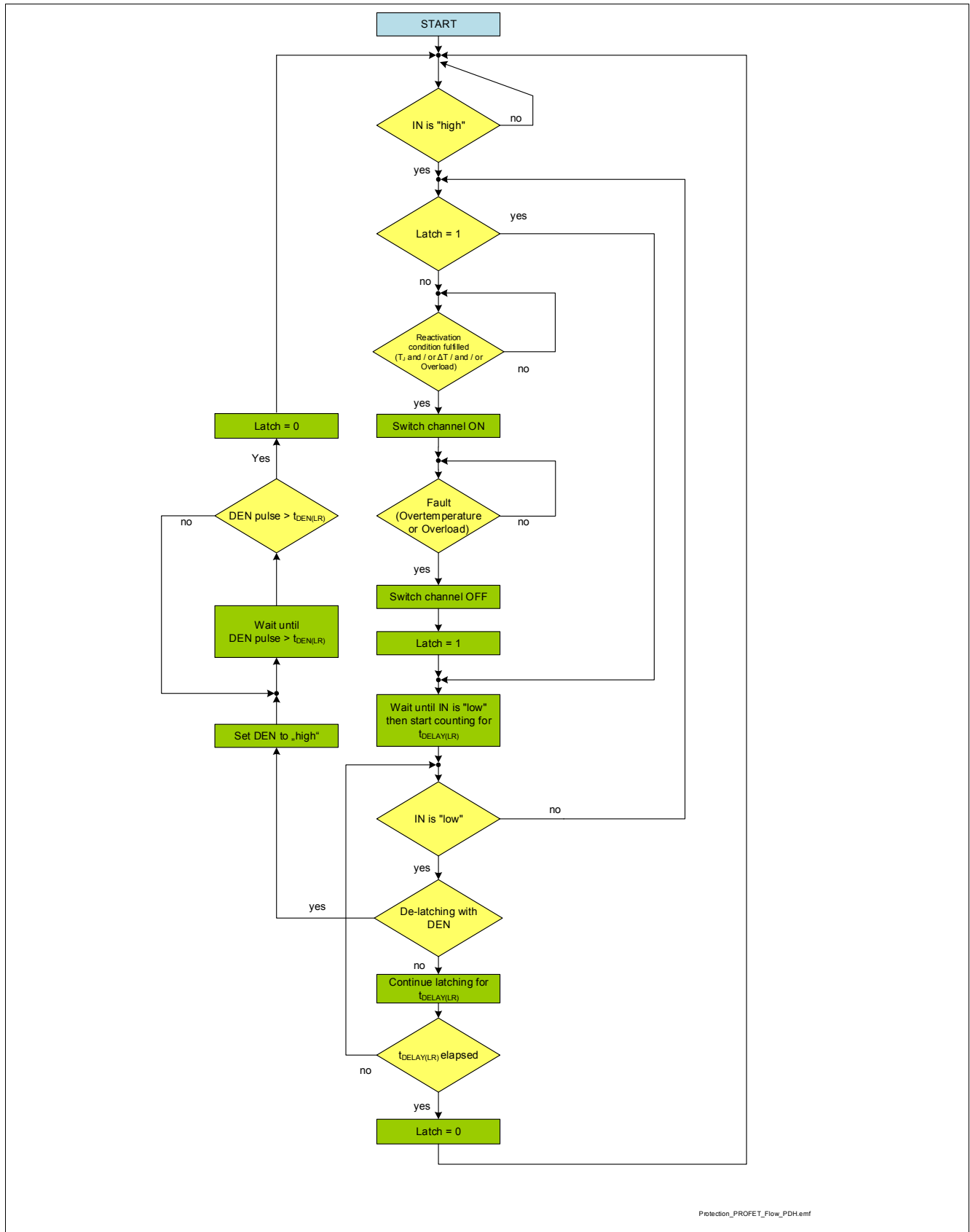


Figure 28 Intelligent Latch Flowchart

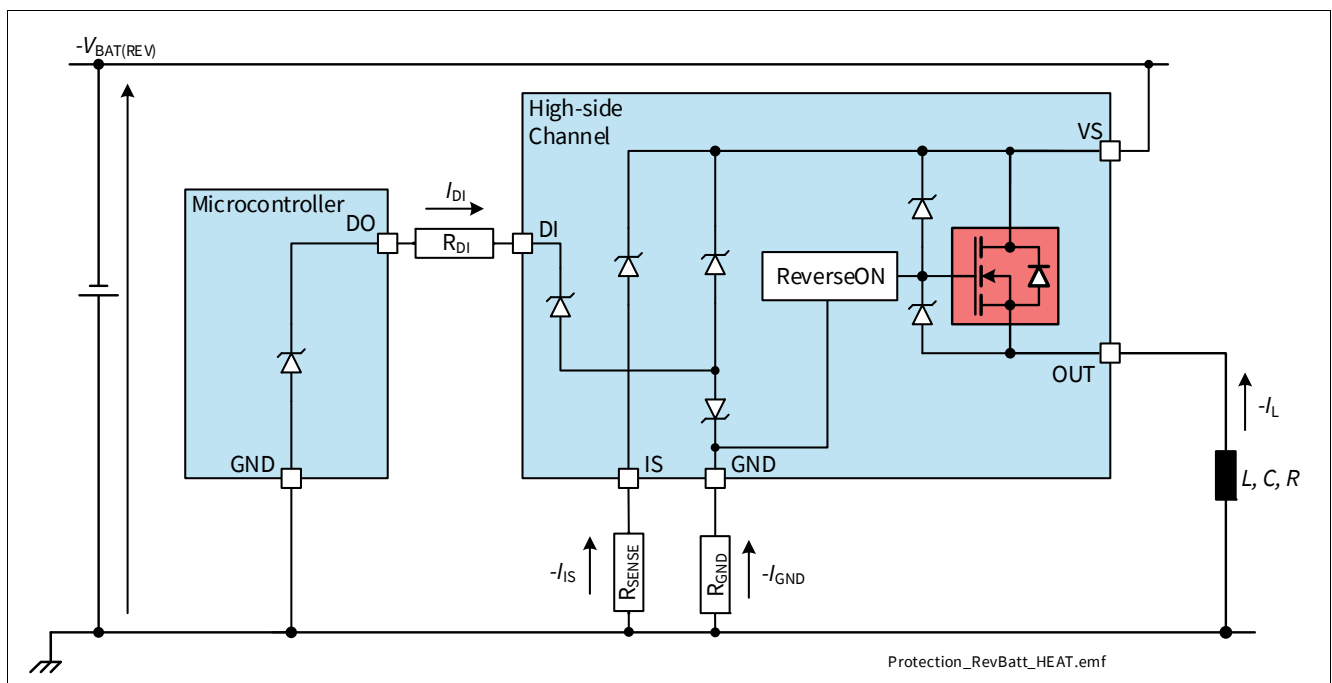
Protection

8.4 Additional protections

8.4.1 Reverse Polarity Protection

In Reverse Polarity condition (also known as Reverse Battery), the output stage is switched ON (see parameter  $R_{DS(REV)}$ ) because of ReverseON feature which limits the power dissipation in the output stage. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stage must be limited by the connected load. The current through digital input pins has to be limited as well by an external resistor (please refer to the Absolute Maximum Ratings listed in [Chapter 4.1](#) and to Application Information in [Chapter 10](#)).

**Figure 29** shows a typical application including a device with ReverseON. A current flowing into GND pin ( $-I_{GND}$ ) during Reverse Polarity condition is necessary to activate ReverseON, therefore a resistive path between module ground and device GND pin must be present.



**Figure 29 Reverse Battery Protection (application example)**

8.4.2 Overvoltage Protection

In the case of supply voltages between  $V_{S(EXT,UP)}$  and  $V_{BAT(LD)}$ , the output transistor is still operational and follows the input pin. In addition to the output clamp for inductive loads as described in [Chapter 7.2.2](#), there is a clamp mechanism available for Overvoltage protection for the logic circuit and the output channel, monitoring the voltage between VS and GND pins ( $V_{S(CLAMP)}$ ).

## 8.5 Protection against loss of connection

### 8.5.1 Loss of Battery and Loss of Load

The loss of connection to battery or to the load has no influence on device robustness when load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled. PROFET™+2 12V devices can handle the inductivity of the wire harness up to 10  $\mu\text{H}$  with  $I_{L(\text{NOM})}$ . In case of applications where currents and/or the aforementioned inductivity are exceeded, an external suppressor diode (like diode  $D_{Z2}$  shown in [Chapter 10](#)) is recommended to handle the energy and to provide a well-defined path to the load current.

### 8.5.2 Loss of Ground

In case of loss of device ground, it is recommended to have a resistor connected between any Digital Input pin and the microcontroller to ensure a channel switch OFF (as described in [Chapter 10](#)).

*Note: In case any Digital Input pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.*

**Protection**

**8.6 Electrical Characteristics Protection**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**Table 15 Electrical Characteristics: Protection - General**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Shutdown Temperature (Absolute)	$T_{J(ABS)}$	150	175	200	°C	1)2) See <a href="#">Figure 21</a>	P_8.6.0.1
Thermal Shutdown Hysteresis (Absolute)	$T_{HYS(ABS)}$	–	30	–	K	3) See <a href="#">Figure 21</a>	P_8.6.0.2
Thermal Shutdown Temperature (Dynamic)	$T_{J(DYN)}$	–	80	–	K	3) See <a href="#">Figure 22</a>	P_8.6.0.3
Power Supply Clamping Voltage at $T_J = -40\text{ °C}$	$V_{S(CLAMP)_{-40}}$	33	36.5	42	V	$I_{VS} = 5\text{ mA}$ $T_J = -40\text{ °C}$ See <a href="#">Figure 16</a>	P_8.6.0.6
Power Supply Clamping Voltage at $T_J \geq 25\text{ °C}$	$V_{S(CLAMP)_{25}}$	35	38	44	V	2) $I_{VS} = 5\text{ mA}$ $T_J \geq 25\text{ °C}$ See <a href="#">Figure 16</a>	P_8.6.0.7
Power Supply Voltage Threshold for Overcurrent Threshold Reduction in case of Short Circuit	$V_{S(JS)}$	20.5	22.5	24.5	V	3) Setup acc. to AEC-Q100-012	P_8.6.0.8

1) Functional test only.

2) Tested at  $T_J = 150\text{ °C}$  only.

3) Not subject to production test - specified by design.

**8.6.1 Electrical Characteristics Protection**

**Table 16 Electrical Characteristics: Protection**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Latch Reset Delay Time after Fault Condition	$t_{DELAY(LR)}$	40	70	100	ms	1)	P_8.6.4.1
Minimum DEN Pulse Duration for Latch Reset	$t_{DEN(LR)}$	50	100	150	µs	2)	P_8.6.4.2

1) Functional test only.

2) Not subject to production test - specified by design.

**Protection**

**8.7 Electrical Characteristics Protection - Power Output Stages**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**8.7.1 Protection Power Output Stage - 2 mΩ**

**Table 17 Electrical Characteristics: Protection - 2 mΩ**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overload Detection Current at $T_J = -40\text{ °C}$	$I_{L(OVL0)\_-40}$	120	135	158	A	1) $T_J = -40\text{ °C}$ $dI/dt = 0.4\text{ A}/\mu\text{s}$ see <a href="#">Figure 23</a> and <a href="#">Figure 24</a>	P_8.7.10.1
Overload Detection Current at $T_J = 25\text{ °C}$	$I_{L(OVL0)\_25}$	116	133	150	A	2) $T_J = 25\text{ °C}$ $dI/dt = 0.4\text{ A}/\mu\text{s}$ see <a href="#">Figure 23</a> and <a href="#">Figure 24</a>	P_8.7.10.7
Overload Detection Current at $T_J = 150\text{ °C}$	$I_{L(OVL0)\_150}$	100	115	130	A	2) $T_J = 150\text{ °C}$ $dI/dt = 0.4\text{ A}/\mu\text{s}$ see <a href="#">Figure 23</a> and <a href="#">Figure 24</a>	P_8.7.10.8
Overload Detection Current at High $V_{DS}$	$I_{L(OVL1)}$	–	81	–	A	2) $dI/dt = 0.4\text{ A}/\mu\text{s}$ see <a href="#">Figure 23</a>	P_8.7.10.5
Overload Detection Current Jump Start Condition	$I_{L(OVL\_JS)}$	–	81	–	A	2) $V_S > V_{S(JS)}$ $dI/dt = 0.4\text{ A}/\mu\text{s}$ see <a href="#">Figure 25</a>	P_8.7.10.6

1) Functional test only.

2) Not subject to production test - specified by design.

**Diagnosis**

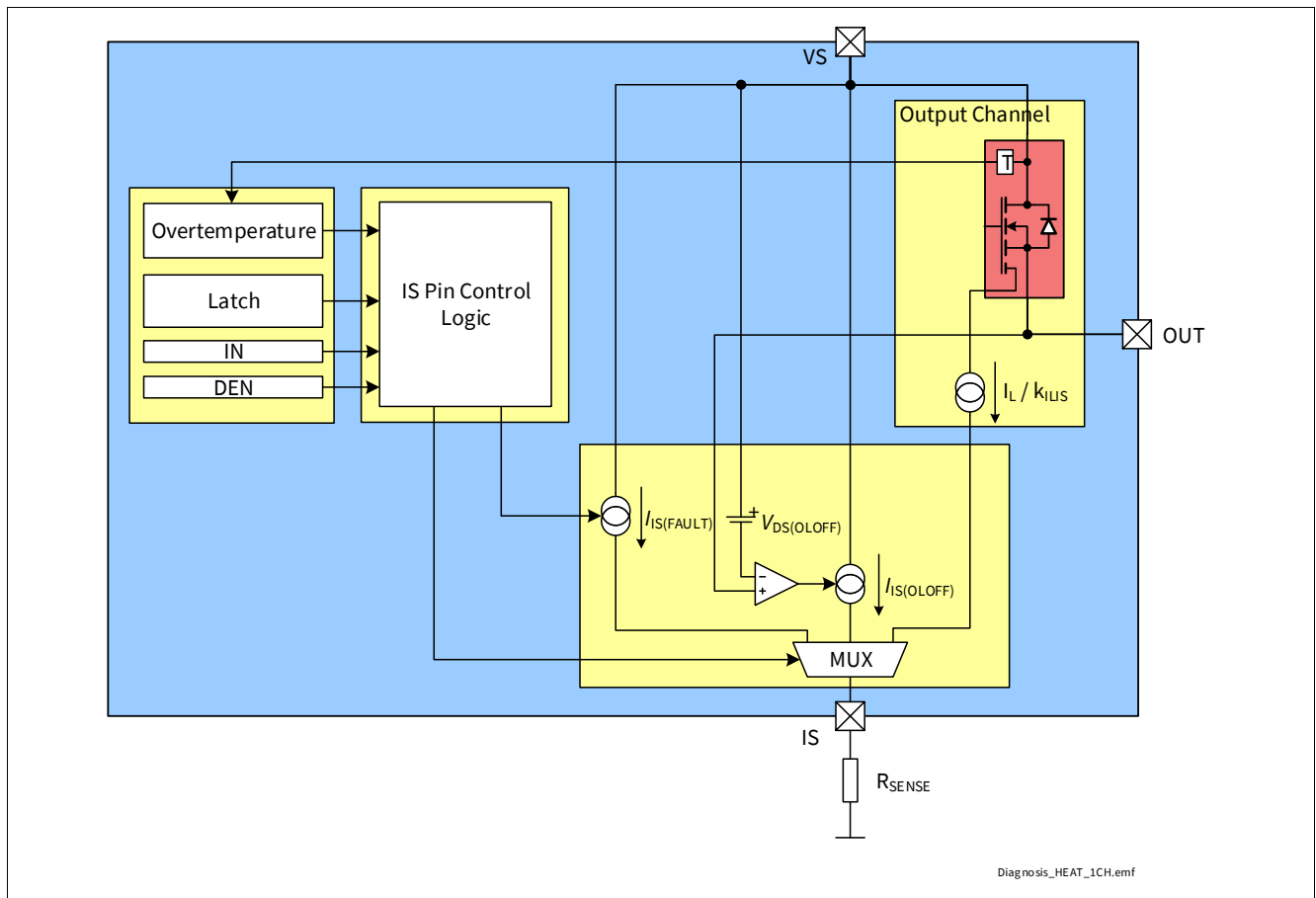
**9 Diagnosis**

For diagnosis purpose, the BTS7002-1EPP provides a sense current signal ( $I_{IS}$ ) at pin IS. In case of disabled diagnostic (DEN pin set to “low”), IS pin becomes high impedance.

A sense resistor  $R_{SENSE}$  must be connected between IS pin and module ground if the current sense diagnosis is used.  $R_{SENSE}$  value has to be higher than 820  $\Omega$  (or 400  $\Omega$  when a central Reverse Battery protection is present on the battery feed) to limit the power losses in the sense circuitry. A typical value is  $R_{SENSE} = 1.2 \text{ k}\Omega$ .

Due to the internal connection between IS pin and  $V_S$  supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

See **Figure 30** for details as an overview.



**Figure 30 Diagnosis Block Diagram**

**Diagnosis**

**9.1 Overview**

**Table 18** gives a quick reference to the state of the IS pin during BTS7002-1EPP operation.

**Table 18 SENSE Signal, Function of Application Condition**

Application Condition	Input level	DEN level	V <sub>OUT</sub>	Diagnostic Output
Normal operation	"low"	"high"	~ GND	Z <i>I</i> <sub>IS(FAULT)</sub> if latch ≠ 0
Short circuit to GND			~ GND	Z <i>I</i> <sub>IS(FAULT)</sub> if latch ≠ 0
Overtemperature			Z	<i>I</i> <sub>IS(FAULT)</sub>
Short circuit to V <sub>S</sub>			V <sub>S</sub>	<i>I</i> <sub>IS(OLOFF)</sub> ( <i>I</i> <sub>IS(FAULT)</sub> if latch ≠ 0)
Open Load			< V <sub>S</sub> - V <sub>DS(OLOFF)</sub> > V <sub>S</sub> - V <sub>DS(OLOFF)</sub> <sup>1)</sup>	Z <i>I</i> <sub>IS(OLOFF)</sub> (in both cases <i>I</i> <sub>IS(FAULT)</sub> if latch ≠ 0)
Inverse current	"high"	"high"	V <sub>OUT</sub> > V <sub>S</sub>	<i>I</i> <sub>IS(OLOFF)</sub> ( <i>I</i> <sub>IS(FAULT)</sub> if latch ≠ 0)
Normal operation			~ V <sub>S</sub>	<i>I</i> <sub>IS</sub> = <i>I</i> <sub>L</sub> / <i>k</i> <sub>ILIS</sub>
Overload			< V <sub>S</sub>	<i>I</i> <sub>IS(FAULT)</sub>
Short circuit to GND			~ GND	<i>I</i> <sub>IS(FAULT)</sub>
Overtemperature			Z	<i>I</i> <sub>IS(FAULT)</sub>
Short circuit to V <sub>S</sub>			V <sub>S</sub>	<i>I</i> <sub>IS</sub> < <i>I</i> <sub>L</sub> / <i>k</i> <sub>ILIS</sub>
Open Load			~ V <sub>S</sub> <sup>2)</sup>	<i>I</i> <sub>IS</sub> = <i>I</i> <sub>IS(EN)</sub>
Under load (e.g. Output Voltage Limitation condition)			~ V <sub>S</sub> <sup>3)</sup>	<i>I</i> <sub>IS(EN)</sub> < <i>I</i> <sub>IS</sub> < <i>I</i> <sub>L(NOM)</sub> / <i>k</i> <sub>ILIS</sub>
Inverse current			V <sub>OUT</sub> > V <sub>S</sub>	<i>I</i> <sub>IS</sub> = <i>I</i> <sub>IS(EN)</sub>
All conditions			n.a.	"low"

- 1) With additional pull-up resistor.
- 2) The output current has to be smaller than *I*<sub>L(OI)</sub>.
- 3) The output current has to be higher than *I*<sub>L(OI)</sub>.

**9.2 Diagnosis in ON state**

A current proportional to the load current (ratio *k*<sub>ILIS</sub> = *I*<sub>L</sub> / *I*<sub>IS</sub>) is provided at pin IS when the following conditions are fulfilled:

- The power output stage is switched ON with V<sub>DS</sub> < V<sub>DS(OLOFF)</sub>
- The diagnosis is enabled
- No fault (as described in **Chapter 8.3**) is present or was present and not cleared yet (see **Chapter 9.2.2** for further details)

If a "hard" failure mode is present or was present and not cleared yet a current *I*<sub>IS(FAULT)</sub> is provided at IS pin.



**Diagnosis**

**9.2.1 Current Sense ( $k_{ILIS}$ )**

The accuracy of the sense current depends on temperature and load current.  $I_{IS}$  increases linearly with  $I_L$  output current until it reaches the saturation current  $I_{IS(SAT)}$ . In case of Open Load at the output stage ( $I_L$  close to 0 A), the maximum sense current  $I_{IS(EN)}$  (no load, diagnosis enabled) is specified. This condition is shown in **Figure 32**. The blue line represents the ideal  $k_{ILIS}$  line, while the red lines show the behavior of a typical product.

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1  $\mu$ s for the RC filter is recommended).

The  $k_{ILIS}$  factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. Tighter limits are possible (within a defined current window) with calibration:

- A well-defined and precise current ( $I_{L(CAL)}$ ) is applied at the output during End of Line test at customer side
- The corresponding current at IS pin is measured and the  $k_{ILIS}$  is calculated ( $k_{ILIS} @ I_{L(CAL)}$ )
- Within the current range going from  $I_{L(CAL)_L}$  to  $I_{L(CAL)_H}$  the  $k_{ILIS}$  is equal to  $k_{ILIS} @ I_{L(CAL)}$  with limits defined by  $\Delta k_{ILIS}$

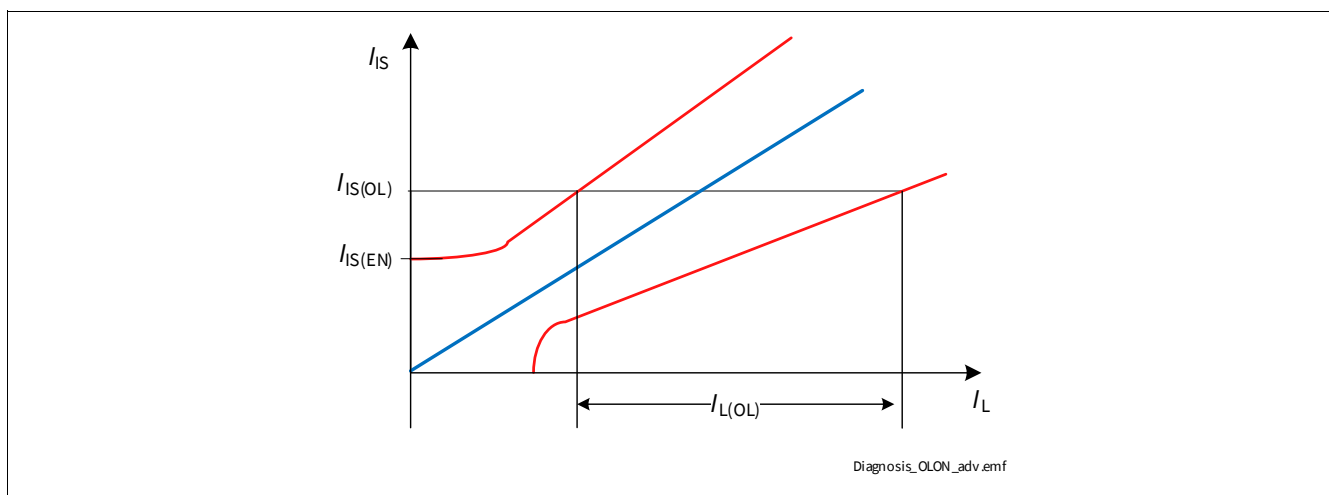
The derating of  $k_{ILIS}$  after calibration is calculated using the formulas in **Figure 31** and it is specified by  $\Delta k_{ILIS}$

$$\Delta k_{ILIS,MAX} = 100 \cdot MAX \left( \frac{k_{ILIS}@I_{L(CAL)_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1 \right)$$

$$\Delta k_{ILIS,MIN} = 100 \cdot MIN \left( \frac{k_{ILIS}@I_{L(CAL)_L}}{k_{ILIS}@I_{L(CAL)}} - 1, \frac{k_{ILIS}@I_{L(CAL)_H}}{k_{ILIS}@I_{L(CAL)}} - 1 \right)$$

**Figure 31  $\Delta k_{ILIS}$  calculation formulas**

The calibration is intended to be performed at  $T_{A(CAL)} = 25^\circ\text{C}$ . The parameter  $\Delta k_{ILIS}$  includes the drift overtemperature as well as the drift over the current range from  $I_{L(CAL)_L}$  to  $I_{L(CAL)_H}$ .



**Figure 32 Current Sense Ratio in Open Load at ON condition**

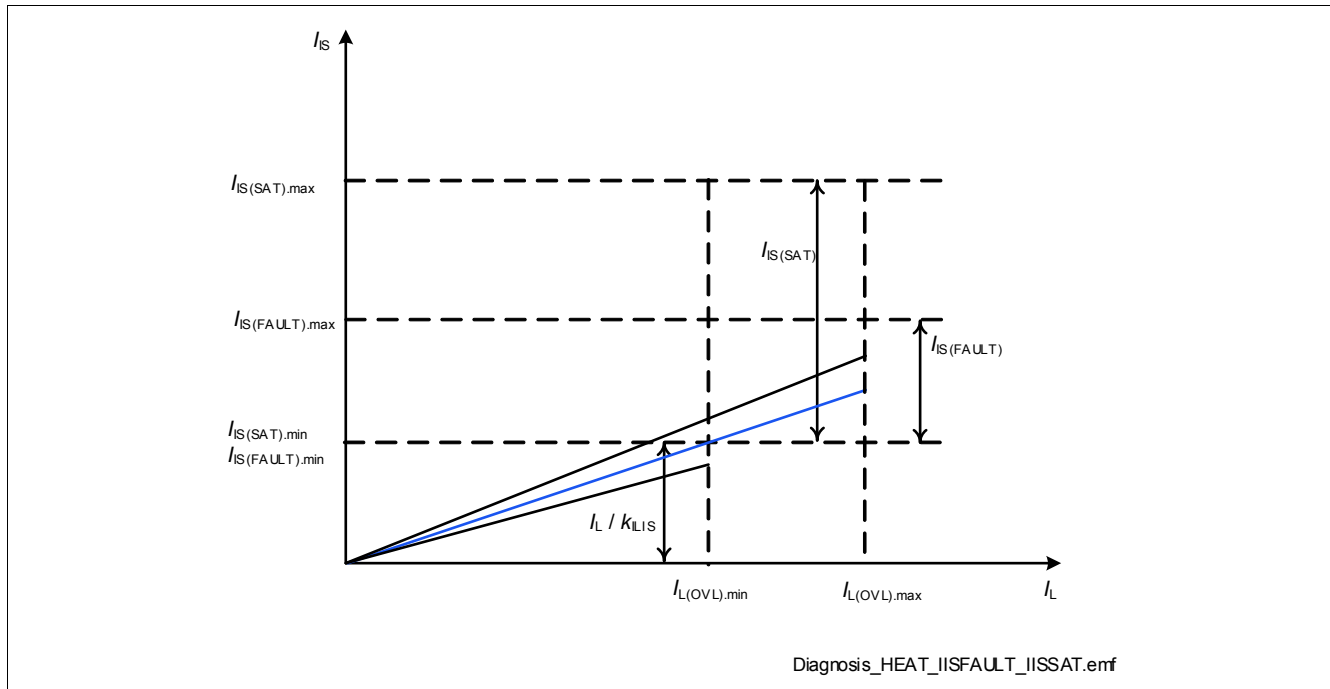
**9.2.2 Fault Current ( $I_{IS(FAULT)}$ )**

As soon as a protection event occurs, the value of the internal latch (see **Chapter 8.3** for more details) is changed from 0 to 1, a current  $I_{IS(FAULT)}$  is provided by pin IS when DEN is set to “high” and the affected device is switched OFF.

**Diagnosis**

If internal latch is 1, and it is not reset, the current  $I_{IS(FAULT)}$  is provided each time the device diagnosis is activated by DEN=High.

**Figure 33** shows the relation between  $I_{IS} = I_L / k_{ILIS}$ ,  $I_{IS(SAT)}$  and  $I_{IS(FAULT)}$ .



**Figure 33 SENSE behavior - overview**

**9.3 Diagnosis in OFF state**

When a power output stage is in OFF state, the BTS7002-1EPP can measure the drain-source voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source), it is possible to detect if the load is missing or if there is a short circuit to battery. If a Fault condition was detected by the device (if internal latch is 1, fault current is provided by IS pin independent of drain-source or output voltage, as long as DEN=High) a current  $I_{IS(FAULT)}$  is provided by IS pin each time the channel diagnosis is checked also in OFF state. See **Chapter 9.2.2** for further details.

**9.3.1 Open Load current ( $I_{IS(OLOFF)}$ )**

In OFF state, when DEN pin is set to “high”, the  $V_{DS}$  voltage is compared with a threshold voltage  $V_{DS(OLOFF)}$ . If the load is properly connected and there is no short circuit to battery,  $V_{DS} \sim V_S$  therefore  $V_{DS} > V_{DS(OLOFF)}$ . When the diagnosis is active and  $V_{DS} \leq V_{DS(OLOFF)}$ , a current  $I_{IS(OLOFF)}$  is provided by IS pin. **Figure 34** shows the relationship between  $I_{IS(OLOFF)}$  and  $I_{IS(FAULT)}$  as functions of  $V_{DS}$ . The two currents do not overlap making it always possible to differentiate between Open Load in OFF and Fault condition.

Diagnosis

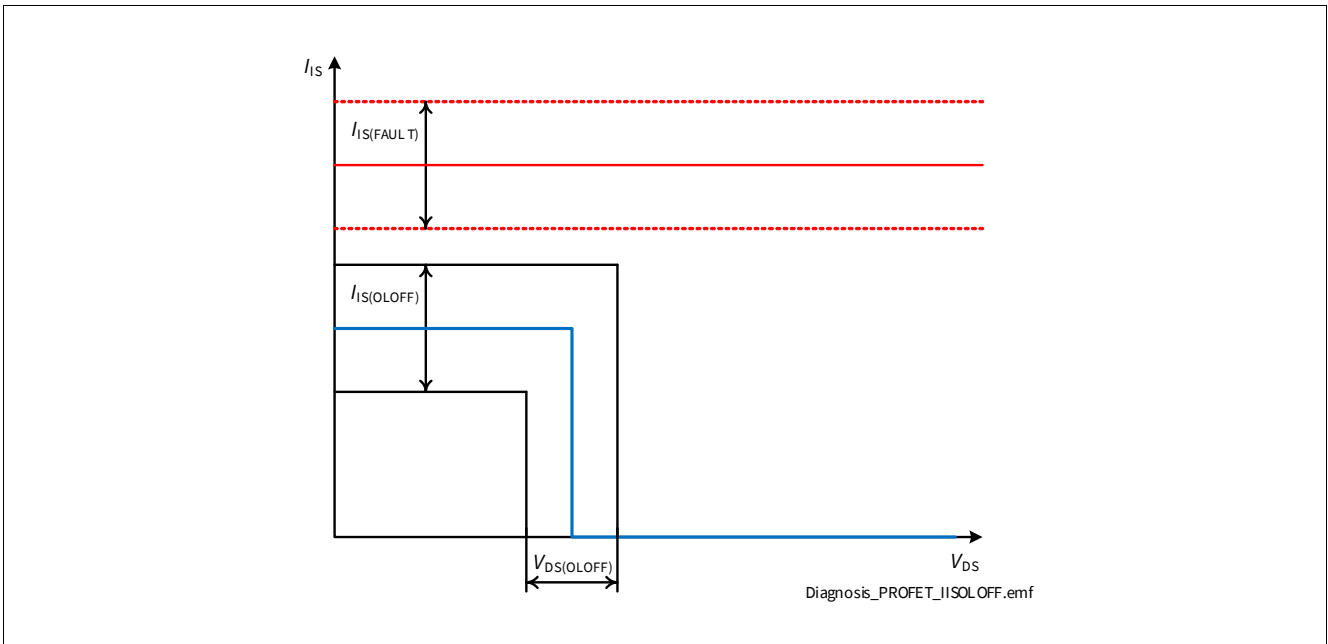


Figure 34  $I_{IS}$  in OFF State

It is necessary to wait a time  $t_{IS(OLOFF)_D}$  between the falling edge of the input pin and the sensing at pin IS for Open Load in OFF diagnosis to allow the internal comparator to settle. In Figure 35 the timings for an Open Load detection are shown - the load is always disconnected.

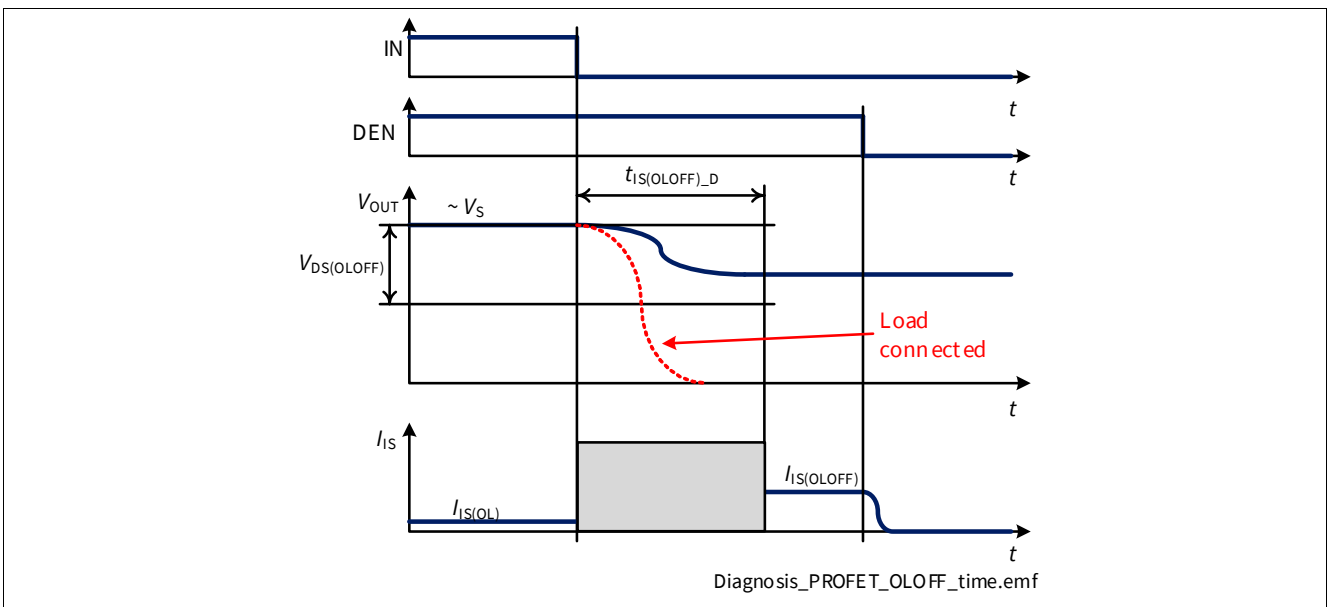
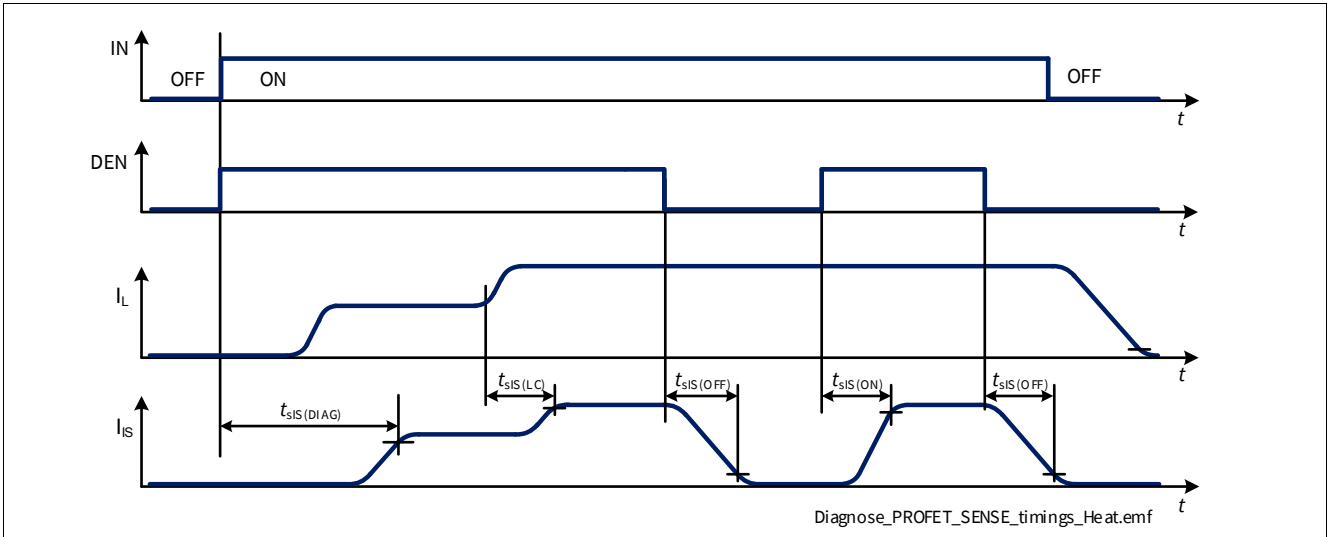


Figure 35 Open Load in OFF Timings - load disconnected

**Diagnosis**

**9.4 SENSE Timings**

**Figure 36** shows the timing during settling  $t_{sIS(ON)}$  and disabling  $t_{sIS(OFF)}$  of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before  $t_{ON}$ ),  $t_{sIS(DIAG)} \leq 3 \times (t_{ON\_max} + t_{sIS(ON)\_max})$ .



**Figure 36 SENSE Settling / Disabling Timing**

**Diagnosis**

**9.5 Electrical Characteristics Diagnosis**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**Table 19 Electrical Characteristics: Diagnosis - General**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Saturation Current	$I_{IS(SAT)}$	4.4	–	15	mA	1) $V_{SIS} = V_S - V_{IS} \geq 2\text{ V}$ See <b>Figure 33</b>	P_9.6.0.1
SENSE Leakage Current when Disabled	$I_{IS(OFF)}$	–	0.01	0.5	$\mu\text{A}$	DEN = “low” $V_{IS} = 0\text{ V}$	P_9.6.0.2
SENSE Leakage Current when Enabled at $T_J \leq 85\text{ °C}$	$I_{IS(EN)_85}$	–	0.2	1	$\mu\text{A}$	1) $T_J \leq 85\text{ °C}$ DEN = “high” $I_L = 0\text{ A}$ See <b>Figure 32</b>	P_9.6.0.3
SENSE Leakage Current when Enabled at $T_J = 150\text{ °C}$	$I_{IS(EN)_150}$	–	0.2	1	$\mu\text{A}$	$T_J = 150\text{ °C}$ DEN = “high” $I_L = 0\text{ A}$ See <b>Figure 32</b>	P_9.6.0.4
SENSE Operative Range for $k_{ILIS}$ Operation ( $V_S - V_{IS}$ )	$V_{SIS\_k}$	–	0.5	1	V	1) $V_S = 6\text{ V}$ IN = DEN = “high” $I_L \leq 2 * I_{L(NOM)}$	P_9.6.0.6
SENSE Operative Range for Open Load at OFF Diagnosis ( $V_S - V_{IS}$ )	$V_{SIS\_OL}$	–	0.5	1	V	1) $V_S = 6\text{ V}$ IN = “low” DEN = “high”	P_9.6.0.7
SENSE Operative Range for Fault Diagnosis ( $V_S - V_{IS}$ )	$V_{SIS\_F}$	–	0.5	1	V	1) $V_S = 6\text{ V}$ IN = “low” DEN = “high” latch $\neq 0$	P_9.6.0.8
Power Supply to IS Pin Clamping Voltage at $T_J = -40\text{ °C}$	$V_{SIS(CLAMP)\_40}$	33	36.5	42	V	$I_{IS} = 1\text{ mA}$ $T_J = -40\text{ °C}$ See <b>Figure 16</b>	P_9.6.0.9
Power Supply to IS Pin Clamping Voltage at $T_J \geq 25\text{ °C}$	$V_{SIS(CLAMP)\_25}$	35	38	44	V	2) $I_{IS} = 1\text{ mA}$ $T_J \geq 25\text{ °C}$ See <b>Figure 16</b>	P_9.6.0.10

1) Not subject to production test - specified by design.

2) Tested at  $T_J = 150\text{ °C}$ .

**Diagnosis**

**9.5.1 Electrical Characteristics Diagnosis**

**Table 20 Electrical Characteristics: Diagnosis**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SENSE Fault Current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	–	P_9.6.4.1
SENSE Open Load in OFF Current	$I_{IS(OLOFF)}$	1.8	2.5	3.5	mA	–	P_9.6.4.2
SENSE Open Load in OFF Delay Time	$t_{IS(OLOFF)_D}$	70	185	300	μs	$V_{DS} < V_{OL(OFF)}$ from IN falling edge to $V_{IS} = R_{SENSE} * 0.9 * I_{IS(OLOFF),MIN}$ DEN = “high”	P_9.6.4.4
Open Load $V_{DS}$ Detection Threshold in OFF State	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	–	P_9.6.4.5
SENSE Settling Time with Nominal Load Current Stable	$t_{SIS(ON)}$	–	5	40	μs	$I_L = I_{L(NOM)}$ DEN from “low” to “high”	P_9.6.4.6
SENSE Disable Time	$t_{SIS(OFF)}$	–	5	20	μs	<sup>1)</sup> From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See <a href="#">Figure 36</a>	P_9.6.4.8
SENSE Settling Time after Load Change	$t_{SIS(LC)}$	–	5	20	μs	<sup>1)</sup> from $I_L = I_{L19}$ to $I_L = I_{L20}$ See <a href="#">Figure 36</a>	P_9.6.4.3

1) Not subject to production test - specified by design.

**Diagnosis**

**9.6 Electrical Characteristics Diagnosis - Power Output Stages**

$V_S = 6\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$

Typical values:  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Typical resistive load connected to the output for testing (unless otherwise specified):

$R_L = 2.1\ \Omega$

**9.6.1 Diagnosis Power Output Stage - 2 mΩ**

**Table 21 Electrical Characteristics: Diagnosis - 2 mΩ**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Open Load Output Current at $I_{IS} = 4\ \mu\text{A}$	$I_{L(OL)\_4u}$	32	91	150	mA	$I_{IS} = I_{IS(OL)} = 4\ \mu\text{A}$ see <a href="#">Figure 32</a>	P_9.7.10.1
Current Sense Ratio at $I_L = I_{L05}$	$k_{ILIS05}$	-65%	22700	+65%		$I_{L05} = 100\text{ mA}$	P_9.7.10.9
Current Sense Ratio at $I_L = I_{L09}$	$k_{ILIS09}$	-65%	22700	+65%		$I_{L09} = 450\text{ mA}$	P_9.7.10.13
Current Sense Ratio at $I_L = I_{L11}$	$k_{ILIS11}$	-55%	22700	+55%		$I_{L11} = 1\text{ A}$	P_9.7.10.15
Current Sense Ratio at $I_L = I_{L15}$	$k_{ILIS15}$	-40%	22700	+40%		$I_{L15} = 4\text{ A}$	P_9.7.10.19
Current Sense Ratio at $I_L = I_{L18}$	$k_{ILIS18}$	-24%	22700	+24%		$I_{L18} = 10\text{ A}$	P_9.7.10.22
Current Sense Ratio at $I_L = I_{L19}$	$k_{ILIS19}$	-8%	22700	+8%		$I_{L19} = 15\text{ A}$	P_9.7.10.23
Current Sense Ratio at $I_L = I_{L20}$	$k_{ILIS20}$	-8%	22700	+8%		<sup>1)</sup> $I_{L20} = 22\text{ A}$	P_9.7.10.24
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	<sup>1)</sup> $I_{L(CAL)} = I_{L09}$ $I_{L(CAL)\_H} = I_{L11}$ $I_{L(CAL)\_L} = I_{L05}$ $T_{A(CAL)} = 25\text{ °C}$	P_9.7.10.27
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-4	0	+4	%	<sup>1)</sup> $I_{L(CAL)} = I_{L19}$ $I_{L(CAL)\_H} = I_{L20}$ $I_{L(CAL)\_L} = I_{L18}$ $T_{A(CAL)} = 25\text{ °C}$	P_9.7.10.29

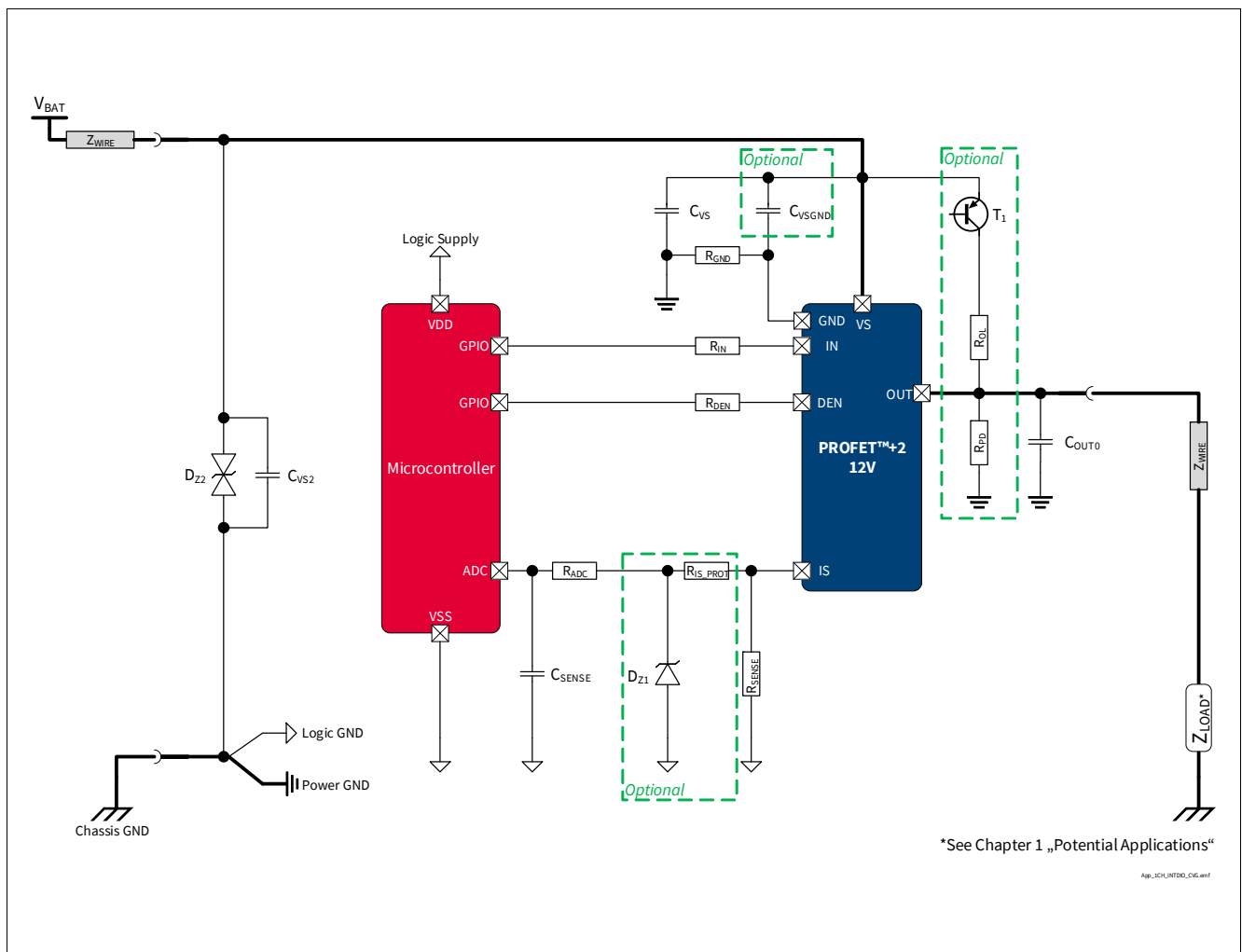
<sup>1)</sup> Not subject to production test - specified by design.

**Application Information**

**10 Application Information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**10.1 Application setup**



**Figure 37 BTS7002-1EPP Application Diagram**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*



**Application Information**

**10.2 External Components**

**Table 22 Suggested Component values**

Reference	Value	Purpose
$R_{IN}$	4.7 k $\Omega$	Protection of the microcontroller during Overvoltage and Reverse Polarity Necessary to switch OFF BTS7002-1EPP output during Loss of Ground
$R_{DEN}$	4.7 k $\Omega$	Protection of the microcontroller during Overvoltage and Reverse Polarity Necessary to switch OFF BTS7002-1EPP output during Loss of Ground
$R_{PD}$	47 k $\Omega$	Output polarization (pull-down) Ensures polarization of BTS7002-1EPP outputs to distinguish between Open Load and Short to $V_S$ in OFF Diagnosis
$R_{OL}$	1.5 k $\Omega$	Output polarization (pull-up) Ensures polarization of BTS7002-1EPP output during Open Load in OFF diagnosis
$C_{OUT}$	10 nF	Protection of BTS7002-1EPP output during ESD events and BCI
$T_1$	BC 807	Switch the battery voltage for Open Load in OFF diagnosis
$C_{VS}$	100 nF	Filtering of voltage spikes on the battery line
$C_{VSGND}$	47 nF	Buffer capacitor for fast transient See <a href="#">Table 5</a> (P_4.3.0.7) for the boundary conditions A placeholder on PCB layout is recommended
$D_{Z2}$	33 V TVS Diode	Transient Voltage Suppressor diode Protection during Overvoltage and in case of Loss of Battery while driving an inductive load
$C_{VS2}$	–	Filtering / buffer capacitor located at $V_{BAT}$ connector
$R_{SENSE}$	1.2 k $\Omega$	SENSE resistor
$R_{IS\_PROT}$	4.7 k $\Omega$	Protection during Overvoltage, Reverse Polarity, Loss of Ground Value to be tuned according to microcontroller specifications
$D_{Z1}$	7 V Z-Diode	Protection of microcontroller during Overvoltage
$R_{ADC}$	4.7 k $\Omega$	Protection of microcontroller ADC input during Overvoltage, Reverse Polarity, Loss of Ground Value to be tuned according to microcontroller specifications
$C_{SENSE}$	220 pF	Sense signal filtering A time constant $(R_{ADC} + R_{IS\_PROT}) * C_{SENSE}$ longer than 1 $\mu$ s is recommended
$R_{GND}$	47 $\Omega$	Protection in case of Overvoltage and Loss of Battery while driving inductive loads

**10.3 Further Application Information**

- Please contact us for information regarding the Pin FMEA
- For further information you may contact <http://www.infineon.com/>

Package Outlines

11 Package Outlines

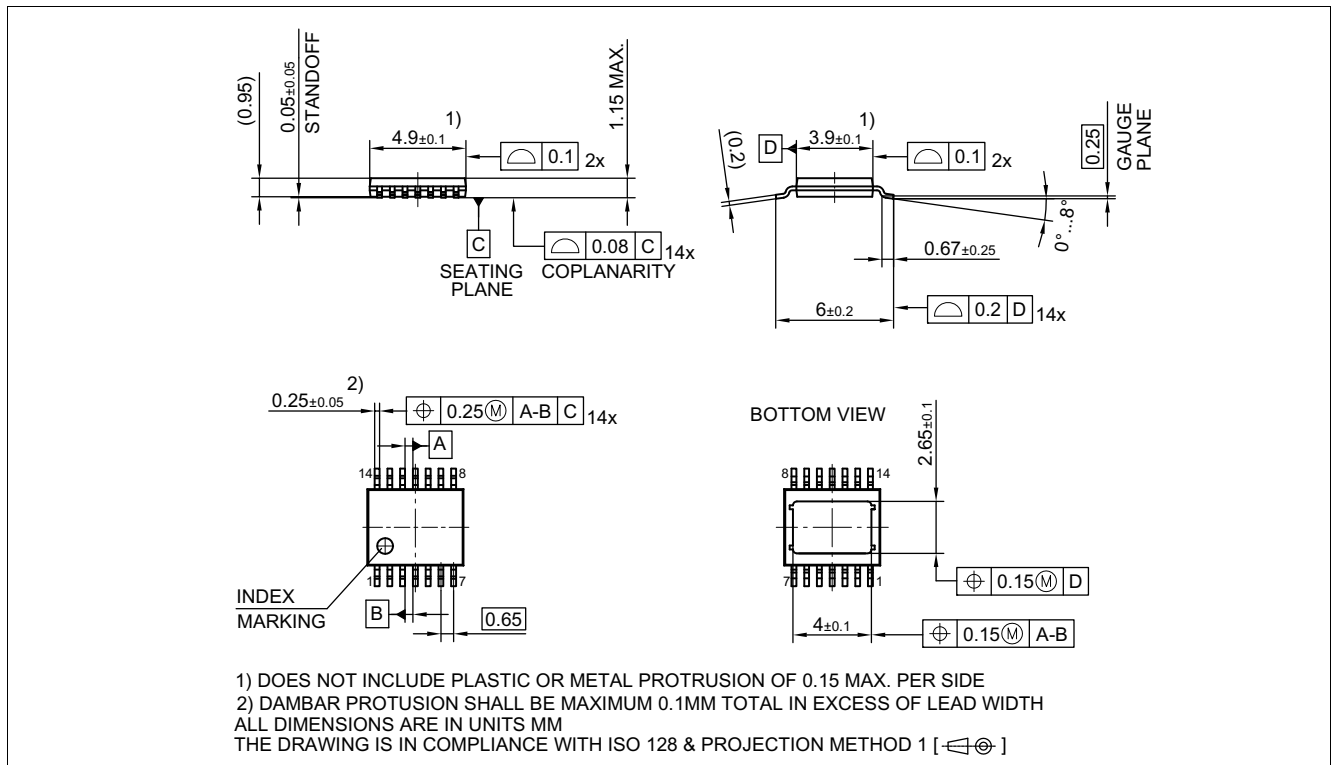


Figure 38 PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package Outline

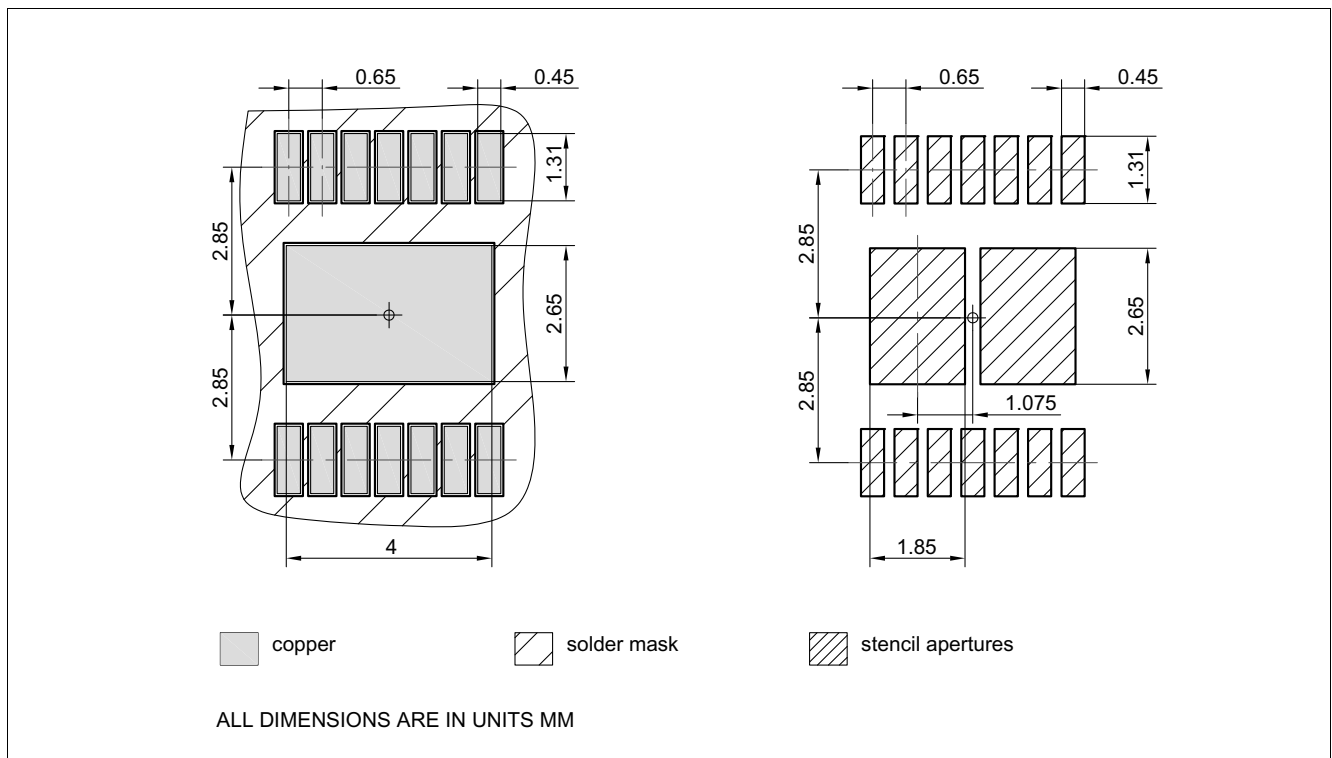


Figure 39 PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package pads and stencil

## **Package Outlines**

### **Green product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### **Further information on packages**

<https://www.infineon.com/packages>

**Revision History**

## 12 Revision History

**Table 23** BTS7002-1EPP - List of changes

Revision	Changes
1.04, 2019-10-15	<p>P_6.5.20.1 updated (Typ.: 0.01 <math>\mu</math>A <math>\rightarrow</math> 0.1 <math>\mu</math>A)  P_8.7.10.1, P_8.7.10.7, P_8.7.10.8 updated (added in Note or Test Condition: link to <a href="#">Figure 24</a>)  P_7.5.10.5 updated (added in Note or Test Condition: see <a href="#">Figure 18</a>)  P_7.5.10.12 updated (added in Note or Test Condition: see <a href="#">Figure 20</a>; deleted unnecessary space in Symbol: <math> dV_{OUT} / dt  \rightarrow  dV_{OUT} / dt </math>)  P_8.7.10.6 updated (added in Note or Test Condition: see <a href="#">Figure 25</a>)  P_9.7.10.1 updated (added in Note or Test Condition: see <a href="#">Figure 32</a>)  <a href="#">Figure 1</a>, <a href="#">Figure 37</a> updated  P_4.3.0.7 added  <b>Table 22</b> updated  <b>Chapter 5.1</b> updated (added: see <a href="#">Chapter 10</a> for the complete application setup overview)  <b>Chapter 9.2</b> updated (<math>2\text{ V} \rightarrow V_{DS(OFF)}</math>)  General: updated (ReverSave™ <math>\rightarrow</math> ReverseON)</p>
1.03, 2019-04-29	<p><b>Chapter 1</b> updated ((inserted headline "Product Validation"), (Qualified in accordance with AEC Q100 grade 1 <math>\rightarrow</math> Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.))  General: updated Product Name (High Current PROFET™ 12V <math>\rightarrow</math> PROFET™+2 12V)  P_9.7.10.1 updated (Min./Typ./Max.: 62/-/138 mA <math>\rightarrow</math> 32/91/150 mA)</p>
1.02, 2019-02-05	<p><a href="#">Figure 9</a>, <a href="#">Figure 10</a> updated  Page 1: updated (figure product)  <b>Table 22</b> updated (punctuation)  <b>Chapter 9.3</b>, <b>Chapter 9.3.1</b> updated (typo)  Page 1: updated (Package PG-TSDSO-14-22 <math>\rightarrow</math> Package PG-TSDSO-14)  <a href="#">Figure 38</a> updated (PG-TSDSO-14-22 (Thin (Slim) Dual Small Outline 14 pins) Package Outline <math>\rightarrow</math> PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package Outline)  <a href="#">Figure 39</a> updated (PG-TSDSO-14-22 (Thin (Slim) Dual Small Outline 14 pins) Package pads and stencil <math>\rightarrow</math> PG-TSDSO-14 (Thin (Slim) Dual Small Outline 14 pins) Package pads and stencil)  <b>Table 1</b> updated (Parameter: Minimum Overvoltage protection (<math>T_J = 25\text{ }^\circ\text{C}</math>) <math>\rightarrow</math> Minimum Overvoltage protection (<math>T_J \geq 25\text{ }^\circ\text{C}</math>))  <b>Table 1</b> updated (corrected typo in table Product Summary: <math>I_{VS(OFF)}</math>: 1 <math>\rightarrow</math> 0.9 <math>\mu</math>A)  <b>Table 1</b> updated (Symbol: <math>I_{VS(OFF)} \rightarrow I_{VS(OFF)_{85}}</math>)  P_6.5.20.1 updated (Symbol: <math>I_{VS(OFF)} \rightarrow I_{VS(OFF)_{85}}</math>)  P_6.5.20.2 updated (Symbol: <math>I_{VS(OFF)} \rightarrow I_{VS(OFF)_{150}}</math>)  P_9.7.10.27, P_9.7.10.29 updated (Note or Test Condition: formatted physical symbols as subscript)</p>
1.01, 2018-06-14	<p>Page numbering corrected  Figure Application Diagram, <a href="#">Figure 29</a>, <a href="#">Figure 37</a> updated</p>
1.00, 2018-05-23	Data Sheet available

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