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www.infineon.com

# USB-Dual I²C Bridge Controller

## Features

- USB 2.0 compliant, Full-Speed (12 Mbps)
  - ❏ Support for communication driver class (CDC), personal health care device class (PHDC), and vendor device class
  - ❏ Battery charger detection (BCD) compliant with USB Battery Charging Specification Rev 1.2 (Peripheral Detect only)
  - ❏ Integrated USB termination resistors
- Two-channel configurable I²C interfaces
  - ❏ Master/slave up to 400 kHz
  - ❏ Supports multi-master I²C
  - ❏ 256 bytes for each transmit and receive buffer per channel
- General-purpose input/output (GPIO) pins: 12
- Configuration utility (Windows) to configure the following:
  - ❏ Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
  - ❏ I²C
  - ❏ Battery Charger Detection compliant to BC-1.2 specification
  - ❏ GPIO
- Driver support for VCOM and DLL
  - ❏ Windows 10: 32- and 64-bit versions
  - ❏ Windows 8.1: 32- and 64-bit versions
  - ❏ Windows 8: 32- and 64-bit versions
  - ❏ Windows 7: 32- and 64-bit versions
  - ❏ Windows Vista: 32- and 64-bit versions
  - ❏ Windows XP: 32- and 64-bit versions
  - ❏ Mac OS-X: 10.6, and later versions
  - ❏ Linux: Kernel version 2.6.35 onwards

- Clocking: Integrated 48-MHz clock oscillator
- Supports bus-/self-powered configurations
- USB suspend mode for low power
- Operating voltage: 1.71 to 5.5 V
- Operating temperature
  - ❏ Commercial: 0 °C to 70 °C
  - ❏ Industrial: –40 °C to 85 °C
- ESD protection: 2.2 kV HBM
- RoHS compliant package
  - ❏ 32-pin QFN (5 × 5 × 1 mm. 0.5 mm pitch)
- Ordering part number
  - ❏ CY7C65216D-32LTXI
  - ❏ CY7C65216D-32LTXIT

## Applications

- Medical/healthcare devices
- Point-of-Sale (POS) terminals
- Test and measurement system
- Gaming systems
- Set-top box PC-USB interface
- Industrial
- Networking
- Enabling USB connectivity in legacy peripherals

***USB Compliant***

*The USB Dual I²C Bridge Controller with BCD is fully compliant with USB2.0 Specification and Battery Charging Specification v1.2.*

**Errata:** For information on silicon errata, see "Errata" on page 27. Details include trigger conditions, devices affected, and proposed workaround.

# USB Serial Bridge Controller Family

USB Serial bridge Controllers are a family of configurable products for most common applications requiring no firmware changes.

Configuration utility is provided to Configure USB-VID, USB-PID, USB Product and Manufacturer Descriptors. The same configuration utility can be used to configure UART, $I^2C$, SPI, Battery Charger Detection, GPIOs, Power mode, and so on.

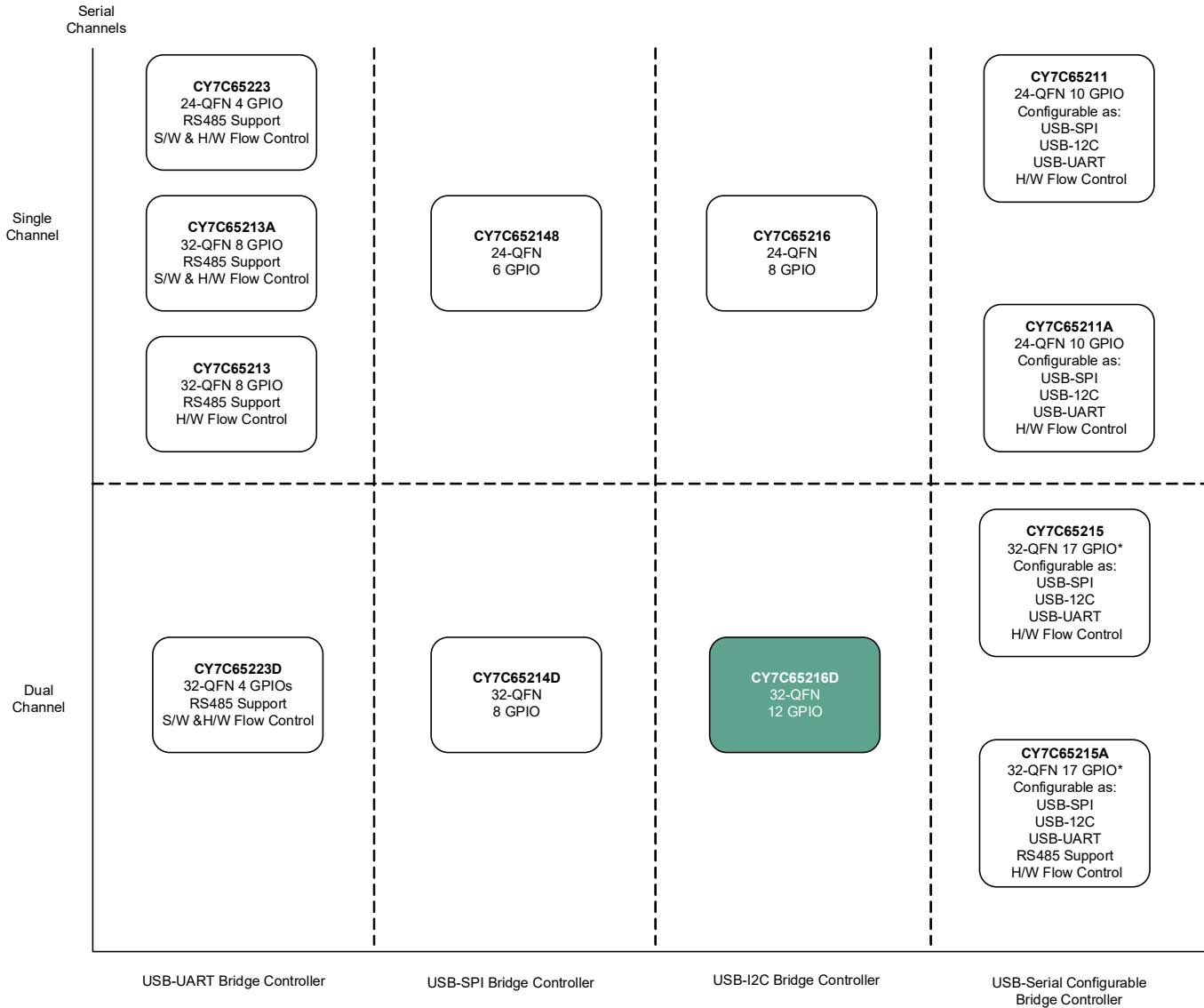**Figure 1.  USB Serial Bridge Controller Family**

**Table 1.  USB Serial Family Feature Comparison**

| MPN | # of Channels | GPIO | USB-UART | | | | USB-SPI | | USB-I²C |
| | | | RS485 Support | Software Flow Control | Hardware Flow Control | UART Pins** | SPI Serial Data Width (bit) | SPI Master/ Slave | I²C Master/ Slave |
|---|---|---|---|---|---|---|---|---|---|
| CY7C65213 | 1 | 8 | N | N | Y | 8 | – | – | – |
| CY7C65213A | 1 | 8 | Y | N | Y | 8 | – | – | – |
| CY7C65223 | 1 | 4 | Y | Y | Y | 2 / 4 / 6 | – | – | – |
| CY7C65223D | 2 | 4 | Y | Y | Y | 2 / 4 / 6 / 8 | – | – | – |
| CY7C652148 | 1 | 6 | – | – | – | – | 4-16 bit | Master/Slave | – |
| CY7C65214D | 2 | 8 | – | – | – | – | 4-16 bit | Master/Slave | – |
| CY7C65216 | 1 | 8 | – | – | – | – | – | – | Master/Slave |
| **CY7C65216D** | **2** | **12** | **–** | **–** | **–** | **–** | **–** | **–** | **Master/Slave** |
| CY7C65211 | 1 | 10* | N | N | Y | 2 / 4 / 6 | 4-16 bit | Master/Slave | Master/Slave |
| CY7C65211A | 1 | 10* | Y | N | Y | 2 / 4 / 6 | 4-16 bit | Master/Slave | Master/Slave |
| CY7C65215 | 2 | 17* | N | N | Y | 2 / 4 / 6 | 4-16 bit | Master/Slave | Master/Slave |
| CY7C65215A | 2 | 17* | Y | N | Y | 2 / 4 / 6 / 8 | 4-16 bit | Master/Slave | Master/Slave |

**Legend**

* Represents the total GPIO count offered by the part. This count can dynamically change based on UART / SPI / I²C pin configuration.
** UART Pins

| **UART Pins | UART Signal |
|---|---|
| 2 | RxD and TxD |
| 4 | RxD, TxD, RTS#, CTS# |
| 6 | RxD, TxD, RTS#, CTS#, DTR#, DSR# |
| 8 | RxD, TxD, RTS#, CTS#, DTR#, DSR#, DCD#, RI# |

**Table 2. Default Serial Channel Configuration**

| MPN | # of Channels | GPIO | USB Protocol | USB- UART | | USB-SPI | USB-I$^2$C |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | Is RS485 Enabled | UART Pins | SPI Master/ Slave | I$^2$C Master/ Slave |
| CY7C65213 | 1 | 4 | CDC** | N | 8 | – | – |
| CY7C65213A | 1 | 4 | CDC** | N | 8 | – | – |
| CY7C65223 | 1 | 4 | CDC** | Y | 4 | – | – |
| CY7C65223D | 2 | 4 | CDC** | Y | 4 | – | – |
| CY7C652148 | 1 | 6 | Vendor*** | – | – | Master | – |
| CY7C65214D | 2 | 8 | Vendor*** | – | – | Master | – |
| CY7C65216 | 1 | 8 | Vendor*** | – | – | – | Slave |
| **CY7C65216D** | **2** | **12** | **Vendor*** | **–** | **–** | **–** | **Master** |
| CY7C65211 | 1 | 3 | CDC** | N | 6 | – | – |
| CY7C65211A | 1 | 3 | CDC** | N | 6 | – | – |
| CY7C65215 | 2 | 4 | CDC** | N | 6 | – | – |
| CY7C65215A | 2 | 4 | CDC** | N | 6 | – | – |

** USB CDC Protocol allows the USB host Operating System to detect the device as Virtual COM Port Device.
*** USB Vendor Protocol allows the USB host operating system to detect the device as general USB device. This device is accessible using Cypress Application Library.

# More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the document USB-Serial Bridge Controller Product Overview.

- Overview: USB Portfolio, USB Roadmap

- USB 2.0 Product Selectors: USB-Serial Bridge Controller, USB to UART Controller (Gen I)

- Knowledge Base Articles: Cypress offers a large number of USB knowledge base articles covering a broad range of topics, from basic to advanced level. Recommended knowledge base articles for getting started with USB-Serial Bridge Controller are:
  - ❏ KBA85909 – Key Features of the Cypress® USB-Serial Bridge Controller
  - ❏ KBA85920 – USB-UART and USB-Serial
  - ❏ KBA85921 – Replacing FT232R with CY7C65213 USB-UART LP Bridge Controller
  - ❏ KBA85913 – Voltage supply range for USB-Serial
  - ❏ KBA89355 – USB-Serial: Cypress Default VID and PID
  - ❏ KBA92641 – USB-Serial Bridge Controller Managing I/Os using API
  - ❏ KBA92442 – Non-Standard Baud Rates in USB-Serial Bridge Controllers
  - ❏ KBA91366 – Binding a USB-Serial Device to a Microsoft® CDC Driver
  - ❏ KBA92551 – Testing a USB-Serial Bridge Controller Configured as USB-UART with Linux®
  - ❏ KBA91299 – Interfacing an External I$^2$C Device with the CYUSBS234/236 DVK

For a complete list of knowledge base articles, click here.

- Code Examples: USB Full-Speed

- Development Kits:
  - ❏ CYUSBS232, Cypress USB-UART LP Reference Design Kit
  - ❏ CYUSBS234, Cypress USB-Serial (Single Channel) Development Kit
  - ❏ CYUSBS236, Cypress USB-Serial (Dual Channel) Development Kit

- Models: IBIS

## Block Diagram
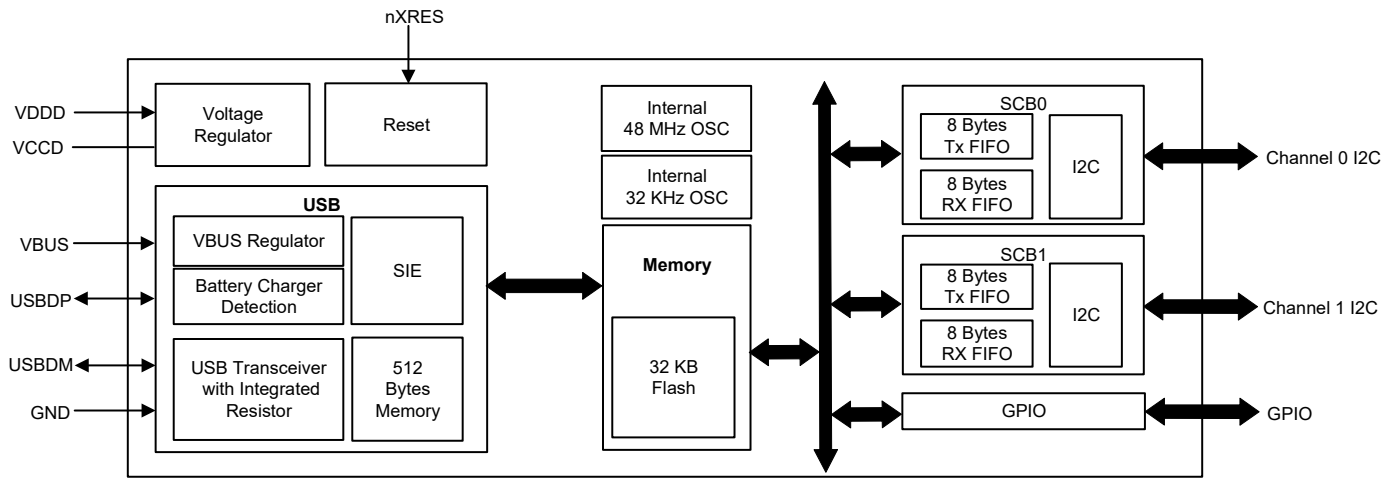
# Contents

## Functional Overview

The CY7C65216D is a Full-Speed USB controller that enables seamless PC connectivity for peripherals with dual-channel I$^2$C interfaces. CY7C65216D also integrates BCD, which is compliant with the USB Battery Charging Specification Rev. 1.2. It integrates a voltage regulator, oscillator, and flash memory for storing configuration parameters, offering a cost-effective solution. CY7C65216D supports bus-powered and self-powered modes, and enables efficient system power management with suspend and remote wake-up signals. It is available in a 32-pin QFN package.

### USB and Charger Detect

*USB*

CY7C65216D has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates the internal USB series termination resistors on the USB data lines and a 1.5-kΩ pull-up resistor on USBDP.

**Table 3. Maximum Speed supported on both SCBs**

| No. | Configuration | SCB0 Maximum Speed | SCB1 Maximum Speed |
|-----|---------------|--------------------|--------------------|
| 1 | SCB0 = I$^2$C Master, SCB1 = Disabled | 400 kHz (Both TX and RX) | NA |
| 2 | SCB0 = I$^2$C Slave, SCB1 = Disabled | 400 kHz (Both TX and RX) | NA |
| 3 | SCB0 = I$^2$C, SCB1 = I$^2$C | 400 kHz (Both TX and RX) | 400 kHz (Both TX and RX) |

*I$^2$C Interface*

The I$^2$C interface implements full multi-master/slave modes and supports up to 400 kHz. The configuration utility tool is used to set the I$^2$C address in slave mode. This tool enables only even slave addresses. For further details on protocol, refer to the NXP I$^2$C specification rev5.

**Notes**

■ I$^2$C ports are not tolerant of higher voltages and cannot be hot-swapped or powered up independently from the rest of the I$^2$C system.

■ The minimum fall time of the SCL is met (as per NXP I$^2$C specification Rev. 5) when V$_{DDD}$ is between 1.71 V and 3.0 V. When V$_{DDD}$ is within the range of 3.0 V to 3.6 V, it is recommended to add a 50 pF capacitor on the SCL signal.

### GPIO Interface

CY7C65216D has 12 GPIOs. The configuration utility allows configuration of the GPIO pins. The configurable options are as follows:

■ TRISTATE: GPIO can be tristated through Config Utility

■ DRIVE 1: Output static 1

■ DRIVE 0: Output static 0

■ POWER#: Power control for bus power designs

■ TXLED#: Drives LED during USB transmit

■ RXLED#: Drives LED during USB receive

■ TX or RX LED#: Drives LED during USB transmit or receive

GPIO can be configured to drive LED at 8-mA drive strength.

*Charger Detection*

CY7C65216D supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification Rev. 1.2. It supports the following charging ports:

■ Standard Downstream Port (SDP): allows the system to draw up to 500 mA current from the host

■ Charging Downstream Port (CDP): allows the system to draw up to 1.5 A current from the host

■ Dedicated Charging Port (DCP): allows the system to draw up to 1.5 A of current from the wall charger

### Serial Communication

CY7C65216D has two serial communication blocks (SCBs). Each SCB can implement I$^2$C interface. A 256-byte buffer is available in both the TX and RX lines.

Table 3 shows maximum speed supported on both SCBs when they are configured as I$^2$C.

■ BCD0/BCD1: Two-pin output to indicate the type of USB charger

■ BUSDETECT: Connects VBUS pin for USB host detection

### Default Configuration

CY7C65216D is configured as Dual I$^2$C Master device.

### Memory

CY7C65216D has a 512-byte flash. The flash is used to store the USB parameters such as VID/PID, serial number, Product, and Manufacturer Descriptors, which can be programmed by the configuration utility.

### System Resources

*Power System*

CY7C65216D supports the USB Suspend mode to control power usage. CY7C65216D operates in bus-powered or self-powered modes over a range of 3.15 to 5.5 V.

*Clock System*

CY7C65216D has a fully integrated clock and does not require any external components. The clock system is responsible for providing clocks to all subsystems.

*Internal 48-MHz Oscillator*

The internal 48-MHz oscillator is the primary source of internal clocking in CY7C65216D.

*Internal 32-kHz Oscillator*

The internal 32-kHz oscillator is primarily used to generate clocks for peripheral operation in the USB Suspend mode.

*Reset*

The reset block ensures reliable power-on reset and brings the device back to the default known state. The nXRES (active low) pin can be used by external devices to reset the CY7C65216D.

## Suspend and Resume

The CY7C65216D device asserts the SUSPEND pin when the USB bus enters the suspend state. This helps in meeting the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus-powered mode. The device will resume from the suspend state under any of the following conditions:

1. Any activity is detected on the USB bus
2. The WAKEUP pin is asserted to generate remote wakeup to the host

## WAKEUP

The WAKEUP pin is used to generate a remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65216D device allows enabling/disabling and polarity of the remote wakeup feature through the configuration utility.

## Software

Cypress delivers a complete set of software drivers and the configuration utility to enable product configuration during system development.

*Drivers for Linux Operating Systems*

Cypress provides a User Mode USB driver library (*libcyusb-serial.so*) that abstracts vendor commands for the I$^2$C interface and provides a simplified API interface to the user applications. This library makes use of the standard open source libUSB library to enable the USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux 'udev' mechanism.

*Drivers for Mac OSx*

Cypress delivers a dynamically linked shared library (CyUSBSerial.dylib) based on libUSB, which enables communication to the CY7C65216D device.

In addition, CY7C65216D binds to native MAC OSx driver. No special driver is required.

*Drivers for Windows Operating Systems*

For Windows operating systems (XP, Vista, Win7, Win8, Win8.1, and Win10), Cypress delivers a User Mode dynamically linked library–CyUSBSerial DLL–that abstracts vendor-specific interface of CY7C65216D devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific I$^2$C and class-specific APIs for PHDC.

USB-I$^2$C Bridge Controller works with Cypress provided USB vendor class driver. The Cypress Windows drivers are MS logo certified drivers.

These drivers are bound to device through WU (Windows Update) services.

Cypress drivers also support Windows plug-and-play and power management and USB Remote Wake-up.

### Device Configuration Utility (Windows Only)

A Windows-based configuration utility is available to configure various device initialization parameters. This graphical user application provides an interactive interface to define the various boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configuration from text or xml formats. The configuration utility allows the following operations:

■ View current device configuration

■ Select and configure I$^2$C, CapSense, battery charging, and GPIOs

■ Configure USB VID, PID, and string descriptors

■ Save or Load configuration

You can download the free configuration utility and drivers from www.cypress.com.

## Internal Flash Configuration

The internal flash memory can be used to store the configuration parameters shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application specific requirements over USB interface. The configuration utility can be downloaded from www.cypress.com/usbserial.

**Table 4. Internal Flash Configuration for CY7C65216D**

| Parameter | Default Value | Description |
|---|---|---|
| **USB Configuration** | | |
| USB Vendor ID (VID) | 0x04B4 | Default Cypress VID. Can be configured to customer VID. |
| USB Product ID (PID) | 0x0005 | Default Cypress PID. Can be configured to customer PID. |
| Manufacturer string | Cypress | Can be configured with any string up to 64 characters |
| Product string | USB-Serial (Dual Channel) | Can be configured with any string up to 64 characters |
| Serial string | | Can be configured with any string up to 64 characters |
| Power mode | Bus powered | Can be configured to bus-powered or self-powered mode |
| Max current draw | 100 mA | Can be configured to any value from 0 to 500 mA. Based on this, the configuration descriptor will be updated. |
| Remote wakeup | Enabled | Can be disabled. Remote wakeup is initiated by asserting WAKEUP pin. |
| USB interface protocol | Vendor | Can be configured to function in CDC, PHDC, or Cypress vendor class. |
| BCD | Disabled | Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD. |

## Electrical Specifications

### Absolute Maximum Ratings

Exceeding maximum ratings [1] may shorten the useful life of the device.

Storage temperature ........................ ...... –55 °C to +100 °C

Ambient temperature with
power supplied (Industrial) .................. ...... –40 °C to +85 °C

Supply voltage to ground potential

$V_{DDD}$ ................................................................. 6.0 V

$V_{BUS}$ ................................................................. 6.0 V

$V_{CCD}$ .............................................................. 1.95 V

$V_{GPIO}$ ........................................................ .....$V_{DDD}$ + 0.5 V

### Device Level Specifications

All specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C, $T_J$ ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Static discharge voltage ESD protection levels:

■ 2.2-kV HBM per JESD22-A114

Latch-up current ....................................................... 140 mA

Current per GPIO ....................................................... 25 mA

### Operating Conditions

$T_A$ (ambient temperature under bias)
Industrial ...................................................... –40 °C to +85 °C

$V_{BUS}$ supply voltage ................................... 3.15 V to 5.25 V

$V_{DDD}$ supply voltage ................................... 1.71 V to 5.50 V

$V_{CCD}$ supply voltage ................................... 1.71 V to 1.89 V

**Table 5. DC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{BUS}$ | $V_{BUS}$ supply voltage | 3.15 | 3.30 | 3.45 | V | Set and configure correct voltage range using the configuration utility for $V_{BUS}$. |
| | | 4.35 | 5.00 | 5.25 | V | |
| $V_{DDD}$ | $V_{DDD}$ supply voltage | 1.71 | 1.80 | 1.89 | V | Used to set I/O and core voltage. Set and configure correct voltage range using the configuration utility for $V_{DDD}$. |
| | | 2.0 | 3.3 | 5.5 | V | |
| $V_{CCD}$ | Output voltage (for core logic) | – | 1.80 | – | V | Do not use this supply to drive external device.<br>• 1.71 V ≤ $V_{DDD}$ ≤ 1.89 V: Short the $V_{CCD}$ pin with the $V_{DDD}$ pin<br>• $V_{DDD}$ > 2 V – connect a 1-μF capacitor (Cefc) between the $V_{CCD}$ pin and ground |
| Cefc | External regulator voltage bypass | 1.00 | 1.30 | 1.60 | μF | X5R ceramic or better |
| $I_{DD1}$ | Operating supply current | – | 13 | 18 | mA | USB 2.0 FS, no GPIO switching at $V_{BUS}$ = 5 V, $V_{DDD}$ = 5 V |
| $I_{DD2}$ | USB Suspend supply current | – | 5 | – | μA | Does not include current through a pull-up resistor on USBDP. In USB suspend mode, the D+ voltage can go up to a maximum of 3.8 V. |

**Table 6. AC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| Zout | USB driver output impedance | 28 | – | 44 | Ω | – |
| Twakeup | Wakeup from USB Suspend mode | – | 25 | – | μs | – |

**Note**
1. Usage above the absolute maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions the device may not operate to specification.

**GPIO**

**Table 7. GPIO DC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$[2] | Input voltage high threshold | $0.7 \times V_{DDD}$ | – | – | V | CMOS Input |
| $V_{IL}$ | Input voltage low threshold | – | – | $0.3 \times V_{DDD}$ | V | CMOS Input |
| $V_{IH}$[2] | LVTTL input, $V_{DDD}$< 2.7 V | $0.7 \times V_{DDD}$ | – | – | V | – |
| $V_{IL}$ | LVTTL input, $V_{DDD}$ < 2.7 V | – | – | $0.3 \times V_{DDD}$ | V | – |
| $V_{IH}$[2] | LVTTL input, $V_{DDD} \geq$ 2.7 V | 2 | – | – | V | – |
| $V_{IL}$ | LVTTL input, $V_{DDD} \geq$ 2.7 V | – | – | 0.8 | V | – |
| $V_{OH}$ | CMOS output voltage high level | $V_{DDD} - 0.4$ | – | – | V | $I_{OH}$ = 4 mA, $V_{DDD}$ = 5 V ± 10% |
| $V_{OH}$ | CMOS output voltage high level | $V_{DDD} - 0.6$ | – | – | V | $I_{OH}$ = 4 mA, $V_{DDD}$ = 3.3 V ± 10% |
| $V_{OH}$ | CMOS output voltage high level | $V_{DDD} - 0.5$ | – | – | V | $I_{OH}$ = 1 mA, $V_{DDD}$ = 1.8 V ± 5% |
| $V_{OL}$ | CMOS output voltage low level | – | – | 0.4 | V | $I_{OL}$ = 8 mA, $V_{DDD}$ = 5 V ± 10% |
| $V_{OL}$ | CMOS output voltage low level | – | – | 0.6 | V | $I_{OL}$ = 8 mA, $V_{DDD}$ = 3.3 V ± 10% |
| $V_{OL}$ | CMOS output voltage low level | – | – | 0.6 | V | $I_{OL}$ = 4 mA, $V_{DDD}$ = 1.8 V ± 5% |
| Rpullup | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| Rpulldown | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DDD}$ = 3.0 V |
| $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| Vhysttl | Input hysteresis LVTTL; $V_{DDD}$ > 2.7 V | 25 | 40 | – | mV | – |
| Vhyscmos | Input hysteresis CMOS | $0.05 \times V_{DDD}$ | – | – | mV | – |

**Table 8. GPIO AC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{RiseFast1}$ | Rise Time in Fast mode | 2 | – | 12 | ns | $V_{DDD}$ = 3.3 V/ 5.5 V, Cload = 25 pF |
| $T_{FallFast1}$ | Fall Time in Fast mode | 2 | – | 12 | ns | $V_{DDD}$ = 3.3 V/ 5.5 V, Cload = 25 pF |
| $T_{RiseSlow1}$ | Rise Time in Slow mode | 10 | – | 60 | ns | $V_{DDD}$ = 3.3 V/ 5.5 V, Cload = 25 pF |
| $T_{FallSlow1}$ | Fall Time in Slow mode | 10 | – | 60 | ns | $V_{DDD}$ = 3.3 V/ 5.5 V, Cload = 25 pF |
| $T_{RiseFast2}$ | Rise Time in Fast mode | 2 | – | 20 | ns | $V_{DDD}$ = 1.8 V, Cload = 25 pF |
| $T_{FallFast2}$ | Fall Time in Fast mode | 20 | – | 100 | ns | $V_{DDD}$ = 1.8 V, Cload = 25 pF |
| $T_{RiseSlow2}$ | Rise Time in Slow mode | 2 | – | 20 | ns | $V_{DDD}$ = 1.8 V, Cload = 25 pF |
| $T_{FallSlow2}$ | Fall Time in Slow mode | 20 | – | 100 | ns | $V_{DDD}$ = 1.8 V, Cload = 25 pF |

**Note**
2. $V_{IH}$ must not exceed $V_{DDD}$ + 0.2 V.

**nXRES**

**Table 9. nXRES DC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high threshold | $0.7 \times V_{DDD}$ | – | – | V | – |
| $V_{IL}$ | Input voltage low threshold | – | – | $0.3 \times V_{DDD}$ | V | – |
| Rpullup | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| $C_{IN}$ | Input capacitance | – | 5 | – | pF | – |
| Vhysxres | Input voltage hysteresis | – | 100 | – | mV | – |

**Table 10. nXRES AC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| Tresetwidth | Reset pulse width | 1 | – | – | µs | – |

## I²C Specifications

**Table 11. I²C AC Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{I2C}$ | I²C frequency | 1 | – | 400 | kHz | – |

## Flash Memory Specifications

**Table 12. Flash Memory Specifications**

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|
| Fend | Flash endurance | 100 K | – | – | cycles | – |
| Fret | Flash retention. $T_A \leq 85\ °C$, 10 K program/erase cycles | 10 | – | – | years | – |

## Pin Description

| Pin[3] | Type | Name | | Default |
|---|---|---|---|---|
| 1 | Power | VDDD | | VDDD Core |
| 2 | GPIO | GPIO_8 | GPIO IN | GPIO Input Pin (see Table 15) |
| 3 | GPIO | GPIO_9 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 4 | Power | VSSD | | Digital Ground |
| 5 | SCB/GPIO | SCL_1 | | SCB1 $I^2$C Clock |
| 6 | SCB/GPIO | SDA_1 | | SCB1 $I^2$C Data |
| 7 | GPIO | GPIO_12 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 8 | GPIO | GPIO_13 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 9 | GPIO | TX_RX LED_1 | | Notification LED for $I^2$C SCB1 Tx/RX |
| 10 | GPIO | TX_RX LED_0 | | Notification LED for $I^2$C SCB0 Tx/RX |
| 11 | Output | Suspend | | Asserted when the part enters Low Power mode |
| 12 | Input | Wakeup | | Wakeup device from suspend mode. Can be configured as active high/low using configuration utility |
| 13 | GPIO | GPIO_16 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 14 | USBIO | USBDP | | USB Data Signal Plus, integrates termination resistor and 1.5-kΩ pull up resistor |
| 15 | USBIO | USBDM | | USB Data Signal Minus, integrates termination resistor |
| 16 | Power | VCCD | | Regulated supply, connect to 1-µF cap or 1.8 V (Internal LDO Output) |
| 17 | Power | VSSD | | Digital Ground |
| 18 | Reset | nXRES | | Chip Reset active, low. Can be left unconnected or have a pull up resistor connected when not in use. |
| 19 | Power | VBUS | | USB VBUS |
| 20 | Power | VSSD (VBUS) | | Digital Ground |
| 21 | GPIO | GPIO_17 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 22 | GPIO | GPIO_18 | GPIO OUT | GPIO Out Pin (see Table 15) |
| 23 | Power | VDDD_IO | | VDDD for IO pins |
| 24 | Power | VSSA | | Analog Ground |
| 25 | GPIO | GPIO_0 | GPIO IN | GPIO Input Pin (see Table 15) |
| 26 | GPIO | GPIO_1 | GPIO IN | GPIO Input Pin (see Table 15) |
| 27 | GPIO | GPIO_2 | GPIO IN | GPIO Input Pin (see Table 15) |
| 28 | SCB/GPIO | SCL_0 | | SCB0 $I^2$C Clock |
| 29 | SCB/GPIO | SDA_0 | | SCB0 $I^2$C Data |
| 30 | GPIO | GPIO_5 | GPIO IN | GPIO Input Pin (see Table 15) |
| 31 | Output | POWER# | | Signal to external logic to indicate USB Unconfigured state and USB Suspend |
| 32 | GPIO | GPIO_7 | GPIO IN | GPIO Input Pin (see Table 15) |

**Note**
3. Any pin acting as an input pin should not be left unconnected.

**Figure 2. 32-Pin QFN Pinout**
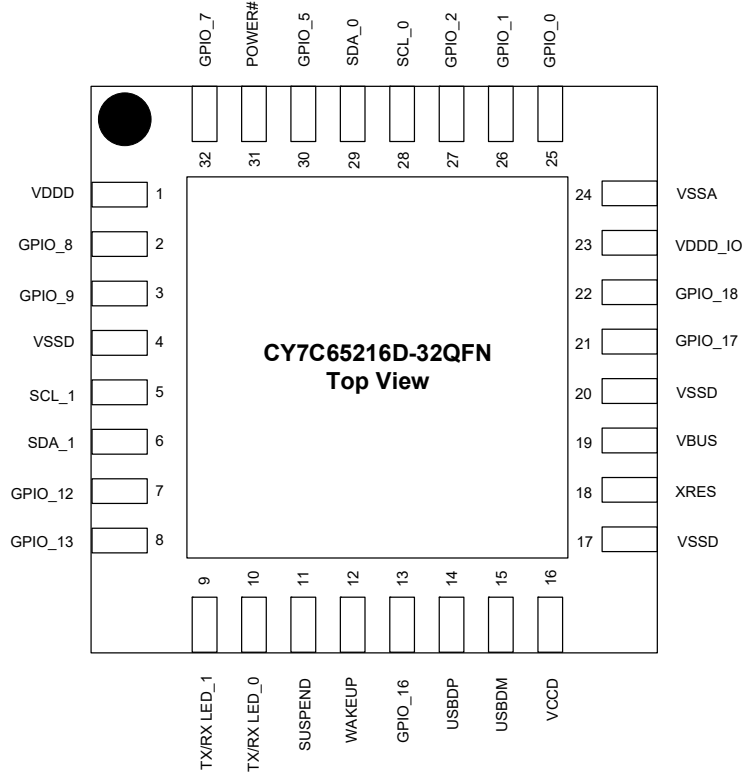
**Table 13. Serial Communication Block (SCB0) Configuration**

| Pin | Serial Port 0 | Mode 0[4] | Mode 1 |
|-----|---------------|-----------|--------|
| | | I$^2$C Master | I$^2$C Slave |
| 2 | SCB0_0 | GPIO_8 | GPIO_8 |
| 27 | SCB0_1 | GPIO_2 | GPIO_2 |
| 28 | SCB0_2 | SCL_OUT_0 | SCL_IN_0 |
| 29 | SCB0_3 | SDA_0 | SDA_0 |
| 30 | SCB0_4 | GPIO_5 | GPIO_5 |
| 3 | SCB0_5 | GPIO_9 | GPIO_9 |

**Table 14. Serial Communication Block (SCB1) Configuration**

| Pin | Serial Port 1 | Mode 0[4] | Mode 1 |
|-----|---------------|-----------|--------|
| | | I$^2$C Master | I$^2$C Slave |
| 5 | SCB1_0 | GPIO_8 | GPIO_8 |
| 6 | SCB1_1 | GPIO_2 | GPIO_2 |
| 7 | SCB1_2 | SCL_OUT_0 | SCL_IN_0 |
| 8 | SCB1_3 | SDA_0 | SDA_0 |
| 9 | SCB1_4 | GPIO_5 | GPIO_5 |
| 10 | SCB1_5 | GPIO_9 | GPIO_9 |

**Legend:**

| | |
|---|---|
| | GPIO |
| | SCB0 |
| | SCB1 |

**Note**
4. Device configured in Mode 0 as default. Other modes can be configured through Cypress-supplied configuration utility.

**Table 15.  GPIO Configuration**[5]

| GPIO Configuration Option | Description |
|---|---|
| TRISTATE | I/O tristated |
| DRIVE 1 | Output static 1 |
| DRIVE 0 | Output static 0 |
| POWER# | This output is used to control power to an external logic via switch to cut power off during uncon-figured USB device and USB suspend.<br>0 - USB device in Configured state<br>1 - USB device in Unconfigured state or during USB suspend mode |
| TXLED# | Drives LED during USB transmit |
| RXLED# | Drives LED during USB receive |
| TX or RX LED# | Drives LED during USB transmit or receive |
| BCD0<br>BCD1 | Configurable battery charger detect pins to indicate type of USB charger (SDP, CDP, or DCP)<br>Configuration example:<br>00 - Draw up to 100 mA (Unconfigured state)<br>01 - SDP (up to 500 mA)<br>10 - CDP/DCP (up to 1.5 A)<br>11 - Suspend (up to 2.5 mA)<br>This truth table can be configured using the configuration utility |
| BUSDETECT | VBUS detection. Connect VBUS to this pin via resistor network for VBUS detection when using BCD feature (see Figure 7). |

**Note**

5.  These signal options can be configured on any of the available GPIO pins using Cypress-supplied configuration utility.

## USB Power Configurations

The following section describes possible USB power configurations for the CY7C65216D. Refer to the Pin Description on page 14 for signal details.

### USB Bus-Powered Configuration

Figure 3 shows an example of the CY7C65216D in a bus-powered design. VBUS is connected directly to the CY7C65216D because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).

2. The system should not draw more than 2.5 mA during USB Suspend mode.

3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration, and 2.5 mA during USB Suspend state.

4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65216D flash should be updated to indicate bus power and the maximum current required by the system using the configuration utility.

**Figure 3.  Bus-Powered Configuration**
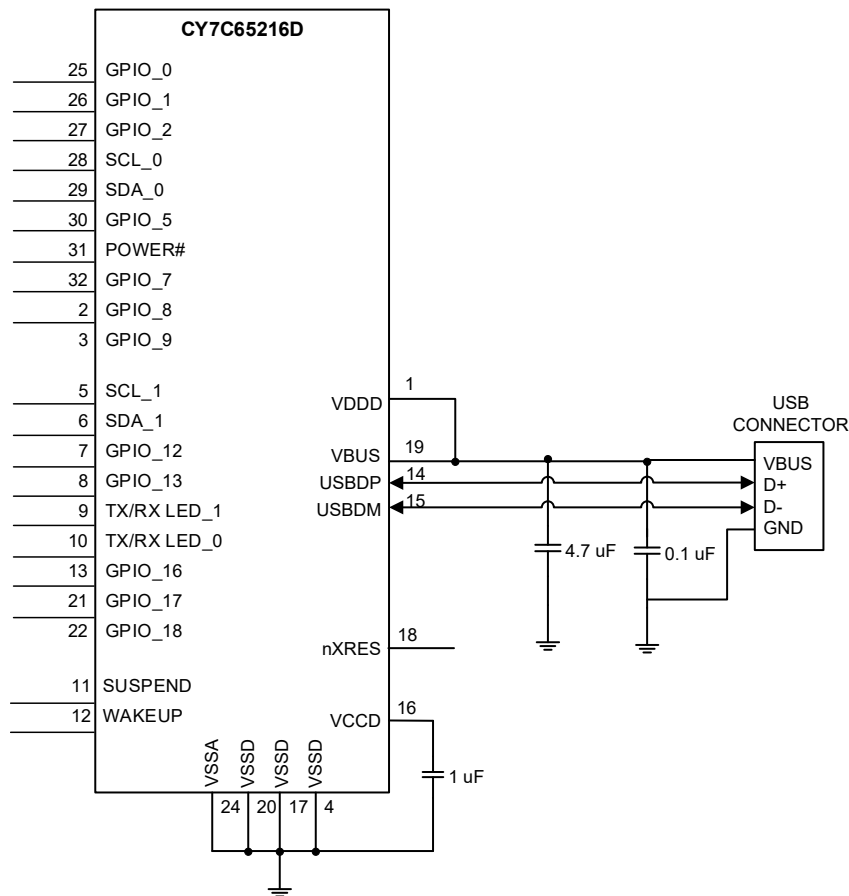
## Self-Powered Configuration

Figure 4 shows an example of CY7C65216D in a self-powered design.

In this configuration:

■ VBUS is powered from USB VBUS. VBUS pin is also used to detect USB connection.

■ VDDD is powered from an external power supply.

When VBUS is present, CY7C65216D enables an internal, 1.5-kΩ pull-up resistor on USBDP. When VBUS is absent (USB host is powered down), CY7C65216D removes the 1.5-kΩ pull-up resistor on USBDP, and this ensures no current flows from the USBDP to the USB host via a 1.5-kΩ pull-up resistor, to comply with USB 2.0 specification.

When reset is asserted to CY7C65216D, all the I/O pins are tristated.

Using the configuration utility, the configuration descriptor in the CY7C65216D flash should be updated to indicate that it is self-powered.

**Figure 4. Self-Powered Configuration**
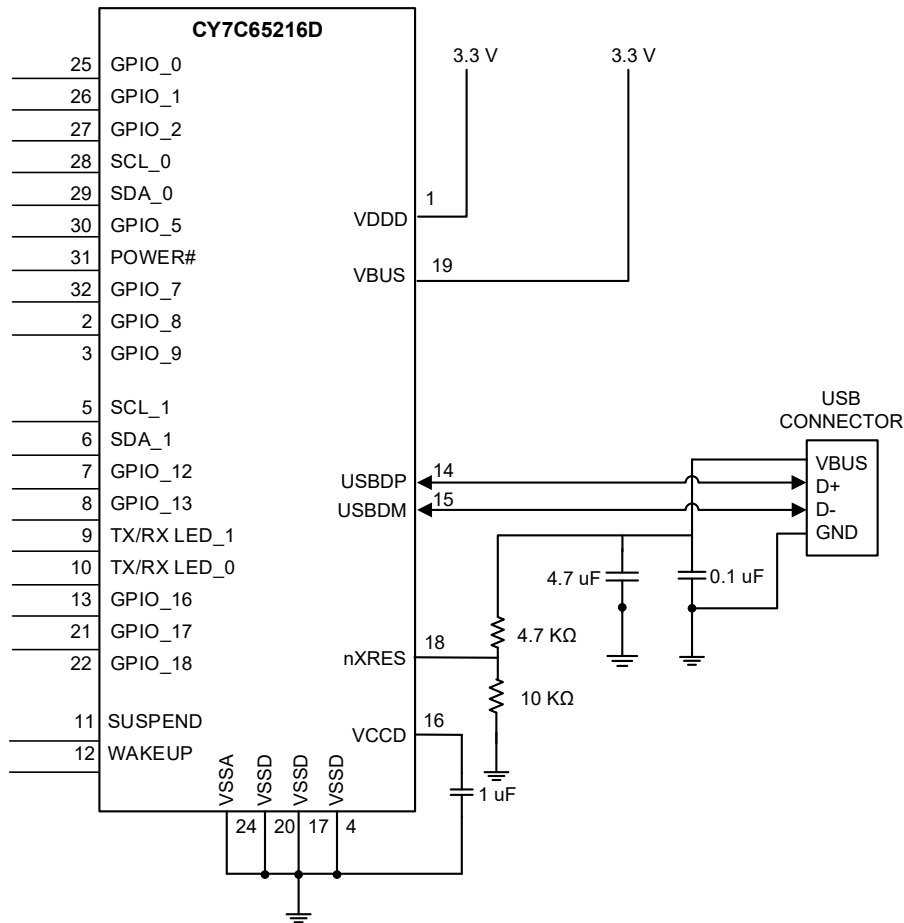
## USB Bus Powered with Variable I/O Voltage

Figure 5 shows CY7C65216D in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V (using a jumper switch) the input of which is 5 V from VBUS. Another jumper switch is used to select 1.8/3.3 V or 5 V from VBUS for the VDDD pin of CY7C65216D. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following:

- The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).

- The system should not draw more than 2.5 mA during USB Suspend mode.

- A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.

**Figure 5. USB Bus-Powered with 1.8 V, 3.3 V, or 5 V Variable I/O Voltage[6]**
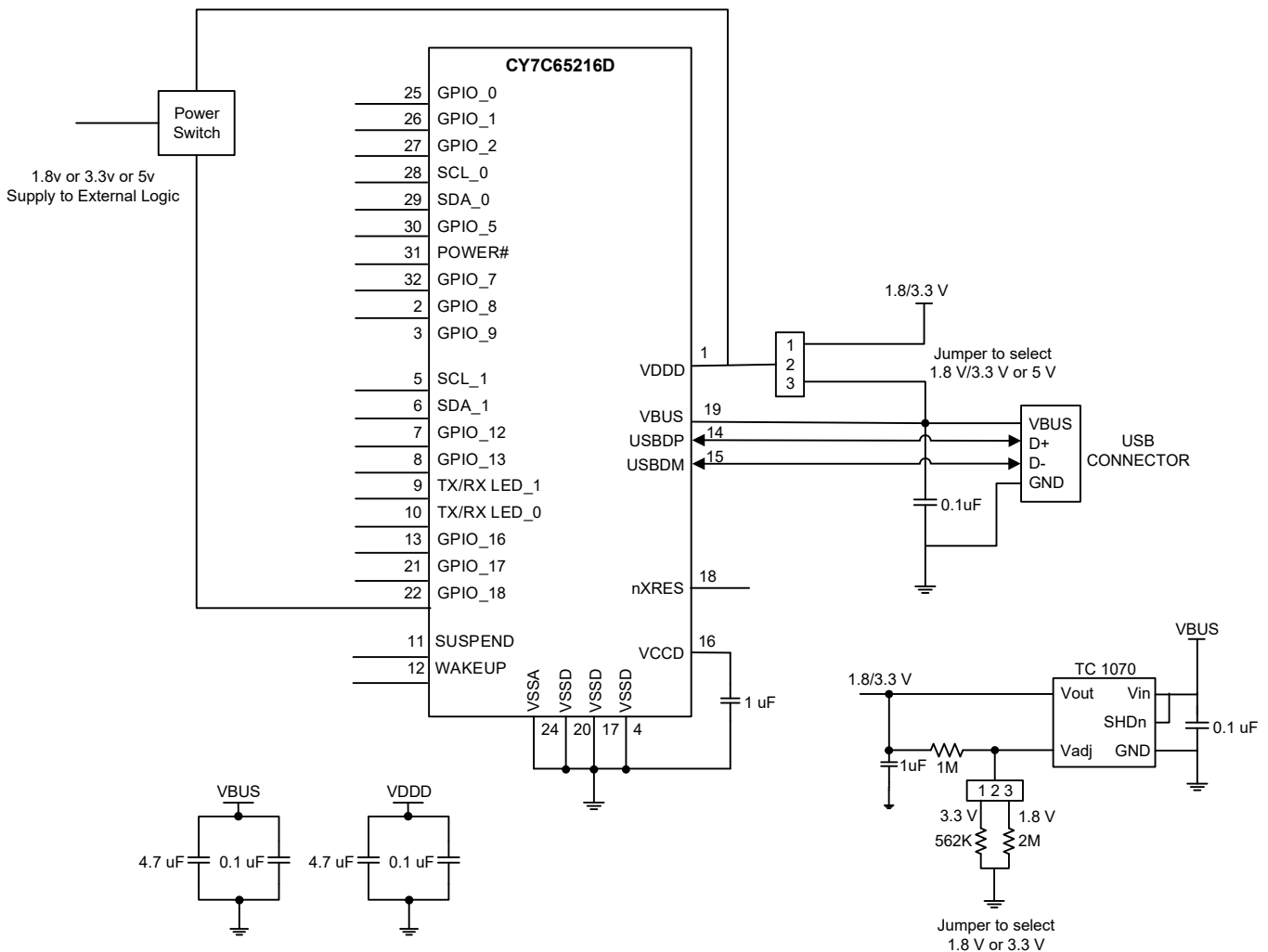


**Note**
6. 1.71 V ≤ VDDD ≤ 1.89 V - Short VCCD pin with VDDD pin; VDDD > 2 V - connect a 1-µF decoupling capacitor to the VCCD pin.

## Application Examples

The following section provides CY7C65216D application examples.

**Figure 6.  USB to Dual I²C Bridge with Battery Charge Detection**[7, 8]
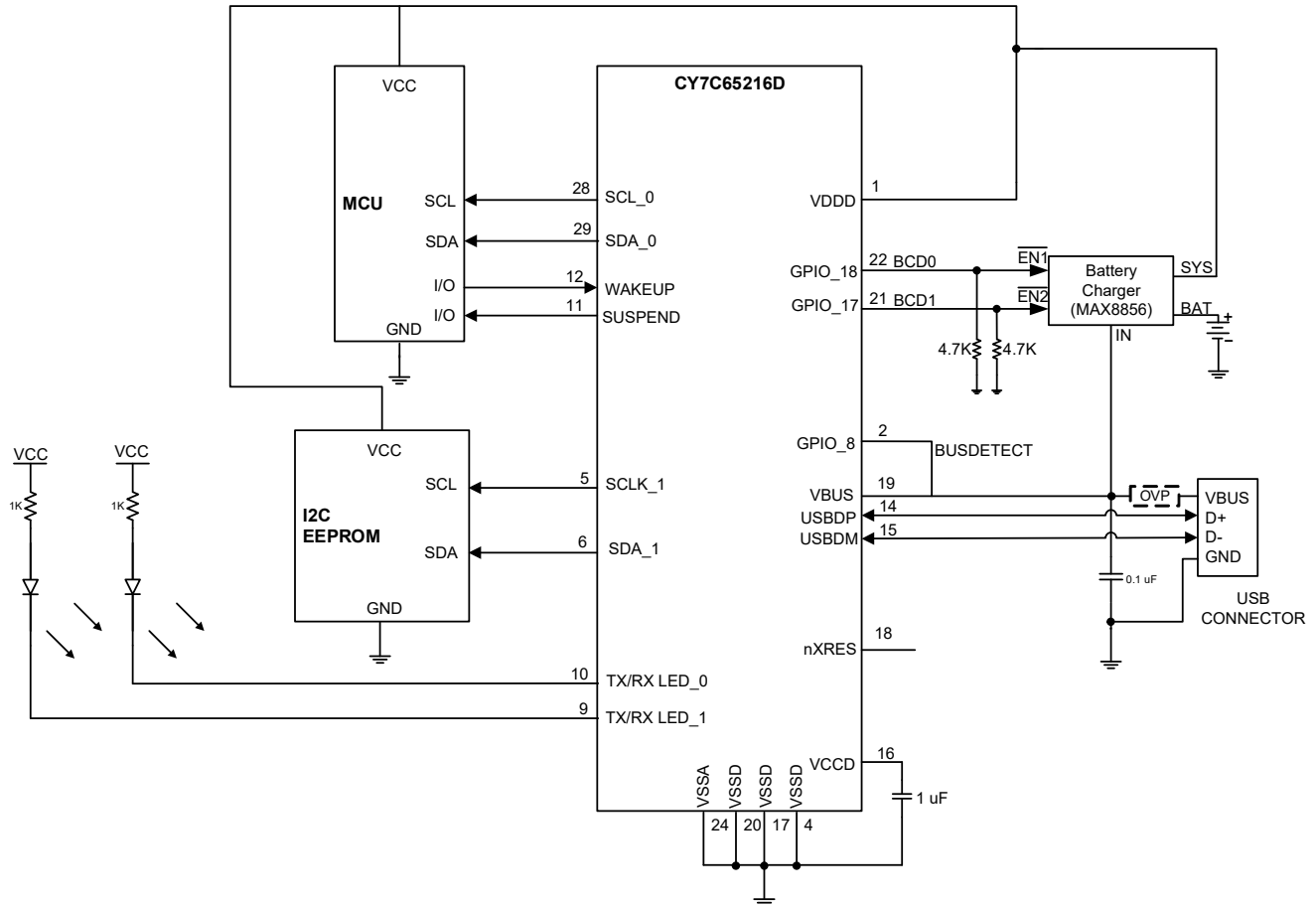


In a battery charger system.a 9-V spike on the VBUS is possible. The CY7C65216D VBUS pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of battery charger to the VBUS pin of CY7C65216D, as shown in Figure 7.

**Figure 7.  GPIO VBUS Detect (BUSDETECT)**
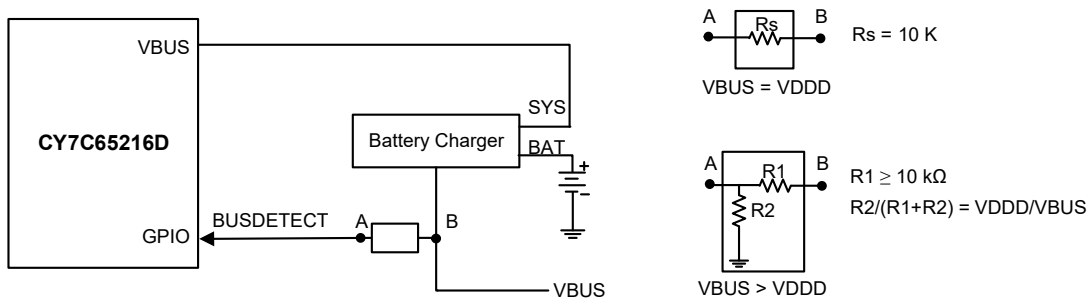


**Notes**
7.  Add a 100-kΩ pull-down resistor on the $V_{BUS}$ pin for quick discharge.
8.  Refer Figure 7, Figure 8, Figure 9 and the corresponding descriptions for handling VBUS Over Voltage Protection (OVP).

When VBUS and VDDD are at the same voltage potential, VBUS can be connected to GPIO using a series resistor (Rs). This is shown in Figure 8. If there is a charger failure and VBUS becomes 9 V, then the 10-kΩ resistor plays two roles. It reduces the amount of current flowing into the forward biased diodes in the GPIO, and it reduces the voltage seen on the pad.

**Figure 8.  GPIO VBUS Detection, VBUS = VDDD**
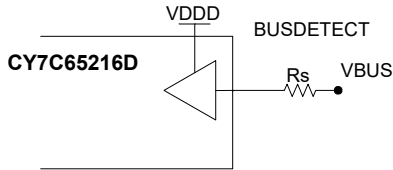


When VBUS > VDDD, a resistor voltage divider is necessary to reduce the voltage from VBUS down to VDDD for the GPIO sensing the VBUS voltage. This is shown in the following figure. The resistors should be sized as follows:

R1 $\geq$ 10 K

R2 / (R1 + R2) = VDDD / VBUS

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

**Figure 9.  GPIO VBUS Detection, VBUS > VDDD**
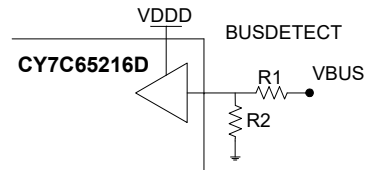
## USB to Dual Channel (I²C) Bridge

In Figure 10, CY7C65216D is configured as a USB-to-Dual Channel (I²C) Bridge. GPIO1 and GPIO0 are configured as RXLED# and TXLED# to drive two LEDs indicating data USB receive and transmit respectively.

**Figure 10.  USB-to-I²C Bridge**
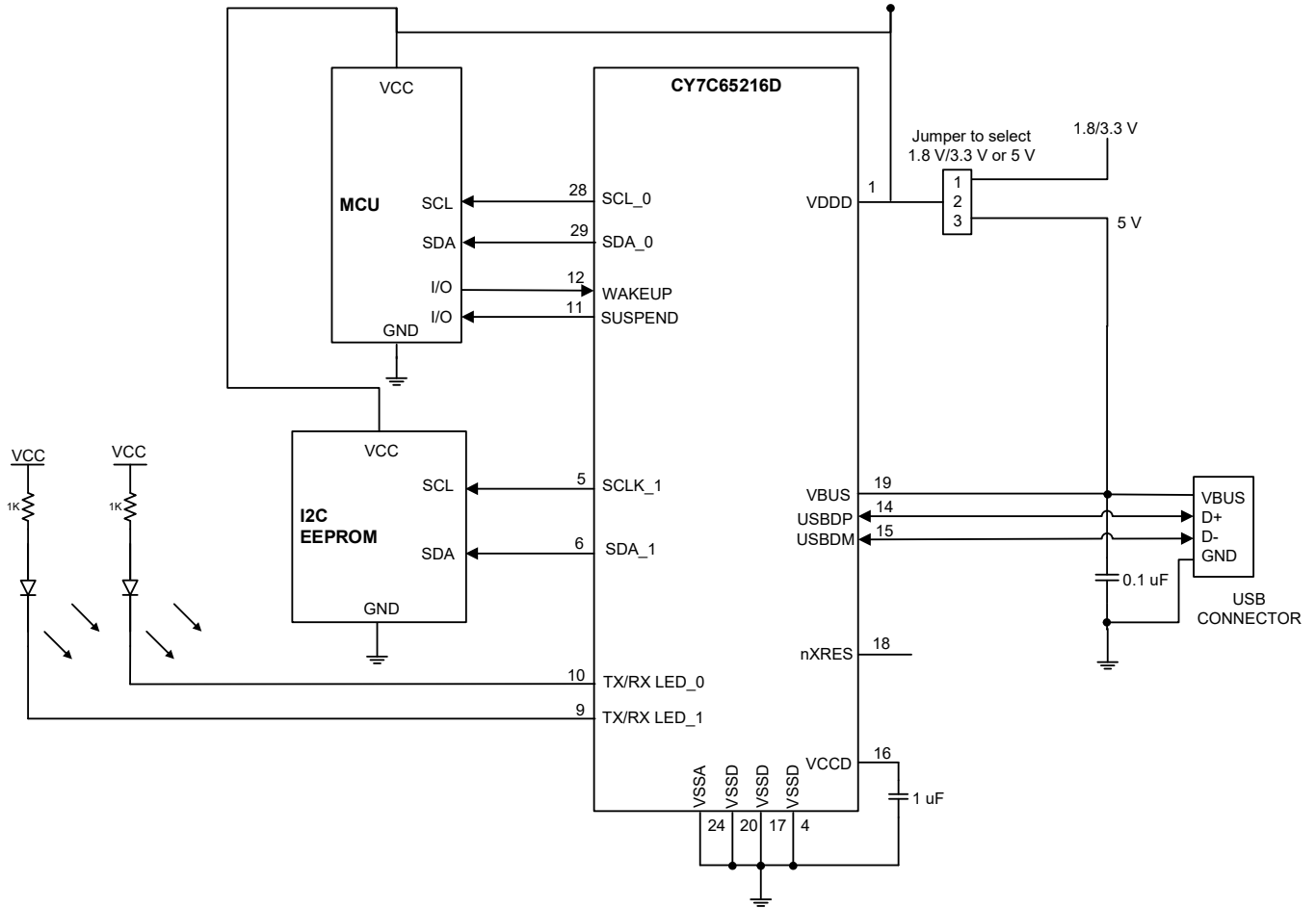


## I²C

The CY7C65216D I²C can be configured as a Master or Slave using the configuration utility. CY7C65216D supports I²C data rates up to 100 kbps in the standard mode (SM) and 400 kbps in the fast mode (FM).

In the master mode, SCL is output from CY7C65216D. In the slave mode, SCL is input to CY7C65216D. The I²C slave address for CY7C65216D can be configured using the configuration utility. The SDA data line is bi-directional in the master and slave modes. The drive modes of the SCL and SDA port pins are always open drain.

Refer to the NXP I²C specification for further details on protocol.

## Ordering Information

lists the CY7C65216D key package features and ordering codes. For more information, contact your local sales representative.

**Table 16.  Key Features and Ordering Information**

| Package | Ordering Code | Operating Range |
|---|---|---|
| 32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free) | CY7C65216D-32LTXI | Industrial |
| 32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel | CY7C65216D-32LTXIT | Industrial |

### Ordering Code Definitions

CY  7C65  XXXX  -  32  LTX  I  X

**X:** Blank or T
Blank = Tray; T= Tape and Reel

**Temperature Range:** I = Industrial; C = Commercial

**Package Type:** LT = QFN; X = Pb-free

**Number of Pins:** 32

**Part Number XXXX:**
216D: Single/Dual Channel USB-I$^2$C Bridge Controller

**Technology Code:** C = CMOS; Family Code: 65 = Full Speed USB-Serial

**Company ID:** CY = Cypress  (An Infineon Technologies Company)
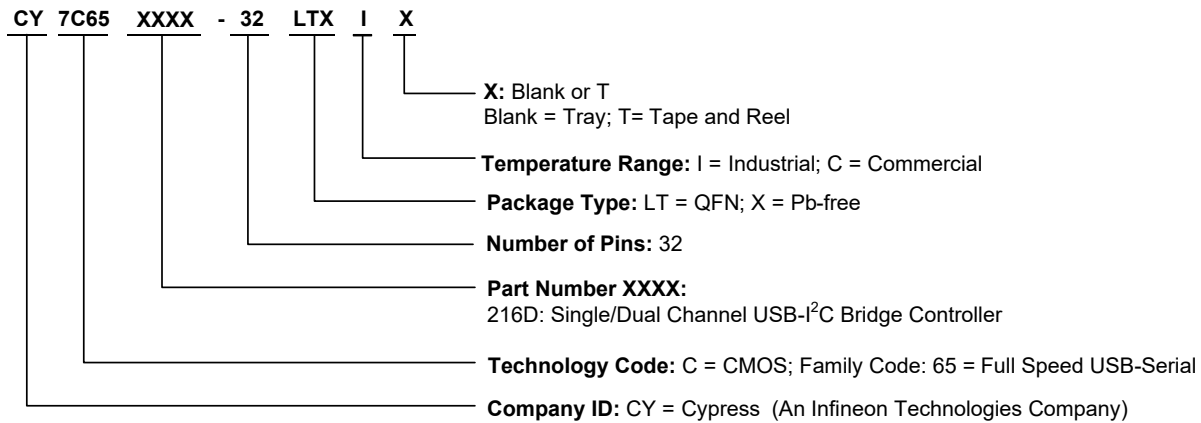
## Package Information

The package currently planned to be supported is the 32-pin QFN.

**Figure 11.  32-pin QFN 5 × 5 × 1.0 mm LT32B 3.5 × 3.5 EPAD (Sawn)**



TOP VIEW    SIDE VIEW    BOTTOM VIEW
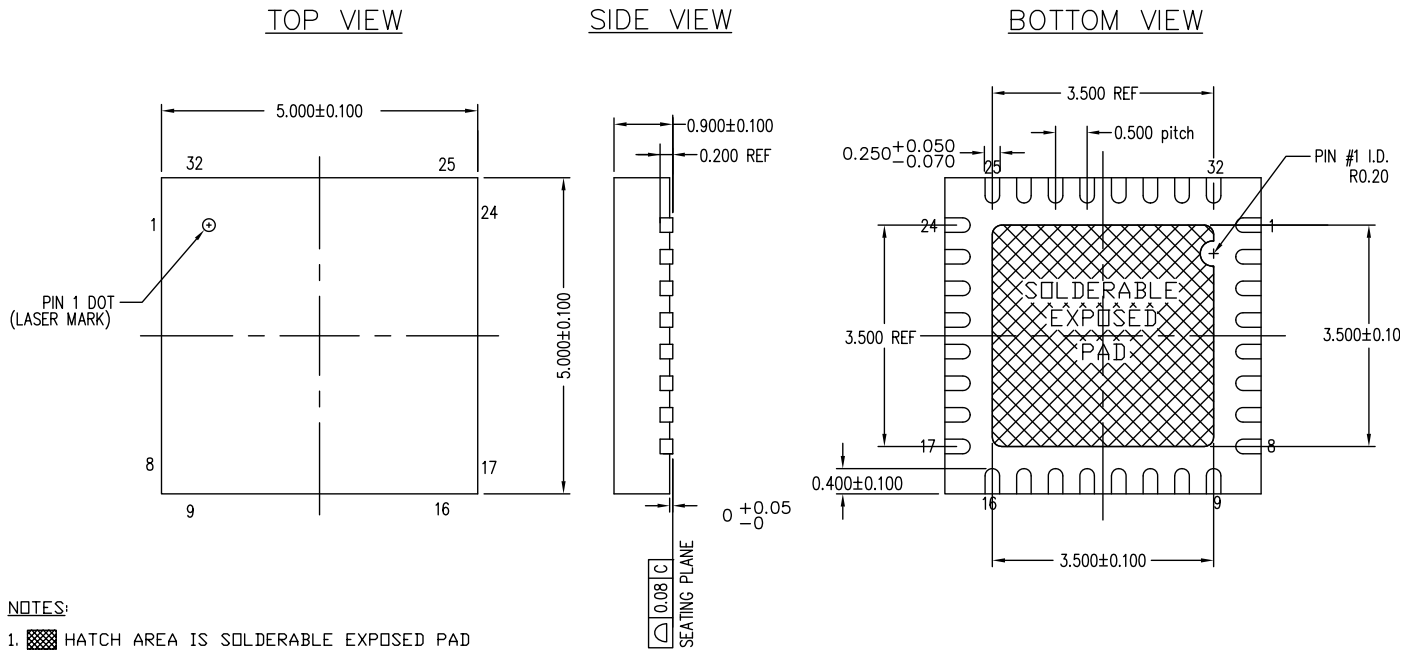
NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. DIMENSIONS ARE IN MILLIMETERS
4. PACKAGE WEIGHT: SEE CYPRESS PACKAGE MATERIAL DECLARATION
   DATASHEET (PMDD) POSTED ON THE CYPRESS WEB

001-30999 *D

**Table 17.  Package Characteristics**

| Parameter | Description | Min | Typ | Max | Units |
|-----------|-------------|-----|-----|-----|-------|
| $T_A$ | Operating ambient temperature | –40 | 25 | 85 | °C |
| THJ | Package $\theta_{JA}$ | – | 19 | – | °C/W |

**Table 18.  Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------|--------------------------|----------------------------------|
| 32-pin QFN | 260 °C | 30 seconds |

**Table 19.  Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---------|-----|
| 32-pin QFN | MSL 3 |

## Acronyms

**Table 20. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| BCD | battery charger detection |
| CDC | communication driver class |
| CDP | charging downstream port |
| DCP | dedicated charging port |
| DLL | dynamic link library |
| ESD | electrostatic discharge |
| GPIO | general purpose input/output |
| HBM | human-body model |
| I$^2$C | inter-integrated circuit |
| MCU | Microcontroller Unit |
| OSC | oscillator |
| PHDC | personal health care device class |
| PID | Product Identification |
| SCB | serial communication block |
| SCL | I$^2$C Serial Clock |
| SDA | I$^2$C Serial Data |
| SDP | Standard Downstream Port |
| SIE | serial interface engine |
| VCOM | virtual communication port |
| USB | Universal Serial Bus |
| VID | Vendor Identification |

## Document Conventions

### Units of Measure

**Table 21. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| DMIPS | dhrystone million instructions per second |
| kΩ | kilo-ohm |
| KB | kilobyte |
| kHz | kilohertz |
| kV | kilovolt |
| Mbps | megabits per second |
| MHz | megahertz |
| mm | millimeter |
| V | volt |

## Errata

This section describes the errata for the CY7C65216D USB-Serial family. Details include errata trigger conditions, scope of impact, and available workaround.

Contact your local Cypress Sales Representative if you have questions.

**Part Numbers Affected**

| Part Number | Device Characteristics |
|---|---|
| CY7C65216D | All Variants |

**Qualification Status**

Production

**Errata Summary**

The following table defines the errata applicability to available USB-Serial devices.

| Items | Affected Part Number | Fix Status |
|---|---|---|
| [1.] I2C Reads are slower when USB-Serial is configured as I2C Master. | CY7C65216D | Workaround Provided |

| **1. I$^2$C Reads are slower when USB-Serial is configured as I$^2$C Master.** | |
|---|---|
| Problem Definition | I$^2$C reads done by USB-Serial configured as I$^2$C Master are observed to be slower. This is because of significant delay between the I$^2$C read initiation and the reception of data from the I$^2$C Slave. |



| Parameters Affected | NA |
|---|---|
| **Trigger Condition(s)** | No specific trigger condition. The delay is observed between every I$^2$C Read initiation from the master and reception of slave data |
| **Scope of Impact** | I$^2$C read operations from the master are slower. |
| **Workaround** | KBA227320 mentions the steps needed to be taken for reducing this delay. |
| **Fix Status** | No fix. Workaround is proven. |

## Document History Page

| Document Title: CY7C65216D, USB-Dual I²C Bridge Controller<br>Document Number: 002-31605 | | | |
|---|---|---|---|
| **Revision** | **ECN** | **Submission Date** | **Description of Change** |
| ** | 6993251 | 11/25/2020 | Final datasheet to NSO. |

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