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The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY7C65223D

USB-Dual UART with Flow Control

Features

- USB 2.0 compliant, Full-Speed (12 Mbps)
  - Support for communication driver class (CDC), personal health care device class (PHDC), and vendor device class
  - Battery charger detection (BCD) compliant with USB Battery Charging Specification Rev 1.2 (Peripheral Detect only)
  - Integrated USB termination resistors
- Two-channel configurable UART interfaces
  - CY7C65223D supports 2-pin, 4-pin, 6-pin, and 8-pin UART interface
  - Data rates up to 3 Mbps
  - 190 bytes each transmit and receive buffer per channel
  - Data format:
    - 7 or 8 data bits
    - 1 or 2 stop bits
    - No parity, even, odd, mark, or space parity
  - Supports parity, overrun, and framing errors
  - Supports Software flow control and hardware flow control
  - Supports UART break signal
  - CY7C65223D supports RS232/RS422/RS485 interfaces
- General-purpose input/output (GPIO) pins: 4
- Supports unique serial number feature for each device, which fixes the COM port number permanently when USB-Serial Bridge controller as CDC device plugs in
- Configuration utility (Windows) to configure the following:
  - Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
  - UART
  - Charger detection
  - GPIO
- Driver support for VCOM and DLL
  - Windows 10: 32- and 64-bit versions
  - Windows 8.1: 32- and 64-bit versions
  - Windows 8: 32- and 64-bit versions
  - Windows 7: 32- and 64-bit versions
  - Windows Vista: 32- and 64-bit versions
  - Windows XP: 32- and 64-bit versions
  - Windows CE
  - Mac OS-X: 10.6, and later versions
  - Linux: Kernel version 2.6.35 onwards
- Clocking: Integrated 48-MHz clock oscillator
- Supports bus-/self-powered configurations
- USB suspend mode for low power
- Operating voltage: 1.71 to 5.5 V
- Operating temperature
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
- ESD protection: 2.2 kV HBM
- RoHS compliant package
  - 32-pin QFN (5 × 5 × 1 mm. 0.5 mm pitch)
- Ordering part number
  - CY7C65223D-32LTXI

Applications

- Medical/healthcare devices
- Point-of-Sale (POS) terminals
- Test and measurement system
- Gaming systems
- Set-top box PC-USB interface
- Industrial
- Networking
- Enabling USB connectivity in legacy peripherals

USB Compliant

The USB-Dual UART with Software Flow Control (CY7C65223D) is fully compliant with the USB2.0 Specification and Battery Charging Specification v1.2. USB- IF compliant.

Errata: For information on silicon errata, see "Errata" on page 28. Details include trigger conditions, devices affected, and proposed workaround.

USB Serial Bridge Controller Family

USB Serial bridge Controllers are a family of configurable products for most common applications requiring no firmware changes.

Configuration utility is provided to Configure USB-VID, USB-PID, USB Product and Manufacturer Descriptors. The same configuration utility can be used to configure UART, I²C, SPI, Battery Charger Detection, GPIOs, Power mode, and so on.

Figure 1. USB Serial Bridge Controller Family

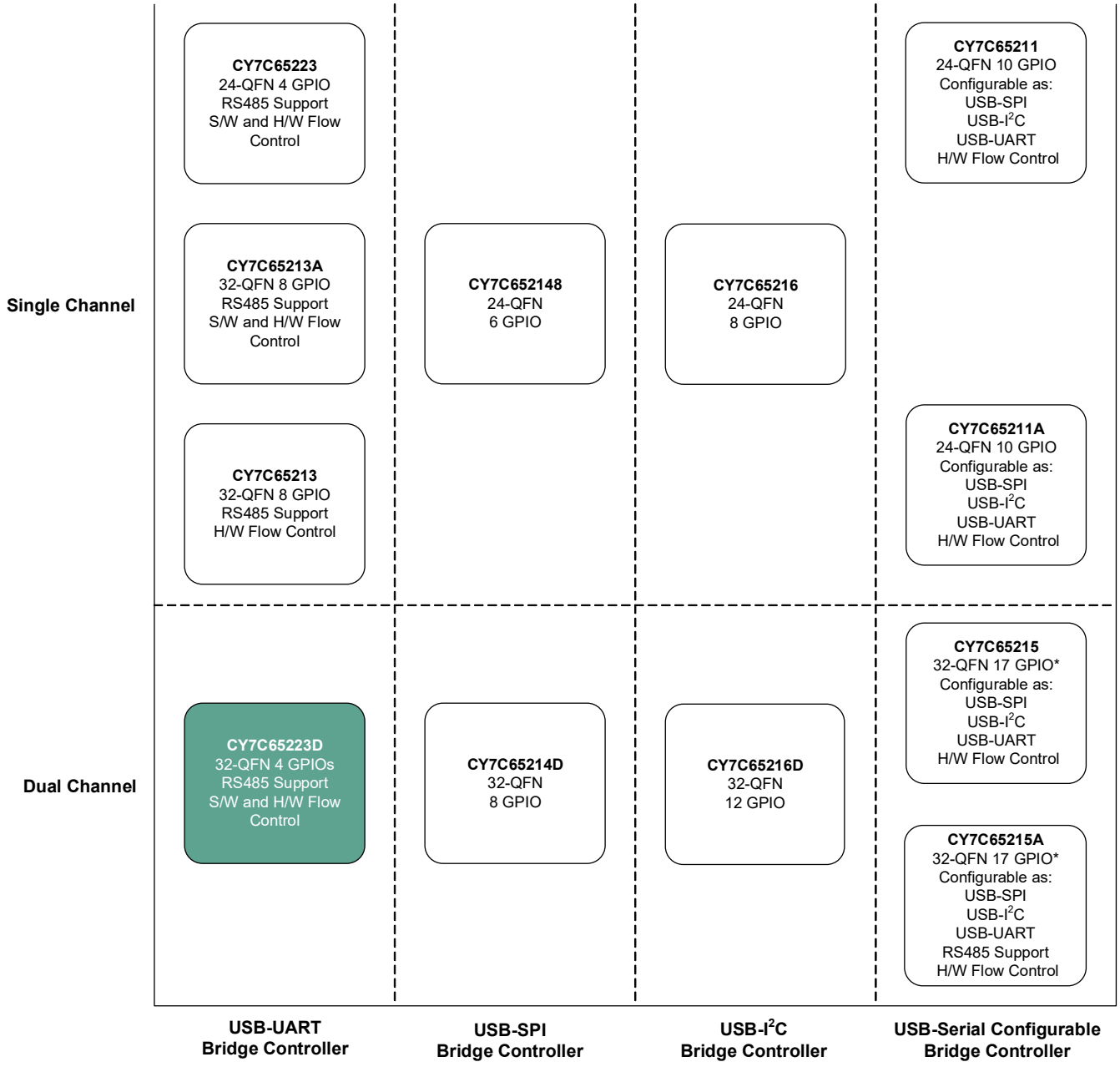


Table 1. USB Serial Family Feature Comparison

MPN	# of Channels	GPIO	USB-UART				USB-SPI		USB-I²C
			RS485 Support	Software Flow Control	Hardware Flow Control	UART Pins**	SPI Serial Data Width (bit)	SPI Master/ Slave	I²C Master/ Slave
CY7C65213	1	8	N	N	Y	8	–	–	–
CY7C65213A	1	8	Y	N	Y	8	–	–	–
CY7C65223	1	4	Y	Y	Y	2 / 4 / 6	–	–	–
CY7C65223D	**2**	**4**	**Y**	**Y**	**Y**	**2 / 4 / 6 / 8**	**–**	**–**	**–**
CY7C652148	1	6	–	–	–	–	4-16 bits	Master/Slave	–
CY7C65214D	2	8	–	–	–	–	4-16 bits	Master/Slave	–
CY7C65216	1	8	–	–	–	–	–	–	Master/Slave
CY7C65216D	2	12	–	–	–	–	–	–	Master/Slave
CY7C65211	1	10*	N	N	Y	2 / 4 / 6	4-16 bits	Master/Slave	Master/Slave
CY7C65211A	1	10*	Y	N	Y	2 / 4 / 6	4-16 bits	Master/Slave	Master/Slave
CY7C65215	2	17*	N	N	Y	2 / 4 / 6	4-16 bits	Master/Slave	Master/Slave
CY7C65215A	2	17*	Y	N	Y	2 / 4 / 6 / 8	4-16 bits	Master/Slave	Master/Slave

Legend

* Represents the total GPIO count offered by the part. This count can dynamically change based on UART / SPI / I²C pin configuration.
** UART Pins

**UART Pins	UART Signal
2	RxD and TxD
4	RxD, TxD, RTS#, CTS#
6	RxD, TxD, RTS#, CTS#, DTR#, DSR#
8	RxD, TxD, RTS#, CTS#, DTR#, DSR#, DCD#, RI#

Table 2. Default Serial Channel Configuration

MPN	# of Channels	GPIO	USB Protocol	USB- UART		USB-SPI	USB-I²C
				Is RS485 Enabled	UART Pins	SPI Master/ Slave	I²C Master/ Slave
CY7C65213	1	4	CDC**	N	8	–	–
CY7C65213A	1	4	CDC**	N	8	–	–
CY7C65223	1	4	CDC**	Y	4	–	–
CY7C65223D	**2**	**4**	**CDC****	**Y**	**4**	**–**	**–**
CY7C652148	1	6	Vendor***	–	–	Master	–
CY7C65214D	2	8	Vendor***	–	–	Master	–
CY7C65216	1	8	Vendor***	–	–	–	Slave
CY7C65216D	2	12	Vendor***	–	–	–	Master
CY7C65211	1	3	CDC**	N	6	–	–
CY7C65211A	1	3	CDC**	N	6	–	–
CY7C65215	2	4	CDC**	N	6	–	–
CY7C65215A	2	4	CDC**	N	6	–	–

** USB CDC Protocol allows the USB host Operating System to detect the device as Virtual COM Port Device.
*** USB Vendor Protocol allows the USB host operating system to detect the device as general USB device. This device is accessible using Cypress Application Library.

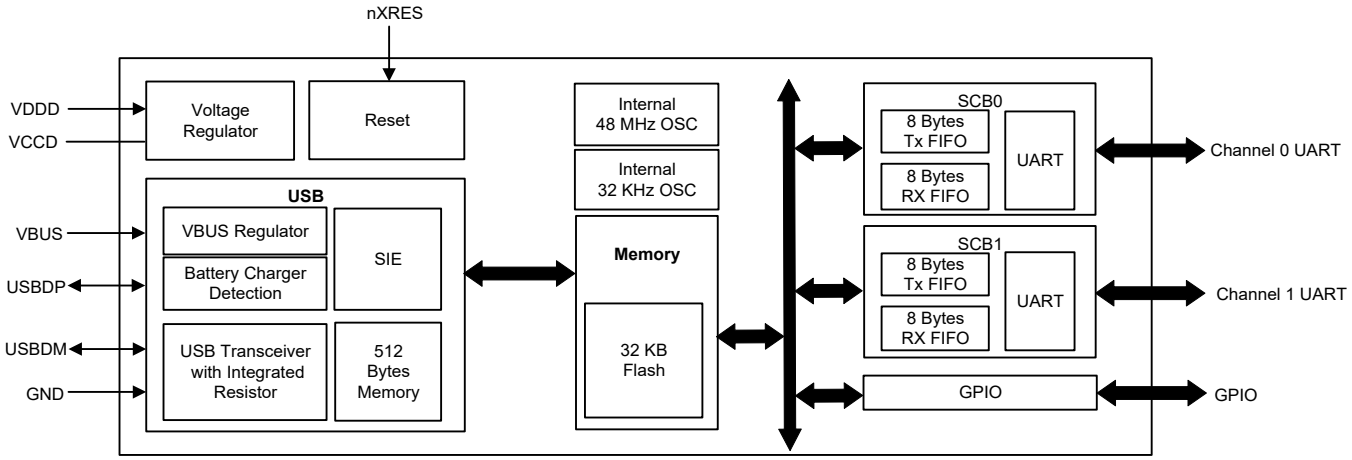
More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the document USB-Serial Bridge Controller Product Overview.

- Overview: USB Portfolio, USB Roadmap
- USB 2.0 Product Selectors: USB-Serial Bridge Controller, USB to UART Controller (Gen I)
- Knowledge Base Articles: Cypress offers a large number of USB knowledge base articles covering a broad range of topics, from basic to advanced level. Recommended knowledge base articles for getting started with USB-Serial Bridge Controller are:
  - KBA85909 – Key Features of the Cypress® USB-Serial Bridge Controller
  - KBA85920 – USB-UART and USB-Serial
  - KBA85921 – Replacing FT232R with CY7C65213 USB-UART LP Bridge Controller
  - KBA85913 – Voltage supply range for USB-Serial
  - KBA89355 – USB-Serial: Cypress Default VID and PID
  - KBA92641 – USB-Serial Bridge Controller Managing I/Os using API
  - KBA92442 – Non-Standard Baud Rates in USB-Serial Bridge Controllers
  - KBA91366 – Binding a USB-Serial Device to a Microsoft® CDC Driver
  - KBA92551 – Testing a USB-Serial Bridge Controller Configured as USB-UART with Linux®
  - KBA91299 – Interfacing an External I^2C Device with the CYUSBS234/236 DVK

  For a complete list of knowledge base articles, click here.
- Code Examples: USB Full-Speed
- Development Kits:
  - CYUSBS232, Cypress USB-UART LP Reference Design Kit
  - CYUSBS234, Cypress USB-Serial (Single Channel) Development Kit
  - CYUSBS236, Cypress USB-Serial (Dual Channel) Development Kit
- Models: IBIS

Block Diagram



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Functional Overview

The CY7C65223D is a Full-Speed USB controller that enables seamless PC connectivity for peripherals with dual-channel interface. CY7C65223D also integrates BCD, which is compliant with the USB Battery Charging Specification Rev. 1.2. It integrates a voltage regulator, oscillator, and flash memory for storing configuration parameters, offering a cost-effective solution. CY7C65223D supports bus-powered and self-powered modes, and enables efficient system power management with suspend and remote wake-up signals. It is available in a 32-pin QFN package.

USB and Charger Detect

USB

CY7C65223D has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates the internal USB series termination resistors on the USB data lines and a 1.5-kΩ pull-up resistor on USBDP.

Charger Detection

CY7C65223D supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification Rev. 1.2. It supports the following charging ports:

- Standard Downstream Port (SDP): allows the system to draw up to 500 mA current from the host
- Charging Downstream Port (CDP): allows the system to draw up to 1.5 A current from the host
- Dedicated Charging Port (DCP): allows the system to draw up to 1.5 A of current from the wall charger

Serial Communication

CY7C65223D has two serial communication blocks (SCBs) implementing UART interface. A 256-byte buffer is available in both the TX and RX lines.

Table 3 shows maximum speed supported on both SCBs when they are configured as UART.

Table 3. Maximum Speed supported on both SCBs

No.	Configuration	SCB0 Maximum Speed	SCB1 Maximum Speed
1	SCB0 = UART, SCB1 = Disabled	3M (TX/RX) with Flow Control	NA
2	SCB0 = UART, SCB1 = UART	1M (TX/RX) with Flow Control	1M (TX/RX) with Flow Control

UART Interface

The UART interface provides asynchronous serial communication with other UART devices operating at speeds of up to 3 Mbps. It supports 7 to 8 data bits, 1 to 2 stop bits, odd, even, mark, space, and no parity. The UART interface supports full duplex communication with a signaling format that is compatible with the standard UART protocol. In CY7C65223D, these UART pins may be interfaced to RS232/RS422/RS485.

CY7C65223D supports common UART functions such as parity error and frame error. In addition, CY7C65223D supports baud rates ranging from 300 baud to 3 Mbaud. UART baud rates can be set using the configuration utility.

Notes

- Parity error gets detected when UART transmitter device is configured for odd parity and UART receiver device is configured for even parity.
- Frame error gets detected when UART transmitter device is configured for 7 bits data width and 1 stop bit, whereas UART receiver device is configured for 8 bit data width and 2 stop bits.

UART Flow Control

UART Data Flow control is the process of signaling the UART partner device to WAIT or RESUME the data transmission. This flow control process is required for the slower device to catch up with the partner device without data loss. The CY7C65223D device supports both UART hardware and software flow control.

By default, flow control is disabled. USB host UART terminal applications can enable or disable either hardware or software flow control through operating system software interfaces.

Hardware flow control uses signal pairs such as RTS# (Request to Send) / CTS# (Clear to Send) to control the data flow between partner UART devices.

Software flow control do not use additional hardware signaling pairs. But, software flow control uses in-band communication using special characters called XON or XOFF. These XON or XOFF characters are exchanged at UART PHY level for data flow control. These XON or XOFF characters doesn't reflect in the actual data received by the USB host application.default. Flow control can be disabled using the configuration utility. Default configuration will not have flow control enabled.

The following section describes the flow control signals:

- CTS# (Input) / RTS# (Output)

CTS# can pause or resume data transmission over the UART interface. Data transmission can be paused by de-asserting the CTS signal and resumed with CTS# assertion. The pause and resume operation does not affect data integrity. With flow control enabled, receive buffer has a watermark level of 93%. After the data in the receive buffer reaches that level, the RTS# signal is de-asserted, instructing the transmitting device to stop data transmission. The start of data consumption by the application reduces device data backlog. When it reaches the 75% watermark level, the RTS# signal is asserted to resume data reception.

- DSR# (Input) /DTR# (Output)

DSR#/DTR# signals are used to establish the communication link with the UART. These signals complement each other in their functionality, similar to CTS# and RTS#.

GPIO Interface

CY7C65223D has four GPIOs. The configuration utility allows configuration of the GPIO pins. The configurable options are as follows:

- GPIO can be tristated through Config Utility
- DRIVE 1: Output static 1
- DRIVE 0: Output static 0
- POWER#: Power control for bus power designs
- TXLED#: Drives LED during USB transmit
- RXLED#: Drives LED during USB receive
- TX or RX LED#: Drives LED during USB transmit or receive

  GPIO can be configured to drive LED at 8-mA drive strength.
- BCD0/BCD1: Two-pin output to indicate the type of USB charger
- BUSDETECT: Connects VBUS pin for USB host detection

Default Configuration

CY7C65223D is configured as Dual 4-Pin UART Device.

Memory

CY7C65223D has a 512-byte flash. The flash is used to store the USB parameters such as VID/PID, serial number, Product, and Manufacturer Descriptors, which can be programmed by the configuration utility.

System Resources

Power System

CY7C65223D supports the USB Suspend mode to control power usage. CY7C65223D operates in bus-powered or self-powered modes over a range of 3.15 to 5.5 V.

Clock System

CY7C65223D has a fully integrated clock and does not require any external components. The clock system is responsible for providing clocks to all subsystems.

Internal 48-MHz Oscillator

The internal 48-MHz oscillator is the primary source of internal clocking in CY7C65223D.

Internal 32-kHz Oscillator

The internal 32-kHz oscillator is primarily used to generate clocks for peripheral operation in the USB Suspend mode.

Reset

The reset block ensures reliable power-on reset and brings the device back to the default known state. The nXRES (active low) pin can be used by external devices to reset the CY7C65223D.

Suspend and Resume

The CY7C65223D device asserts the SUSPEND pin when the USB bus enters the suspend state. This helps in meeting the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus-powered mode. The device will resume from the suspend state under any of the following conditions:

1. Any activity is detected on the USB bus
2. The WAKEUP pin is asserted to generate remote wakeup to the host

WAKEUP

The WAKEUP pin is used to generate a remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65223D device allows enabling/disabling and polarity of the remote wakeup feature through the configuration utility.

Software

Cypress delivers a complete set of software drivers and the configuration utility to enable product configuration during system development.

Drivers for Linux Operating Systems

Cypress provides a User Mode USB driver library (*libcyusb-serial.so*) that abstracts vendor commands for the UART interface and provides a simplified API interface to the user applications. This library makes use of the standard open source libUSB library to enable the USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux ‘udev’ mechanism.

CY7C65223D supports the standard USB CDC UART class driver, which is bundled with the Linux kernel.

Drivers for Mac OSx

Cypress delivers a dynamically linked shared library (CyUSBSerial.dylib) based on libUSB, which enables communication to the CY7C65223D device.

Drivers for Windows Operating Systems

For Windows operating systems (XP, Vista, Win7, Win8, Win8.1, and Win10), Cypress delivers a User Mode dynamically linked library–CyUSBSerial DLL–that abstracts vendor-specific interface of CY7C65223D devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific UART/SPI/I^2C and class-specific APIs for PHDC.

USB-Serial Bridge Controller works with the Windows-standard USB CDC class driver, when either CY7C65223D is configured as CDC USB to UART device. A virtual COM port driver–CyUSB-Serial.sys–is also delivered, which implements the USB CDC class driver. The Cypress Windows drivers are Windows hardware certification kit-compliant.

These drivers are bound to device through WU (Windows Update) services.

Cypress drivers also support Windows plug-and-play and power management and USB Remote Wake-up.

Windows-CE Support

The CY7C65223D solution includes a CDC UART driver library for Windows-CE platforms.

Device Configuration Utility (Windows Only)

A Windows-based configuration utility is available to configure various device initialization parameters. This graphical user application provides an interactive interface to define the various boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configuration from text or xml formats.

The configuration utility allows the following operations:

- View current device configuration
- Configure USB VID, PID, and string descriptors
- Save or Load configuration

You can download the free configuration utility and drivers from www.cypress.com.

Internal Flash Configuration

The internal flash memory can be used to store the configuration parameters shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application specific requirements over USB interface. The configuration utility can be downloaded from www.cypress.com/usbserial.

Table 4. Internal Flash Configuration for CY7C65223D

Parameter	Default Value	Description
USB Configuration		
USB Vendor ID (VID)	0x04B4	Default Cypress VID. Can be configured to customer VID
USB Product ID (PID)	0x0005	Default Cypress PID. Can be configured to customer PID
Manufacturer string	Cypress	Can be configured with any string up to 64 characters
Product string	USB-Serial (Dual Channel)	Can be configured with any string up to 64 characters
Serial string	–	Can be configured with any string up to 64 characters
Power mode	Bus powered	Can be configured to bus-powered or self-powered mode
Max current draw	100 mA	Can be configured to any value from 0 to 500 mA. Based on this, the configuration descriptor will be updated.
Remote wakeup	Enabled	Can be disabled. Remote wakeup is initiated by asserting WAKEUP pin
USB interface protocol	CDC	Can be configured to function in CDC, PHDC, or Cypress vendor class
BCD	Disabled	Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD.

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings[1] may shorten the useful life of the device.

Storage temperature .... –55 °C to +100 °C

Ambient temperature with power supplied (Industrial) .... –40 °C to +85 °C

Supply voltage to ground potential

V_{DDD} ..... 6.0 V

V_{BUS} ..... 6.0 V

V_{CCD} ....1.95 V

V_{GPIO} ....V_{DDD} + 0.5 V

Static discharge voltage ESD protection levels:

■ 2.2-kV HBM per JESD22-A114

Latch-up current ..... 140 mA

Current per GPIO ..... 25 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

V_{BUS} supply voltage ..... 3.15 V to 5.25 V

V_{DDD} supply voltage ..... 1.71 V to 5.50 V

V_{CCD} supply voltage ..... 1.71 V to 1.89 V

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 5. DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{BUS}	V_{BUS} supply voltage	3.15	3.30	3.45	V	Set and configure correct voltage range using the configuration utility for V_{BUS}.
		4.35	5.00	5.25	V	
V_{DDD}	V_{DDD} supply voltage	1.71	1.80	1.89	V	Used to set I/O and core voltage. Set and configure correct voltage range using the configuration utility for V_{DDD}.
		2.0	3.3	5.5	V	
V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	Do not use this supply to drive external device. • 1.71 V ≤ V_{DDD} ≤ 1.89 V: Short the V_{CCD} pin with the V_{DDD} pin • V_{DDD} > 2 V – connect a 1-µF capacitor (Cefc) between the V_{CCD} pin and ground
Cefc	External regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better
I_{DD1}	Operating supply current	–	13	18	mA	USB 2.0 FS, UART at 1 Mbps single channel, no GPIO switching at V_{BUS} = 5 V, V_{DDD} = 5 V
I_{DD2}	USB Suspend supply current	–	5	–	µA	Does not include current through a pull-up resistor on USBDP. In USB suspend mode, the D+ voltage can go up to a maximum of 3.8 V.

Table 6. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Zout	USB driver output impedance	28	–	44	Ω	–
Twakeup	Wakeup from USB Suspend mode	–	25	–	µs	–

Note

1. Usage above the absolute maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions the device may not operate to specification.

GPIO

Table 7. GPIO DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
V_{IH}[2]	LVTTL input, V_{DDD}< 2.7 V	0.7 × V_{DDD}	–	–	V	–
V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	–
V_{IH}[2]	LVTTL input, V_{DDD} ≥ 2.7 V	2	–	–	V	–
V_{IL}	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8	V	–
V_{OH}	CMOS output voltage high level	V_{DDD} – 0.4	–	–	V	I_{OH} = 4 mA, V_{DDD} = 5 V ± 10%
V_{OH}	CMOS output voltage high level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA, V_{DDD} = 3.3 V ± 10%
V_{OH}	CMOS output voltage high level	V_{DDD} – 0.5	–	–	V	I_{OH} = 1 mA, V_{DDD} = 1.8 V ± 5%
V_{OL}	CMOS output voltage low level	–	–	0.4	V	I_{OL} = 8 mA, V_{DDD} = 5 V ± 10%
V_{OL}	CMOS output voltage low level	–	–	0.6	V	I_{OL} = 8 mA, V_{DDD} = 3.3 V ± 10%
V_{OL}	CMOS output voltage low level	–	–	0.6	V	I_{OL} = 4 mA, V_{DDD} = 1.8 V ± 5%
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	–
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
C_{IN}	Input capacitance	–	–	7	pF	–
Vhysttl	Input hysteresis LVTTL; V_{DDD} > 2.7 V	25	40	–	mV	–
Vhyscmos	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	–

Table 8. GPIO AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RiseFast1}$	Rise Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallFast1}$	Fall Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseSlow1}$	Rise Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallSlow1}$	Fall Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseFast2}$	Rise Time in Fast mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallFast2}$	Fall Time in Fast mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{RiseSlow2}$	Rise Time in Slow mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallSlow2}$	Fall Time in Slow mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

nXRES

Table 9. nXRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	–
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	–
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	–
C_{IN}	Input capacitance	–	5	–	pF	–
Vhysxres	Input voltage hysteresis	–	100	–	mV	–

Table 10. nXRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Tresetwidth	Reset pulse width	1	–	–	µs	–

Table 11. UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	UART bit rate	0.3	–	3000	kbps	Single SCB: TX + RX Dual SCB: TX or RX

Flash Memory Specifications

Table 12. Flash Memory Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fend	Flash endurance	100 K	–	–	cycles	–
Fret	Flash retention. $T_A \leq 85$ °C, 10 K program/erase cycles	10	–	–	years	–

Pin Description

Pin[3]	Type	Name	Default	Description
1	Power	VDDD		Supply to the device core and Interface, 1.71 to 5.5 V
2	SCB0	RxD_0		UART Rx SCB0
3	SCB/GPIO	DTR#_0/GPIO_9	GPIO Input Pin	GPIO IN (see Table 15)
4	Power	VSSD		Digital Ground
5	SCB1	RxD_1		UART Rx SCB1
6	SCB1	TxD_1		UART Tx SCB1
7	SCB/GPIO	RTS#_1		UART RTS SCB1 Hardware Flow Control Signal
8	SCB/GPIO	CTS#_1		UART CTS SCB1 Hardware Flow Control Signal
9	SCB/GPIO	TXLED_1		Notification LED for UART SCB1 Tx
10	SCB/GPIO	RXLED_1		Notification LED for UART SCB1 Rx
11	Output	Suspend		Indicates device in suspend mode. Can be configured as active high/low using configuration utility
12	Input	Wakeup		Wakeup device from suspend mode. Can be configured as active high/low using configuration utility
13	GPIO	TxEN_1		SCB1 UART RS485 Transmitter Enable
14	USBIO	USBDP		USB Data Signal Plus, integrates termination resistor and 1.5-kΩ pull up resistor
15	USBIO	USBDM		USB Data Signal Minus, integrates termination resistor
16	Power	VCCD		Regulated supply, connect to 1-µF cap or 1.8 V (Internal LDO Output)
17	Power	VSSD		Digital Ground
18	Reset	nXRES		Chip Reset active, low. Can be left unconnected or have a pull up resistor connected when not in use.
19	Power	VBUS		VBUS Supply, 3.15 V to 5.25 V
20	Power	VSSD (VBUS)		Digital Ground
21	GPIO	GPIO_17	GPIO Output Pin	GPIO OUT (see Table 15)
22	GPIO	GPIO_18	GPIO Output Pin	GPIO OUT (see Table 15)
23	Power	VDDD_IO		Supply to the device core and Interface, 1.71 to 5.5 V
24	Power	VSSA		Analog Ground
25	GPIO	TXLED_0		Notification LED for SCB0 UART Tx (see Table 15)
26	GPIO	RXLED_0		Notification LED for SCB0 UART Rx (see Table 15)
27	SCB/GPIO	GPIO_2	GPIO Input Pin	GPIO IN (see Table 15)
28	SCB/GPIO	RTS#_0		SCB0 UART Hardware Flow Control
29	SCB/GPIO	CTS#_0		SCB0 UART Hardware Flow Control
30	SCB0	TxD_0		SCB0 UART Tx
31	Output	POWER#		Signal to external logic to indicate USB Unconfigured state and USB Suspend
32	GPIO	TxEN_0		SCB0 UART RS485 Transmit Enable

Note
3. Any pin acting as an input pin should not be left unconnected.

Figure 2. 32-Pin QFN Pinout

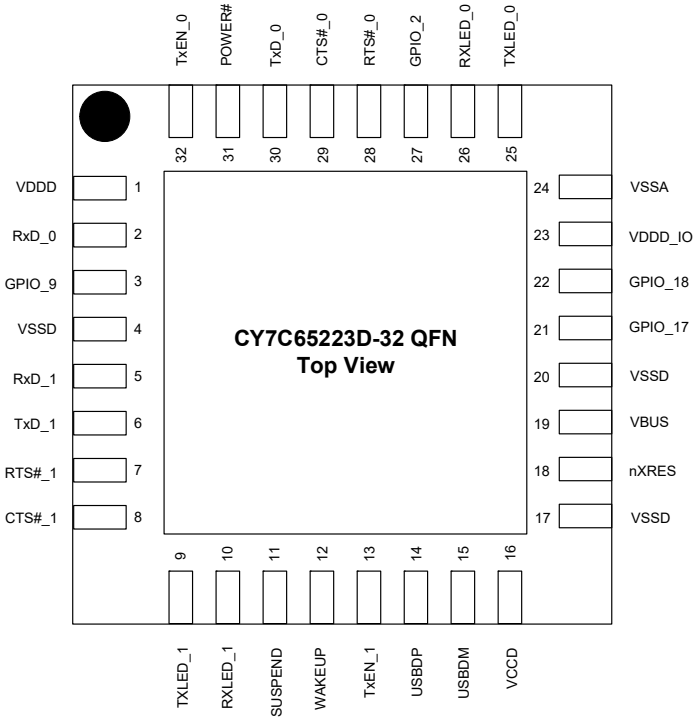


Table 13. Serial Communication Block (SCB0) Configuration

Pin	Serial Port 0	Mode 0[4]	Mode 1	Mode 2	Mode 3
		4-pin UART	6-pin UART	2-pin UART	8-pin UART
2	SCB0_0	RxD_0	RxD_0	RxD_0	RxD_0
27	SCB0_1	GPIO_2	DSR#_0	GPIO_2	DSR#_0
28	SCB0_2	RTS#_0	RTS#_0	GPIO_3	RTS#_0
29	SCB0_3	CTS#_0	CTS#_0	GPIO_4	CTS#_0
30	SCB0_4	TxD_0	TxD_0	TxD_0	TxD_0
3	SCB0_5	GPIO_9	DTR#_0	GPIO_9	DTR#_0
21	SCB0_6	GPIO_17	GPIO_17	GPIO_17	DCD#_0
13	SCB0_7	GPIO_16	GPIO_16	GPIO_16	RI#_0

Table 14. Serial Communication Block (SCB1) Configuration

Pin	Serial Port 1	Mode 0[4]	Mode 1	Mode 2	Mode 3
		4-pin UART	6-pin UART	2-pin UART	8-pin UART
5	SCB1_0	RxD_1	RxD_1	RxD_0	RxD_1
6	SCB1_1	TxD_1	TxD_1	TxD_1	TxD_1
7	SCB1_2	RTS#_1	RTS#_1	GPIO_12	RTS#_1
8	SCB1_3	CTS#_1	CTS#_1	GPIO_13	CTS#_1
9	SCB1_4	GPIO_14	DSR#_1	GPIO_14	DSR#_1
10	SCB1_5	GPIO_15	DTR#_1	GPIO_9	DTR#_1
22	SCB1_6	GPIO_18	GPIO_18	GPIO_17	DCD#_1
26	SCB1_7	GPIO_1	GPIO_1	GPIO_16	RI#_1

Legend

GPIO
SCB0
SCB1

Note
4. Device configured in Mode 0 as default. Other modes can be configured through Cypress-supplied configuration utility.

Table 15. GPIO Configuration[5]

GPIO Configuration Option	Description
TRISTATE	I/O tristated
DRIVE 1	Output static 1
DRIVE 0	Output static 0
POWER#	This output is used to control power to an external logic via switch to cut power off during unconfigured USB device and USB suspend. 0 - USB device in Configured state 1 - USB device in Unconfigured state or during USB suspend mode
TXLED#	Drives LED during USB transmit
RXLED#	Drives LED during USB receive
TX or RX LED#	Drives LED during USB transmit or receive
BCD0 BCD1	Configurable battery charger detect pins to indicate type of USB charger (SDP, CDP, or DCP) Configuration example: 00 - Draw up to 100 mA (Unconfigured state) 01 - SDP (up to 500 mA) 10 - CDP/DCP (up to 1.5 A) 11 - Suspend (up to 2.5 mA) This truth table can be configured using the configuration utility
BUSDETECT	VBUS detection. Connect VBUS to this pin via resistor network for VBUS detection when using BCD feature (see Figure 7).

Note
5. These signal options can be configured on any of the available GPIO pins using Cypress-supplied configuration utility.

USB Power Configurations

The following section describes possible USB power configurations for the CY7C65223D. Refer to the Pin Description on page 14 for signal details.

USB Bus-Powered Configuration

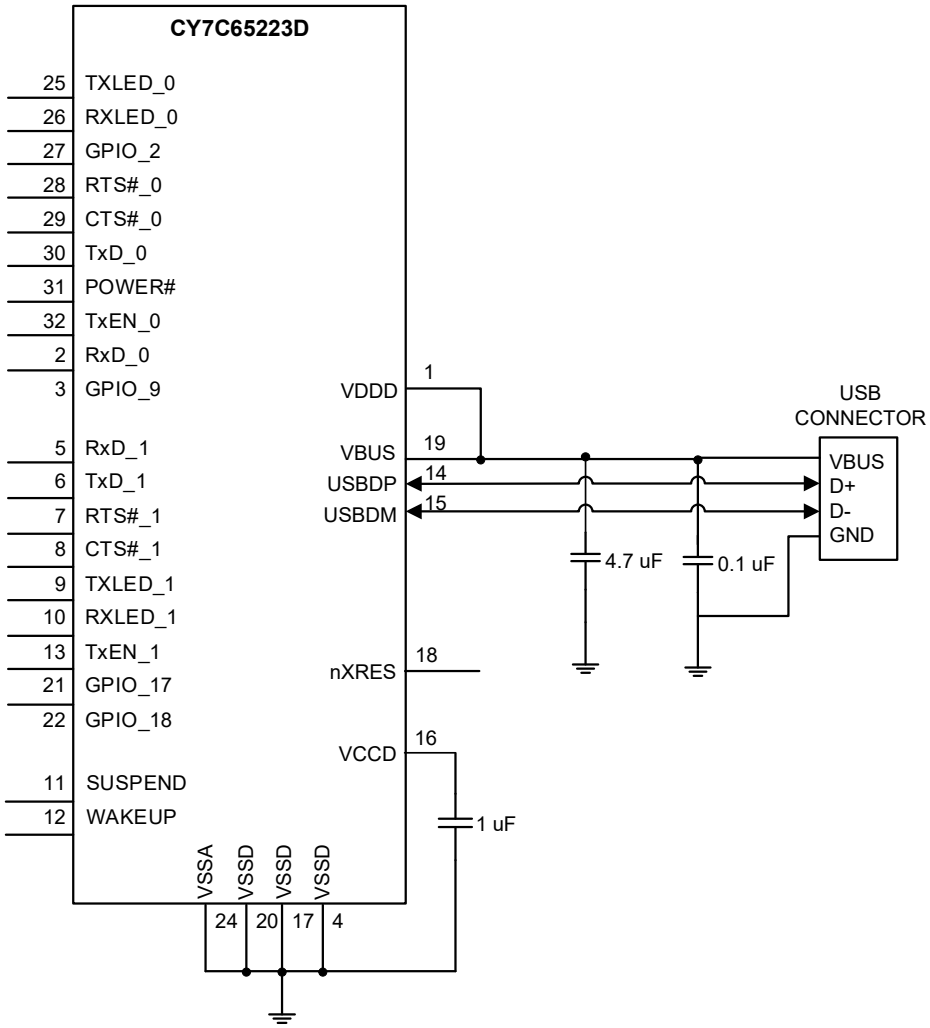
Figure 3 shows an example of the CY7C65223D in a bus-powered design. VBUS is connected directly to the CY7C65223D because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
2. The system should not draw more than 2.5 mA during USB Suspend mode.
3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration, and 2.5 mA during USB Suspend state.
4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65223D flash should be updated to indicate bus power and the maximum current required by the system using the configuration utility.

Figure 3. Bus-Powered Configuration



Self-Powered Configuration

Figure 4 shows an example of CY7C65223D in a self-powered design.

In this configuration:

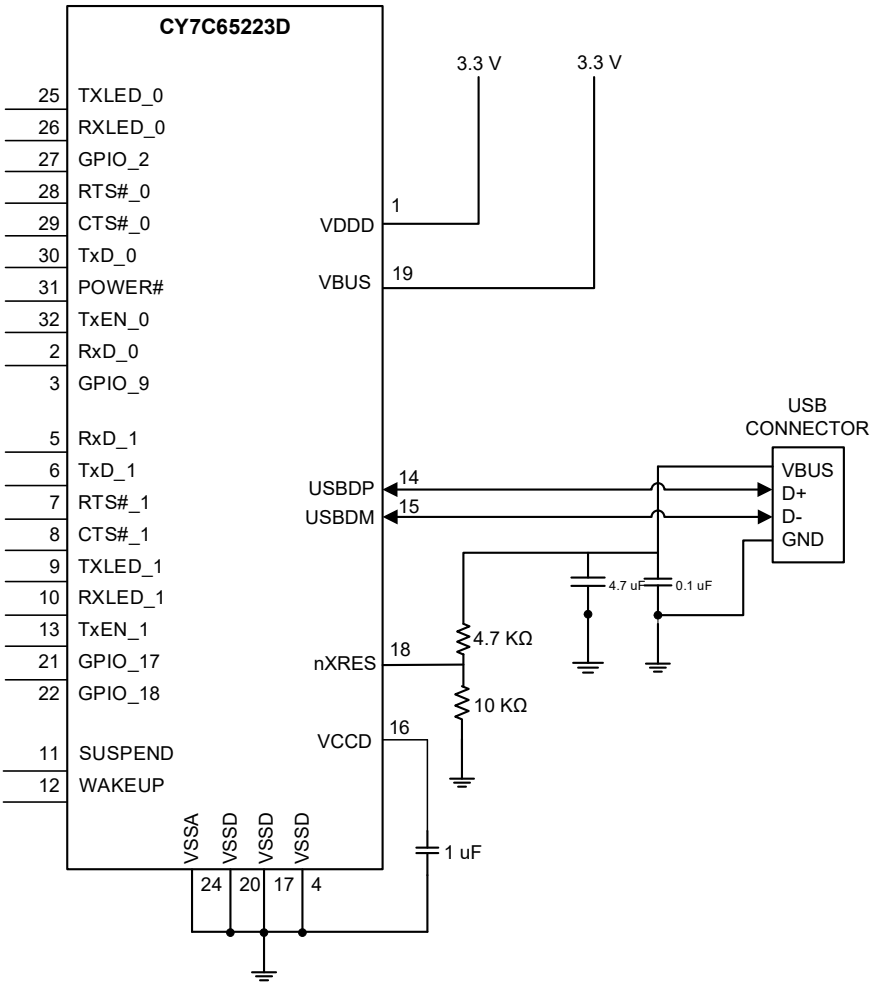
- VBUS is powered from USB VBUS. VBUS pin is also used to detect USB connection.
- VDDD is powered from an external power supply.

When VBUS is present, CY7C65223D enables an internal, 1.5-kΩ pull-up resistor on USBDP. When VBUS is absent (USB host is powered down), CY7C65223D removes the 1.5-kΩ pull-up resistor on USBDP, and this ensures no current flows from the USBDP to the USB host via a 1.5-kΩ pull-up resistor, to comply with USB 2.0 specification.

When reset is asserted to CY7C65223D, all the I/O pins are tristated.

Using the configuration utility, the configuration descriptor in the CY7C65223D flash should be updated to indicate that it is self-powered.

Figure 4. Self-Powered Configuration



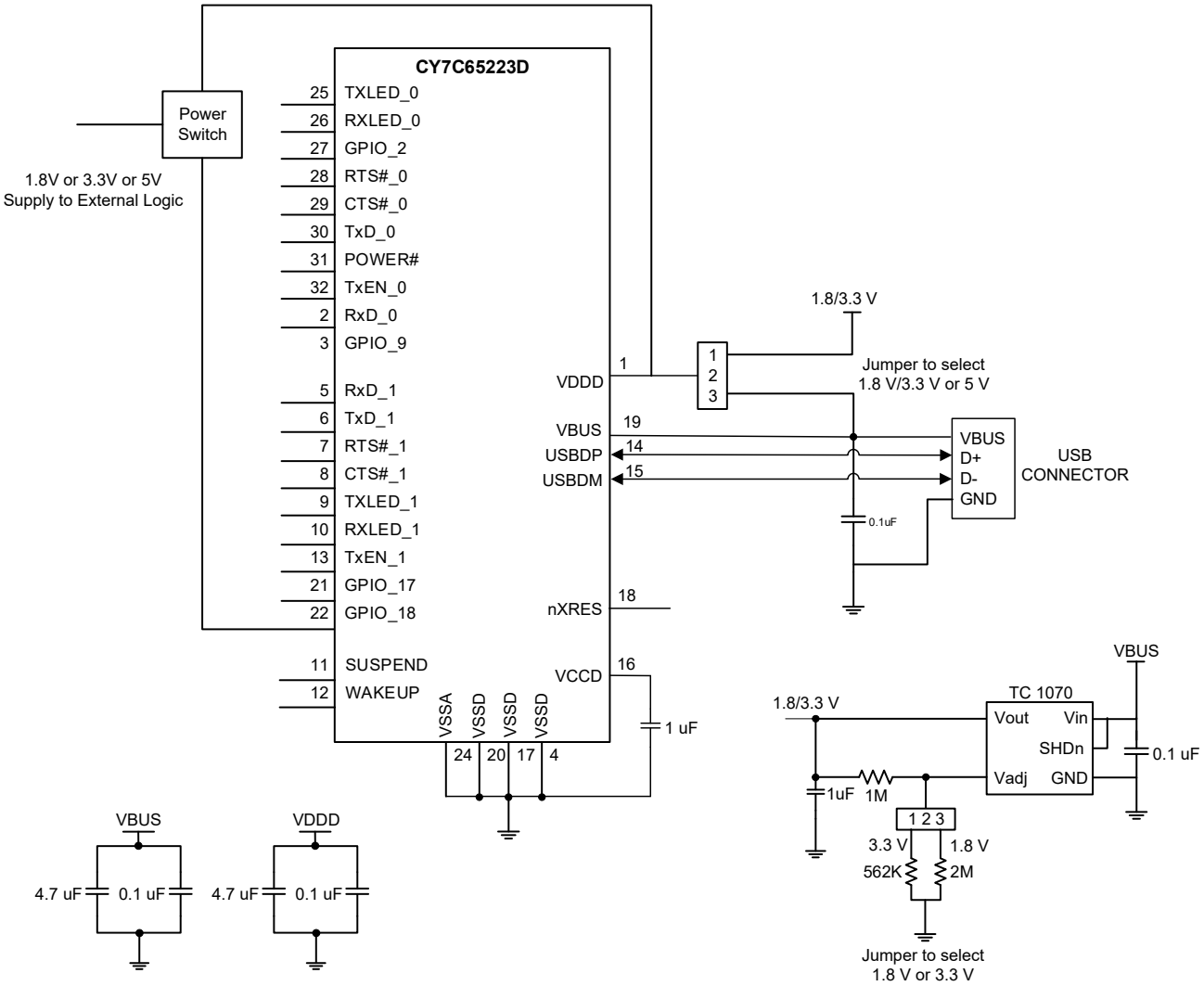
USB Bus Powered with Variable I/O Voltage

Figure 5 shows CY7C65223D in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V (using a jumper switch) the input of which is 5 V from VBUS. Another jumper switch is used to select 1.8/3.3 V or 5 V from VBUS for the VDDD pin of CY7C65223D. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following:

- The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
- The system should not draw more than 2.5 mA during USB Suspend mode.
- A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.

Figure 5. USB Bus-Powered with 1.8 V, 3.3 V, or 5 V Variable I/O Voltage[6]



Note
6. 1.71 V ≤ VDDD ≤ 1.89 V - Short VCCD pin with VDDD pin; VDDD > 2 V - connect a 1-µF decoupling capacitor to the VCCD pin.

Application Examples

The following section provides CY7C65223D application examples.

USB-to-Dual UART Bridge with Battery-Charge Detection

CY7C65223D can connect any embedded system, with a serial port, to a host PC through USB. CY7C65223D enumerates as a dual COM port on the host PC.

SUSPEND is connected to the MCU to indicate USB suspend or USB Unconfigured and the WAKEUP pin is used to wake up CY7C65223D, which in turn issues a remote wakeup to the USB host. GPIO1 and GPIO0 are configured as RXLED# and TXLED# to drive two LEDs indicating data receive and transmit respectively.

CY7C65223D implements the battery charger detection functionality based on the USB Battery Charging Specification Rev 1.2.

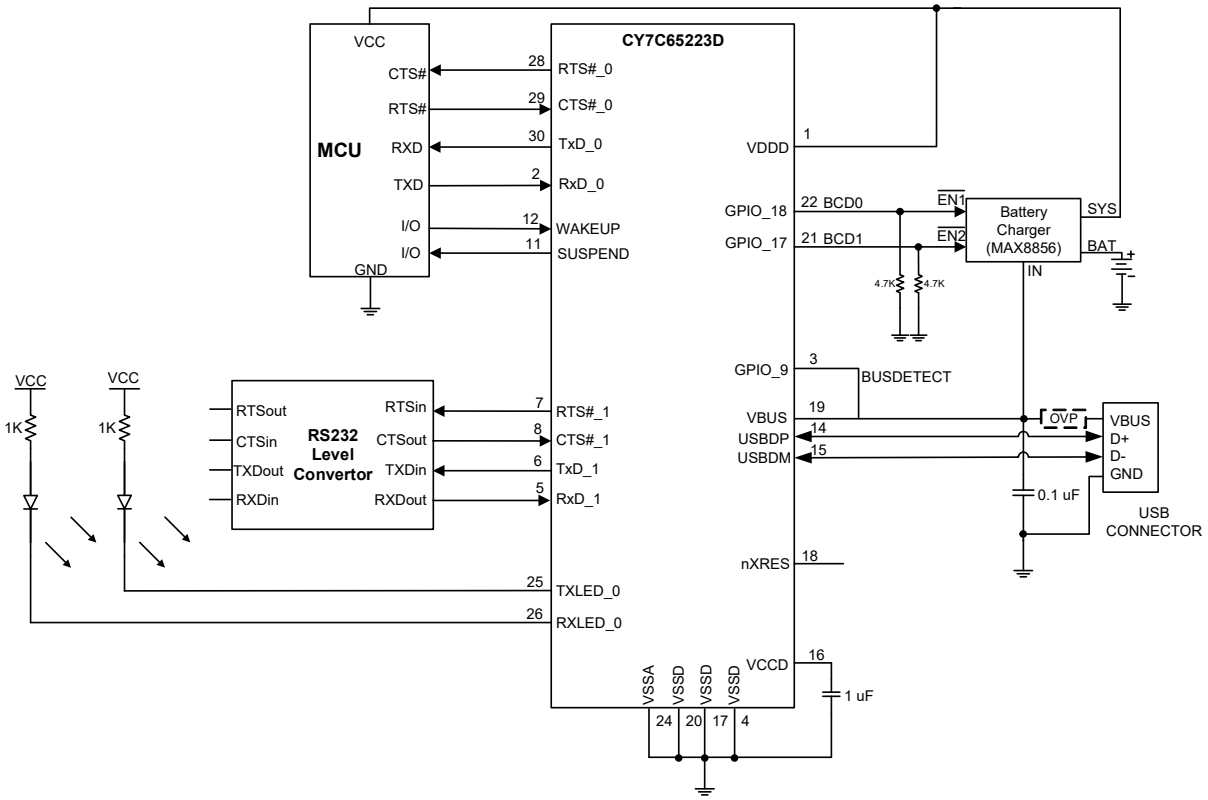
Battery-operated bus power systems must comply with the following conditions:

- The system can be powered from the battery (if not discharged) and be operational if VBUS is not connected or powered down.
- The system should not draw more than 100 mA from the VBUS prior to USB enumeration and USB Suspend mode.
- The system should not draw more than 500 mA for SDP and 1.5 A for CDP/DCP

To comply with the first requirement, VBUS from the USB host is connected to the battery charger as well as CY7C65223D as shown in Figure 6. When VBUS is connected, CY7C65223D initiates battery charger detection and indicates the type of USB charger over BCD0 and BCD1. If the USB charger is SDP or CDP, CY7C65223D enables a 1.5-K pull-up resistor on the USBDP for Full-Speed enumeration. When VBUS is disconnected CY7C65223D indicates absence of the USB charger over BCD0 and BCD1, and removes the 1.5-K pull-up resistor on USBDP. Removing this resistor ensures no current flows from the supply to the USB host through the USBDP, to comply with the USB 2.0 specification.

To comply with the second and third requirements, two signals (BCD0 and BCD1) are configured over GPIO to communicate the type of USB host charger and the amount of current it can draw from the battery charger. The BCD0 and BCD1 signals can be configured using the configuration utility.

Figure 6. USB to Dual UART Bridge with Battery Charge Detection[7, 8]

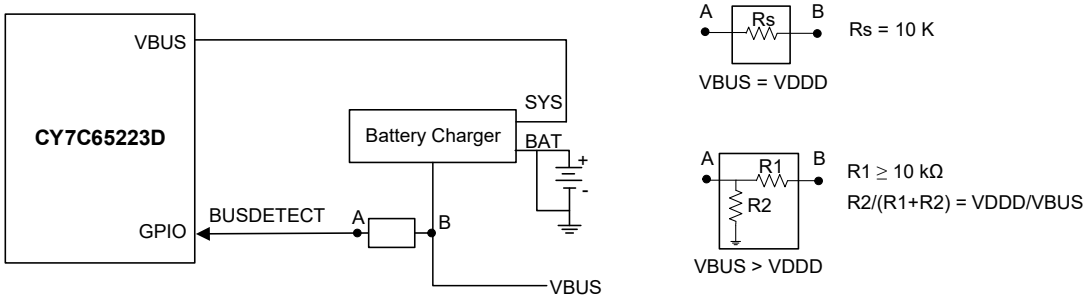


Notes

7. Add a 100-kΩ pull-down resistor on the V_{BUS} pin for quick discharge.
8. Refer Figure 7, Figure 8, Figure 9 and the corresponding descriptions for handling VBUS Over Voltage Protection (OVP).

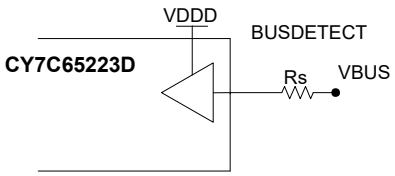
In a battery charger system.a 9-V spike on the VBUS is possible. The CY7C65223D VBUS pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of battery charger to the VBUS pin of CY7C65223D, as shown in Figure 7.

Figure 7. GPIO VBUS Detect (BUSDETECT)



When VBUS and VDDD are at the same voltage potential, VBUS can be connected to GPIO using a series resistor (Rs). This is shown in Figure 8. If there is a charger failure and VBUS becomes 9 V, then the 10-kΩ resistor plays two roles. It reduces the amount of current flowing into the forward biased diodes in the GPIO, and it reduces the voltage seen on the pad.

Figure 8. GPIO VBUS Detection, VBUS = VDDD



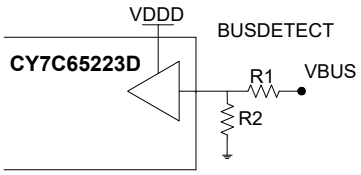
When VBUS > VDDD, a resistor voltage divider is necessary to reduce the voltage from VBUS down to VDDD for the GPIO sensing the VBUS voltage. This is shown in Figure 9. The resistors should be sized as follows:

R1 ≥ 10 K

R2 / (R1 + R2) = VDDD / VBUS

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

Figure 9. GPIO VBUS Detection, VBUS > VDDD



USB to RS232 Bridge

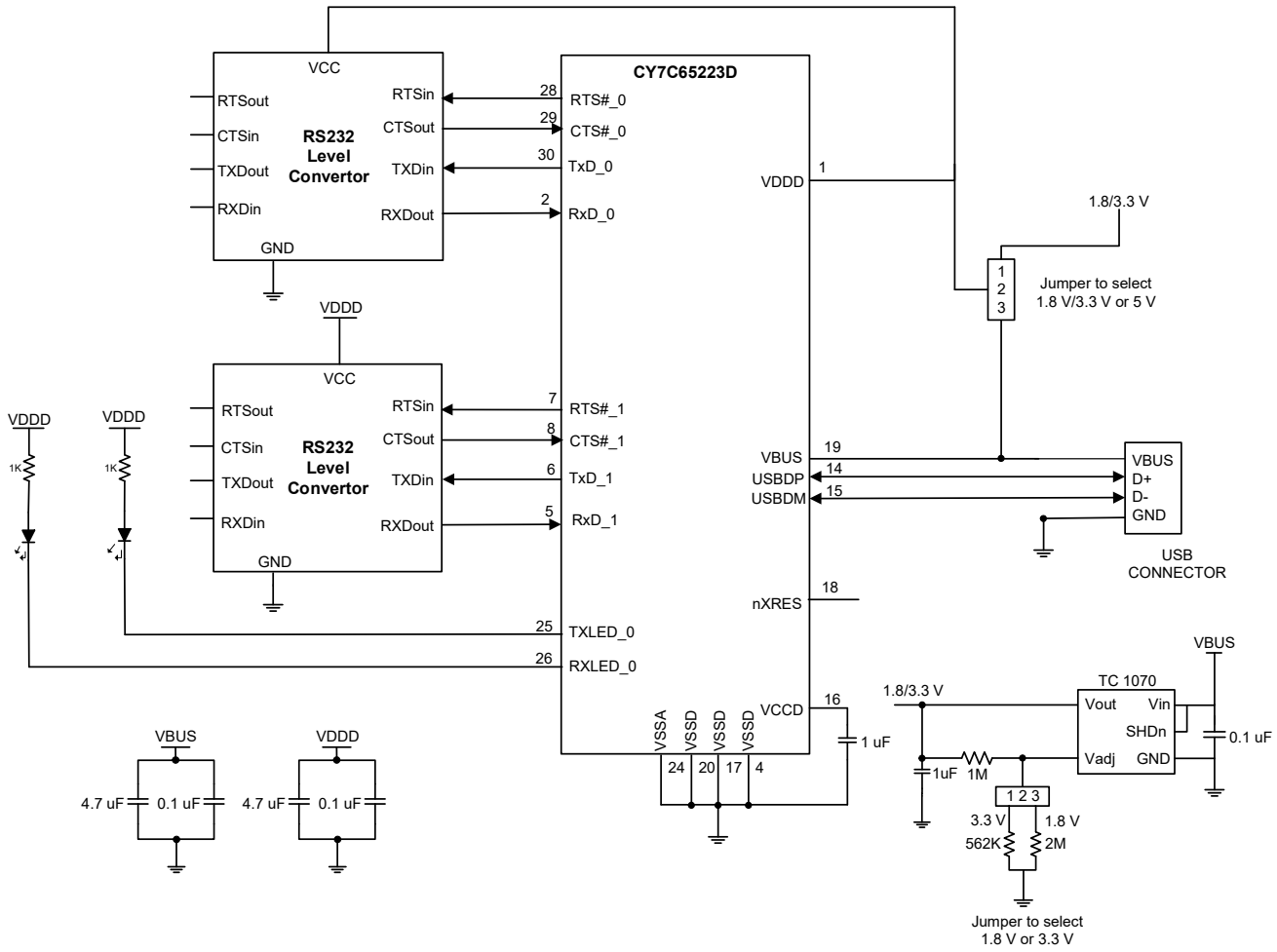
CY7C65223D can connect any embedded system, with a serial port, to a host PC through USB. CY7C65223D enumerates as a COM port on the host PC.

The RS232 protocol follows bipolar signaling - that is, the output signal toggles between negative and positive polarity. The valid RS232 signal is either in the -3-V to -15-V range or in the +3-V to +15-V range, and the range between -3 V to +3 V is invalid. In the RS232, Logic 1 is called “Mark” and it corresponds to a negative voltage range. Logic 0 is called “Space” and it corresponds to a positive voltage range. The RS232 level converter facilitates this polarity inversion and the voltage-level translation between the CY7C65223D’s UART interface and RS232 signaling.

In this application, as shown in Figure 10, SUSPEND is connected to the SHDN# pin of the RS232-level converter to indicate USB suspend or USB not enumerated.

GPIO8 and GPIO9 are configured as RXLED# and TXLED# to drive two LEDs, indicating data transmit and receive.

Figure 10. USB to RS232 Bridge



USB to RS485 Application

CY7C65223D can be configured as dual USB to UART interface. This UART interface operates at TTL level and it can be converted to RS485 interface using a GPIO and any half duplex RS485 transceiver IC (to convert TTL level to RS485 level) as shown in Figure 12. This GPIO (TXD Enable) enables and disables the RS485 transceiver IC based on availability of character in UART buffer of CY7C65223D. This GPIO can be configured using USB-Serial Configuration utility. Figure 11 shows timing diagram of this GPIO.

RS485 is a multi-drop network – that is, many devices can communicate with each other over a single two-wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

Figure 11. USB-to-RS485 Bridge

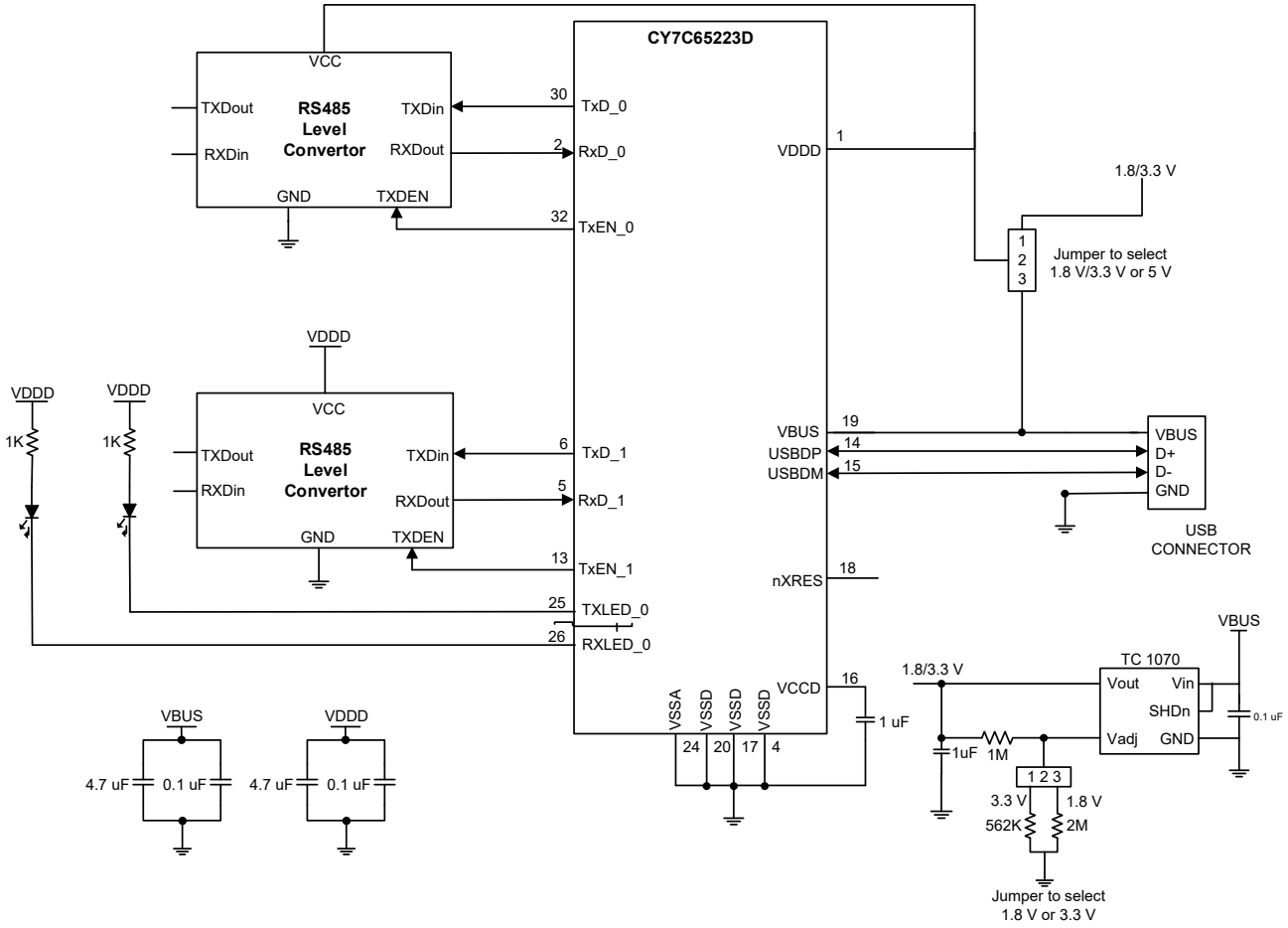
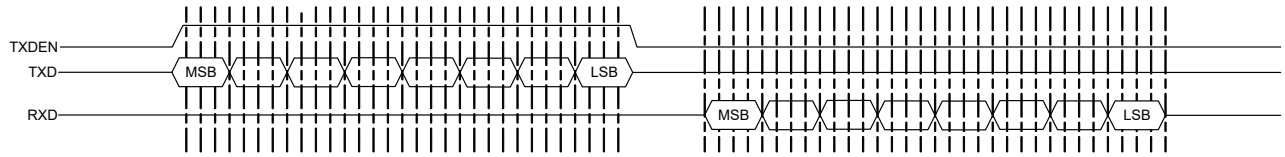


Figure 12. RS485 GPIO (TXDEN) Timing Diagram



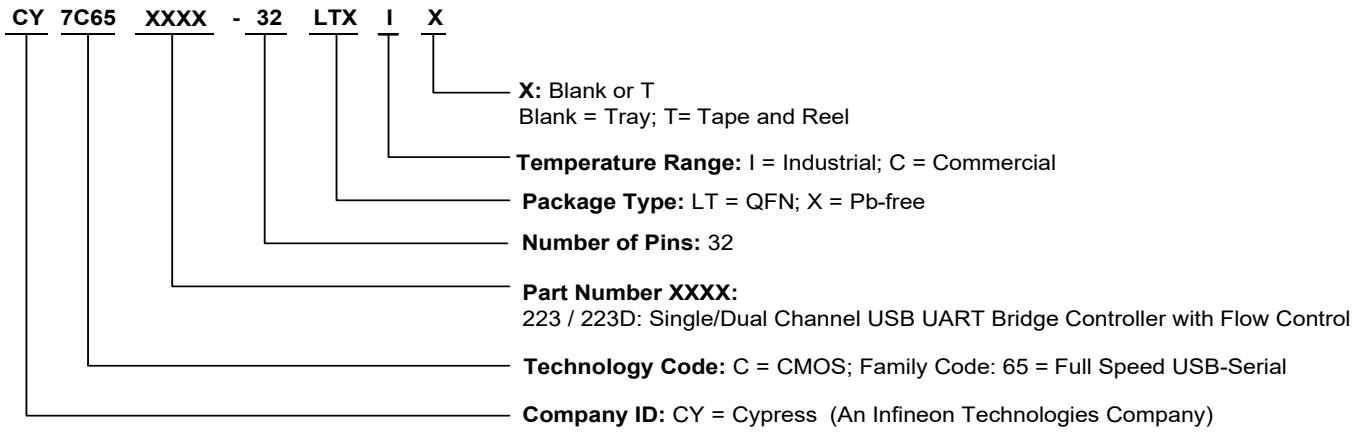
Ordering Information

Table 16 lists the CY7C65223D key package features and ordering codes. For more information, contact your local sales representative.

Table 16. Key Features and Ordering Information

Package	Ordering Code	Operating Range
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free)	CY7C65223D-32LTXI	Industrial
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel	CY7C65223D-32LTXIT	Industrial

Ordering Code Definitions



Package Information

The package currently planned to be supported is the 32-pin QFN.

Figure 13. 32-pin QFN 5 × 5 × 1.0 mm LT32B 3.5 × 3.5 EPAD (Sawn)

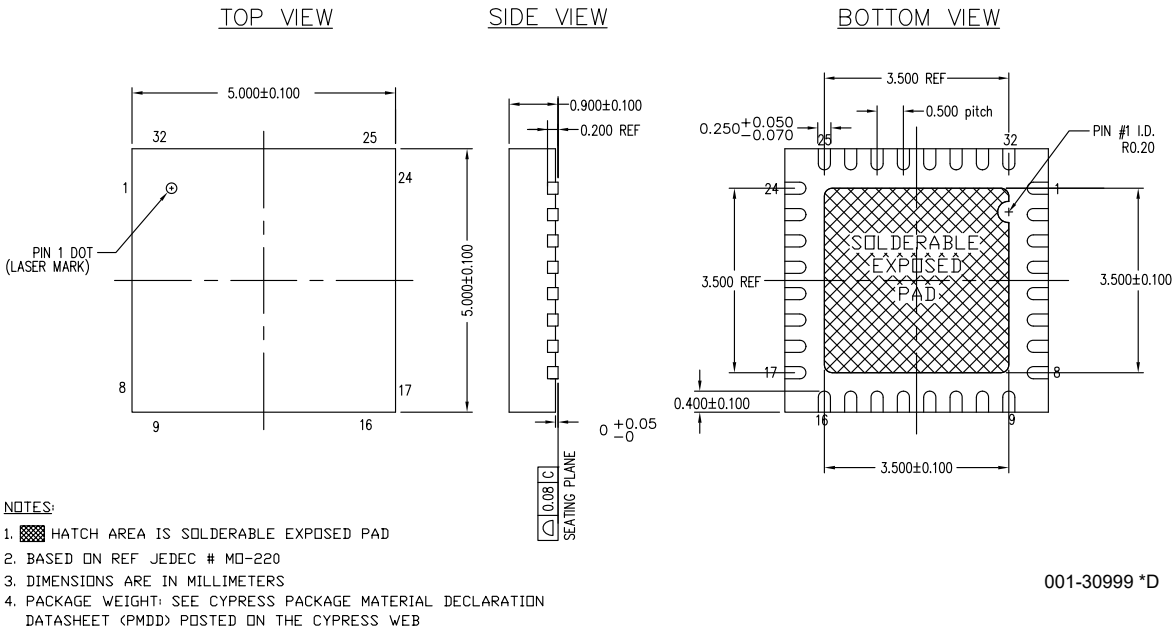


Table 17. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	25	85	°C
THJ	Package θ_{JA}	–	19	–	°C/W

Table 18. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
32-pin QFN	260 °C	30 seconds

Table 19. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
32-pin QFN	MSL 3

Acronyms

Table 20. Acronyms Used in this Document

Acronym	Description
BCD	battery charger detection
CDC	communication driver class
CDP	charging downstream port
DCP	dedicated charging port
DLL	dynamic link library
ESD	electrostatic discharge
GPIO	general purpose input/output
HBM	human-body model
MCU	Microcontroller Unit
OSC	oscillator
PHDC	personal health care device class
PID	Product Identification
SCB	serial communication block
SDP	Standard Downstream Port
SIE	serial interface engine
VCOM	virtual communication port
USB	Universal Serial Bus
UART	universal asynchronous receiver transmitter
VID	Vendor Identification

Document Conventions

Units of Measure

Table 21. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
DMIPS	dhrystone million instructions per second
kΩ	kilo-ohm
KB	kilobyte
kHz	kilohertz
kV	kilovolt
Mbps	megabits per second
MHz	megahertz
mm	millimeter
V	volt

Errata

This section describes the errata for the CY7C65223D USB-Serial family. Details include errata trigger conditions, scope of impact, and available workaround.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY7C65223D	All Variants

Qualification Status

Production

Errata Summary

The following table defines the errata applicability to available USB-Serial devices.

Items	Affected Part Number	Fix Status
[1.] USB-Serial does not report UART Frame errors.	CY7C65223D	No Fix
[2.] USB-Serial does not report MARK or SPACE Parity errors.	CY7C65223D	No Fix

1. USB-Serial does not report UART Frame errors.	
Problem Definition	USB-Serial does not report UART Frame Errors while receiving UART data when the number of stop bits is set as 1.
Parameters Affected	NA
Trigger Condition(s)	USB-Serial fails to report a UART Frame error when the number of stop bits is set as 1. It correctly reports the error when the stop bits is not 1
Scope of Impact	No impact
Workaround	No workaround. In general, applications using UART will have to include checksum or CRC in the data to ensure frame integrity.
Fix Status	No fix

2. USB-Serial does not report MARK or SPACE Parity errors.	
Problem Definition	USB-Serial does not report UART Parity error while receiving the data when configured for MARK or SPACE parity.
Parameters Affected	NA
Trigger Condition(s)	USB Serial fails to report UART Parity errors while receiving data when configured for MARK or SPACE parity. Note that USB-Serial detects parity errors when configured for ODD or EVEN parity settings.
Scope of Impact	No impact
Workaround	No workaround. In general, applications using UART will have to include checksum or CRC in the data to ensure frame integrity.
Fix Status	No fix

Document History Page

Document Title: CY7C65223D, USB-Dual UART with Flow Control Document Number: 002-31603			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6993251	11/25/2020	Final datasheet to NSO.

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