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CYBT-483056-02/CYBT-483062-02

EZ-BT™ XR WICED® Module

General Description

The CYBT-483056-02/CYBT-483062-02 are dual-mode Bluetooth BR/EDR and Low Energy wireless module solutions. The CYBT-483056-02 include onboard crystal oscillators, passive components, PA/LNA, and the Cypress CYW20719 silicon device. The CYBT-483062-02 includes onboard crystal oscillators, passive components, PA/LNA, and the Cypress CYW20721 silicon device.

CYBT-4830xx-02 supports a number of peripheral functions (ADC, PWM), as well as multiple serial communication protocols (UART, SPI, I^2C, I^2S/PCM). CYBT-4830xx-02 includes a royalty-free stack compatible with Bluetooth 5.0 in a 12.75 × 18.59 × 1.80 mm module form-factor.

CYBT-4830xx-02 includes an integrated chip antenna, onboard external power/low noise amplifier, qualified by Bluetooth SIG, and includes regulatory certification approval for FCC, ISED, MIC, and CE.

Module Description

- Module size: 12.75 mm × 18.59 mm × 1.80 mm
- Complies with Bluetooth Core Specification version 5.0 supporting BR, EDR 2/3 Mbps, eSCO, Bluetooth LE, and LE 2 Mbps.
  - QDID: 152528
  - Declaration ID: D050856
- True Extended Range with up to +20 dBm output power:
  - Up to 1 kilometer bidirectional communication[1, 2]
- Certified up to +20 dBm for FCC and ISED
- Certified up to +10 dBm for MIC and CE standards
- Up to 15 GPIOs
- 1024-KB flash memory, 512-KB SRAM memory
- Industrial temperature range: –30 °C to +85 °C
- Integrated Arm® Cortex®-M4 microprocessor core with floating point unit (FPU)

RF Characteristics

- Maximum TX output power: +20.0 dBm
- Bluetooth LE RX Receive Sensitivity: –95.0 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution

Power Consumption

- TX current consumption
  - Bluetooth LE silicon: 5.6 mA (MCU + radio only, 0 dbm)
  - RFX2401C: 100 mA peak (PA/LNA only, +20 dBm Pout)
  - RFX2401C: 27 mA peak (PA/LNA only, +7.5 dBm Pout)
- RX current consumption
  - Bluetooth silicon: 5.9 mA (MCU + radio only)
  - RFX2401C: 8.0 mA (PA/LNA only)
- Cypress CYW20719/21 silicon low power mode support
  - PDS: 6.1 µA with 512 KB SRAM retention
  - SDS: 1.6 µA
  - HIDOFF (External Interrupt): 400 nA

Functional Capabilities

- 1x ADC with (12-bit ENoB for DC measurement and 13-bit ENoB for Audio measurement) with 10 channels.
- 1x HCI UART for programming and HCI
- 1x peripheral UART (PUART)
- 2x SPI (master or slave) blocks (SPI, Quad SPI, MIPI DBI-C)
- 1x I^2C master/slave and 1x I^2C master only
- I^2S/PCM audio interfaces
- Up to 6 16-bit PWMs
- Watchdog Timer (WDT)
- Bluetooth Basic Rate (BR) and Enhanced Data Rate (EDR) Support
- Bluetooth LE protocol stack supporting generic access profile (GAP) Central, Peripheral, or Broadcaster roles
- Hardware Security Engine

Benefits

CYBT-4830xx-02 is a fully integrated and certified solution that provides all necessary components required to operate Bluetooth communication standards.

- Proven hardware design ready to use
- Ultra-flexible supermux I/O design allows maximum flexibility for GPIO function assignment
- Large nonvolatile memory for complex application development
- Over-the-Air (OTA) update capable for development or field updates
- Bluetooth SIG qualified with QDID and Declaration ID
- WICED™ Studio provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test your Bluetooth application

Notes
1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +19 dBm POUT.
2. Specified as EZ-BT XT module to module range. Mobile phone connection will decrease based on the PA/LNA performance of the mobile phone used.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/EZ-BT Module Portfolio, Module Roadmap
- Development Kits:
  - CYBT-483039-EVAL, CYBT-483039-02 Evaluation Board
  - CYW920719Q40EVB-01, Evaluation Kit for CYW20719 silicon device
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA224516 - RF Regulatory Certifications for CYBT-483039-02, CYBT-483056-02 and CYBT-483062-02 EZ-BT™ WICED Modules
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Files for EZ-BLE/EZ-BT Modules
  - KBA223428 - Programming an EZ-BT WICED Module
  - KBA225450 - Putting 2073x, 2070x, and 20719 Based Devices or Modules in HCI Mode

Development Environments

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (IoT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you're a customer, partner or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ECO System.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

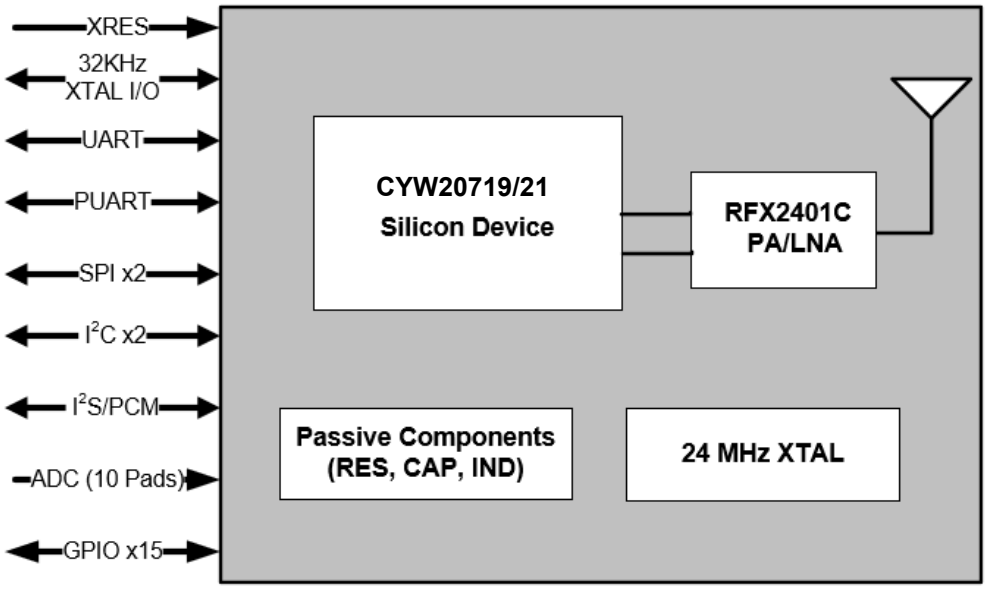
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-4830xx-02 functional block diagram.

Figure 1. Functional Block Diagram



Note General Purpose Input/Output pins shown in Figure 1 are configurable to any specified input or output function in the SuperMux table detailed in Table 5 in the Module Connections section.

Note Connections shown in the above block diagram are maximum number of connections per function. The total number of GPIOs available on the CYBT-4830xx-02 is 15.

Module Description

The CYBT-4830xx-02 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

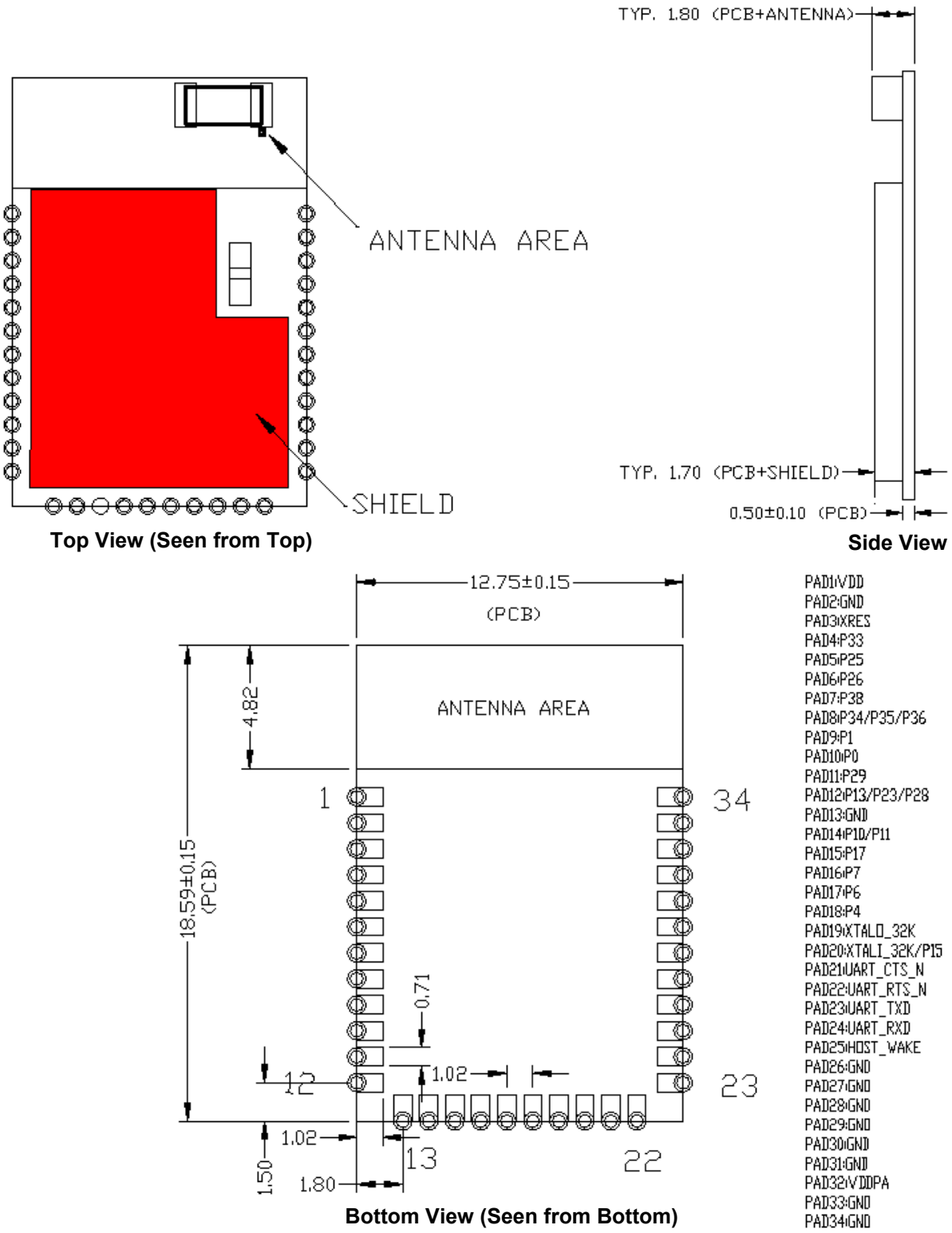
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Any changes to the current BOM for the CYBT-4830xx-02 will not be made until approval is provided by the end customer for this product. The CYBT-4830xx-02 will be held within the physical dimensions shown in the mechanical drawings in Figure 2. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	12.75 ± 0.15 mm
	Width (Y)	18.59 ± 0.15 mm
Antenna location dimensions	Length (X)	12.75 mm
	Width (Y)	4.82 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.20 mm
Maximum component height	Height (H)	1.30 mm typical (Chip Antenna)
Total module thickness (bottom of module to top of shield)	Height (H)	1.80 mm typical

See Figure 2 for the mechanical reference drawing for CYBT-4830xx-02.

Figure 2. Module Mechanical Drawing



Note

3. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 8.

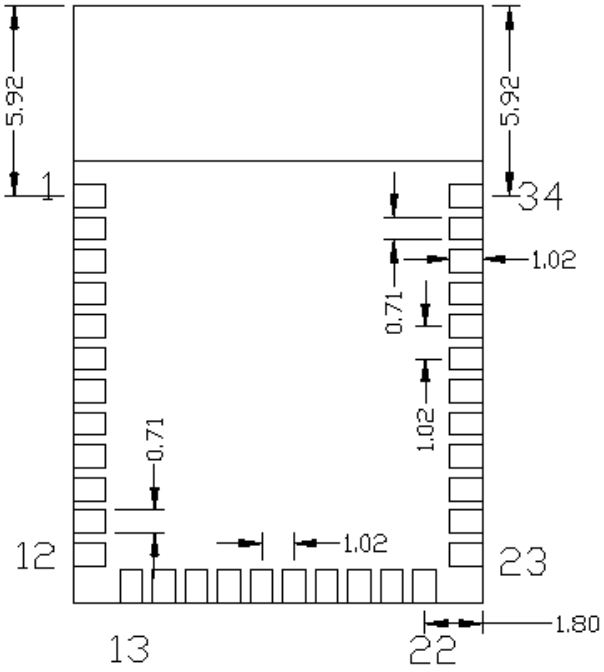
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-4830xx-02 has 34 connections to a host board via solder pads (SP). Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-4830xx-02 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	34	Solder Pad	1.02 mm	0.71 mm	1.02 mm

Figure 3. Solder Pad Dimensions (Seen from Bottom)

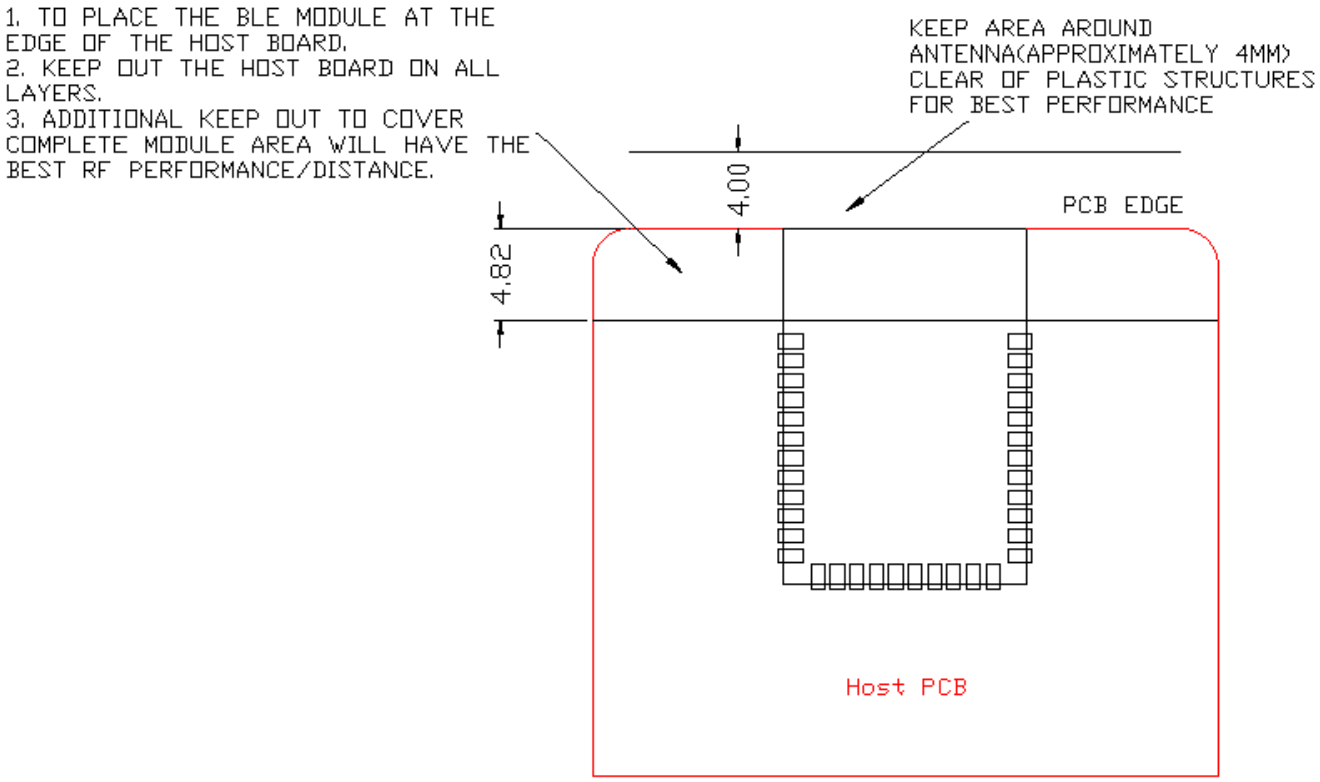


Solder Pad Connections (Seen from Bottom)

To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the chip antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 3 below. Refer to AN96841 for module placement best practices.
3. Optional Keepout: To maximize RF performance, the area immediately around the Cypress Bluetooth module chip antenna may contain an additional keep out area, where there are no grounding or signal traces. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in Figure 4 (dimensions are in mm).

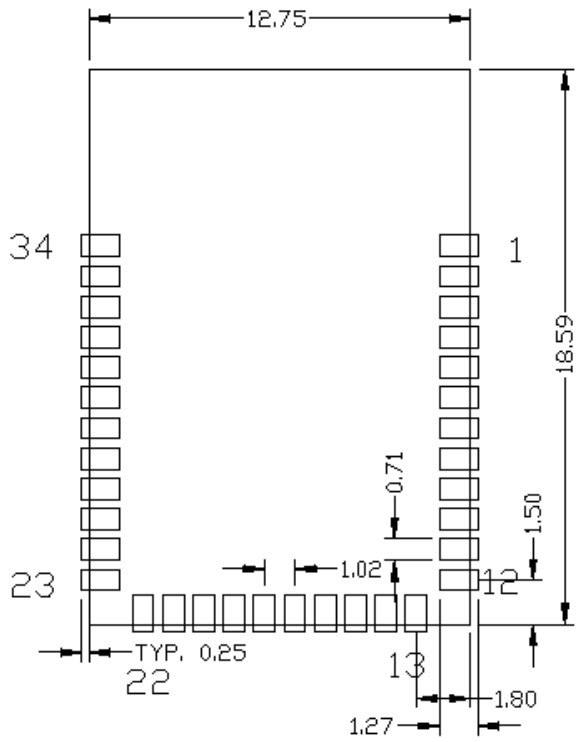
Figure 4. Optional Additional Host PCB Keep Out Area Around the CYBT-4830xx-02 Chip Antenna



Recommended Host PCB Layout

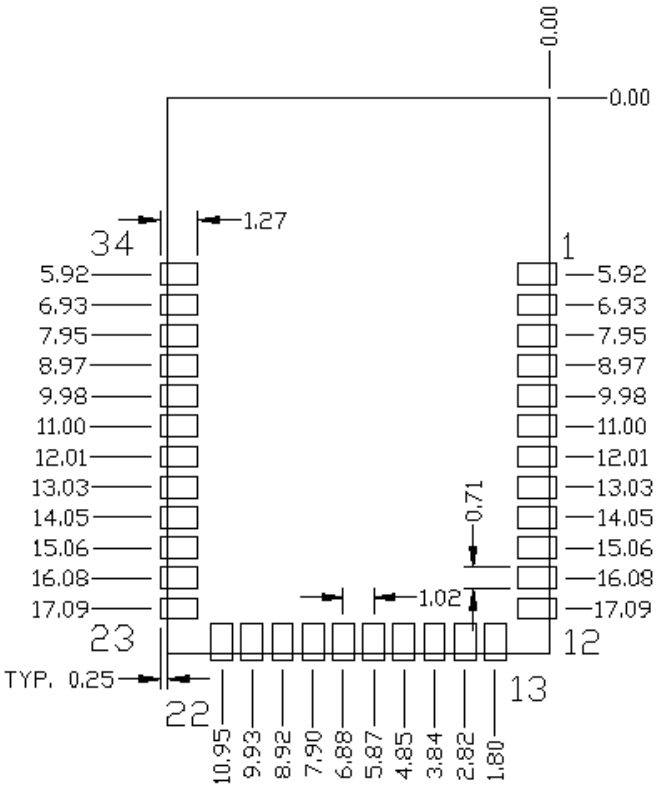
Figure 5, Figure 6, Figure 7, and Table 3 on page 9 provide details that can be used for the recommended host PCB layout pattern for CYBT-4830xx-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBT-4830xx-02 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 6. CYBT-4830xx-02 Host Layout (Relative to Origin)



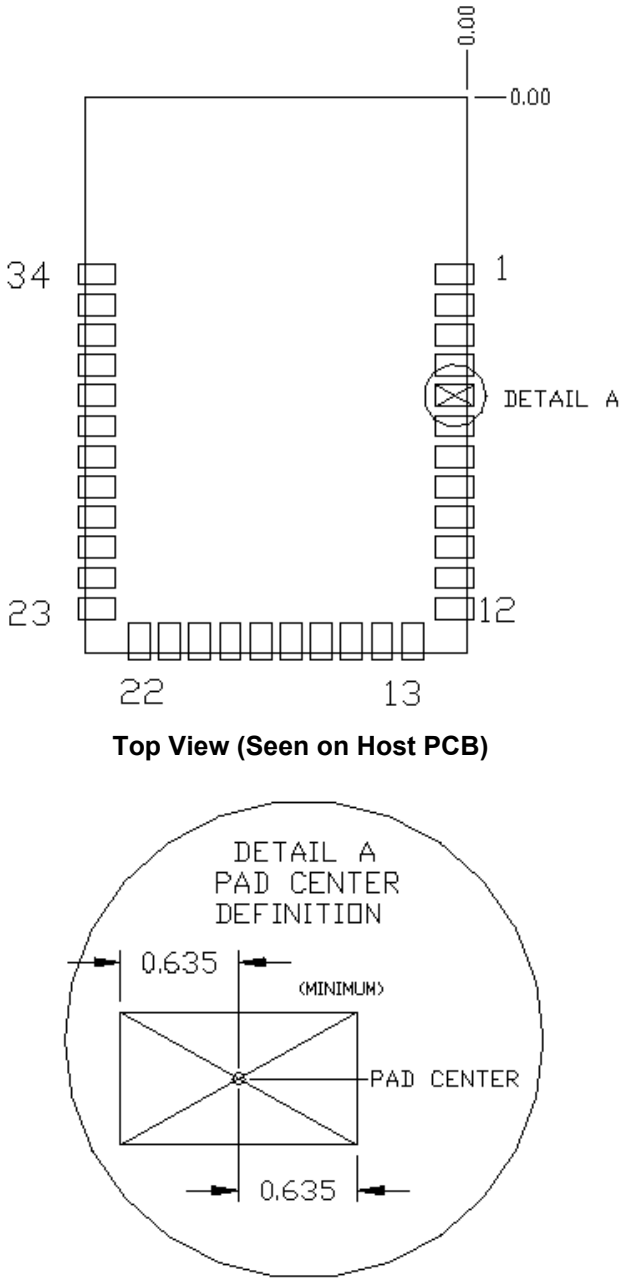
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-4830xx-02. All dimensions are referenced to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.38, 5.92)	(14.96, 233.07)
2	(0.38, 6.93)	(14.96, 272.83)
3	(0.38, 7.95)	(14.96, 312.99)
4	(0.38, 8.97)	(14.96, 353.15)
5	(0.38, 9.98)	(14.96, 392.91)
6	(0.38, 11.00)	(14.96, 433.07)
7	(0.38, 12.01)	(14.96, 472.83)
8	(0.38, 13.03)	(14.96, 512.99)
9	(0.38, 14.05)	(14.96, 553.15)
10	(0.38, 15.06)	(14.96, 592.91)
11	(0.38, 16.08)	(14.96, 633.07)
12	(0.38, 17.09)	(14.96, 672.83)
13	(1.80, 18.21)	(70.87, 716.93)
14	(2.82, 18.21)	(111.02, 716.93)
15	(3.84, 18.21)	(151.18, 716.93)
16	(4.85, 18.21)	(190.94, 716.93)
17	(5.87, 18.21)	(231.10, 716.93)
18	(6.88, 18.21)	(270.87, 716.93)
19	(7.90, 18.21)	(311.02, 716.93)
20	(8.92, 18.21)	(351.18, 716.93)
21	(9.93, 18.21)	(390.94, 716.93)
22	(10.95, 18.21)	(431.10, 716.93)
23	(12.37, 17.09)	(487.01, 672.83)
24	(12.37, 16.08)	(487.01, 633.07)
25	(12.37, 15.06)	(487.01, 592.91)
26	(12.37, 14.05)	(487.01, 553.15)
27	(12.37, 13.03)	(487.01, 512.99)
28	(12.37, 12.01)	(487.01, 472.83)
29	(12.37, 11.00)	(487.01, 433.07)
30	(12.37, 9.98)	(487.01, 392.91)
31	(12.37, 8.97)	(487.01, 353.15)
32	(12.37, 7.95)	(487.01, 312.99)
33	(12.37, 6.93)	(487.01, 272.83)
34	(12.37, 5.92)	(487.01, 233.07)

Figure 7. Solder Pad Reference Location



Top View (Seen on Host PCB)

Module Connections

Table 4 details the solder pad connection definitions and available functions for each connection pad. The GPIO connections available on the CYBT-4830xx-02 can be configured to any of the input or output functions listed in Table 5. Table 4 specifies any function that is required to be used on a specific solder pad, and also identifies GPIOs that can be configured using the SuperMux.

Table 4. CYBT-4830xx-02 Solder Pad Connection Definitions

Pad	Pad Name	Silicon Pin Name	XTAL I/O	ADC	GPIO	SuperMux Capable[4]
1	VDD	VDDIO	Silicon Power Supply Input (1.76V ~ 3.63V)			
2	GND	GND	Ground			
3	XRES	RST_N	External Reset (Active Low)			
4	P33	P33	–	IN6	✓	✓ see Table 5
5	P25	P25	–	–	✓	✓ see Table 5
6	P26	P26	–	–	✓	✓ see Table 5
7	P38	P38	–	IN1	✓	✓ see Table 5
8	P34/P35/P36	P34 P35 P36	–	IN5 (P34) IN4 (P35) IN3 (P36)	✓ (P34/P35/P36)	✓ see Table 5
9	P1	P1	–	IN28	✓	✓ see Table 5
10	P0	P0	–	IN29	✓	✓ see Table 5
11	P29	P29	–	IN10	✓	✓ see Table 5
12	P13/P23/P28	P13 P23 P28	–	IN22 (P13) IN12 (P23) IN11 (P28)	✓(P13/P23/P28)	✓ see Table 5
13	GND	GND	Ground			
14	P10/P11	P10 P11	–	IN25 (P10) IN24 (P11)	✓ (P10/P11)	✓ see Table 5
15	P17	P17	–	IN18	✓	✓ see Table 5
16	P7	P7	–	–	✓	–
17	P6	P6	–	–	✓	✓ see Table 5
18	P4	P4	–	–	✓	–
19	XTALO_32K	XTALO_32K	External Oscillator Output (32kHz)	–	–	–
20	XTALI_32K/ P15[5]	XTALI_32K P15	External Oscillator Input (32kHz)	IN20 (P15)	✓(P15)	✓(P15), see Table 5
21	UART_CTS_N	BT_UART_CTS_N	UART (HCI UART) Clear To Send Input Only			
22	UART_RTS_N	BT_UART_RTS_N	UART (HCI UART) Request To Send Output Only			
23	UART_TXD	BT_UART_TXD	UART (HCI UART) Transmit Data Only			
24	UART_RXD	BT_UART_RXD	UART (HCI UART) Receive Data Only			
25	HOST_WAKE	BT_HOST_WAKE	A signal from the CYBT-4830xx-02 module to the host indicating that the Bluetooth device requires attention.			
26	GND	GND	Ground			
27	GND	GND	Ground			
28	GND	GND	Ground			
29	GND	GND	Ground			
30	GND	GND	Ground			
31	GND	GND	Ground			

Notes
4. The CYBT-483056-02/CYBT-483062-02 can configure GPIO connections to any Input/Output function described in Table 5.
5. P15 should not be driven high externally while the part is held in reset (it can be floating or driven low). Failure to do so may cause some current to flow through P15 until the device comes out of reset.

Table 4. CYBT-4830xx-02 Solder Pad Connection Definitions (continued)

Pad	Pad Name	Silicon Pin Name	XTAL I/O	ADC	GPIO	SuperMux Capable[4]
32	VDDPA	N/A	PA/LNA Power Supply Voltage (2.0 ~ 3.6V)			
33	GND	GND	Ground			
34	GND	GND	Ground			

Table 5 details the available Input and Output functions configurable to any solder pad in Table 4 that are marked as SuperMux capable.

Table 5. GPIO SuperMux Input and Output Functions

Function	Input/Output	Function Type	GPIOs Required	Function Connection Description
SPI 1	Input/Output	Serial Communication (Master or Slave)	4 ~ 8	SPI 1 Clock
				SPI 1 Chip Select
				SPI 1 MOSI
				SPI 1 MISO
				SPI 1 I/O 2 (Quad SPI)
				SPI 1 I/O 3 (Quad SPI)
				SPI 1 Interrupt
	Output			SPI 1 DCX (DBI-C DCX 8-bit mode)
SPI 2	Input/Output	Serial Communication (Master or Slave)	4 ~ 8	SPI 2 Clock
				SPI 2 Chip Select
				SPI 2 MOSI
				SPI 2 MISO
				SPI 2 I/O 2 (Quad SPI)
				SPI 2 I/O 3 (Quad SPI)
				SPI 2 Interrupt
	Output			SPI 2 DCX (DBI-C DCX 8-bit mode)
PUART	Input	Serial Communication Input	4	Peripheral UART RX
				Peripheral UART CTS
	Output	Serial Communication Output		Peripheral UART TX
				Peripheral UART RTS
I^2C	Input/Output	Serial Communication (Master or Slave)	2	I2C Clock
				I2C Data
PCM In	Input	Audio Input Communication	3	PCM Input
				PCM Clock
				PCM Sync
PCM Out	Output	Audio Output Communication	3	PCM Output
				PCM Clock
				PCM Sync
I^2S In	Input	Audio Input Communication	3	I2S DI, Data Input
				I2S WS, Word Select
				I2S Clock
I^2S Out	Output	Audio Output Communication	3	I2S DO, Data Output
				I2S WS, Word Select
				I2S Clock

Table 5. GPIO SuperMux Input and Output Functions (continued)

Function	Input/Output	Function Type	GPIOs Required	Function Connection Description
PDM	Input	Microphone	1 ~ 2	PDM Input Channel 1
				PDM Input Channel 2
PWM	Output	Pulse Width Modulator	1 ~ 6	PWM Channel 0
				PWM Channel 1
				PWM Channel 2
				PWM Channel 3
				PWM Channel 4
				PWM Channel 5

Connections and Optional External Components

Power Connections (V_{DD} and V_{DDPA})

The CYBT-4830xx-02 contains two power supply connections, V_{DD} and V_{DDPA}.

V_{DD} is the power supply connection for the Cypress CYW20719/21 silicon device. V_{DD} accepts a supply input of 1.76 V to 3.63 V. Table 14 on page 27 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 14.

V_{DDPA} is the power supply connection for the on-module power amplifier/low-noise amplifier. V_{DDPA} accepts a supply input of 2.00 V to 3.60 V, as shown in Table 14. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 14.

Considerations and Optional Components for Brownout (BO) Conditions

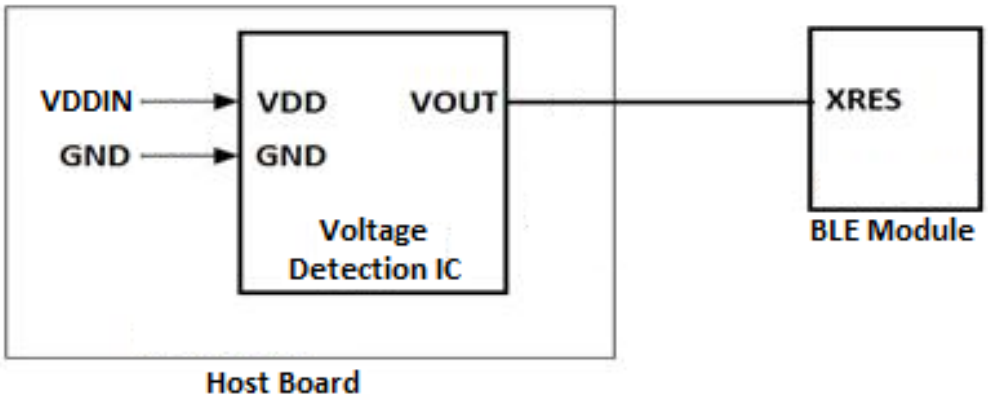
Power supply design must be completed to ensure that the CYBT-4830xx-02 module does not encounter a Brownout condition, which can lead to unexpected functionality, or module lock up. A Brownout condition may be met if power supply provided to the module during power up or reset is in the range shown below: $V_{IL} \leq V_{DD} \leq V_{IH}$.

Refer to Table 20 on page 30 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (i.e. battery installation, high value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brownout voltage range from occurring during power removal.

Figure 8 shows the recommended circuit design when using an external voltage detection IC.

Figure 8. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brownout condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brownout conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brownout condition.

External Reset (XRES)

CYBT-4830xx-02 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be invoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-4830xx-02 module (solder pad 3). The CYBT-4830xx-02 module does not require an external pull-up resistor on the XRES input.

During power on operation, the XRES connection to the CYBT-4830xx-02 is required to be held low 50 ms after the V_{DD} power supply input to the module is stable. This can be accomplished in the following ways:

- The host device can connect a GPIO to the XRES of Cypress CYBT-4830xx-02 module and pull XRES low until V_{DD} is stable. XRES is recommended to be released 50 ms after V_{DD} is stable.
- If the XRES connection of the CYBT-4830xx-02 module is not used in the application, a 0.33 µF capacitor may be connected to the XRES solder pad of the CYBT-4830xx-02 in order to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the V_{DD} power supply ramp time of the system. The capacitor value should result in an XRES release timing of at least 50 ms after V_{DD} stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after V_{DD} is stable.

Refer to Figure 11 on page 19 for XRES operating and timing requirements during power on events.

HCI UART Connections

The recommendations in this section apply to the HCI UART (Solder Pads 21, 22, 23, and 24). For full UART functionality, all UART signals must be connected to the Host device. If full UART functionality is not being used, and only UART RXD and TXD are desired or capable, then the following connection considerations should be followed for UART RTS and CTS:

- UART RTS: Can be left floating, pulled low, or pulled high. RTS is not critical for initial firmware uploading at power on.
- UART CTS: Must be pulled low to bypass flow control and to ensure that continuous data transfers are made from the host to the module.

External Component Recommendation

Power Supply Input Options and Circuitry

Two connection options are available for the V_{DD} and V_{DDPA} power supplies:

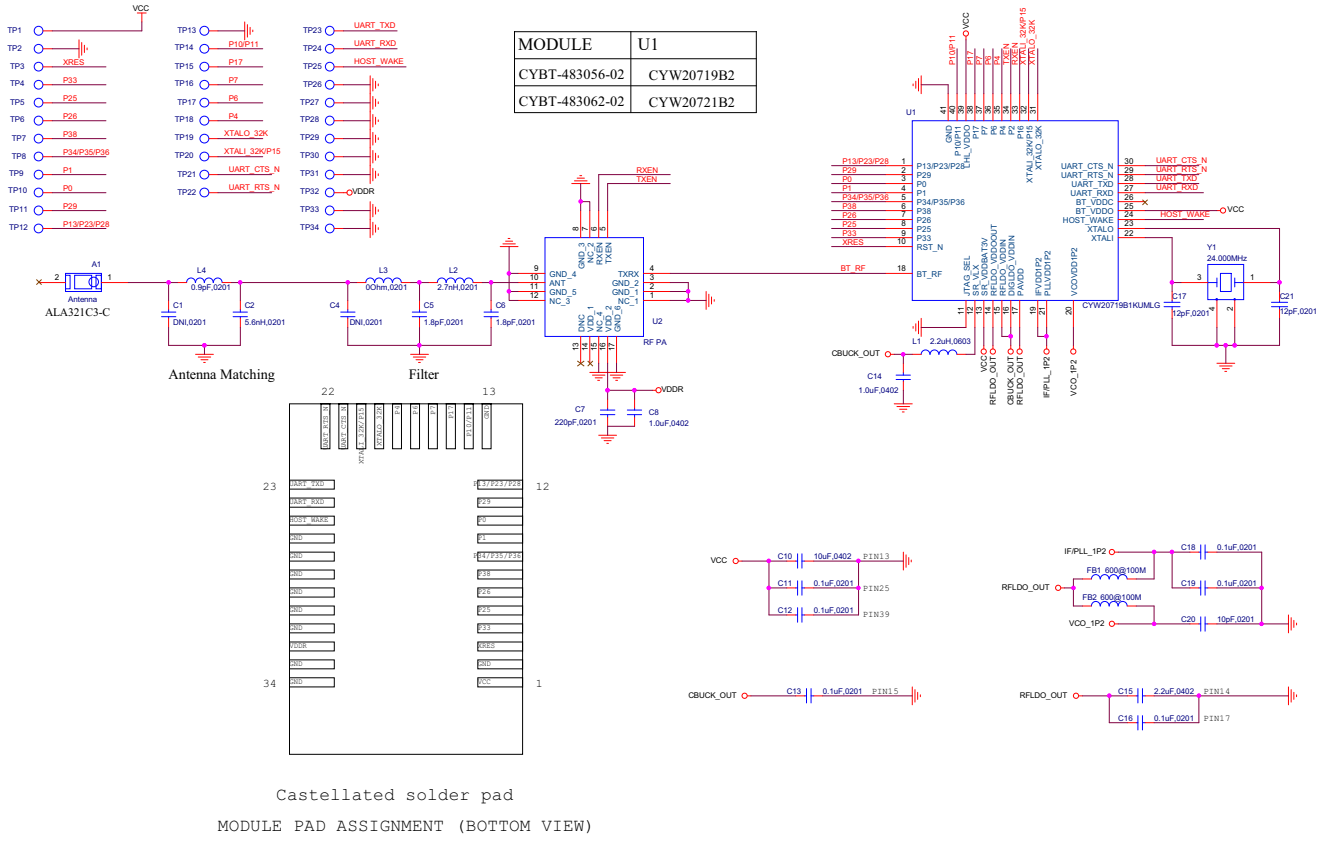
1. Single supply: Connect V_{DD} and V_{DDPA} to the same supply.
2. Independent supply: Power V_{DD} and V_{DDPA} separately.

In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pad connection.

The recommended ferrite bead value is 330Ω, 100 MHz. (Murata BLM21PG331SN1D).

Figure 9 illustrates the CYBT-4830xx-02 schematic.

Figure 9. CYBT-4830xx-02 Schematic Diagram



Critical Components List

Table 6 details the critical components used in the CYBT-4830xx-02 module.

Table 6. Critical Component List

Component	Reference Designator	Description
Silicon	U2	40-pin QFN Bluetooth Silicon Device - CYW20719/21
Chip Antenna	A1	Antenna, 2.4 GHz, ALA321C3-C
PA/LNA	U2	PA/LNA, +25 dBm maximum boost, RFX2401C
Crystal	Y1	24 MHz, 8 pF

Antenna Design

Table 7 details the chip antenna used in the CYBT-4830xx-02 module.

Table 7. Chip Antenna Specifications

Item	Description
Frequency Range	2400 – 2500 MHz
Peak Gain	2.5 dBi typical
Return Loss	10.0 dB typical

Power Amplifier (PA) and Low Noise Amplifier (LNA)

Table 8 details the PA/LNA that is used on the CYBT-4830xx-02 module.

Table 8. Power Amplifier/Low Noise Amplifier Details

Item	Description
PA/LNA Manufacturer	Skyworks Inc.
PA/LNA Part Number	RFX2401C
Power Supply Range	2.0V to 3.6V

Table 9 details the power consumption of the integrated PA/LNA used on the CYBT-4830xx-02 module. Table 9 only details the current consumption of the RFX2401C PA/LNA. V_{DD} = 3.3 V, TA = +25 °C, measured on the RFX2401C evaluation board, unless otherwise noted.

Table 9. Power Amplifier/Low Noise Amplifier Current Consumption Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
TX High Power Current	Pout = +20dBm	–	100	–	mA
TX Quiescent Current	No RF applied	–	17	–	mA
RX Quiescent Current	No RF applied	–	8	–	mA

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

Table 10. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive Frequency Hopping	–
Paging and Inquiry	eSCO	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	eSCO	–
Bluetooth 4.1	**Bluetooth 4.2**	**Bluetooth 5.0**
Low Duty Cycle Advertising	Data Packet Length Extension	LE 2 Mbps
Dual Mode	LE Secure Connection	Slot Availability Mask
LE Link Layer Topology	Link Layer Privacy	High Duty Cycle Advertising

BQB and Regulatory Testing Support

The CYBT-4830xx-02 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYBT-4830xx-02 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

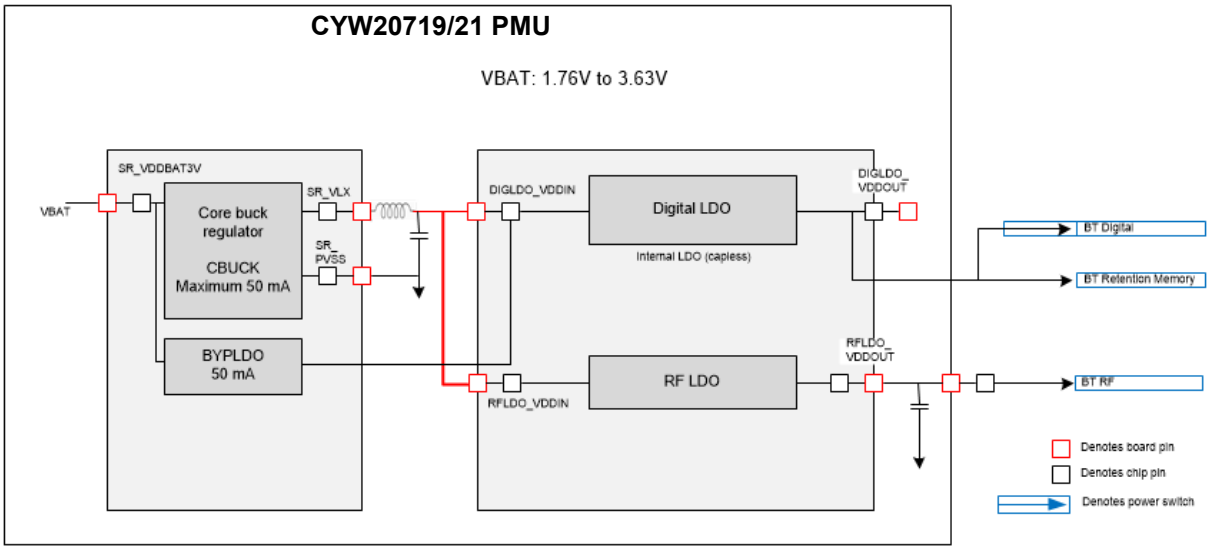
- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

Power Management Unit

Figure 10 shows the CYW20719/21 power management unit (PMU) block diagram. The CYW20719/21 includes an integrated buck regulator, a bypass LDO, a capless LDO for digital circuits and a separate LDO for RF. The bypass LDO automatically takes over from the buck once V_{BAT} supply falls below 2.1V.

The voltage levels shown in this figure are the default settings; the firmware may change voltage levels based on operating conditions.

Figure 10. Default Usage Mode



Integrated Radio Transceiver

The CYBT-4830xx-02 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 3.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

CYBT-4830xx-02 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYBT-4830xx-02 includes an external power amplifier (ePA) that can transmit up to +20 dBm for class 1 operation.

Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYBT-4830xx-02 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-4830xx-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYBT-4830xx-02 uses an internal loop filter.

Microcontroller Unit

The CYBT-4830xx-02 includes a Arm Cortex-M4 processor with 2 MB of ROM, 448 KB of data RAM, 64 KB of patch RAM, and 1 MB of on-chip flash. The CM4 has a maximum speed of 96 MHz. CYBT-4830xx-02 supports execution from on-chip flash (OCF).

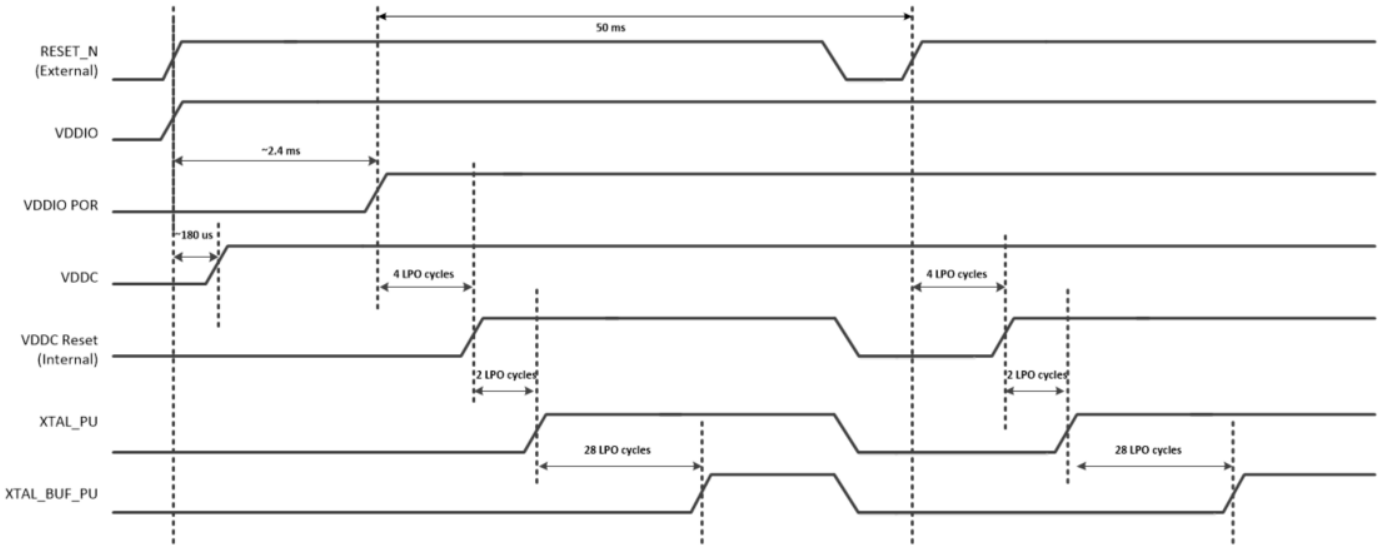
The CM4 also includes a single precision IEEE 754 compliant floating point unit (FPU).

The CM4 runs all the BT layers as well as application code. The ROM includes LM, HCI, L2CAP, GATT, as well as other stack layers freeing up the flash for application usage. A standard serial wire debug (SWD) interface provides debugging support.

External Reset

An external active-low reset signal, XRES, can be used to put the CYBT-4830xx-02 in the reset state. An external voltage detector reset IC with 50 ms delay is recommended on the XRES connection. The XRES must only be released after the V_{DDO} supply voltage level has been stabilized for 50 ms.

Figure 11. Reset Timing



Peripheral and Communication Interfaces

I²C

The CYBT-4830xx-02 provides a 2-pin I²C compatible master interface to communicate with I²C compatible peripherals. The following transfer clock rates are supported are:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I²C-compatible speed)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed)

SCL and SDA lines can be routed to any of the P0-P39 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. I²C block does not support multi master capability by either master or slave devices.

I²C is Master Only.

HCI UART Interface

The CYBT-4830xx-02 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 1.5 Mbps. Typical rates are 115200, 921600, 1500000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYBT-4830xx-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The CYBT-4830xx-02 can wake up the host as needed or allow the host to sleep via the HOST_WAKE signal (solder pad 2). signal allows the CYBT-4830xx-02 to optimize system power consumption by allowing a host device to remain in low power modes as long as possible. The HOST_WAKE signal can be enabled via a vendor specific command.

Peripheral UART Interface

The CYBT-4830xx-02 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYBT-4830xx-02 can map the peripheral UART to any GPIO. The Peripheral UART functionality is the same as the HCI UART, but with a 256-byte transmit and receive FIFO.

Serial Peripheral Interface

The CYBT-4830xx-02 has two independent SPI interfaces. Both interfaces support Single, Dual, and Quad mode SPI operations as well as MIPI DBI-C Interface.Either of the interface can be a master or a slave. SPI2 can support only 1 slave. SPI1 has a 1024 byte transmit and receive buffers which is shared with the host UART interface. SPI2 has a dedicated 256-byte transmit and receive buffers. To support more flexibility for user applications, the CYBT-4830xx-02 has optional I/O ports that can be configured individually and separately for each functional pin. SPI IO voltage depends on V_{DDO}.

MIPI Interface

There are three options in DBI type-C corresponding to 9-bit, 16-bit, and 8-bit modes. The CYBT-4830xx-02 plays the role of host, and only the 9-bit and 8-bit modes (option 1 and option 3 in DBI-C spec) are supported. In the 9-bit mode, the SCL, CS, MOSI, and MISO pins are used. In the 8-bit mode, an additional pin (DCX) is required. The DCX pin indicates if the current outgoing bit stream is a command or data byte.

32 kHz Crystal Oscillator

The CYBT-4830xx-02 utilizes the built-in Local Oscillator (LO) on the CYW20719/21 silicon device for 32 kHz timing. The accuracy of the LO is +/- 500 ppm. The use of an external XTAL oscillator is optional. CYBT-4830xx-02 includes external XTAL oscillator connections for applications requiring higher timing accuracy. Figure 12 shows an external 32 kHz XTAL oscillator with external components and Table 11 lists the recommended external oscillator's characteristics. This oscillator input can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 12. 32 kHz Oscillator Block Diagram

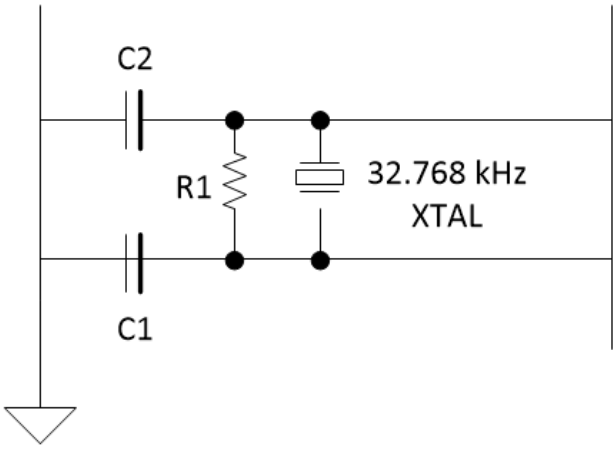


Table 11. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency Tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up Time	$T_{startup}$	–	–	500	–	ms
XTAL Drive Level	P_{drv}	For crystal selection	–	–	0.5	µW
XTAL Series Resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL Shunt Capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF
External AC Input Amplitude	V_{IN} (AC)	C_{couple} = 100 pF; R_{bias} = 10 MΩ	400	–	–	mVpp

ADC Port

The ADC is a Σ-Δ ADC core designed for audio (13 bits) and DC (12 bits) measurement. It operates at 12 MHz and has 10 solder pad connections that can act as input channels. The internal bandgap reference has ±5% accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

The following CYBT-4830xx-02 module solder pads can be used as ADC inputs:

- Pad 4: P33, ADC Input Channel 6
- Pad 7: P38, ADC Input Channel 1
- Pad 8: P34/P35/P36, ADC Input Channels 5/4/3 respectively.
  Note Only one ADC input on this solder pad can be active at a given time.
- Pad 9: P1, ADC Input Channel 28
- Pad 10: P0, ADC Input Channel 29
- Pad 11: P29, ADC Input Channel 10
- Pad 12: P13/P23/28, ADC Input Channels 22/12/11 respectively.
  Note Only one ADC input on this solder pad can be active at a given time.
- Pad 14: P10/P11, ADC Input Channels 25/24 respectively.
  Note Only one ADC input on this solder pad can be active at a given time.
- Pad 15: P17, ADC Input Channel 18
- Pad 20: P15, ADC Input Channel 20. P15 should not be driven high externally while the part is held in reset (it can be floating or driven low). Failure to do so may cause some current to flow through P15 until the device comes out of reset.

GPIO Ports

The CYBT-4830xx-02 has a maximum of 15 general-purpose I/Os (GPIOs). All GPIOs support the following:

- Programmable pull-up/down of approximately 45 kΩ.
- Input disable, allowing pins to be left floating or analog signals connected without risk of leakage.
- Source/sink 8 mA at 3.3V and 4 mA at 1.8V.
- P15 is Bonded to the same pin as XTALI_32K (Pad 20). If an External 32.768 kHz crystal is not used, then this pin can be used as GPIO P15.
- P26/P28/P29 can sink/source 16 mA at 3.3V and 8 mA at 1.8V.

Most peripheral functions can be assigned to any GPIO. For details, refer to Table 5 on page 11. For more details on Supermux configuration and control, refer to “Supermux Wizard for CYW20719” user guide.

The list below details the GPIOs that are available on the CYBT-4830xx-02 module:

- P0-P1, P4, P6, P7, P17, P25, P26, P29, P33, and P38
- P10/P11 (Double bonded connection on the CYBT-4830xx-02 module, only one of two is available)
- P13/P23/P28 (Triple bonded connection on the CYBT-4830xx-02 module, only one of three is available)
- P15/XTALI_32K (Double bonded pin on the CYBT-4830xx-02 module, only one of two is available)
- P34/P35/P36 (Triple bonded pin on the CYBT-4830xx-02 module, only one of three is available)
- P19, P20 and P39 are reserved for system use. Do not use these three GPIOs.

For GPIOs highlighted as double or triple bonded connections, only one of the connections can be used at a given time. When a certain GPIO is selected, the other GPIOs bonded to the same connection must be configured to input with output disable.

PWM

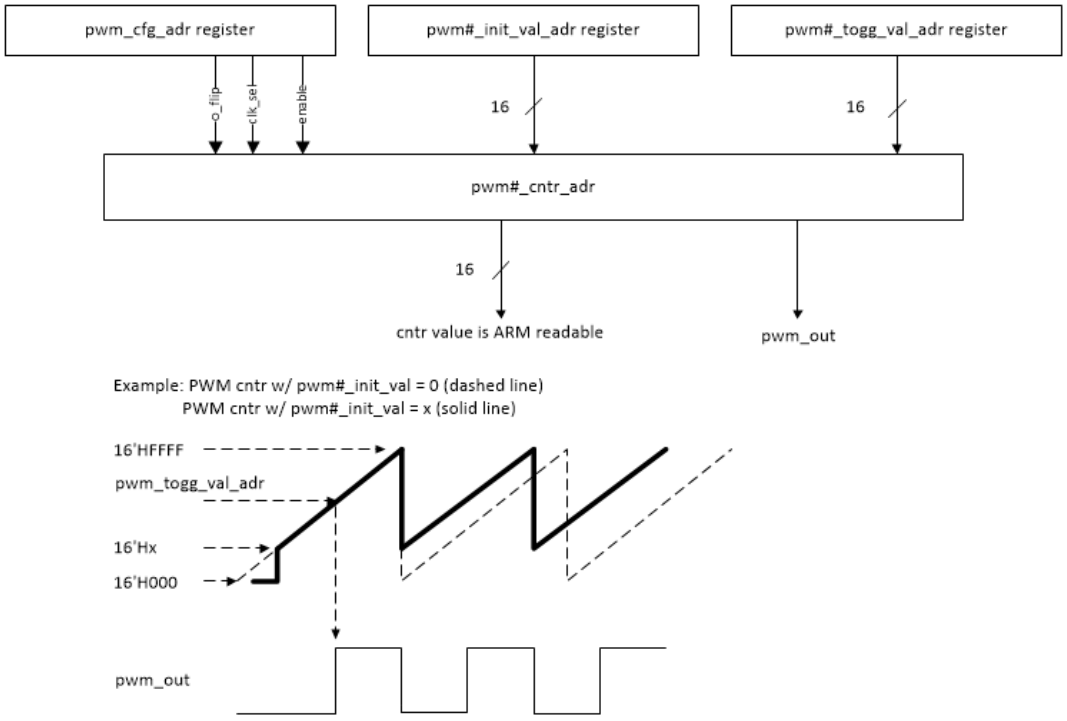
The CYBT-4830xx-02 has six internal PWMs, labeled PWM0-5. The PWM module consists of the following:

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

The application can access the PWM module through the FW driver.

Figure 13 shows the structure of one PWM channel.

Figure 13. PWM Block Diagram



PDM Microphone

The CYBT-4830xx-02 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM input shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYBT-4830xx-02 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

Note Subject to the driver support in WICED Studio.

I^2S Interface

The CYBT-4830xx-02 supports a single I^2S digital audio port with both master and slave modes. The I^2S signals are:

- I^2S Clock: I^2S SCK
- I^2S Word Select: I^2S WS
- I^2S Data Out: I^2S DO
- I^2S Data In: I^2S DI

I^2S SCK and I^2S WS become outputs in master mode and inputs in slave mode, while I^2S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSN of the left-channel data is aligned with the MSB of the I^2S bus, per I^2S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I^2S WS transition, synchronous with the falling edge of bit clock. Left Channel data is transmitted when I^2S WS is low, and right-channel data is transmitted when I^2S WS is high. Data bits sent by the CYBT-4830xx-02 are synchronized with the falling edge of I^2S SCK and should be sampled by the receiver on the rising edge of the I^2S SCK.

Note The PCM interface shares HW with the I^2S interface and only one can be used at a given time.

PCM Interface

The CYBT-4830xx-02 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-4830xx-02 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-4830xx-02.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Note The PCM interface shares HW with the I^2S interface and only one can be used at a given time.

Slot Mapping

The CYBT-4830xx-02 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The CYBT-4830xx-02 supports both short- and long-frame synchronization in both master and slave modes. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCGM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The CYBT-4830xx-02 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYBT-4830xx-02 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Security Engine

The CYBT-4830xx-02 includes a hardware security accelerator which greatly decreases the time required to perform typical security operations. Access to the hardware block is provided via a firmware interface.

This security engine includes:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)

Note Security Engine is used only by the Bluetooth stack to reduce CPU overhead. It is not available for application use.

Random Number Generator

This hardware block is used for key generation for Bluetooth.

Note Availability for use by the application is subject to the support in WICED Studio.

Note The Random Number Generator block must be warmed up prior to use. A delay of 500 ms from cold boot is necessary prior to using the Random Number Generator.

Power Modes

The CYBT-4830xx-02 support the following HW power modes are supported:

- **Active mode** - Normal operating mode in which all peripherals are available and the CPU is active.
- **Idle mode** - In this mode, the CPU is in “Wait for Interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- **Sleep mode** - In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- **PDS mode** - This mode is an extension of the PMU Sleep wherein most of the peripherals such as UART and SPI are turned off. The entire memory is retained, and on wakeup the execution resumes from where it paused.
- **Shut Down Sleep (SDS)** - Everything is turned off except the IO Power Domain, RTC, and LPO. The device can come out of this mode either due to BT activity or by an external interrupt. Before going into this mode, the application can store some bytes of data into “Always On RAM” (AON). When the device comes out of this mode, the data from AON is restored. After waking from SDS, the application will start from the beginning (warmboot) and has to restore its state based on information stored in AON. In the SDS mode, a single BT task with no data activity, such as an ACL connection, Bluetooth LE connection, or Bluetooth LE advertisement can be performed.
- **HIDOFF (Timed-Wake) mode** - The device can enter this mode asynchronously, that is, the application can force the device into this mode at any time. IO Power Domain, RTC, and LPO are the only active blocks. A timer that runs off the LPO is used to wake the device up after a predetermined fixed time.
- **HIDOFF (External Interrupt-Waked) mode** - This mode is similar to Timed-Wake, but in HID-off mode even the LPO and RTC are turned off. So, the only wakeup source is an external interrupt.

Transition between power modes is handled by the on-chip firmware with host/application involvement. Refer to the Firmware Section for details.

Firmware

The CYBT-4830xx-02 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the BT/LE baseband, LM, HCI, GATT, ATT, L2CAP and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes.

The CYBT-4830xx-02 is fully supported by the Cypress WICED Studio platform. WICED releases provide latest ROM patches, drivers, and sample applications allowing customized applications using the CYBT-4830xx-02 to be built quickly and efficiently.

Refer to WICED Technical Brief and CYBT-4830xx-02 Product Guide for details on the firmware architecture, driver documentation, power modes and how to write applications/profiles using the .

Electrical Characteristics

The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 12. Silicon Absolute Maximum Ratings

Requirement Parameter	Specification			Unit
	Min	Nom	Max	
Maximum Junction Temperature	–	–	125	°C
VDD IO	–0.5	–	3.795	V
VDD RF	–0.5	–	1.38	V
VDDBAT3V	–0.5	–	3.795	V
DIGLDO_VDDIN1P5	–0.5	–	1.65	V
RFLDO_VDDIN1P5	–0.5	–	1.65	V
PALDO_VDDIN_5V	–0.5	–	3.795	V
MIC_AVDD	–0.5	–	3.795	V

Table 13. ESD/Latchup

Requirement Parameter	Specification			Unit
	Min	Nom	Max	
ESD Tolerance HBM (Silicon)	–2000	–	2000	V
ESD Tolerance CDM (Silicon)	–500	–	500	V
Latch-up	–	200	–	mA

Table 14. Power Supply Specifications

Parameter	Conditions	Min	Typ	Max	Unit
V_{DD} Input	Module Chipset Input	1.76	3.0	3.63	V
V_{DDPA} Input	Module PA/LNA Input	2.0	3.0	3.60	V
V_{DD} Ripple	Module Input Ripple (V_{DDPA}, V_{DD})	–	–	100	mV
V_{BAT} Input	Internal to Module (not accessible)	1.90	3.0	3.6	V
PMU turn-on time	V_{BAT} is ready	–	–	300	µs

The CYBT-4830xx-02 uses an onboard low voltage detector to shut down the part when supply voltage (V_{DD}) drops below operating range.

Table 15. Power Supply Shut Down Specifications

Parameter	Min	Typ	Max	Unit
V_{SHUT}	1.625	1.7	1.76	V

Table 16. Bluetooth, Bluetooth LE, BR and EDR Current Consumption

Parameter	Description	Silicon or Module Parameter	Typ	Unit
HCI	48 MHz with Pause	Silicon	1.1	mA
HCI	48 MHz without Pause	Silicon	2.2	mA
RX	Continuous RX	Silicon	5.9	mA
TX	Continuous TX - 0 dBm	Silicon	5.6	mA
PDS	–	Silicon	6.1	µA
HID-Off (SDS)	32 kHz XTAL and 16 KB Retention RAM on	Silicon	1.6	µA
Advertising	Unconnectable - 1 second	Silicon	14	µA
Advertising	Connectable Undirected - 1 second	Silicon	17	µA
Page Scan - PDS	Interlaced - R1	Silicon	122	µA
Sniff - PDS	500 ms Sniff, 1 attempt, 0 timeout - Master	Silicon	132	µA
Sniff - PDS	500 ms Sniff, 1 attempt, 0 timeout - Slave	Silicon	138	µA
Bidirectional Data Exchange	Continuous DM5 or DH5 packets - Master or Slave	Silicon	6.9	mA
Bluetooth Low Energy (20 dBm)				
RX Peak	Peak RX current	Module	8.8	mA
TX Peak	Peak TX Current	Module	90	mA
PDS	–	Module	13.9	µA
HID-Off (SDS)	–	Module	14.9	µA
Advertising - SDS	Connectable Undirected - 1 second	Module	48	µA
LE Connection - SDS	Slave - 1 second	Module	35	µA
Bluetooth Classic (BR, EDR, 20 dBm)				
IDLE	Module is idle, non-discoverable and non-connectable	Module	8.3	µA
Iscan	Inquiry scan (1.28 seconds)	Module	160	µA
Pscan	Page scan (1.28 seconds)	Module	160	µA
IScan + Pscan	Inquiry scan + Page Scan (1.28 seconds)	Module	10.4	µA
Connected	Connected with no data transfer	Module	12.7	mA
Connected + Pscan	Connected with no data transfer + Page Scan (1.28 seconds)	Module	12.75	mA
Connected + IScan + Pscan	Connected with no data transfer + Inquiry Scan (1.28 seconds) + Page Scan (1.28 seconds)	Module	12.9	mA
Connected + SNIFF	Connected with no data transfer + SNIFF (500 ms)	Module	10	mA
Connected + SNIFF + IScan + Pscan	Connected with no data transfer + SNIFF (500 ms) + Inquiry Scan and Page Scan 1.28 seconds	Module	10.5	mA
TX_BR	Data transfer @115200 baud rate	Module	21.5	mA
TX + SNIFF_BR	Data transfer @115200 baud rate + Sniff (500 ms)	Module	14.5	mA

Table 17. Power Amplifier/Low Noise Amplifier Current Consumption Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
TX High Power Current	Pout = +20dBm	–	100	–	mA
TX Quiescent Current	No RF applied	–	17	–	mA
RX Quiescent Current	No RF applied	–	8	–	mA

Core Buck Regulator

Table 18. Silicon Core Buck Regulator

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage DC, V_{BAT}	DC voltage range inclusive of disturbances	1.90	3.0	3.63	V
CBUCK output current	LPOM only	–	–	65	mA
Output voltage range	Programmable, 30 mV/step default = 1.2V (bits = 0000)	1.2	1.26	1.5	V
Output voltage DC accuracy	Includes load and line regulation	–4	–	+4	%
LPOM efficiency (high load)	–	–	85	–	%
LPOM efficiency (low load)	–	–	80	–	%
Input supply voltage ramp-up time	0 to 3.3V	40	–	–	µs

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

Digital LDO

Table 19. Digital LDO

Parameter	Conditions	Min	Typ	Max	Unit
Input supply voltage, Vin	Minimum Vin = Vo + 0.12V requirement must be met under maximum load.	1.2	1.2	1.6	V
Nominal output voltage, Vo	Internal default setting	–	1.1	–	V
Dropout voltage	At maximum load	–	–	120	mV

Digital I/O Characteristics

Table 20. Digital I/O Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage (V_{DD} = 3V)	V_{IL}	–	–	0.8	V
Input high voltage (V_{DD} = 3V)	V_{IH}	2.4	–	–	V
Input low voltage (V_{DD} = 1.8V)	V_{IL}	–	–	0.4	V
Input high voltage (V_{DD} = 1.8V)	V_{IH}	1.4	–	–	V
Output low voltage	V_{OL}	–	–	0.45	V
Output high voltage	V_{OH}	V_{DDO} – 0.45V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (V_{DD} = 3V, V_{OL} = 0.5V)	I_{OL}	–	–	8.0	mA
Output low current (V_{DD} = 1.8V, V_{OL} = 0.5V)	I_{OL}	–	–	4.0	mA
Output high current (V_{DD} = 3V, V_{OH} = 2.55V)	I_{OH}	–	–	8.0	mA
Output high current (V_{DD} = 1.8V, V_{OH} = 1.35V)	I_{OH}	–	–	4.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

ADC Electrical Characteristics

Table 21. Electrical Characteristics

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
Current consumption	I_{TOT}	–	–	2	3	mA
Power down current	–	At room temperature	–	1	–	µA
ADC Core Specification						
ADC reference voltage	V_{REF}	From BG with ±3% accuracy	–	0.85	–	V
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset and distortion. Without factory calibration.	–	–	5	%
		Includes gain error, offset and distortion. After factory calibration.	–	–	2	%
ENOB	–	For audio application	12	13	–	Bit
		For static measurement	10	–	–	
ADC input full scale	FS	For audio application	–	1.6	–	
		For static measurement	1.8	–	3.6	
Conversion rate	–	For audio application	8	16	–	kHz
		For static measurement	50	100	–	
Signal bandwidth	–	For audio application	20	–	8K	Hz
		For static measurement	–	DC	–	
Input impedance	R_{IN}	For audio application	10	–	–	KW
		For static measurement	500	–	–	
Startup time	–	For audio application	–	10	–	ms
		For static measurement	–	20	–	µs
MIC PGA Specifications						
MIC PGA gain range	–	–	0	–	42	dB
MIC PGA gain step	–	–	–	1	–	dB
MIC PGA gain error	–	Includes part-to-part gain variation	–1	–	1	dB
PGA input referred noise	–	At 42 dB PGA gain A-weighted	–	–	4	µV
Passband gain flatness	–	PGA and ADC, 100 Hz–4 kHz	–0.5	–	0.5	dB
MIC Bias Specifications						
MIC bias output voltage	–	At 2.5-V supply	–	2.1	–	V
MIC bias loading current	–	–	–	–	3	mA
MIC bias noise	–	Refers to PGA input 20 Hz to 8 kHz, A-weighted	–	–	3	µV
MIC bias PSRR	–	at 1 kHz	40	–	–	dB
ADC SNR	–	A-weighted 0 dB PGA gain	78	–	–	dB
ADC THD + N	–	–3 dB FS input 0 dB PGA gain	74	–	–	dB
GPIO input voltage		Always lower than V_{DDBAT}	–	–	3.6	V
GPIO source impedance[6]	–	Resistance	–	–	1	kΩ
		Capacitance	–	–	10	pF

Note
6. Conditional requirement for the measurement time of 10 ms. Relaxed with longer measurement time for each GPIO input channel.

Chipset RF Specifications

Table 22 and Table 23 apply to single-ended industrial temperatures. Unused inputs are left open.

Table 22. Chipset Receiver RF Specifications

Parameter	Mode and Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity[7]	GFSK, 0.1% BER, 1 Mbps	–	–92.0[7]	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–94.0[8]	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–88.0[8]	–	dBm
Maximum input	All data rates	–	–	–20	dBm
GFSK Modulation					
C/I cochannel	GFSK, 0.1% BER[7]	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER[8]	–	–	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER[9]	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER[7]	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER[9]	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER[9]	–	–	–20.0	dB
QPSK Modulation					
C/I cochannel	π/4-DQPSK, 0.1% BER[9]	–	–	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER[4]	–	–	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER[9]	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER[5]	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER[9]	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER[9]	–	–	–20.0	dB
8PSK Modulation					
C/I cochannel	8-DPSK, 0.1% BER[9]	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER[9]	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER[9]	–	–	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER[5]	–	–	–33.0	dB
C/I image channel	8-DPSK, 0.1% BER[9]	–	–	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER[9]	–	–	13	dB
Out-of-Band Blocking Performance (CW)[10]					
30 MHz to 2000 MHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
2000 MHz to 2399 MHz	BDR GFSK 0.1% BER	–	–27.0	–	dBm
2498 MHz to 3000 MHz	BDR GFSK 0.1% BER	–	–27.0	–	dBm
3000 MHz to 12.75 GHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
Inter-modulation Performance[7]					
BT, interferer signal level	BDR GFSK 0.1% BER	–	–	–39.0	dBm
Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–55.0	dBm

Notes
7. Dirty TX is Off.
8. Up to 1 dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
9. The receiver sensitivity is measured at BER of 0.1% on the device interface.
10. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
11. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
12. Desired signal is -64 dBm Bluetooth-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth modulated signal at frequency f2, f0 = 2 * f1 – f2, and |f2 – f1| = n * 1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.

Table 23. Chipset Transmitter RF Specifications

Parameter	Min	Typ	Max	Unit
Transmitter Section				
Frequency range	2402	–	2480	MHz
Class 2: GFSK TX power	–	4.0	–	dBm
Class 2: EDR TX Power	–	0	–	dBm
20 dB bandwidth	–	930	1000	kHz
Adjacent Channel Power				
|M – N| = 2	–	–	–20	dBm
|M – N| ≥ 3	–	–	–40	dBm
Out-of-Band Spurious Emission				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	dBm
1.8 GHz to 1.9 GHz	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–47.0	dBm
LO Performance				
Initial carrier frequency tolerance	–75	–	+75	kHz
Frequency Drift				
DH1 packet	–25	–	+25	kHz
DH3 packet	–40	–	+40	kHz
DH5 packet	–40	–	+40	kHz
Drift rate	–20		20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	kHz
Channel spacing	–	1	–	MHz
Modulation Accuracy				
π/4-DQPSK Frequency Stability	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	20	%
π/4-QPSK Peak DEVM	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	30	%
8-DPSK frequency stability	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	13	%
8-DPSK Peak DEVM	–	–	25	%
8-DPSK 99% DEVM	–	–	20	%
In-Band Spurious Emissions				
1.0 MHz < |M – N| < 1.5 MHz	–	–	–26	dBm
1.5 MHz < |M – N| < 2.5 MHz	–	–	–20	dBm
|M – N| > 2.5 MHz	–	–	–40	dBm

Table 24. Bluetooth LE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sensitivity (QFN)[13]	LE GFSK, 0.1% BER, 1 Mbps	–	–95.0[14]	–	dBm
TX power	Bluetooth LE Silicon Device CYW20719 Only	–	4.0	–	dBm
TX power	Module total output power	–	–	20	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[15]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

Notes
13. Dirty TX is Off.
14. Up to 1 dB of variation may potentially be seen from typical sensitivity specs due to the chip, board and associated variations.
15. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Table 25. CYBT-4830xx-02 GPS and GLONASS Band Spurious Emission

Parameter	Condition	Min	Typ	Max	Unit
1570-1580 MHz	GPS	–	–160	–	dBm/Hz
1592-1610 MHz	GLONASS	–	–159	–	dBm/Hz

Timing and AC Characteristics

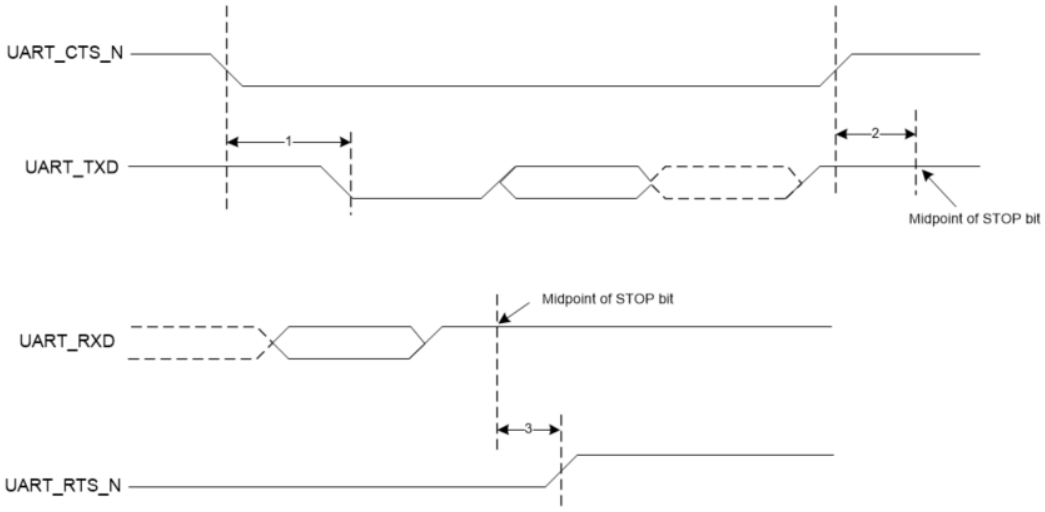
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 26. UART Timing Specifications

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

Figure 14. UART Timing



SPI Timing

The SPI interface can be clocked up to 24 MHz.

Table 27 and Figure 15 show the timing requirements when operating in SPI Mode 0 and 2.

Table 27. SPI Mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 15. SPI Timing, Mode 0 and 2

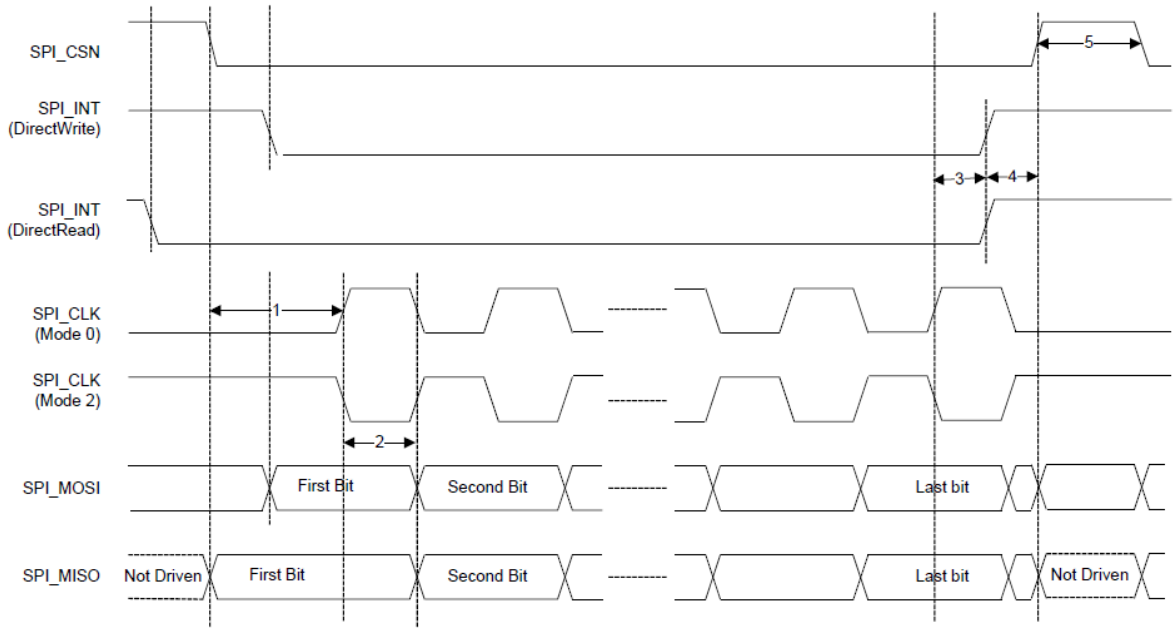
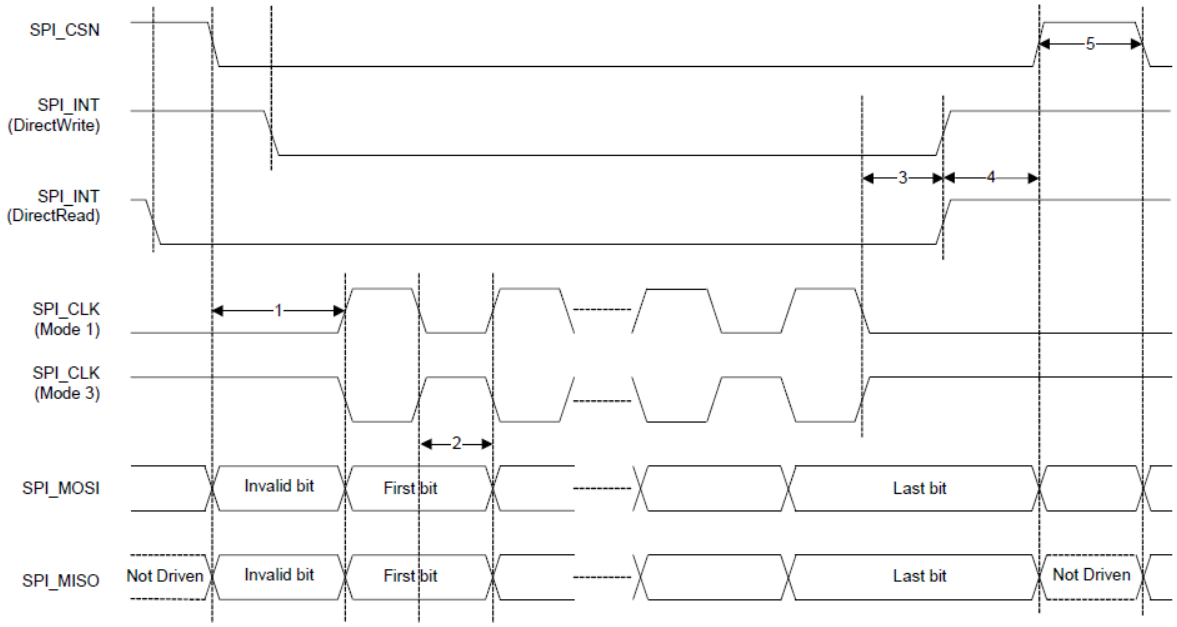


Table 28 and Figure 16 show the timing requirements when operating in SPI Mode 1 and 3.

Table 28. SPI Mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 16. SPI Timing, Mode 1 and 3



I²C Compatible Interface Timing

The specifications in Table 29 references Figure 17.

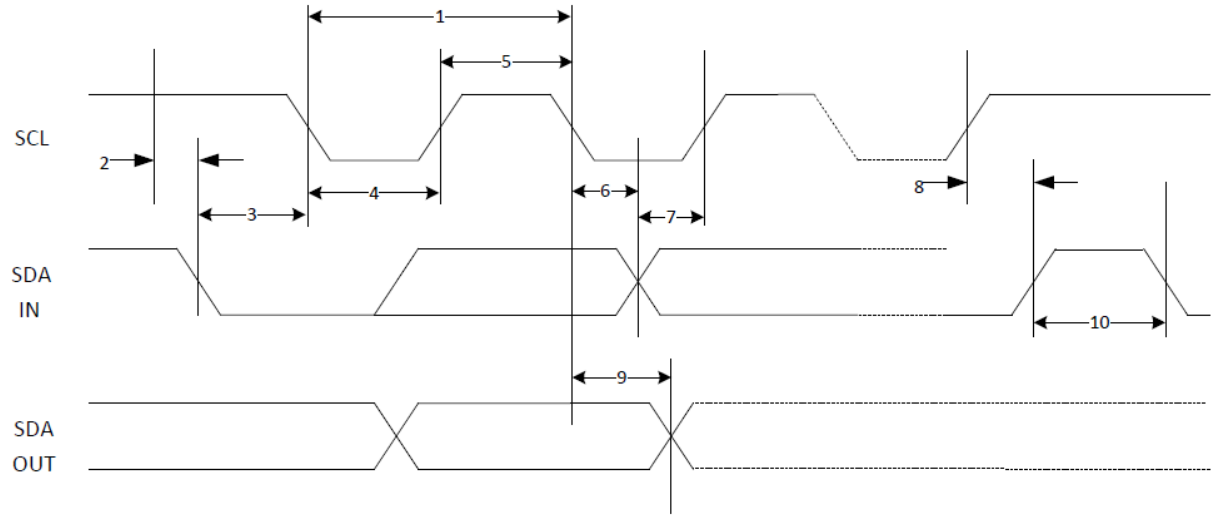
Table 29. I²C Compatible Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[16]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[17]	650	–	ns

Notes

16. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
17. Time that the CBUS must be free before a new transaction can start.

Figure 17. I²C Interface Timing Diagram



I²S Interface Timing

I²S timing is shown below in Table 30, Figure 18, and Figure 19.

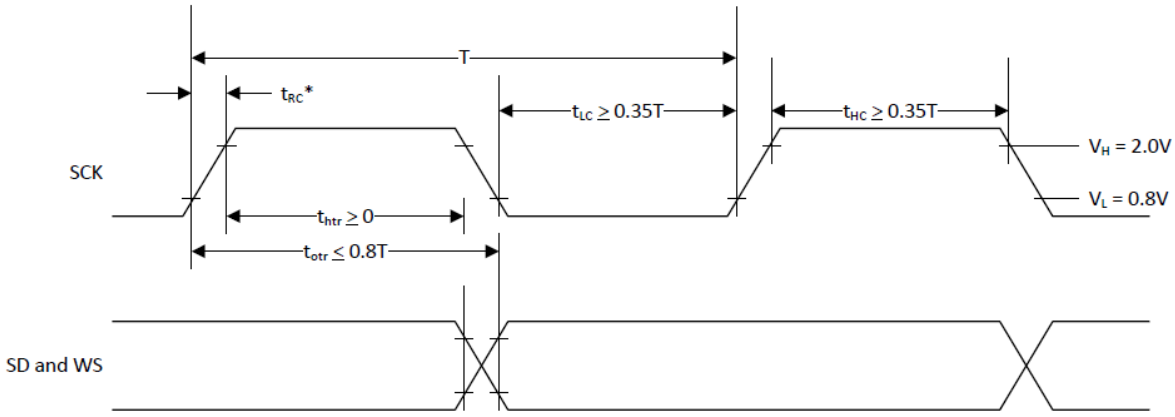
Table 30. Timing for I²S Transmitters and Receivers

Parameter	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	Note 18
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 19
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 19
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 20
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 20
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	Note 21
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	Note 22
Hold time t_{htr}	0	–	–	–	–	–	–	–	Note 21
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_{tr}$	–	–	–	Note 23
Hold time t_{hr}	–	–	–	–	$0.2T_{tr}$	–	–	–	Note 23

Notes

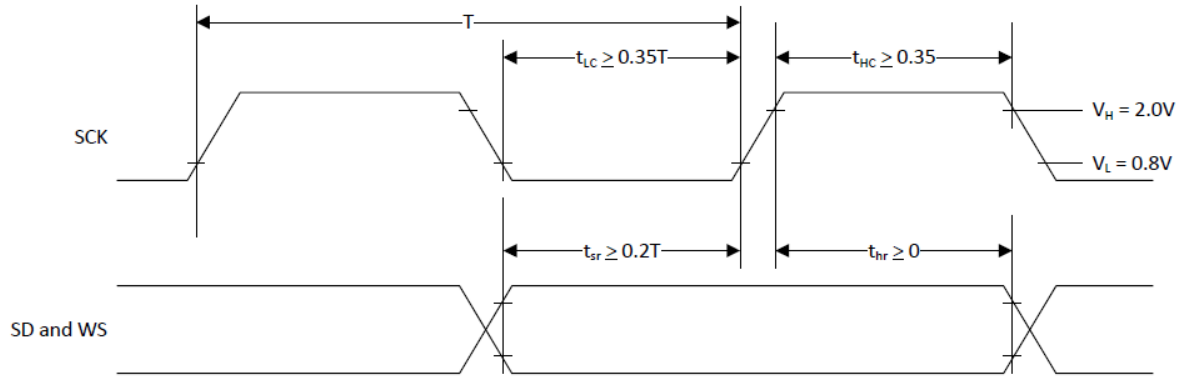
18. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
19. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
20. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
21. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
22. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
23. The data setup and hold time must not be less than the specified receiver setup and hold time.

Figure 18. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 19. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Environmental Specifications

Environmental Compliance

This Cypress Bluetooth LE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

RF Certification

The CYBT-4830xx-02 module is certified under the following RF certification standards:

- FCC: WAP3039
- IC: 7922A-3039
- MIC: 203-JN0875
- CE

Safety Certification

The CYBT-4830xx-02 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

Environmental Conditions

Table 31 describes the operating and storage conditions for the Cypress Bluetooth LE module.

Table 31. Environmental Conditions for CYBT-4830xx-02

Description	Minimum Specification	Maximum Specification
Operating temperature	–30 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	10 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into system Components[24]	–	15 kV Air 2.0 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
24. This does not apply to the RF pins (ANT).

Regulatory Information

FCC

FCC NOTICE:

The device CYBT-4830xx-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP3039.

In any case the end product must be labeled exterior with “Contains FCC ID: WAP3039”.

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in Table 7 on page 15. When integrated in the OEMs product, this fixed antenna requires installation preventing end-users from replacing them with non-approved antennas. Any antenna not in Table 7 must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in Table 7, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBT-4830xx-02 with the integrated chip antenna (FCC ID: WAP3039) is far below the FCC radio frequency exposure limits. Nevertheless, use CYBT-4830xx-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

ISED

Innovation, Science and Economic Development (ISED) Canada Certification

CYBT-4830xx-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-3039

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 7 on page 15, having a maximum gain of -0.5 dBi. Antennas not included in Table 7 or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 Ω. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBT-4830xx-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBT-4830xx-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is 7922A-3039. In any case, the end product must be labeled in its exterior with “Contains IC: 7922A-3039”.

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage ISED sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Cypress Semiconductor IC approprié pour ce produit ainsi que l'avis ISED ci-dessus. L'identificateur IC est 7922A-3039. En tout cas, le produit final doit être étiqueté dans son extérieur avec “Contient IC: 7922A-3039”.

European Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBT-4830xx-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

All versions of the CYBT-4830xx-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBT-4830xx-02 is certified as a module with certification number 203-JN0875. End products that integrate CYBT-4830xx-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Model Name: EZ-BT WICED Module

Part Number: CYBT-483056-02, CYBT-483062-02

Manufactured by Cypress Semiconductor.

203-JN0875

Packaging

Table 32. Solder Reflow Peak Temperature

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBT-483056-02	34-pad SMT	260 °C	30 seconds	2
CYBT-483062-02	34-pad SMT	260 °C	30 seconds	2

Table 33. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBT-483056-02	34-pad SMT	MSL 3
CYBT-483062-02	34-pad SMT	MSL 3

CYBT-4830xx-02 is offered in tape and reel packaging. Figure 20 details the tape dimensions used for the CYBT-4830xx-02.

Figure 20. CYBT-4830xx-02 Tape Dimensions

Item	W	A_0	B_0	K_0	P	F	E	D_0	D_1	P_0	P_2	T
Measurement	$24.0^{+0.30}_{-0.30}$	$19.00^{+0.10}_{-0.10}$	$13.20^{+0.10}_{-0.10}$	$2.30^{+0.10}_{-0.10}$	$24.00^{+0.10}_{-0.10}$	$11.5^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$1.50^{+0.10}_{-0.10}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$0.30^{+0.05}_{-0.05}$

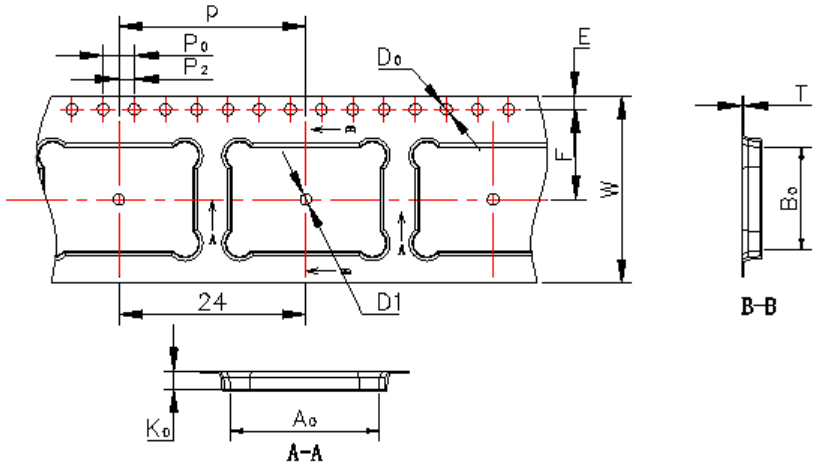


Figure 21 details the orientation of the CYBT-4830xx-02 in the tape as well as the direction for unreeling.

Figure 21. Component Orientation in Tape and Unreeling Direction (TBD)

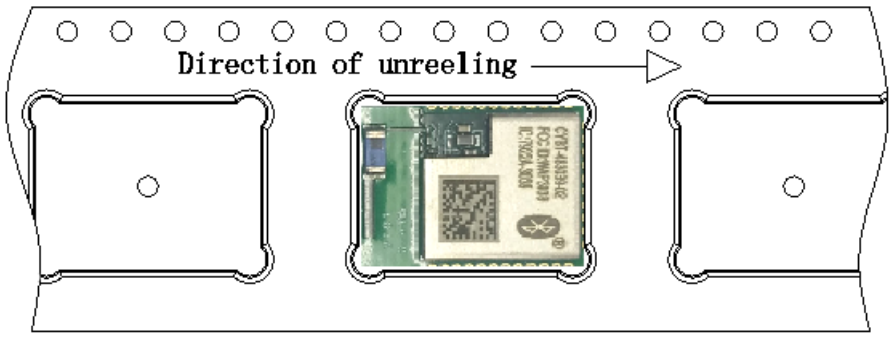
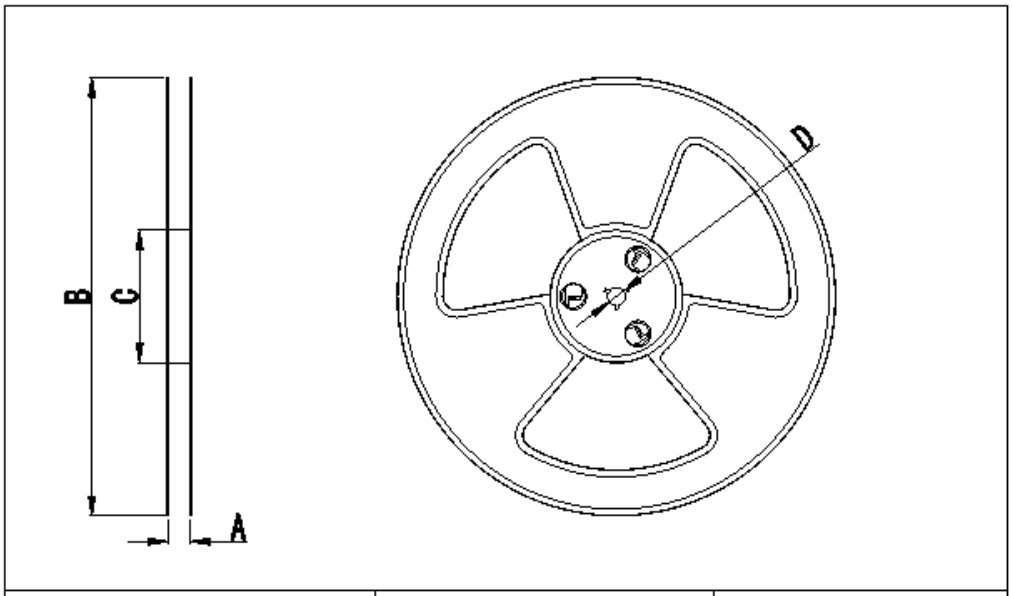


Figure 22 details reel dimensions used for the CYBT-4830xx-02.

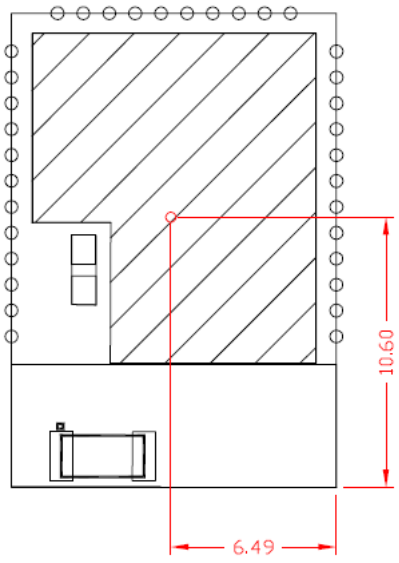
Figure 22. Reel Dimensions



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.4	+2.0mm	-0.0mm
B	Reel Diameter	254.00	+2.0mm	-2.0mm
C	Outer Axis Diameter	100.00	+2.0mm	-2.0mm
D	Inner Axis Diameter	13.20	+0.3mm	-0.2mm

CYBT-4830xx-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBT-4830xx-02 is detailed in Figure 23.

Figure 23. CYBT-4830xx-02 Center of Mass



Top View (Seen from Top)

Ordering Information

Table 34 lists the CYBT-4830xx-02 part number and features. Table 34 also lists the target program for the respective module ordering codes. Table 35 lists the reel shipment quantities for the CYBT-4830xx-02.

Table 34. Ordering Information

Ordering Part Number	Main Chip Part Number	Max CPU Speed (MHz)	Flash Size (KB)	RAM Size (KB)	UART	I^2C	SPI	I^2S	PCM	PWM	ADC Inputs	GPIOs	Package	Packaging
CYBT-483056-02	CYW20719B2KUMLG	96	1024	512	Yes	Yes	Yes	Yes	Yes	6	10	15	34-SMT	Tape and Reel
CYBT-483062-02	CYW20721B2KUMLG	96	1024	512	Yes	Yes	Yes	Yes	Yes	6	10	15	34-SMT	Tape and Reel

Table 35. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	500	500	Ships in 500 unit reel quantities.
Minimum Order Quantity (MOQ)	500	–	–
Order Increment (OI)	500	–	–

CYBT-4830xx-02 is offered in tape and reel packaging. CYBT-4830xx-02 ships in a reel size of 500 units.

For additional information and a complete list of Cypress Semiconductor Bluetooth products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

U.S. Cypress Headquarters Address	198 Champion Court, San Jose, CA 95134
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Acronyms

Table 36. Acronyms Used in this Document

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
ISED	Innovation, Science and Economic Development (Canada)
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
OTA	Over-the-Air
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

Document Conventions

Units of Measure

Table 37. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
µA	microamperes
µm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

Document History Page

Document Title: CYBT-483056-02/CYBT-483062-02, EZ-BT™ XR WICED® Module Document Number: 002-30915			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	6935829	07/28/2020	Initial release.
*A	7047771	12/17/2020	Replaced “Bluetooth Low Energy (BLE)” with “Bluetooth Low Energy” in all instances across the document. Replaced “BLE” with “Bluetooth LE” in all instances across the document.

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