EZ-PD™ CCG3PA2 Datasheet

USB Type-C Port Controller

General Description

EZ-PD™ CCG3PA2 is Cypress' highly integrated USB Type-C port controller that complies with the latest USB Type-C and PD standards and is targeted for cable and power adapters applications. In such applications, CCG3PA2 provides additional functionalities and BOM integration advantages. CCG3PA2 uses Cypress' proprietary M0S8 technology with a 32-bit Arm® Cortex®-M0 processor, 2×64-KB flash, a complete Type-C USB-PD transceiver, all termination resistors required for a Type-C port, an integrated feedback control circuitry for voltage (VBUS) regulation, and system-level ESD protection in 32-pin QFN and 30-ball CSP packages.

Features

Type-C Support and USB-PD Support

- Supports USB PD3.0 Version 1.1 Spec including Programmable Power Supply Mode
- Configurable resistors R_P, R_D, and R_A
- Supports one USB Type-C port and one Type-A port
- Firmware control to electrically disconnect R_A when not required in order to save source power

2× Legacy/Proprietary Charging Blocks

- Supports QC 4.0, Apple charging 2.4A, AFC, BC 1.2
- Integrates all required terminations on DP/DM lines

Integrated Voltage (VBUS) Regulation and Current Sense Amplifier

- Analog regulation of secondary side feedback node (direct feedback or opto coupler)
- Integrated shunt regulator function for VBUS control
- Constant current or constant voltage mode
- Supports low-side current sensing for constant current control

System-Level Fault Protection

- On-chip OVP, OCP, UVP, and SCP
- Supports OTP through integrated ADC circuit
- Short to VBUS protection for CC, SBU, and VCONN pins up to 24.5VDC

32-bit MCU Subsystem

- Arm Cortex-M0 CPU
- 2x64-KB Flash
- 8-KB SRAM

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 3.0 V to 24.5 V operation (using on-chip 30VAC tolerant LDO)
- Deep Sleep: 15 µA, Sleep: 3 mA
- Integrated 24.5VDC, 30VAC tolerant regulator and VBUS control signals

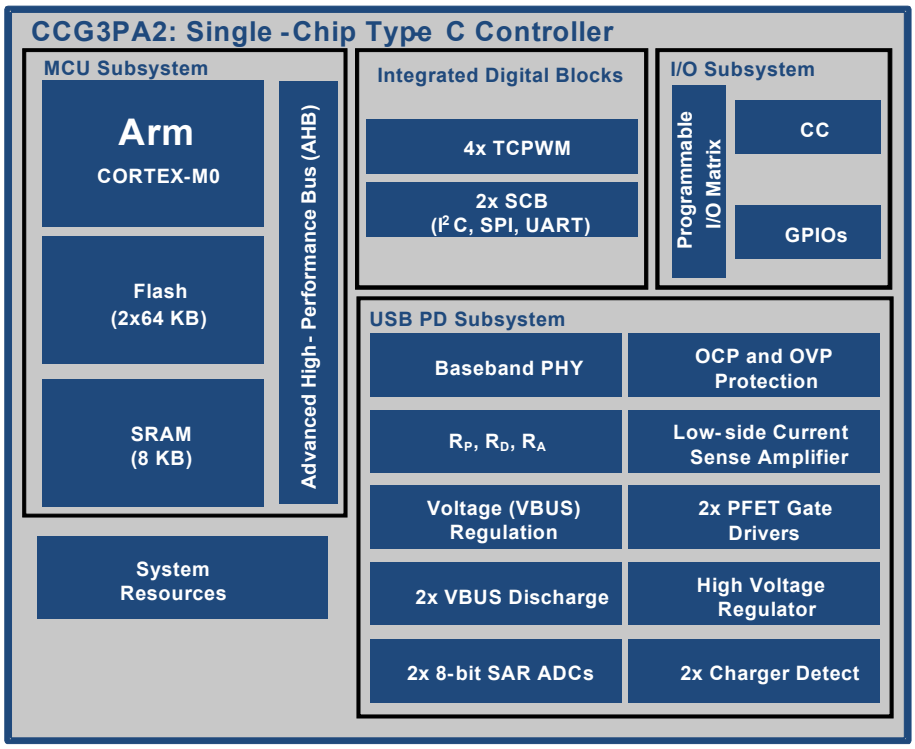
System-Level ESD Protection

- On CC, VCONN, VBUS_C_MON_DISCHARGE, SBU, and DP0/DM0 pins
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

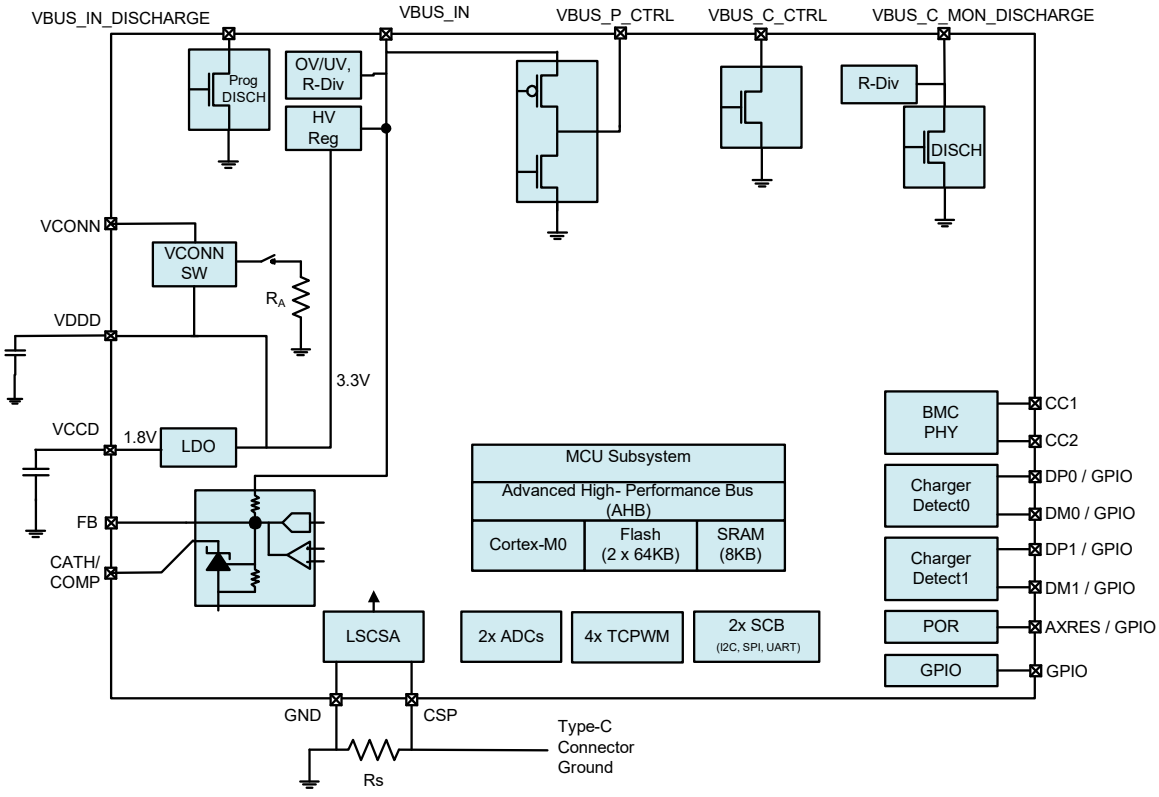
Packages

- 32-pin QFN
- 30-Ball WLCSP
- Supports extended industrial temperature range (–40 °C to +105 °C)

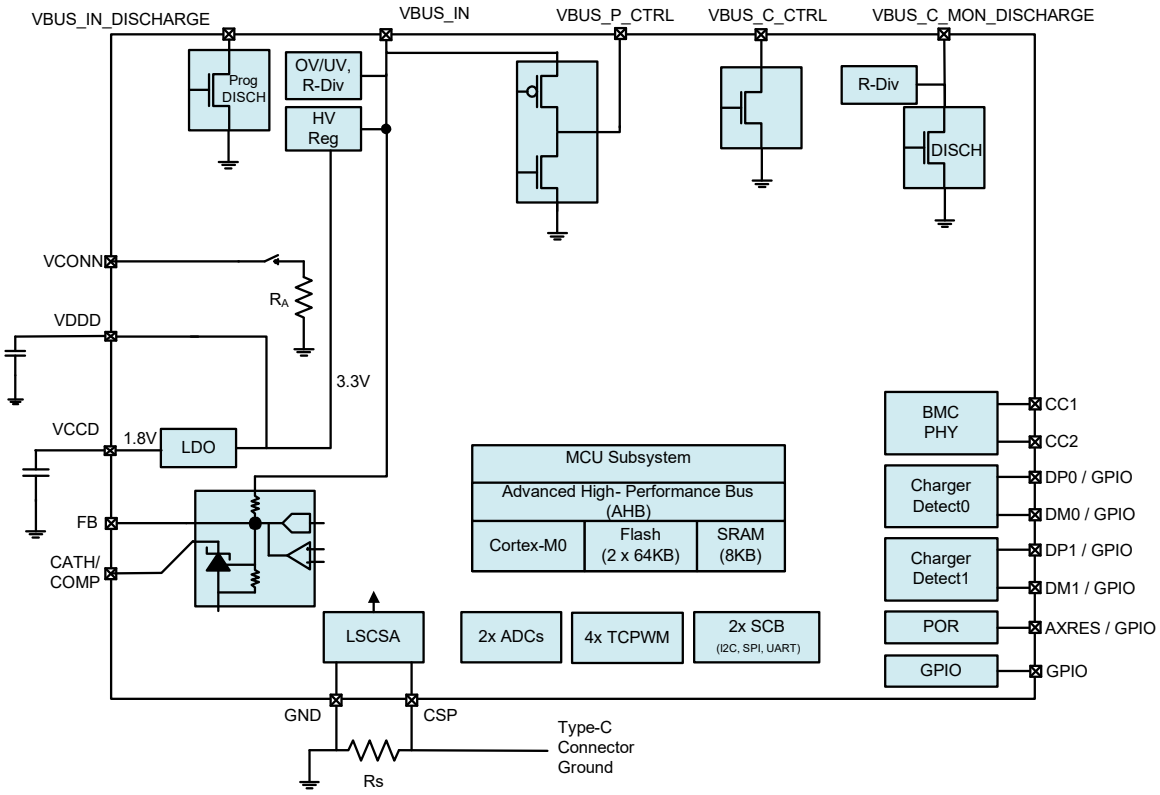
Logic Block Diagram



Internal Block Diagram (Silicon Rev = B1)



Internal Block Diagram (Silicon Rev = B2)



Contents

Functional Overview

MCU Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3PA2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG3PA2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3PA2 device has a flash module with two banks of 64-KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

The USB-PD subsystem provides the interface to the Type-C USB port. This subsystem comprises a current sense amplifier, a high-voltage regulator, OVP, OCP, and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD spec. R_P and R_D resistors are required to implement connection detection, plug orientation detection, and for establishing USB DFP/UFP roles. The R_P resistor is implemented as a current source.

ADC

The ADC is a low-footprint 8-bit SAR ADC that is available for general-purpose A-D conversion applications in the chip. This ADC can be accessed from all GPIOs and the DP/DM pins through an on-chip analog mux. CCG3PA2 contains two instances of the ADC. The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

Charger Detection

The two charger detection blocks connected to the two pairs of DP/DM pins allow CCG3PA2 to detect conventional battery chargers conforming to BC 1.2, and the following proprietary charger specifications: Apple, Qualcomm's QuickCharge 4.0, and Samsung AFC.

VBUS Overcurrent and Overvoltage Protection

The CCG3PA2 chip has an integrated hardware block for VBUS overvoltage protection (OVP)/overcurrent protection (OCP) with configurable thresholds and response times on the Type C port.

VBUS Short Protection

CCG3PA2 provides four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, CCG3PA2 can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the OVT pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without CCG3PA2 connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when CCG3PA2 is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

Low-side Current Sense Amplifier (CSA)

The CCG3PA2 chip also has an integrated low-side current sense amplifier that is capable of detecting current in the order of 100 mA across a 5-mΩ external resistor. It also supports constant current mode of operation in power adapter application as a provider.

PFET Gate Drivers on VBUS Path

CCG3PA2 has two integrated PFET gate drivers to drive external PFETs on the VBUS provider and consumer path. The VBUS_P_CTRL gate driver has an active pull-up, and thus can drive high, low or High-Z.

The VBUS_C_CTRL gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

VBUS Discharge FETs

CCG3PA2 also has two integrated VBUS discharge FETs used to discharge VBUS to meet the USB-PD specification timing on a detach condition. VBUS Discharge FET on the provider side can be used to accelerate the ramp down of VBUS to the default 5 V on the secondary side.

Voltage (VBUS) Regulation

CCG3PA2 contains an integrated feedback control circuitry (for AC/DC applications) for secondary side control with analog regulation of the feedback/cathode pins to achieve the appropriate voltage on VBUS pin as per the negotiated contract with the peer device over Type-C.

Integrated Digital Blocks

Serial Communication Blocks (SCB)

EZ-PD CCG3PA2 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD CCG3PA2 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on the SCB blocks of EZ-PD CCG3PA2 are not completely compliant with the I^2C spec in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3PA2 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

I/O Subsystem

EZ-PD CCG3PA2 has up to 17 GPIOs of which, some of them can be re-purposed to support functions of SCB (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (up to 7V).

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate Fault for OCP/SCP/OVP/UVP conditions. Any two fault conditions can be mapped to two GPIOs or all the four faults can be OR'ed to indicate over one GPIO.

Power Systems Overview

CCG3PA2 can operate from three possible external supply sources: VBUS_IN (2.7 V–24.5 V), VDDD (2.7 V–5.5 V) or VCONN (3.0 V–5.5 V). When powered through VBUS_IN, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. VCONN is chosen as a power source for EMCA cable applications only, as it offers the necessary termination resistance (Ra). Figure 1 and Figure 2 show the power sources supported by specific revisions of the silicon.

CCG3PA2 has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS_IN pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 1. CCG3PA2 Power Modes

Mode	Description
Power-On Reset (POR)	Power is valid and an internal reset source is asserted or Sleep Controller is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. Deep-Sleep regulator powers logic, but only low-frequency clock is available.

Figure 1. Power System Requirement Block Diagram (For Silicon Rev = B1)

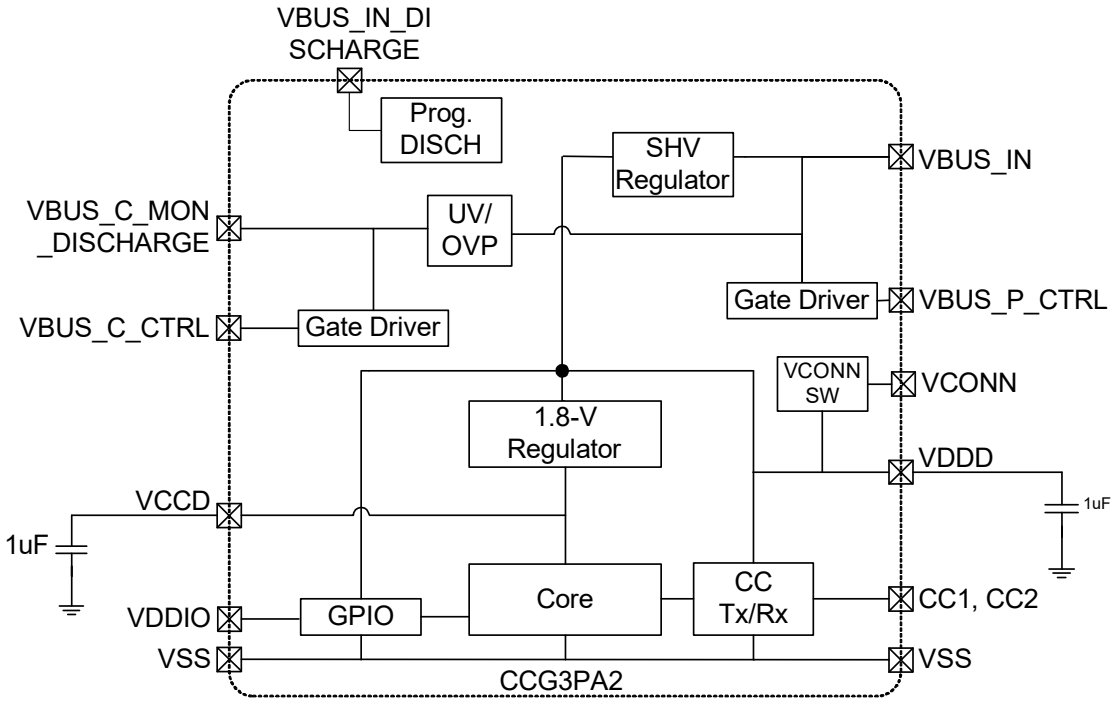
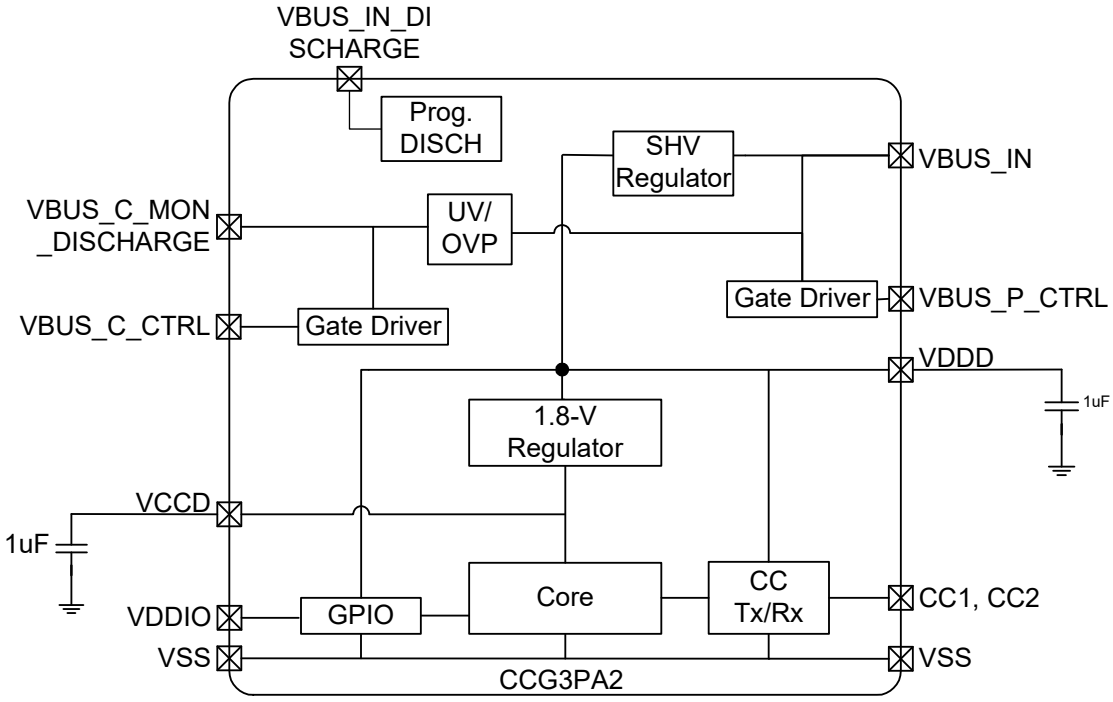


Figure 2. Power System Requirement Block Diagram (For Silicon Rev = B2)



Pinouts

Table 2. CCG3PA2 Pin Description

32-Pin QFN	30-Ball CSP	Pin Name	Description
1	E5	P1.0	This pin's default operation at chip power up is GPIO port 1, pin 0. It can also be reconfigured after chip power up as: I/O Operation: UART_1_CTS, SPI_0_SEL, I2C_SDA_1[1] or TCPWM_line_2[2]. Analog Operation: Input with programmable thresholds for simultaneous Short Circuit Protection (SCP), Over-Current Protection (OCP), Over-Voltage Protection (OVP) or Under-Voltage Protection (UVP) fault indication.
2	D5	P1.1	This pin's default operation at chip power up is GPIO port 1, pin 1. This pin can also be reconfigured after chip power up as: I/O Operation: UART_1_RTS, SPI_0_MISO, I2C_SCL_1[1] or TCPWM_line_3[3]. Analog Operation: Input with programmable thresholds for simultaneous Short Circuit Protection (SCP), Over-Current Protection (OCP), Over-Voltage Protection (OVP) or Under-Voltage Protection (UVP) fault indication.
3	D4	XRES	Chip RESET pin
4	E4	P1.4	This pin is a GPIO on port 1, pin 4.
5	N/A	P1.5	This pin is a GPIO on port 1, pin 5.
6	E3	VBUS_P_CTRL	Provider (PMOS) FET control (30VAC Tolerant) 0: Path ON 1: Path OFF
7	D3	VBUS_C_CTRL	VBUS Consumer (PMOS) FET Control (30VAC Tolerant) 0: Path ON Z: Path OFF
8	E2	DP1/P1.2	This pin's default operation at chip power up is USB Port 1 D-Positive pin and is capable of charging protocols for AFC, QC, USB BC1.2 and Apple Charging simultaneously. It can also be reconfigured after chip power up as: I/O Operation: UART_1_TX1 or SPI_0_MOSI.
9	E1	DM1/P1.3	This pin's default operation at chip power up is USB Port 1 D-Minus pin and is capable of charging protocols for AFC, QC, USB BC1.2 and Apple Charging simultaneously. This pin can also be reconfigured after chip power up as: I/O Operation: UART_1_RX1 or SPI_0_CLK.
10	N/A	P2.4	This pin is a GPIO on port 2, pin 4.
11	N/A	P2.5	This pin is a GPIO on port 2, pin 5.

Notes
1. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.
2. TCPWM_line_2 can be mapped to port pins P1.0 or P2.0.
3. TCPWM_line_3 can be mapped to port pins P2.1 or P1.1.

Table 2. CCG3PA2 Pin Description *(continued)*

32-Pin QFN	30-Ball CSP	Pin Name	Description
12	C3	P2.0	This pin's default operation at chip power up is GPIO port 2, pin 0. It can also be configured after chip power up as: I/O Operation: UART_0_TX0, SPI_1_SEL or TCPWM_line_2[4].
13	D2	P2.1	This pin's default operation at chip power up is GPIO port 2, pin 1. It can also be configured after chip power up as: I/O Operation: UART_0_RX0, SPI_1_CLK or TCPWM_line_3[5].
14	D1	VCONN	Protection: Tolerant to temporary short to VBUS with a maximum of 24.5VDC. 8kV IEC ESD protection for direct connection to the Type-C connector pin. VCONN input with R_A termination (3.0 V–5.5 V).
15	C1	SWD_DAT_0/P0.0	Protection: Tolerant to voltages above VDDIO with a maximum of 7VDC (OVT). This pin's default operation at chip power up is SWD_DAT_0 which is the data signal for chip programming and debug. This pin can also be reconfigured after chip power up as: I/O Operation: GPIO port 0 pin 0, UART_0_CTS, SPI_1_MOSI, I2C_SDA_0 or TCPWM_line_0[6]. Analog Operation: Input for Over Temperature Protection input from an external thermistor.
16	B1	SWD_CLK_0/P0.1	Protection: Tolerant to voltages above VDDIO with a maximum of 7VDC (OVT). This pin's default operation at chip power up is SWD_CLK_0 which is the clock signal for chip programming and debug. It can also be reconfigured after chip power up as: I/O Operation: GPIO port 0 pin 1, UART_0_RTS, SPI_1_MISO, I2C_SCL_0 or TCPWM_line_1[7].
17	C2	VBUS_C_MON_ DISCHARGE	VBUS consumer path voltage monitor with internal discharge FET. 8kV IEC ESD protection for direct connection to the Type-C connector pin (30VAC tolerant).
18	A1	P2.2/SBU1/GPIO_20VT[8]/ SWD_DAT_1	Protection: 8kV IEC ESD protection for direct connection to the Type-C connector pin. GPIO with Open drain with pull-up assist. Tolerant to temporary short to VBUS pin. This pin's default operation at chip power up is GPIO port 2, pin 2. This pin can also be reconfigured after chip power up as: I/O Operation: GPIO_20VT[8], I2C_SDA_1[9] or TCPWM_line_0[6].

Notes
4. TCPWM_line_2 can be mapped to port pins P1.0 or P2.0.
5. TCPWM_line_3 can be mapped to port pins P2.1 or P1.1.
6. TCPWM_line_0 can be mapped to port pins P0.0 or P2.2.
7. TCPWM_line_1 can be mapped to port pins P0.1 or P2.3.
8. See Table 9 on page 19 and Table 10 on page 19 for specifications related to these pins.
9. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I^2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I^2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.

Table 2. CCG3PA2 Pin Description *(continued)*

32-Pin QFN	30-Ball CSP	Pin Name	Description
19	A2	P2.3/SBU2/GPIO_20VT[10] /SWD_CLK_1	Protection: 8kV IEC ESD protection for direct connection to the Type-C connector pin. GPIO with Open drain with pull-up assist. Tolerant to temporary short to VBUS pin. This pin's default operation at chip power up is GPIO port 2, pin 3. It can also be reconfigured after chip power up as: I/O Operation: GPIO_20VT[10], I2C_SCL_1[11] orTCPWM_line_1[12].
20	B3	CC1	Protection: 8kV IEC ESD protection for direct connection to the Type-C connector pin. This pin is Communication Channel 1 pin.
21	A3	CC2	Protection: 8kV IEC ESD protection for direct connection to the Type-C connector pin. This pin is Communication Channel 2 pin.
22	A4	DP0/P3.0	Protection: 8kV IEC ESD protection for direct connection to the Type-C connector pin. This pin's default operation at chip power up is USB Port 0 D-Positive pin and is capable of charging protocols for AFC, QC, USB BC1.2 and Apple Charging simultaneously. It can also be reconfigured after chip power up as: I/O Operation: UART_1_TX0.
23	B2	VBUS_IN	Chip power input for internal LDO (2.0VDC–24.5VDC, 30VAC tolerant)
24	B5	VBUS_IN_DISCHARGE	Internal Discharge FET for the provider path of VBUS (3.0VDC–24.5VDC, 30VAC tolerant).
25	B6	CSP	CS+: Current Sense Input
26	A5	DM0/P3.1	Protection: 8 kV IEC ESD protection for direct connection to the Type-C connector pin. This pin's default operation at chip power up is USB Port 0 D-Minus pin and is capable of charging protocols for AFC, QC, USB BC1.2 and Apple Charging simultaneously. It can also be reconfigured after chip power up as: I/O Operation: UART_1_RX0.
27	C6	FB	Voltage regulation feedback pin
28	D6	CATH/COMP	Cathode of voltage regulation and compensation for other applications.
29	B4	VSS	Ground
30	E6	VDDD	Power Supply Input/Output pin[13]
31	C5	VDDIO	VDDIO Input: 1.71 V–5.5 V
32	C4	VCCD	1.8-V Core Voltage pin (not intended for use as a power source)
EPAD	N/A	EPAD	Ground
N/A	A6	CSA_GND	CSA Ground, on the CSP package this ground signal is associated with the CSP input for low side current sensing.

Notes
10. See Table 9 on page 19 and Table 10 on page 19 for specifications related to these pins.
11. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.
12. TCPWM_line_1 can be mapped to port pins P0.1 or P2.3.
13. VDDD can be used as power supply input or output. Refer to Table 5 for specifications related to VDDD as power supply input pin. Refer to Table 39 for specifications related to VDDD as power supply output pin.

Table 3. GPIO Ports, Pins and Their Functionality

Port Pin	32-QFN Pin#	30-CSP Pin#	SCB Function			TCPWM	Fault Indicator[14]	Protection Capability		USB Charging Signal				IEC4[16]
			UART	SPI	I^2C			VBUS Short	OVT[15]	AFC	QC	BC1.2	Apple	
P0.0	15	C1	UART_0_CTS	SPI_1_MOSI	I2C_0_SDA	TCPWM_line_0:0	–	–	Yes	–	–	–	–	–
P0.1	16	B1	UART_0_RTS	SPI_1_MISO	I2C_0_SCL	TCPWM_line_1:0	–	–	Yes	–	–	–	–	–
P1.0	1	E5	UART_1_CTS	SPI_0_SEL	I2C_1_SDA:1[17]	TCPWM_line_2:1	Yes	–	–	–	–	–	–	–
P1.1	2	D5	UART_1_RTS	SPI_0_MISO	I2C_1_SCL:1[17]	TCPWM_line_3:1	Yes	–	–	–	–	–	–	–
P1.2	8	E2	UART_1_TX1	SPI_0_MOSI	–	–	–	–	–	D+	D+	D+	D+	–
P1.3	9	E1	UART_1_RX1	SPI_0_CLK	–	–	–	–	–	D–	D–	D–	D–	–
P1.4	4	E4	–	–	–	–	–	–	–	–	–	–	–	–
P1.5	5	N/A	–	–	–	–	–	–	–	–	–	–	–	–
P2.0	12	C3	UART_0_TX0	SPI_1_SEL	–	TCPWM_line_2:0	–	–	–	–	–	–	–	–
P2.1	13	D2	UART_0_RX0	SPI_1_CLK	–	TCPWM_line_3:0	–	–	–	–	–	–	–	–
P2.2	18	A1	UART_0_TX1	–	I2C_1_SDA:0[17]	TCPWM_line_0:1	–	Yes	–	–	–	–	–	Yes
P2.3	19	A2	UART_0_RX1	–	I2C_1_SCL:0[17]	TCPWM_line_1:1	–	Yes	–	–	–	–	–	Yes
P2.4	10	N/A	–	–	–	–	–	–	–	–	–	–	–	–
P2.5	11	N/A	–	–	–	–	–	–	–	–	–	–	–	–
P3.0	22	A4	UART_1_TX0	–	–	–	–	–	–	D+	D+	D+	D+	Yes
P3.1	26	A5	UART_1_RX0	–	–	–	–	–	–	D–	D–	D–	D–	Yes

Notes

14. Input pin with programmable thresholds for simultaneous short-circuit protection, overcurrent protection, overvoltage protection, and undervoltage protection fault indication.
15. Tolerant to voltages above V_{DDIO} with a maximum of 6.5VDC (OVT).
16. Eliminates external 8kV IEC ESD protection on all the USB-C connector pins.
17. Out of the two SCB blocks (SCB0 and SCB1), while the SCB0's I2C functionality is mapped out to the P0.0/P0.1 GPIO pins, the I2C functionality of SCB1 provides flexibility to have it mapped either on P1.0/P1.1 OR P2.2/P2.3 GPIO pins.

Figure 3. Pinout of 32-QFN Package (Top View)

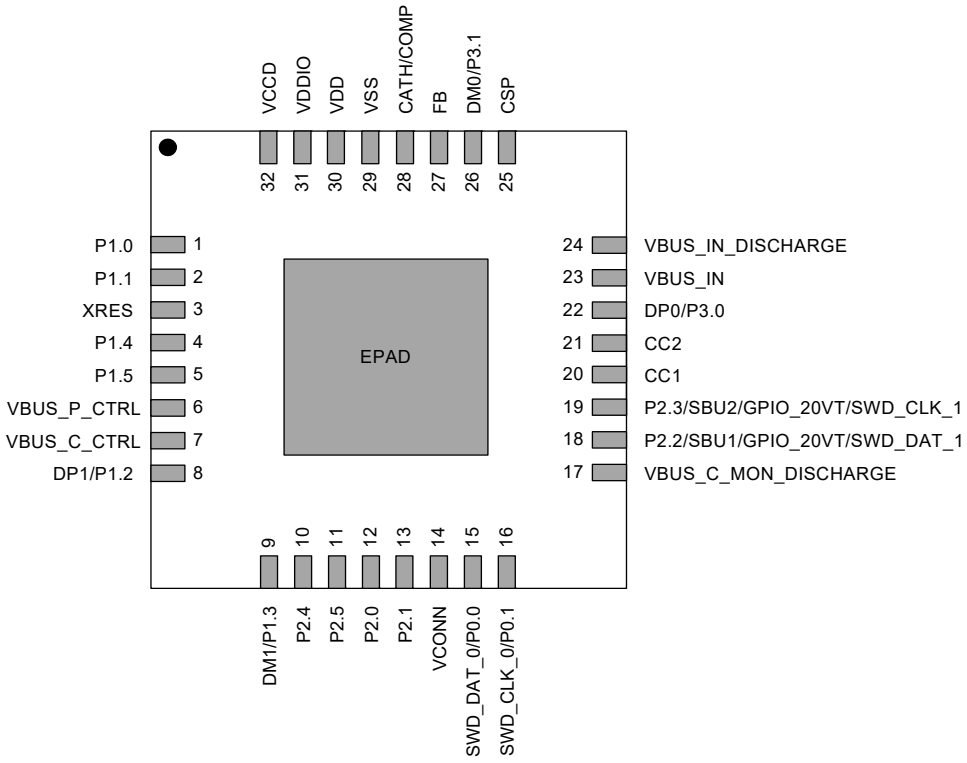
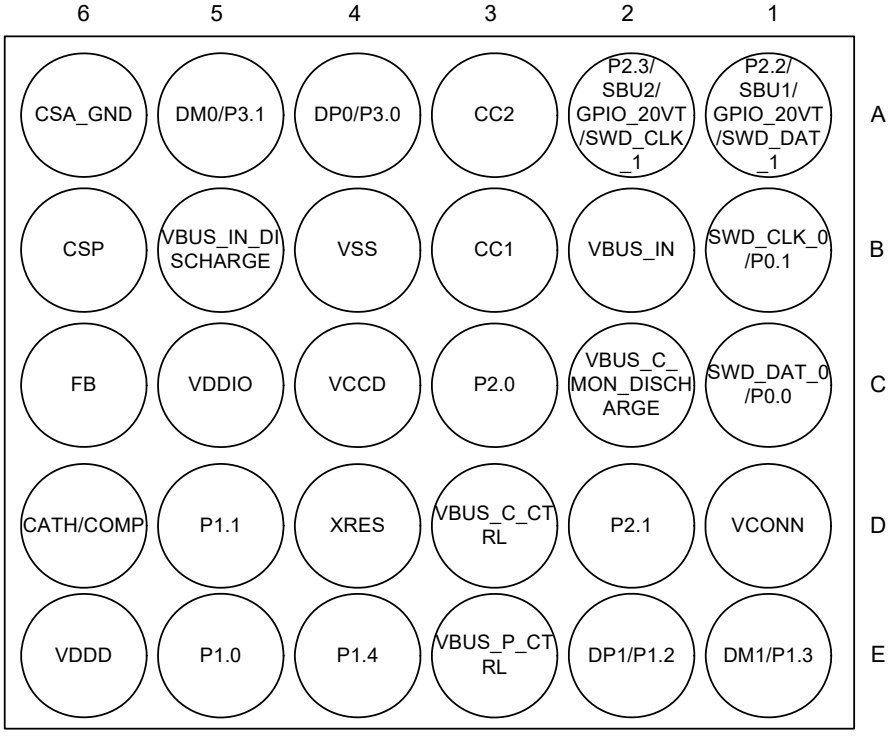


Figure 4. Pinout of 30-WLCSP Package (Bottom View, Balls Up)



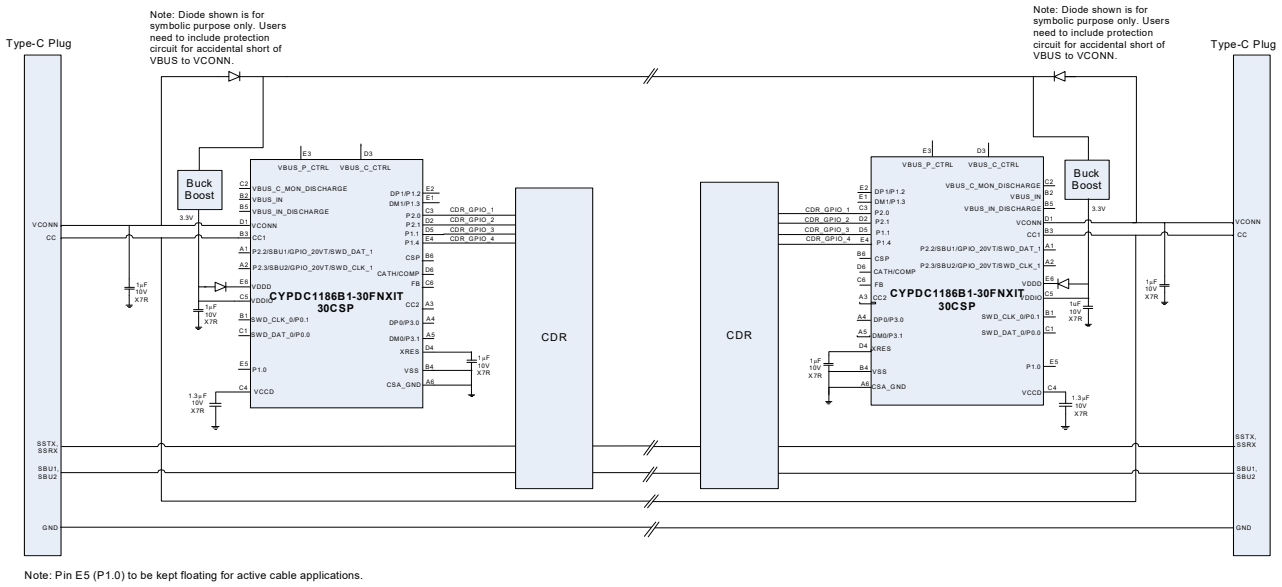
Applications Diagrams

Figure 5 ,Figure 6, and Figure 7 illustrate the application diagrams of Thunderbolt active and passive cables respectively using CCG3PA2 devices. The CCG3PA2 devices are used in conjunction with the Clock Data Recovery chip (shown as the “CDR” block in Figure 5, Figure 6, and Figure 7) of these cable designs.

The CC and VCONN signals from the Type-C plug are connected to the CC1 and VCONN pins of the CCG3PA2 device at both ends of the cable. The SSTX, SSRX, SBU1, and SBU2 signals are routed from one end of the plug to the other end via CDR devices. Each end of the cable has a CDR to re-time and re-condition the signals.

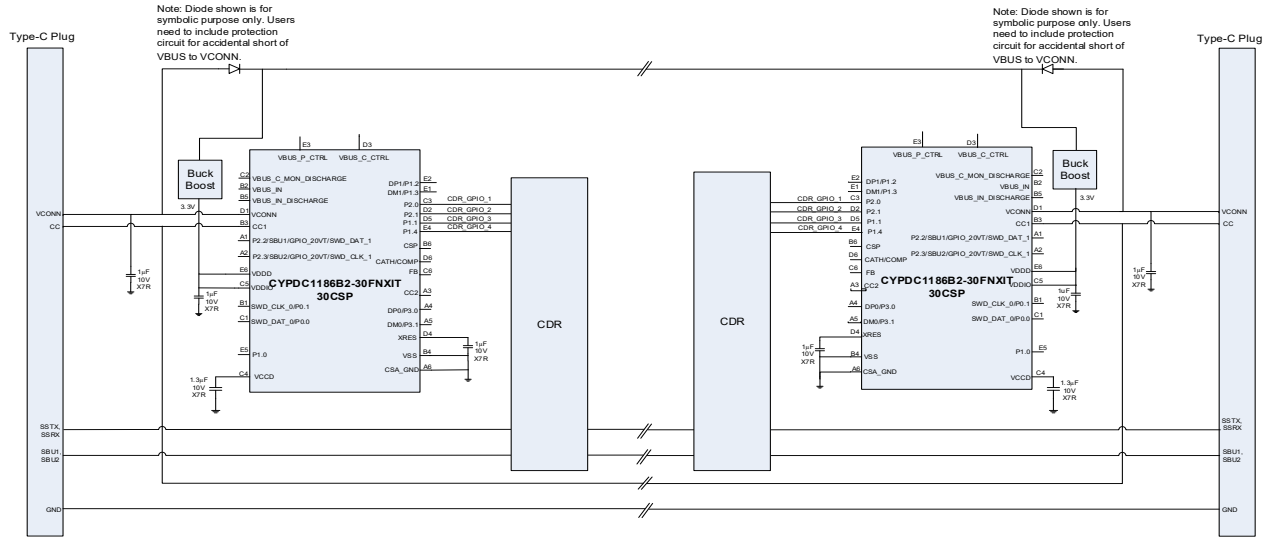
Note: CCG3PA2 devices cannot be used in a single chip-based passive cable applications. Also, pin E5 (P1.0) of the CCG3PA2 device needs to be kept floating for active cable applications, whereas for passive cable applications with two chips per cable, pin E5 (P1.0) needs to be connected to GND.

Figure 5. Thunderbolt™ Active Cable Application Diagram (Two Chips Per Cable) (For Silicon Rev = B1)



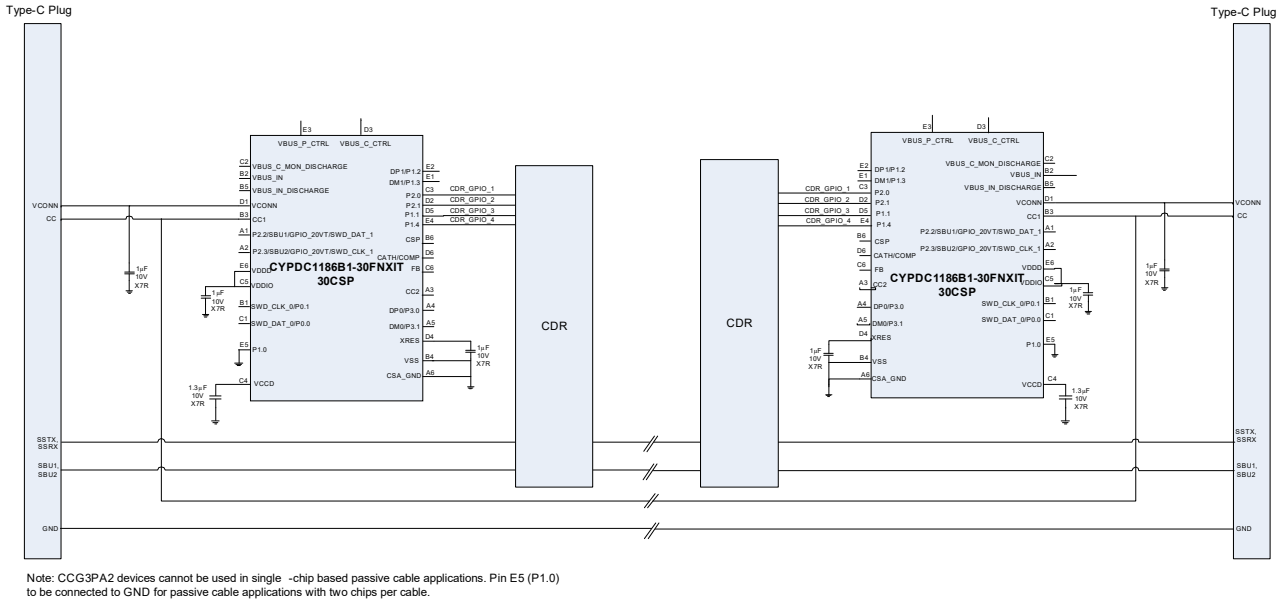
Note: Pin E5 (P1.0) to be kept floating for active cable applications.

Figure 6. Thunderbolt™ Active Cable Application Diagram (Two Chips Per Cable) (For Silicon Rev = B2)



Note: Pin E5 (P1.0) to be kept floating for active cable applications.

Figure 7. Thunderbolt™ Passive Cable Application Diagram (Two Chips Per Cable) (For Silicon Rev = B1)

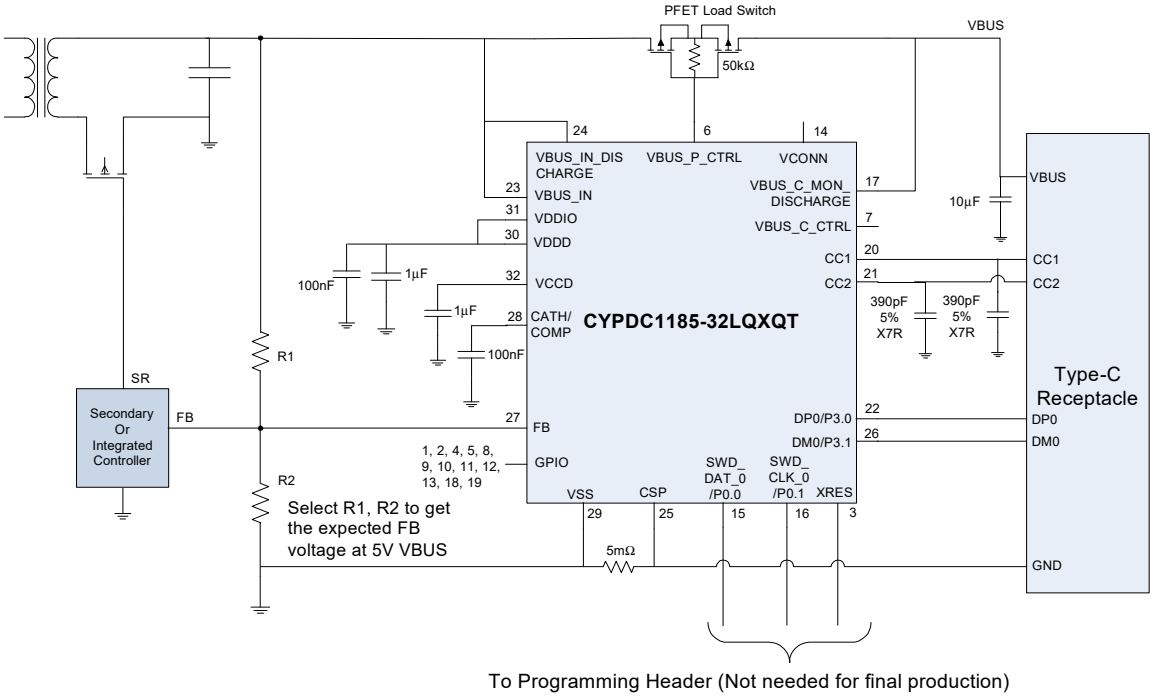


Note: CCG3PA2 devices cannot be used in single -chip based passive cable applications. Pin E5 (P1.0) to be connected to GND for passive cable applications with two chips per cable.

Figure 8 shows the application diagram of CCG3PA2-based power adapter with Direct Feedback control. The default value of VBUS upon power-up (which is usually at 5 V) is set up by choosing the appropriate resistor divider that will set the FB node at a voltage expected by the secondary controller.

The feedback node is regulated using internal IDACs. Whenever a change in VBUS voltage is needed, CCG3PA2 will either source or sink a proportional current at feedback node, based on the amount of voltage change needed.

Figure 8. CCG3PA2 Based Power Adapter Application Diagram with Direct Feedback Control



Electrical Specifications

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS}	–	–	30	VAC	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}			6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins	–	–	22		
V_{CONN_MAX}	Max supply voltage relative to Vss	–	–	25		
$V_{SWD\_PIN\_ABS}$	Max SWD voltage	–	–	24.5		
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5		
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, SBU, VBUS_C_MON_DISCHARGE and V_{CONN} pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–		Air discharge for CC1, CC2, SBU, VBUS_C_MON_DISCHARGE and V_{CONN} pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 105 °C and T_J ≤ 120 °C, except where noted.

Table 5. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#2	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	Sink mode, –40 °C ≤ T_A ≤ 105 °C.
SID.PWR#2_A	V_{DDD}	Power supply input voltage	3.0	–	5.5		Source mode, –40 °C ≤ T_A ≤ 105 °C.
SID.PWR#3	V_{BUS_IN}	Power supply input voltage	3.0	–	24.5		–40 °C ≤ T_A ≤ 105 °C
SID.PWR#5	V_{CCD}	Output voltage for core logic	–	1.8	–		–
SID.PWR#19	V_{CONN}	Power Supply Input Voltage	3.0	–	5.5		–40 °C ≤ T_A ≤ 105 °C
SID.PWR#20	V_{DDIO}	IO supply voltage	1.71	–	5.5		2.7 V < V_{DDD} < 5.5 V
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS_IN_DISHCARGE	–	0.1	–		

Table 5. DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Active Mode. Typical values measured at V_{DDD} = 5.0 V or V_{BUS} = 5.0 V and T_A = 25 °C.							
SID.PWR#8	IDD_A	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25 °C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz.
Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25 °C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25 °C, All blocks except CPU are on, CC I/O on, EA/ADC/CSA/UVOV On.
Deep Sleep Mode. Typical values measured at T_A = 25 °C.							
SID_DS	I_{DD_DS}	V_{DDD} = 3.0 to 5.5 V	–	15	–	µA	Power Source = V_{DDD} = 5 V, T_A = 25 °C, Type-C disabled. Wake-up sources: GPIO, I^2C and WDT enabled.
SID_PA_DS_UA	$I_{DD\_PA\_DS\_UA}$	V_{BUS} = 4.5 to 5.5 V. CC Attach, I^2C, WDT Wakeup on	–	100	–		Power Adapter/Charger application Power Source = V_{BUS} = 5 V, T_A = 25 °C, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
SID_PA_DS_A	$I_{DD\_PA\_DS\_A}$	V_{BUS} = 3.0 to 24.5V. CC, I^2C, WDT Wakeup on	–	500	–		Power Adapter/Charger application V_{BUS} = 24.5 V, T_A = 25 °C, Part is in Deep Sleep. Attached, CC I/O on, ADC/CSA/UVOV On
XRES Current Consumption							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	15	–	µA	Power Source = V_{CONN} = 3.3 V, Type-C device not attached, T_A = 25 °C.

Table 6. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	0	–	48	MHz	All V_{DDD}
SID.PWR#17	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35		–
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR\_HIZ\_T}$	Power-on I/O Initialization Time	–	3	–		–

I/O

Table 7. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}		
SID.GIO#39	$V_{IH\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–		–
SID.GIO#40	$V_{IL\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID.GIO#41	$V_{IH\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–		–
SID.GIO#42	$V_{IL\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} – 0.6	–	–		I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6		I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5		
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all package, All I_{OS}
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	–	mV	–
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DDD} < 4.5 V
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	–
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 8. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12		

Table 9. GPIO_20VT DC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25 °C T_A, 1.4 V to GPIO_20VT_Voh(min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20		+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40 °C to +85 °C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT Output Voltage low level.	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL Input Voltage high level.	2	–	–		$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL Input Voltage low level.	–	–	0.8		
SID.GPIO_20VT#43	GPIO_20VT_Vhysttl	GPIO_20VT Input hysteresis LVTTL	15	40	–	mV	
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 10. GPIO_20VT AC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GPIO_20VT#70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	2	–	15		

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 11. PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between quadrature-phase inputs

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4		–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	20	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312		–

Table 15. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 16. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560		–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600		–

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 18. Fixed SPI Master Mode AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–		Referred to slave capturing edge

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42 + 3 \times T_{CPU}$		$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48		–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–		–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–		–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 20. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4		–

Table 21. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5		–

Table 22. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDD} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$2.7\ V \le V_{DDD} \le 3.3\ V$	–	–	7		
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T		
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		

Internal Main Oscillator

Table 23. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 24. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 25. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 26. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	–
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	–
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Power Delivery

Table 27. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194.4		–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356.4		–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12		All supplies forced to 0 V and 1.32 V applied at CC1 or CC2
SID.PD.6	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter.
SID.PD.7	Ra	Power Cable Termination	0.8	1	1.2	kΩ	All supplies forced to 0 V and 0.2 V applied at V_{CONN}
SID.PD.8	Ra_off	Power Cable Termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at V_{CONN} with Ra disabled

Table 28. LS-CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.1	Cin_inp	CSP Input capacitance	2	–	6	pF	Measured at F = 1MHz.
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active Mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10		
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6		
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5		
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4		
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4		
SID.LSCSA.8	Csa_SCP_Acc1	CSA SCP 80 mV	–16.5	–	16.5		
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	13.4		
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	9.4		
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	7.5		
SID.LSCSA.12	Av	Nominal Gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	–
SID.LSCSA.24	Av1_E_Trim	Gain Error	–2	–	2	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage	–3	–	3		–

Table 29. LS-CSA AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET Power Gate Turn off	–	–	50		–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15		Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET Power Gate Turn off	–	–	50		–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20		Available on P1.0 or P1.1

Table 30. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	V_{THOV1}	Overvoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3	%	Active Mode
SID.UVOV.2	V_{THOV2}	Overvoltage Threshold Accuracy, 11 V to 27.4 V	–3.2	–	3.2		
SID.UVOV.3	V_{THUV1}	Undervoltage Threshold Accuracy, 2.7 V to 3.3 V	-4	–	4		
SID.UVOV.4	V_{THUV2}	Undervoltage Threshold Accuracy, 3.3 V to 4.0 V	–3.5	–	3.5		
SID.UVOV.5	V_{THUV3}	Undervoltage Threshold Accuracy, 4.0 V to 11.0 V	–3	–	3		
SID.UVOV.6	V_{THUV4}	Undervoltage Threshold Accuracy, 11.0 V to 22.0 V	–2.9	–	2.9		

Table 31. UV/OV AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.AC.1	T_{OV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.UVOV.AC.2	T_{OV_GATE}	Delay from UV threshold trip to external PFET power gate turn off	–	–	50		–
SID.UVOV.AC.3	T_{UV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20		Available on P1.0 or P1.1

Gate Driver Specifications

Table 32. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	5	kΩ	Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	10	kΩ	Applicable on VBUS_P_CTRL to turn OFF external PFET
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	$I_{\_leak\_p1}$	Pin leakage on VBUS_P_CTRL	–	–	0.012	µA	+25 °C T_J, 5-V V_{DDD}, 20-V V_{BUS}
SID.GD.10	$I_{\_leak\_c1}$	Pin leakage on VBUS_C_CTRL	–	–	0.012	µA	+25 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.11	$I_{\_leak\_p2}$	Pin leakage on VBUS_P_CTRL	–	–	2	µA	+85 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.12	$I_{\_leak\_c2}$	Pin leakage on VBUS_C_CTRL	–	–	2	µA	+85 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.13	$I_{\_leak\_p3}$	Pin leakage on VBUS_P_CTRL	–	–	7	µA	+125 °C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.14	$I_{\_leak\_c3}$	Pin leakage on VBUS_C_CTRL	–	–	7	µA	+125 °C T_J, 5-V V_{DDD}, 20-V V_{BU}

Table 33. Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GD.15	T_{PD1}	Pull down delay on VBUS_C_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on VBUS_C_CTRL	–	–	5	V/µs	80% to 20%, 50 KΩ tied between VBUS_C_CTRL and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_P_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_P_CTRL	–	–	18	µs	Cload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_P_CTRL range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_P_CTRL range

Table 34. V_{BUS} Discharge Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	$V_{BUS\_Stop\_Error}$	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by Characterization.

Table 35. Voltage (V_{BUS}) Regulation DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.DC.VR.1	$V_{\_IN\_3}$	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	$V_{\_IN\_5}$	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	$V_{\_IN\_9}$	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	$V_{\_IN\_15}$	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	$V_{\_IN\_20}$	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	$V_{\_IN\_3\_DS}$	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	$V_{\_IN\_5\_DS}$	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	$V_{\_IN\_9\_DS}$	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	$V_{\_IN\_15\_DS}$	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	$V_{\_IN\_20\_DS}$	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I_{KA_OFF}	Off-state cathode current	–	–	10	µA	–
SID.DC.VR.12	I_{KA_ON}	Current through cathode pin	–	–	10	mA	–

Table 36. VBUS Short Protection Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VSP.1	$V_{\_SHORT\_TRIGGER}$	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by Characterization.

Table 37. V_{BUS} Regulator DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VREG.2	V_{BUS_DETECT}	V_{BUS} detect threshold voltage	1.08	–	2.62	V	–
SID.VREG.5	$V_{BUSLINREG}$	V_{BUS} Regulator line regulation for V_{BUS} from 4.2 V to 25 V	–	–	0.5	%/V	–
SID.VREG.7	$V_{BUSLOADREG}$	V_{BUS} Regulator load regulation for V_{BUS} from 4.2 V to 25 V	–	–	0.2	%/mA	–

Table 38. V_{BUS} Regulator AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	–

Table 39. V_{CONN}–V_{DDD} Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
DC.VCONN_SW.9	V_{DDD_OUT}	V_{DDD} supply output with V_{CONN} powering the chip.	2.4	–	5.5	V	For Silicon Rev = B1. For $V_{CONN} \le 5.5$ V, max value = $V_{CONN.}$ For $V_{CONN} \ge 5.5$ V, max value = 5.5 V.
SID.VREG.1	V_{DDD_OUT}	V_{DDD} supply output with V_{BUS_IN} range = 3.0V to 24.5V.	2.7	–	3.6	V	For Silicon Rev = B1 and B2. V_{DDD} supply output can only be used to power V_{DDIO}.

Analog to Digital Converter

Table 40. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from V_{DDD}
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from V_{DDD}
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

Table 41. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Memory

Table 42. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–40 °C ≤ T_A ≤ 85 °C, all V_{DDD}
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20		
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7		25 °C ≤ T_A ≤ 55 °C, all V_{DDD}
SID178	TBULKERASE	Bulk erase time (32k Bytes)	–	–	35		–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	–
SID182	FRET1	Flash retention, T_A ≤ 55 °C, 100K P/E cycles	20	–	–	years	–
SID182A	FRET2	Flash retention, T_A ≤ 85 °C, 10K P/E cycles	10	–	–		–
SID182B	FRET3	Flash retention, T_A ≤ 105 °C, 10K P/E cycles	3	–	–		–

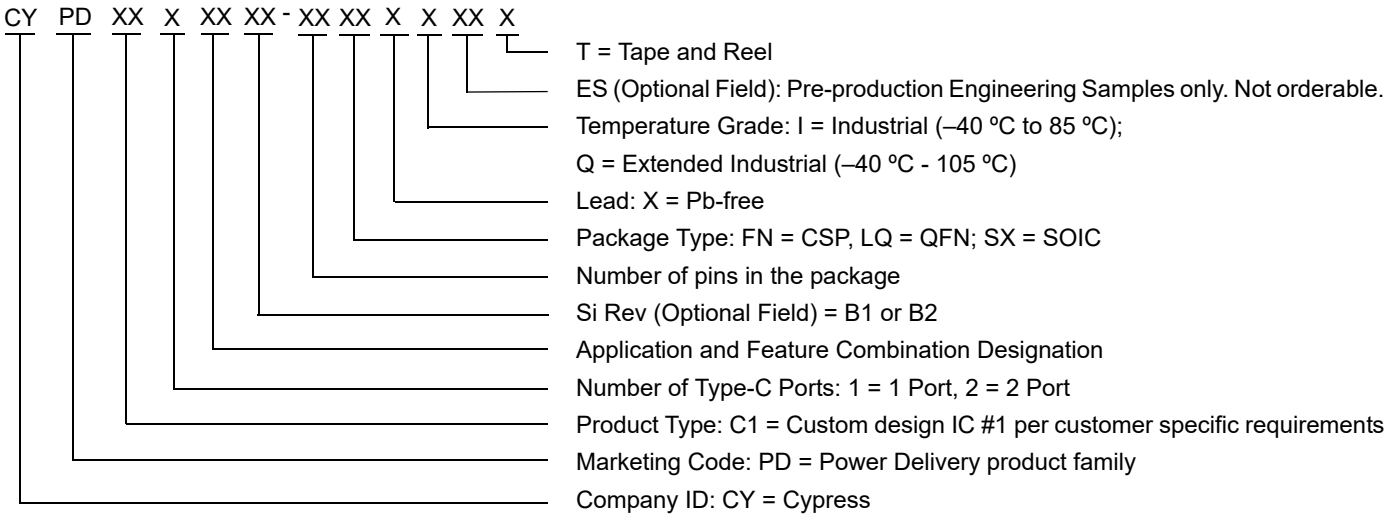
Ordering Information

Table 43 lists the EZ-PD CCG3PA2 part numbers and features.

Table 43. CCG3PA2 Ordering Information

MPN	Application	Termination Resistor	Type-C Ports	Role	Bootloader	Package Type	Si ID	Si Rev
CYPDC1185-32LQXQEST	Power Adapter	R_P	1	DFP	DFP CC with Direct Feedback Bootloader	32-QFN	2400	A0
CYPDC1185-32LQXQT								B1
CYPDC1185B1-32LQXQT								B1
CYPDC1185B2-32LQXQT								B2
CYPDC1186-30FNXIEST	Thunderbolt Active EMCA	R_A	1	EMCA	EMCA CC Bootloader	30-WLCSP	2401	A0, B0, B1
CYPDC1186-30FNXIT								B1
CYPDC1186B1-30FNXIT								B1
CYPDC1186B2-30FNXIT							2402	B2

Ordering Code Definitions



Package Diagrams

Table 44. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	-40	25	85	°C
T_J	Operating junction temperature	Industrial	-40	25	100	°C
T_{JA}	Package θ_{JA} (32-pin QFN)	-	-	18.76	-	°C/W
T_{JC}	Package θ_{JC} (32-pin QFN)	-	-	19.88	-	°C/W
T_{JA}	Package θ_{JA} (30-ball WLCSP)	-	-	43.3	-	°C/W
T_{JC}	Package θ_{JC} (30-ball WLCSP)	-	-	31.68	-	°C/W

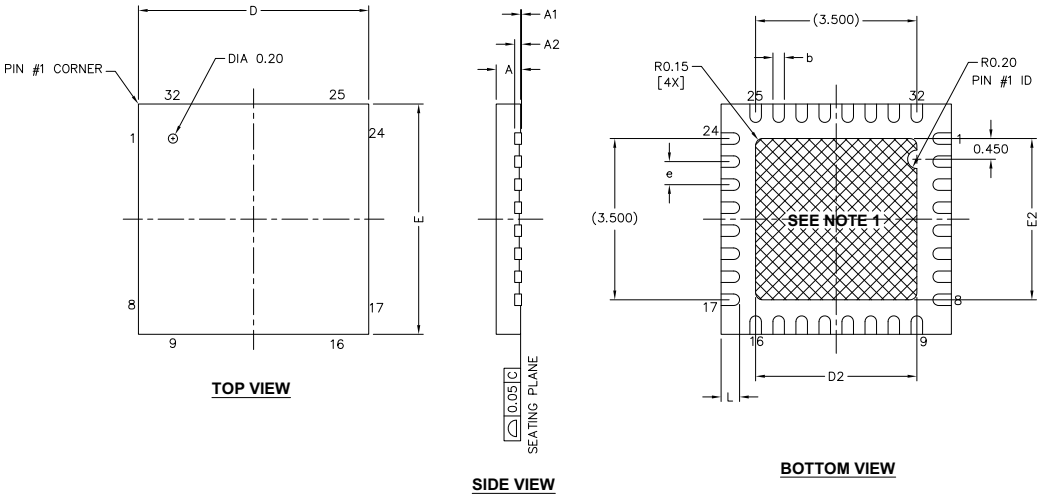
Table 45. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5° C of Peak Temperature
32-pin QFN	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Table 46. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
32-pin QFN	MSL3
30-ball WLCSP	MSL1

Figure 9. 32-pin QFN Package Outline



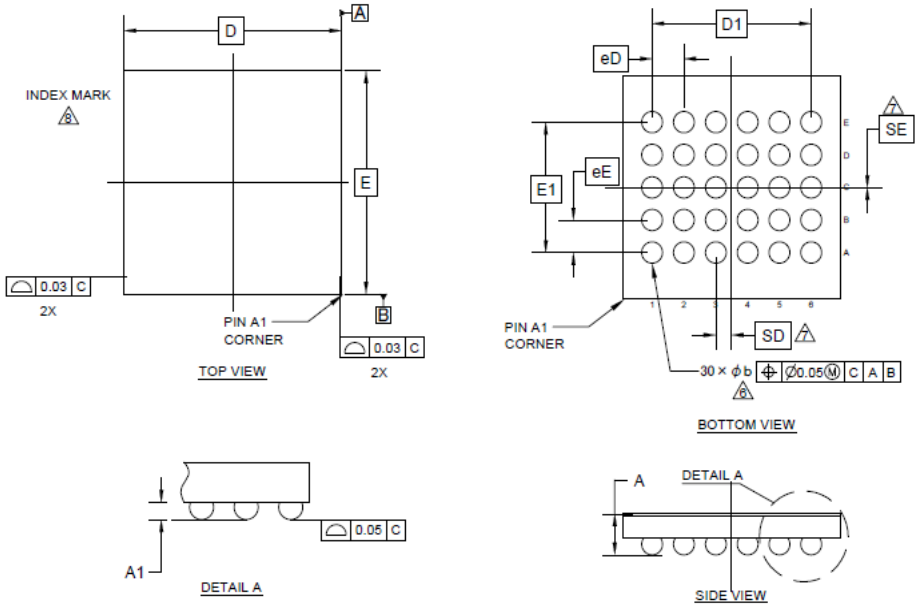
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	-	0.020	0.045
A2	0.15 BSC		
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
b	0.18	0.25	0.30
e	0.50 TYP		

NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *F

Figure 10. 30-ball WLCSP Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.545
A1	0.175	—	0.235
D	2.741 BSC		
E	2.744 BSC		
D1	2.000 BSC		
E1	1.600 BSC		
MD	6		
ME	5		
n	30		
φb	0.231	0.261	0.291
eD	0.400 BSC		
eE	0.400 BSC		
SD / SE	0.20 / 0 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF: N/A.

002-20044 **

Acronyms

Table 47. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
ARM®	advanced RISC machine, a CPU architecture
CCG3	Cable Controller Generation 3
CPU	central processing unit
CS	current sense
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I/O	input/output, see also GPIO
MCU	microcontroller unit
OCP	overcurrent protection
OTP	over temperature protection
OVP	overvoltage protection
PHY	physical layer
PRES	precise power-on reset
PWM	pulse-width modulator
RAM	random-access memory
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SCP	short circuit protection

Table 47. Acronyms Used in this Document *(continued)*

Acronym	Description
SDA	I^2C serial data
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
UVP	undervoltage protection
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 48. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
KB	1024 bytes
MΩ	mega-ohm
µA	microampere
µF	microfarad
mA	milliampere
V	volt

Document History Page

Document Title: EZ-PD™ CCG3PA2 Datasheet USB Type-C Port Controller Document Number: 002-18400				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5587836	ZKR	01/25/2017	New data sheet.
*A	5727719	MSMI	05/05/2017	Changed status from Advance to Preliminary. Updated General Description: Updated description. Updated Features: Updated Power: Updated description. Updated Packages: Updated description. Updated Pinouts: Updated Table 2. Added Figure 3. Added Figure 4. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 4. Updated Ordering Information: Updated Table 43: Updated part numbers. Updated Package Diagrams: Added spec 002-18455 **. Updated to new template.
*B	5774994	VGT	06/19/2017	Updated Features: Updated Type-C Support and USB-PD Support: Updated description. Updated System-Level Fault Protection: Updated description. Updated Logic Block Diagram. Added Internal Block Diagram (Silicon Rev = B1). Updated Pinouts: Updated Table 2. Added Table 3. Updated Figure 3. Updated Figure 4. Added “Firmware and Configuration Settings”. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 4. Added Device-Level Specifications. Added Digital Peripherals. Added System Resources. Updated Ordering Information: Updated Table 43: No change in part numbers. Added columns “Termination Resistor” and “Si ID” and added details in those columns.
*C	5885057	VGT	12/21/2017	Updated General Description: Updated description (with correct end applications). Updated Features: Updated Power: Removed “Reset: 30 µA”; replaced “Deep Sleep: 30 µA” with “Deep Sleep: 15 µA”. Updated Internal Block Diagram (Silicon Rev = B1).

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3PA2 Datasheet USB Type-C Port Controller Document Number: 002-18400				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*C (cont.)	5885057	VGT	12/21/2017	Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to pin names P0.0, P0.1, P1.0, and P1.1. Updated Table 3: Updated details in “TCPWM” column corresponding to P0.0, P0.1, P1.0, and P1.1 port pins. Removed “Firmware and Configuration Settings”. Added Applications Diagrams. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 5 (Changed typical value of SID_DS parameter from 5 µA to 15 µA). Updated System Resources: Updated Gate Driver Specifications: Added Table 39. Updated Ordering Information: Updated Table 43: Updated part numbers. Added Errata. Updated to new template.
*D	6062553	VGT	02/09/2018	Updated Pinouts: Updated Table 2: Updated details in “Pin Name” column corresponding to pin 18 and pin 19 of 32-pin QFN device. Updated details in “Description” column corresponding to pin 31 of 32-pin QFN device. Updated Figure 3 (pin name of pins 18 and 19). Updated Figure 4 (pin name of pins A1 and A2). Updated Applications Diagrams: Updated Figure 6. Added Figure 7 (for Thunderbolt Passive cable application). Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 5: Added VDDIO parameter (Spec ID SID.PWR#10) and its details. Updated I/O: Added Table 9. Added Table 10. Updated Ordering Information: Updated Table 43: Updated part numbers. Added a column “Bootloader” and added details in that column. Removed Errata. Completing Sunset Review.
*E	6093653	VGT	03/23/2018	Changed status from Preliminary to Final. Updated General Description: Updated description. Added Functional Overview. Added Power Systems Overview.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3PA2 Datasheet USB Type-C Port Controller Document Number: 002-18400				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	6093653	VGT	03/23/2018	Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to pin names P0.0, P0.1, P2.2, P2.3, CC1, and CC2. Updated Table 3 (with information on Fault Indicator and VBUS Short Protection Capability). Updated Applications Diagrams: Added descriptions above Figure 6, Figure 7 and Figure 8. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 4: Updated details in “Max” column corresponding to $V_{CC\_PIN\_ABS}$ parameter. Added V_{CONN_MAX} parameter and its details. Updated Device-Level Specifications: Updated Table 5: Added V_{CONN} parameter and its details. Replaced SID.PWR#10 with SID.PWR#20 in SpecID column corresponding to V_{DDIO} parameter. Updated Table 6: Updated details in “Min” column corresponding to F_{CPU} parameter. Updated I/O: Updated Table 9: Removed GPIO_20VT_Voh parameter and its details. Updated I^2C: Updated Table 12: Updated details in “Max” column corresponding to I_{I2C1} parameter. Updated Table 14: Updated details in “Max” column corresponding to I_{UART1} parameter. Updated System Resources: Updated Power Delivery: Replaced “Power Down” with “Power Delivery” in heading. Updated Table 28: Updated details in “Min” column corresponding to Cin_inp, Av1_E_Trim, Av_E_SCP parameters. Updated details in “Max” column corresponding to Cin_inp, Av1_E_Trim, Av_E_SCP parameters. Updated details in “Details/Conditions” column corresponding to Cin_inp parameter. Updated Gate Driver Specifications: Updated Table 32: Updated details in “Max” column corresponding to R_{PD}, R_{PU} parameters. Updated details in “Description” and “Details/Conditions” columns corresponding to I_{PD0}, I_{PD1}, I_{PD2}, I_{PD3}, I_{PD4}, I_{PD5} parameters. Added $I_{\_leak\_p1}$, $I_{\_leak\_c1}$, $I_{\_leak\_p2}$, $I_{\_leak\_c2}$, $I_{\_leak\_p3}$, $I_{\_leak\_c3}$ parameters and their details. Updated Table 33: Updated details in all columns for all parameters. Updated Table 34: Removed R_{ON1}, R_{ON2}, R_{ON3}, R_{ON4}, R_{ON5} parameters and their details. Added I1, I2, I4, I8, I16 parameters and their details. Updated details in “Spec ID#” and “Details/Conditions” columns corresponding to $V_{BUS\_Stop\_Error}$ parameter. Updated Table 35: Added $V_{\_IN\_3}$, $V_{\_IN\_3\_DS}$ parameters and their details. Added Table 36.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3PA2 Datasheet USB Type-C Port Controller Document Number: 002-18400				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	6093653	VGT	03/23/2018	Updated Analog to Digital Converter: Updated Table 40: Added INL parameter (Spec ID SID.ADC.2A) and its details. Added DNL parameter (Spec ID SID.ADC.3A) and its details. Removed V_{REF_ADC1} parameter and its details. Updated details in "Description" column corresponding to V_{REF_ADC2} parameter.
*F	6161548	VGT	04/30/2018	Added I_{DD_XR} parameter in Table 5. Updated Table 28.
*G	6261344	VGT	07/25/2018	Added Packaging Characteristics in Table 44, Table 45, Table 46. Updated title of figure: Internal Block Diagram (Silicon Rev = B1) and updated Figure 5 and Figure 7. Added Internal Block Diagram (Silicon Rev = B2), Figure 2 and Figure 6. Updated Table 2, Table 37, Table 39 and Table 43. Updated Ordering Code Definitions. Updated Power Systems Overview section.

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