27 W 12 V 5 V SMPS demo board with ICE5QR1680AG

About this document

Scope and purpose

This document is an engineering report that describes a universal-input 27 W 12 V and 5 V off-line flyback converter using the newest 5th generation Infineon QR CoolSET™ ICE5QR1680AG. It offers high-efficiency, low-standby power with selectable entry and exit standby power options, a wider V CC operating range with fast start-up, robust line protection with input Over Voltage Protection (OVP), and brownout and various modes of protection for a highly reliable system. This demo board is designed for users who wish to evaluate the performance of ICE5QR1680AG and its ease of use.

Intended audience

This document is intended for power-supply design/application engineers, students, etc., who wish to design low-cost and highly reliable systems of off-line SMPS, such as auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for blu-ray players, set-top boxes, games consoles, etc.

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Abstract

1 Abstract

This is an engineering report for a 27 W 12 V and 5 V demo board designed in a QR flyback converter topology using the 5th generation QR CoolSET™ ICE5QR1680AG. The target applications of ICE5QR1680AG are set-top boxes, portable games controllers and blu-ray/DVD players, as well as auxiliary power supplies for home appliances/white goods, PCs, printers, TVs, home theater/audio systems, etc. With the CoolMOS™ integrated into this IC, it greatly simplifies the design and layout of the PCB. The improved digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low- and high-line. The enhanced Active Burst Mode (ABM) power enables flexibility in standby power operation range selection, and QR operation during ABM. As a result, the system efficiency over the entire load range is significantly improved compared to a conventional free-running QR converter implemented with only maximum switching frequency limitation at light loads. In addition, numerous adjustable protection functions have been implemented in ICE5QR1680AG to protect the system and customize the IC for the chosen application. In case of failure modes such as brownout or line over-voltage, VCC over-/under-voltage, open control-loop or over-load, output over-voltage, over-temperature, VCC short-to-ground and Current Sense (CS) short-to-ground, the device enters protection mode. By means of the cycle-by-cycle Peak Current Limitation (PCL), the dimensions of the transformer and the current rating of the secondary diode can both be optimized. Thus, a cost-effective solution can easily be achieved.

2 Demo board

This document contains the list of features, the power supply specifications, schematics, bill of materials and the transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are shown at the end of the report.

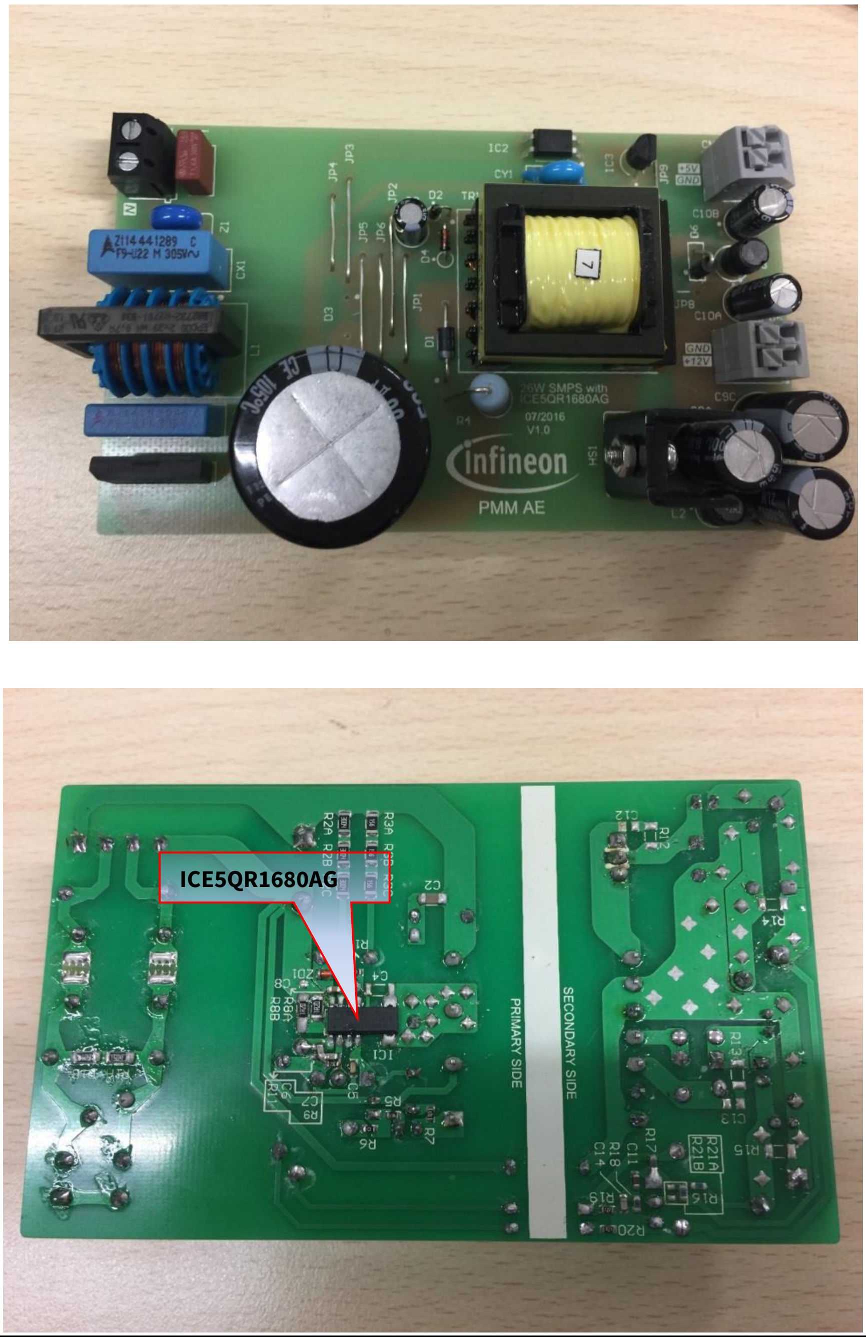


Figure 1 **DEMO_5QR1680AG_27W1**

3 Specifications of the demo board

Table 1 Specifications of DEMO_5QR1680AG_27W1

Input voltage and frequency	85 V AC (60 Hz)~300 V AC (50 Hz)
Output voltage, current and power	(12 V x 2.17 A) + (5 V x 0.2 A) = 27 W
Regulation	+5 V: < ±5% +12 V: < ±10%
Output ripple voltage (full-load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$ < 100 mV 12 $V_{ripple\_p\_p}$ < 200 mV
Active mode four-point average efficiency (25%, 50%, 75%, 100% load)	> 83% at 115 V AC and 230 V AC
No-load power consumption	< 100 mW at 230 V AC
Conducted emissions (EN 55022 class B)	Pass with 10 dB margin for 115 V AC and 6 dB margin for 230 V AC
ESD immunity (EN 61000-4-2)	Special level (±14 kV for contact and 6±14 kV air discharge)
Surge immunity (EN 61000-4-5)	Installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth)
Form factor case size (L x W x H)	(110 x 66 x 27) mm^3

Note: *The demo board is designed for dual output with cross-regulated loop feedback. It may not regulate properly if loading is applied only to single output. If the user wants to evaluate for single-output (12 V only) conditions, the following changes are necessary on the board.*

1. Remove D6, L3, C10A, C10B, R16 (to disable 5 V output)

2. Change R21A to 10 kΩ and R16 to 38 kΩ (to disable 5 V feedback and enable 100% weighted factor on 12 V output)

Since the board (especially the transformer) is designed for dual output with optimized cross-regulation, single-output efficiency might not be optimized. It is only for IC functional evaluation under single-output conditions.

4 Circuit description

4.1 Line input

The AC-line input side comprises the input fuse F1 as over-current protection. The choke L1, X-capacitors CX1 and CX2 and Y-capacitor CY1 act as EMI suppressors. The sparking gap and varistor Z1 can absorb HV stress during a lightning surge test. A rectified DC voltage (120~424 V DC) is obtained through the bridge rectifier BR1 together with the bulk capacitor C1.

4.2 Start-up

To achieve fast and safe start-up, ICE5QR1680AG is implemented with a start-up resistor and VCC short-to-GND protection. When V_{VCC} reaches the turn-on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5QR1680AG is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase in increments from 0.3 V to 1 V. After IC turn-on, the VCC voltage is supplied by auxiliary windings of the transformer. VCC short-to-GND protection is implemented during the start-up time.

4.3 Integrated MOSFET and PWM control

ICE5QR1680AG is comprised of a power MOSFET and the new proprietary QR controller, which enables higher average efficiency and low EMI. This integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacture. The PWM switch-on is determined by the Zero Crossing Detection (ZCD) input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback (FB) signal V_{FB} and the CS signal V_{CS}. ICE5QR1680AG also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R4, C2 and D1) dissipates the energy of the leakage inductance and suppresses ringing on the SMPS transformer.

4.5 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via Schottky diodes D5 and D6. The capacitors C9A and C10A provide energy buffering, followed by the L-C filters L2-C9B and L3-C10B to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency. Storage capacitors C9A and C10A are designed to have as small an internal resistance (ESR) as possible to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback loop

For FB, the output is sensed by the voltage divider of R16, R17, R21A and R21B and compared to the IC3 (TL431) internal reference voltage. C11, C14 and R18 comprise the compensation network. The output voltage of IC3 (TL431) is converted to the current signal via optocoupler IC2 and two resistors, R19 and R20, for regulation control.

4.7 Primary side peak-current control

The MOSFET drain source current is sensed via external resistors R8A and R8B. Since ICE5QR1680AG is a current mode controller, it would have a cycle-by-cycle primary current and FB voltage control, which ensures the converter’s maximum power is controlled in every switching cycle.

For a QR flyback converter, the maximum possible output power is increased when a constant current limit value is used for the whole-line input voltage range. This is usually not desirable, as this will increase the cost of the transformer and output diode in case of output over-power conditions.
Internal current limitation with a line-dependent V_{CS} curve and the new proprietary QR switching, which reduces switching frequency difference between the minimum and maximum line, are implemented in the ICE5QR1680AG. As a result, the maximum output power can be limited against the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE5QR1680AG is digitally reduced with decreasing load. At light loads, the MOSFET will be turned on – not at the first minimum drain-source voltage time, but on the n^{th}. The counter is within a range of 1 to 8 for low-line and 3 to 10 for high-line, which depends on FB voltage in a time-base. The FB voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active Burst Mode (ABM)

ABM entry and exit power (two levels) can be selected in ICE5QR1680AG. Details are illustrated in the product datasheet. In light load conditions, the SMPS enters into ABM with QR switching. At this stage, the controller is always active but the V_{VCC} must be kept above the switch-off threshold. During ABM, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load-jump.

For determination of entering ABM operation, three conditions apply:

1. The FB voltage is lower than the threshold of V_{FBEB}
2. The up/down counter is 8 for low-line and 10 for high-line, and
3. A certain blanking time (t_{BEB} = 20 ms) is required

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low during the preset blanking time.

During ABM, the maximum CS voltage is reduced from 1 V to 0.31/0.35 V to reduce the conduction loss and the audible noise. In ABM, the FB voltage changes like a sawtooth between 2 V and 2.4 V.

The FB voltage immediately increases if there is a high load-jump. This is observed by one comparator. As the current limit is 31/35% during ABM a certain load is needed so that FB voltage can exceed V_{FBLB} (2.75 V). After leaving ABM, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 (low-line) or 3 (high-line) immediately after leaving ABM. This is helpful to decrease the output voltage undershoot.

5 Protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5QR1680AG provides comprehensive protection to ensure the system is operating safely. This includes line over-voltage, brownout, VCC over-voltage and under-voltage, over-load, output over-voltage, over-temperature (controller junction), CS short-to-GND and V CC short-to-GND. When those faults are found, the system will go into protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions are shown in the table below.

Table 2 Protection functions of ICE5QR1680AG

Protection function	Failure condition	Protection mode
Line over-voltage	V_{VIN} > 2.9 V	Non-switch auto restart
Brownout	V_{VIN} < 0.4 V	Non-switch auto restart
VCC over-voltage	V_{VCC} > 25 V	Odd-skip auto restart
VCC under-voltage	V_{VCC} < 10 V	Auto restart
Over-load	V_{FB} > 2.75 V and lasts for 30 ms	Odd-skip auto restart
Output over-voltage	V_{ZCD} > 2 V and lasts for 10 consecutive pulses	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J > 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} < 0.1 V, lasts for 5 µs and 3 consecutive pulses	Odd-skip auto restart
V CC short-to-GND (V_{VCC} = 0 V, $R_{StartUp}$ = 50 MΩ and V_{Drain} = 90 V)	V_{VCC} < 1.2 V, $I_{VCC\_Charge1}$ ≈ 0.2 A	Cannot start up

6 Circuit diagram

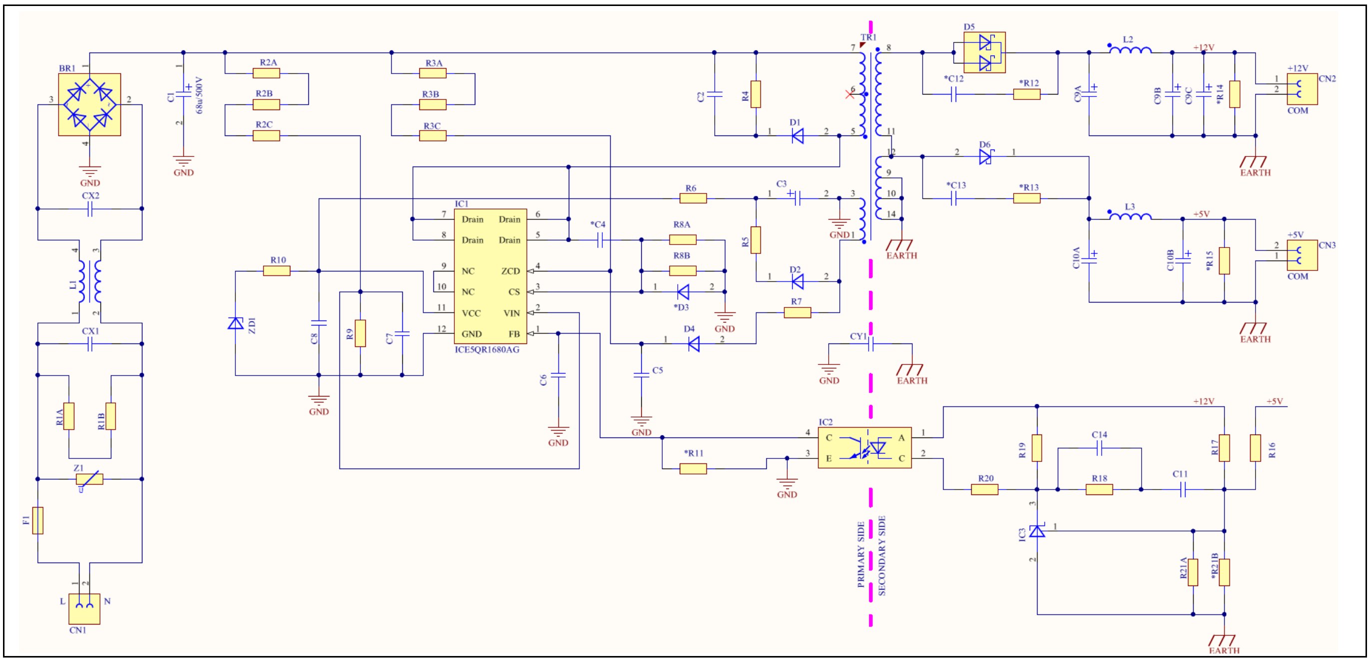


Figure 2 Schematic of DEMO_5QR1680AG_27W1

Note: General guidelines for layout design of PCB:

1. *Star ground at bulk capacitor C1: all primary grounds should be connected to the ground of bulk capacitor C1 separately in one point. This effectively reduces the switching noise going into the sensitive pins of the CoolSET™ device. The primary star ground can be split into four groups, as follows:*
   i. *Combine signal (all small signal grounds connecting to the CoolSET™ GND pin, such as filter capacitor grounds C6, C7, C8 and optocoupler ground) and power grounds (CS resistors R8A and R8B)*
   ii. *VCC ground includes the VCC capacitor ground C3 and the auxiliary winding ground, pin 3 of the power transformer*
   iii. *EMI return ground includes Y capacitor CY1*
   iv. *DC ground from bridge rectifier BR1*
2. *Filter capacitor close to the controller ground: filter capacitors C6, C7 and C8 should be placed as close to the controller ground and the controller pin as possible to reduce the switching noise coupled into the controller.*
3. *HV traces clearance: HV traces should retain enough spacing from the nearby traces. Otherwise, arcing could occur.*
   i. *400 V traces (positive rail of bulk capacitor C1) to nearby trace: greater than 2.0 mm*
   ii. *600 V traces (drain voltage of CoolSET™ IC1) to nearby trace: greater than 2.5 mm*
4. *Recommended minimum 232 mm² copper area at drain pin to add on PCB for better thermal performance.*
5. *Power-loop area (bulk capacitor C1, primary winding of the transformer TR1 (pins 7 and 5), IC1 drain pin, IC1 CS pin and CS resistor R8A/R8B) should be as small as possible to minimize the switching emissions.*

7 PCB layout

7.1 Top side

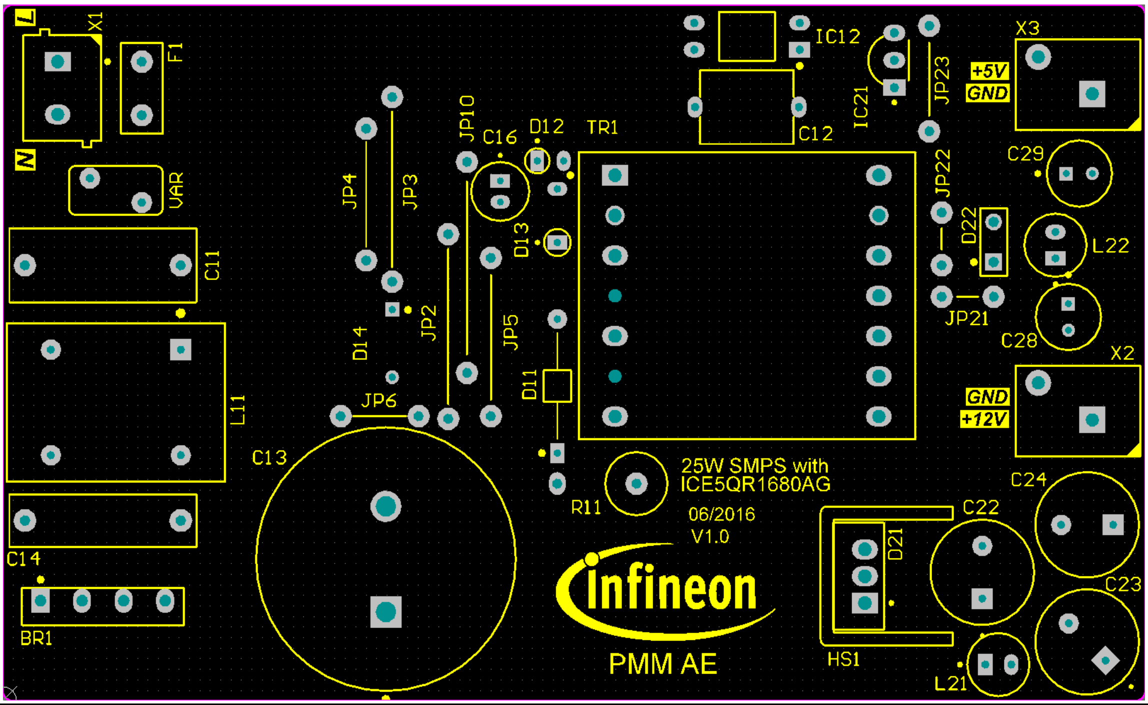


Figure 3 Top side component legend

7.2 Bottom side

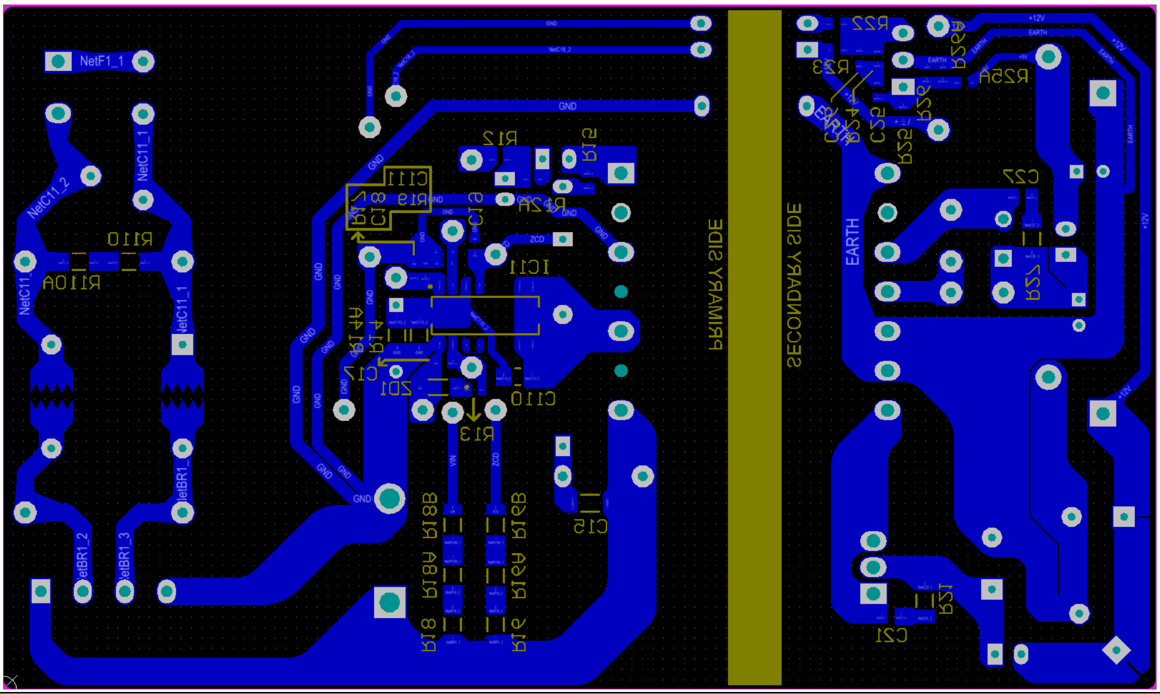


Figure 4 Bottom side copper and component legend

8 Bill of materials

Table 3 Bill of materials (V 0.7)

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/1 A	S1VBA60	Shindengen	1
2	CX1	0.22 µF/305 V	B32922C3224	Epcos	1
3	CY1	2.2 nF/500 V	DE1E3RA222MA4BQ	Murata	1
4	C1	68 µF/500 V	LGN2H680MELA25	Nichicon	1
5	CX2	0.1 µF/305 V	B329221C3104K	Epcos	1
6	C2	1 nF/1000 V	GRM31BR73A102KW01#	Murata	1
7	C3	22 µF/50 V	50PX22MEFC5X11	Rubycon	1
8	C8	100 nF/50 V	GRM188R71H104KA93D	Murata	1
9	C6, C7, C14	1 nF/50 V	GRM1885C1H102GA01D	Murata	3
10	C5	100 pF/50 V	GRM1885C1H101GA01D	Murata	1
11	C9A, C9B, C9C	1000 uF/16 V	16ZLH1000MEFC10X16	Rubycon	3
12	C11	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
13	C10A, C10B	330 uF/10 V	10ZLH330MEFC6.3X11	Rubycon	2
14	C100	22 nF/25 V	GRM188B11E223KA01D	Murata	1
15	D1	1 A/800 V	UF4006		1
16	D2	0.2 A/200 V	1N485B		1
17	D4	0.2 A/150 V/50 ns	FDH400		1
18	D5	10 A/100 V	MBRF10100CT	Vishay	1
19	D6	1 A/45 V	SB150	Vishay	1
20	F1	1.6 A/300 V	36911600000	Littlefuse	1
21	HS1	Heatsink	577202B00000G	AAVID	1
22	IC1	ICE5QR1680AG	ICE5QR1680AG	Infineon	1
23	IC2	Optocoupler	SFH617A-3		1
24	IC3	Shunt regulator	TL431BVLPG		1
25	L1	39 mH/0.7 A	B82732R2701B030	Epcos	1
26	L2	2.2 uH/4.3 A	744 746 202 2	Wurth Electronics	1
27	L3	4.7 uH/4.2 A	744 746 204 7	Wurth Electronics	1
28	R4	68 kR/2 W/500 V	MO2CT631R683J	KOA Speer	1
29	R6, R10	0 Ω (0603)			2
30	R5	4.7 Ω (0603)			1
31	R8A, R8B	1.2 R/0.25 W/±1%	ERJ8RQF1R2V	Panasonic	2
32	R7	30 kΩ/±1% (0603)			1
33	R3A, R3B, R3C	15 MR/0.25 W/5%	RC1206JR-0715ML		3
34	R2A, R2B, R2C	3 MR/0.25 W/1%	RC1206FR-073ML		3
35	R19	58.3 kR/0.1 W/0.5%	RT0603DRE0758K3L		1
36	R1A, R1B	1.5 MΩ/5%/200 V	RC1206FR-071M5L		2
37	R20	820 Ω (0603)			1
38	R19	1.2 kΩ (0603)			1
39	R18	68 kΩ (0603)			1
40	R17	110 kΩ (0603)			1

Bill of materials

41	R16	15 kΩ (0603)			1
42	R21A	10 kΩ (0603)			1
43	TR1	400 µH	750343389 (Rev 0.0)	Wurth Electronics	1
44	Z1	0.25 W/320 V	B72207S2321K101	Epcos	1
45	ZD1	22 V Zener			1
46	CN1 (L N)	Connector	691102710002	Wurth Electronics	1
47	CN2 (+12 V com), CN3 (+5 V com)	Connector	691 412 120 002B	Wurth Electronics	2

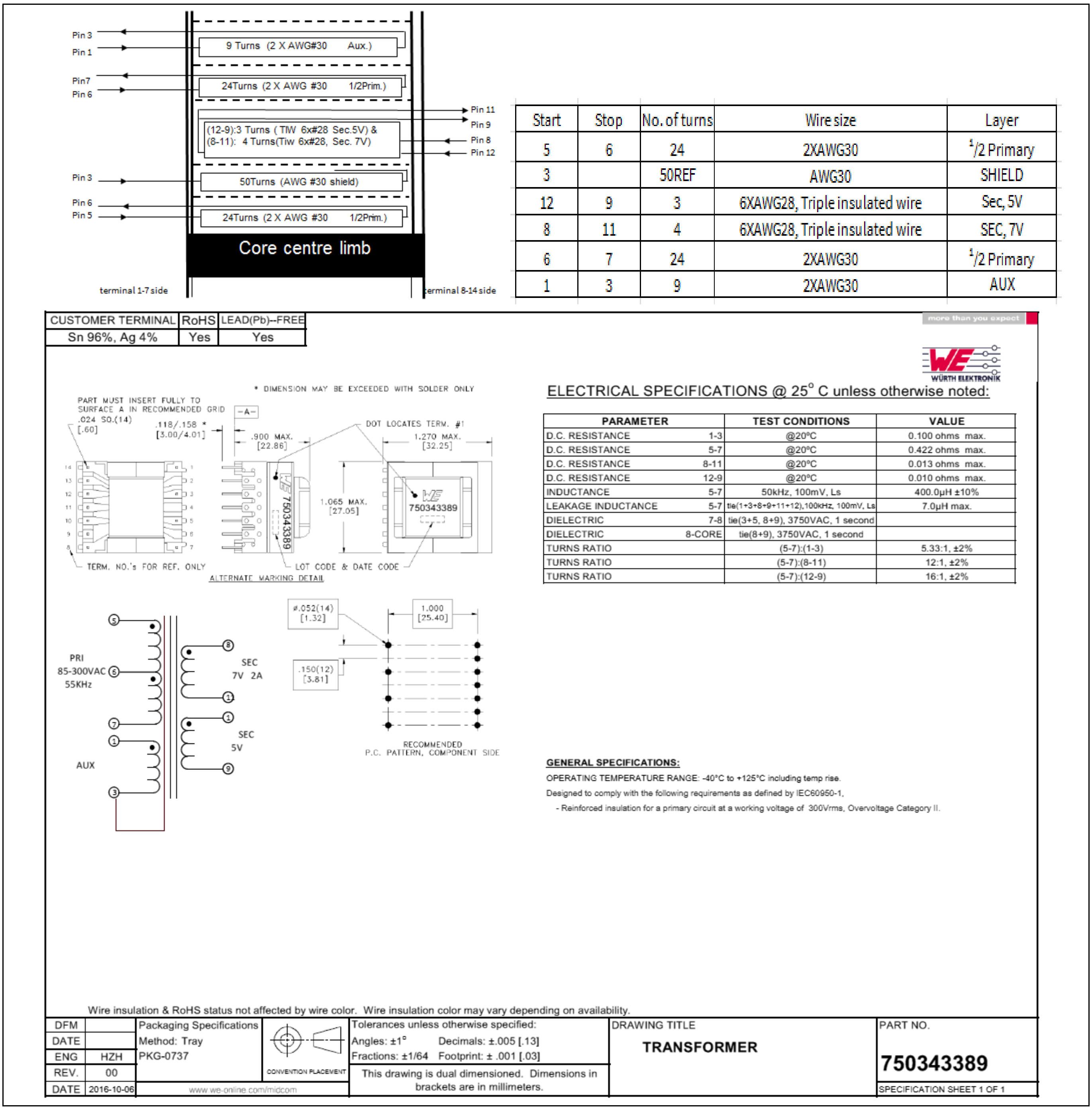
9 Transformer construction

Core and materials: EE25/13/7(EF25), TP4A (TDG)

Bobbin: 070-5644 (14-pin, THT, horizontal version)

Primary inductance: Lp = 400 µH (±10%), measured between pin 5 and pin 7

Manufacturer and part number: Wurth Electronics Midcom (750343389)



Start	Stop	No. of turns	Wire size	Layer
5	6	24	2XAWG30	1/2 Primary
3		50REF	AWG30	SHIELD
12	9	3	6XAWG28, Triple insulated wire	Sec, 5V
8	11	4	6XAWG28, Triple insulated wire	SEC, 7V
6	7	24	2XAWG30	1/2 Primary
1	3	9	2XAWG30	AUX

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-3	@20°C	0.100 ohms max.
D.C. RESISTANCE	5-7	@20°C	0.422 ohms max.
D.C. RESISTANCE	8-11	@20°C	0.013 ohms max.
D.C. RESISTANCE	12-9	@20°C	0.010 ohms max.
INDUCTANCE	5-7	50kHz, 100mV, Ls	400.0µH ±10%
LEAKAGE INDUCTANCE	5-7	tie(1+3+8+9+11+12),100kHz, 100mV, Ls	7.0µH max.
DIELECTRIC	7-8	tie(3+5, 8+9), 3750VAC, 1 second	
DIELECTRIC	8-CORE	tie(8+9), 3750VAC, 1 second	
TURNS RATIO		(5-7):(1-3)	5.33:1, ±2%
TURNS RATIO		(5-7):(8-11)	12:1, ±2%
TURNS RATIO		(5-7):(12-9)	16:1, ±2%

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	V_{out1} (V DC)	I_{out1} (A)	V_{out2} (V DC)	I_{out2} (A)	$V_{OutRPP1}$ (mV)	$V_{OutRPP2}$ (mV)	P_{out} (W)	Efficiency η (%)	Average η (%)	OLP P_{in} (W)	OLP I_{out12V} (fixed 5 V at 0.2 A) (A)
85 V AC/ 60 Hz	0.0360	11.94	0.000	4.93	0.0000	40	17				41.50	2.72
	0.080	12.92	0.0000	4.80	0.0060	23	76	0.03				
	8.040	11.93	0.540	4.93	0.0500	15	80	6.69	83.19			
	14.770	11.87	1.000	4.94	0.0600	116	14	12.17	82.37	82.26		
	16.14	11.92	1.080	4.93	0.1000	103	17	13.37	82.82			
	24.47	11.91	1.630	4.93	0.1500	113	17	20.15	82.36			
	33.29	11.92	2.170	4.93	0.2000	110	16	26.85	80.66			
115 V AC/ 60 Hz	0.0400	11.94	0.000	4.93	0.0000	42	18				46.00	3.17
	0.085	12.94	0.0000	4.80	0.0060	25	80	0.03				
	7.990	11.93	0.540	4.93	0.0500	83	17	6.69	83.72			
	14.520	11.87	1.000	4.94	0.0600	116	17	12.17	83.79	83.88		
	15.88	11.93	1.080	4.93	0.1000	103	15	13.38	84.24			
	24.04	11.92	1.630	4.93	0.1500	113	17	20.17	83.90			
	32.10	11.92	2.170	4.93	0.2000	126	17	26.85	83.65			
230 V AC/ 50 Hz	0.069	11.94	0.000	4.93	0.0000	45	20				47.50	3.31
	0.114	12.97	0.0000	4.79	0.0060	28	82	0.03				
	8.220	11.92	0.540	4.93	0.0500	83	23	6.68	81.31			
	14.620	11.87	1.000	4.94	0.0600	110	25	12.17	83.22	83.23		
	16.05	11.92	1.080	4.93	0.1000	110	25	13.37	83.28			
	24.04	11.92	1.630	4.93	0.1500	130	20	20.17	83.90			
	31.81	11.92	2.170	4.93	0.2000	133	22	26.85	84.42			
265 V AC/ 50 Hz	0.071	11.93	0.000	4.93	0.0000	46	20				48.50	3.40
	0.134	12.98	0.0000	4.79	0.0060	27	88	0.03				
	8.360	11.92	0.540	4.93	0.0500	83	22	6.68	79.95			
	14.750	11.86	1.000	4.94	0.0600	103	22	12.16	82.42	82.43		
	16.19	11.92	1.080	4.93	0.1000	106	23	13.37	82.56			
	24.23	11.91	1.630	4.94	0.1500	113	22	20.15	83.18			
	31.95	11.92	2.170	4.93	0.2000	133	23	26.85	84.05			
300 V AC/ 50 Hz	0.101	11.93	0.000	4.93	0.0000	46	20				50.50	3.50
	0.155	12.97	0.0000	4.79	0.0060	45	87	0.03				
	8.520	11.91	0.540	4.94	0.0500	86	20	6.68	78.38			
	14.760	11.85	1.000	4.94	0.0600	103	20	12.15	82.29	81.57		
	16.33	11.91	1.080	4.94	0.1000	103	20	13.36	81.79			
	24.40	11.91	1.630	4.94	0.1500	110	22	20.15	82.60			
	32.13	11.91	2.170	4.93	0.2000	130	23	26.83	83.51			

Minimum load condition : 5 V @ 6 mA

Typical load condition : 5 V @ 60 mA and 12 V @ 1 A

Maximum load condition : 5 V @ 200 mA and 12 V @ 2.17 A

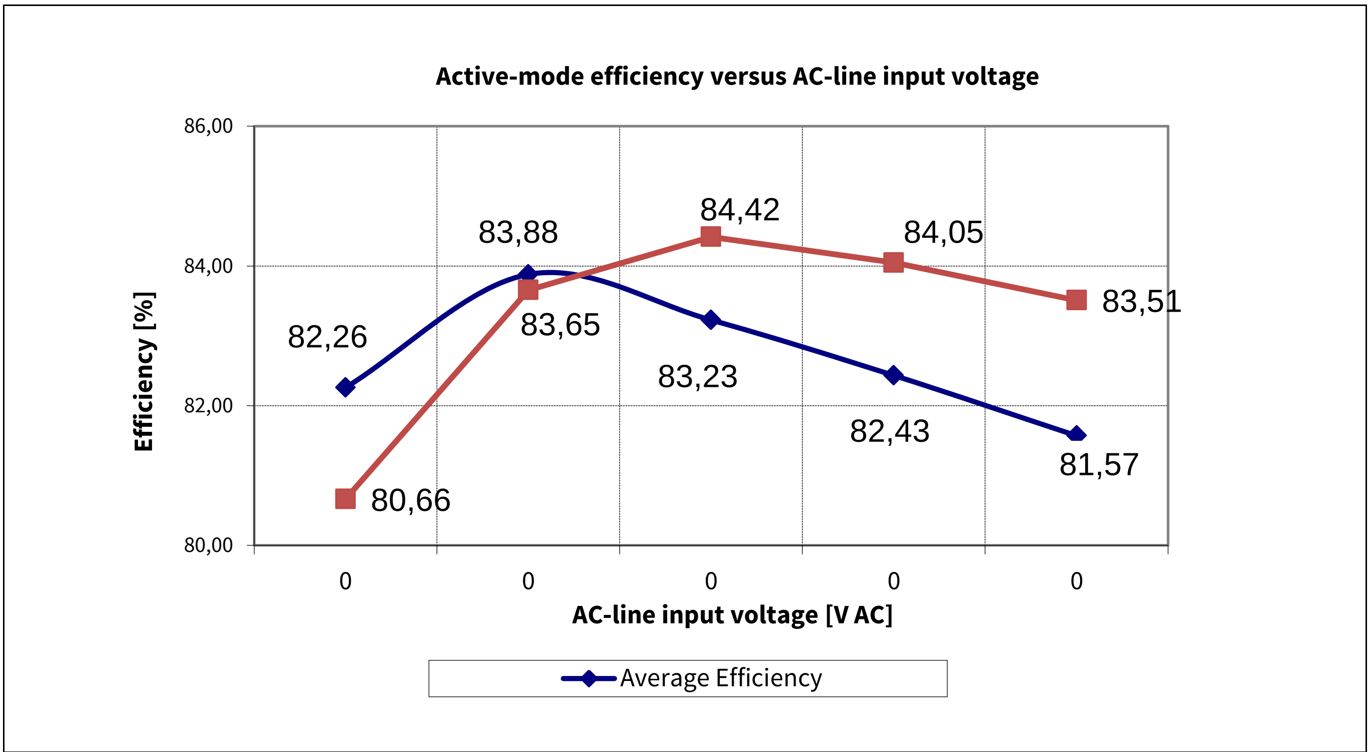


Figure 6 Efficiency vs AC-line input voltage

10.2 Standby power

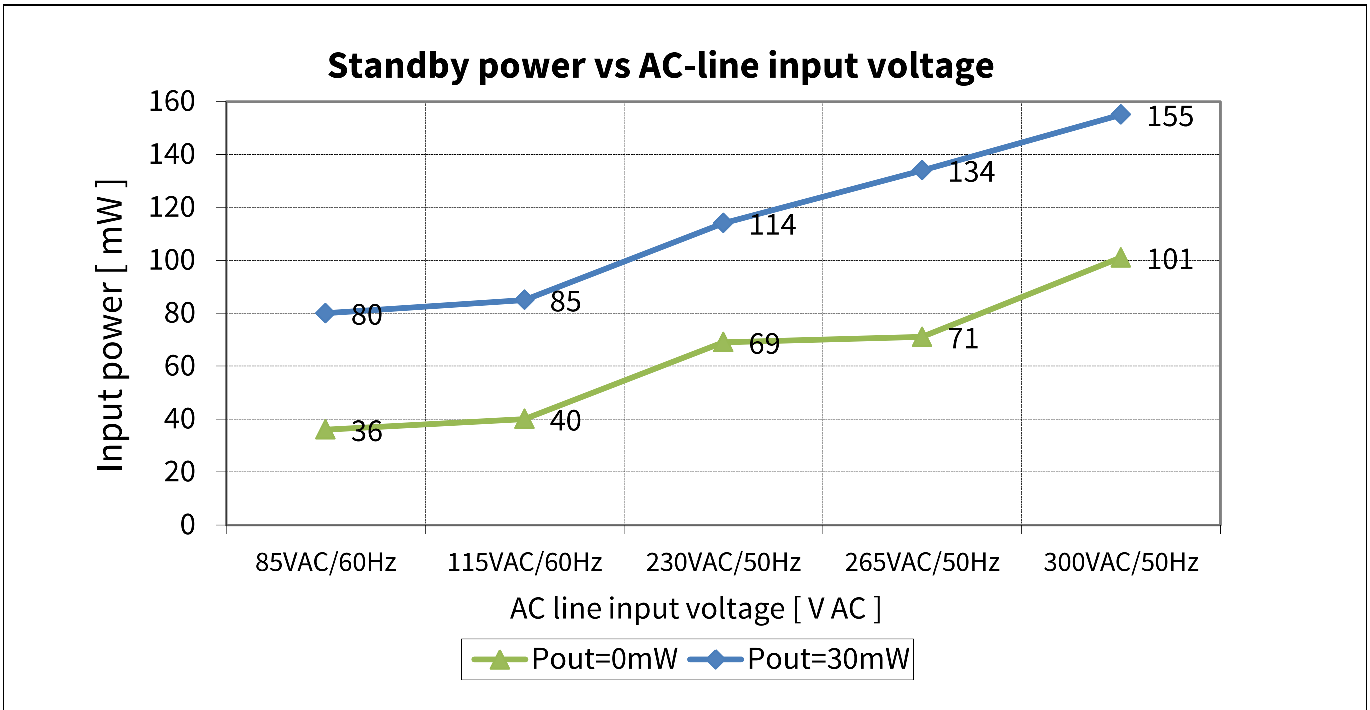


Figure 7 Standby power at no-load and 30 mW load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

10.3 Line regulation

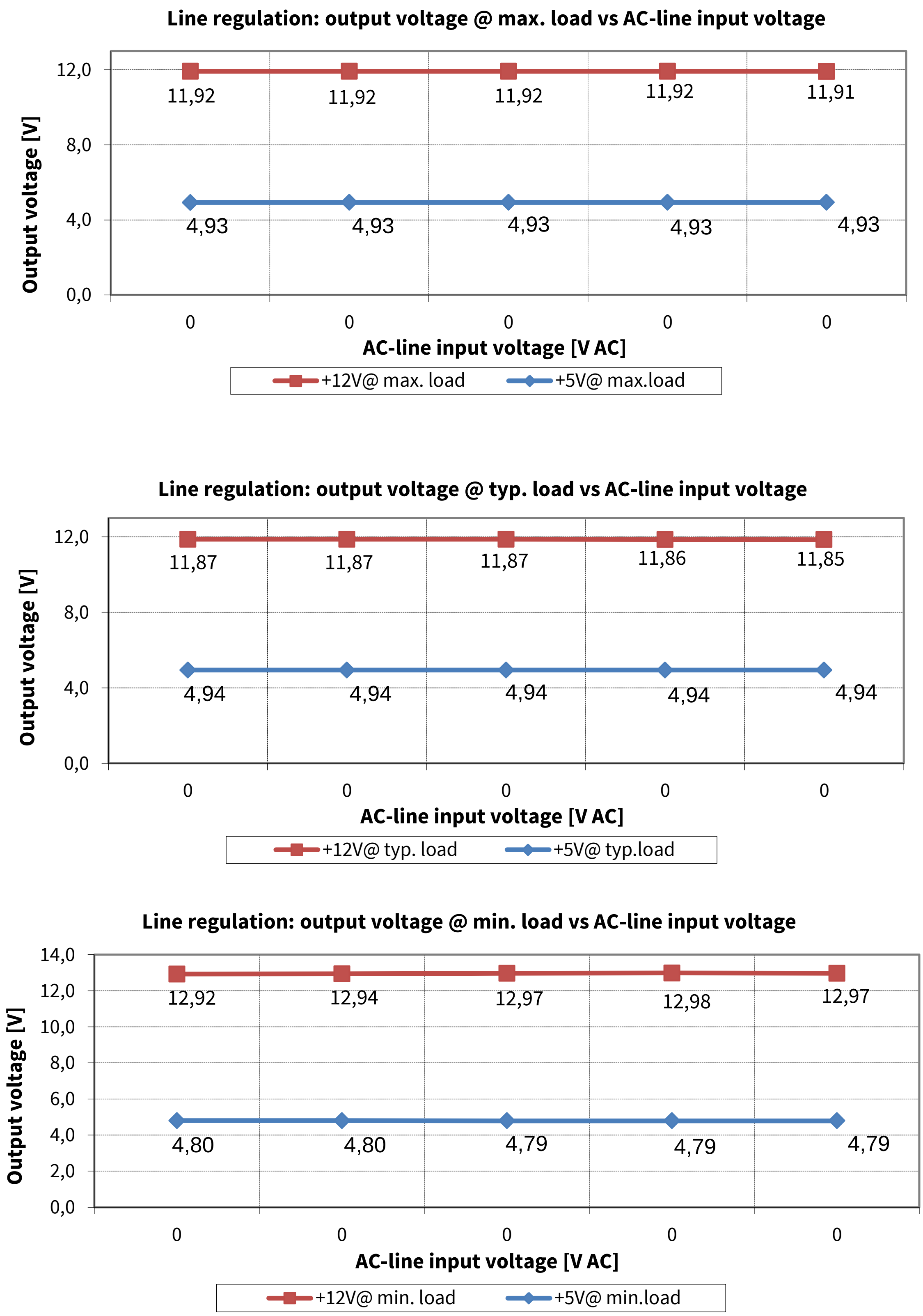


Figure 8 Line regulation V_{Out} at full-load vs AC-line input voltage

10.4 Load regulation

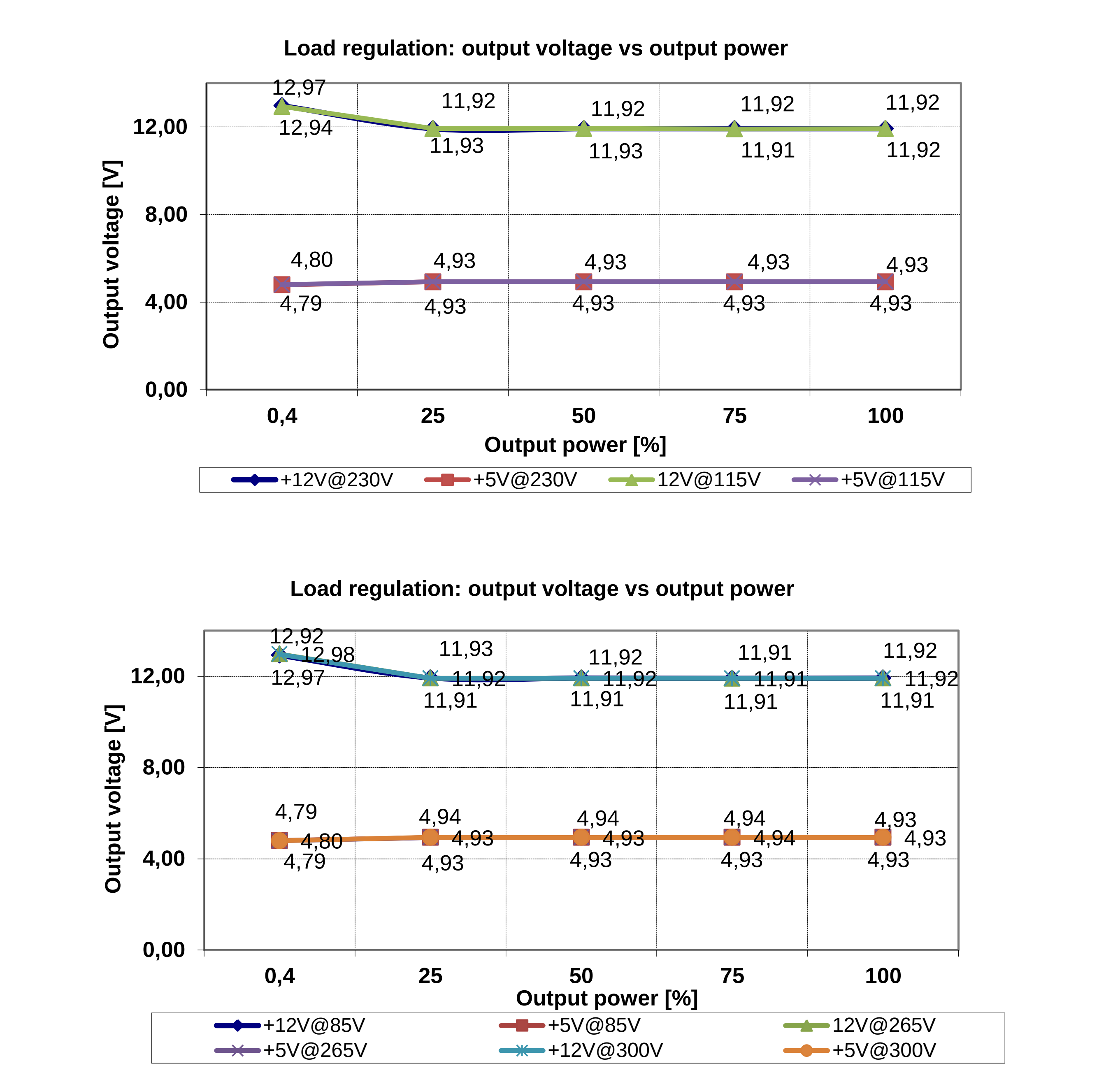


Figure 9 Load regulation V_{Out} vs output power

10.5 Maximum input power

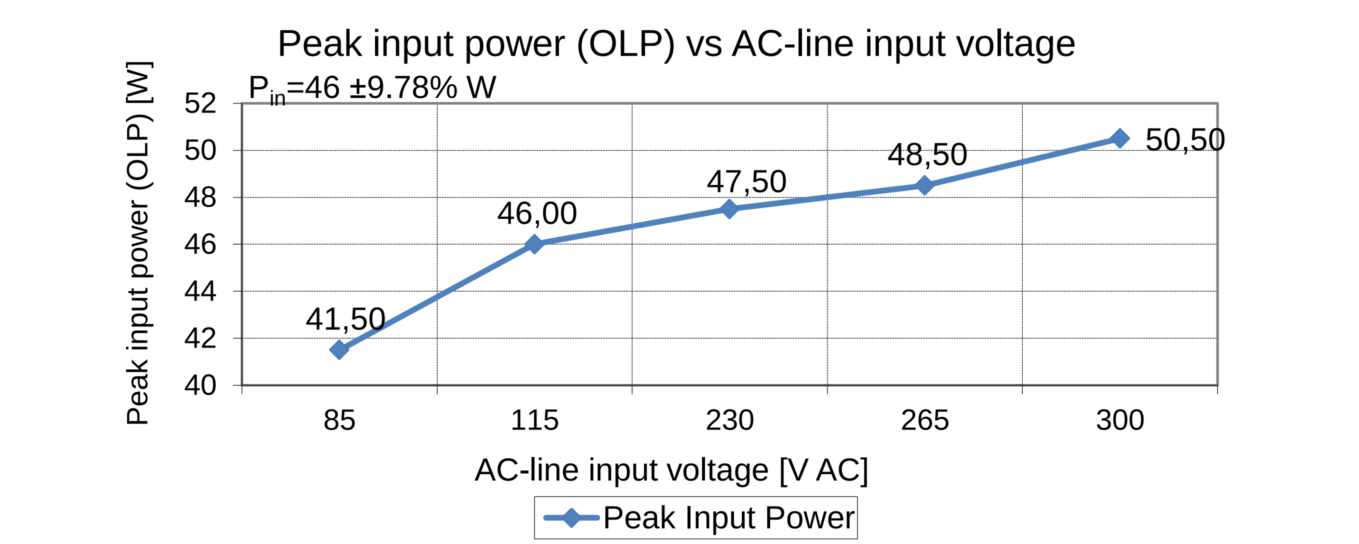


Figure 10 Maximum input power (before over-load protection) vs AC-line input voltage

10.6 ESD immunity (EN 61000-4-2)

Pass EN 61000-4-2 special level (±14 kV for contact discharge and ±16 kV air discharge).

10.7 Surge immunity (EN 61000-4-5)

Pass EN 61000-4-5 installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth).[1]

10.8 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The demo board was set up at maximum load (27 W) with input voltage of 115 V AC and 230 V AC.

[1] PCB spark-gap distance needs to reduce to 0.5 mm and C1 change to 120 µF.

Test results

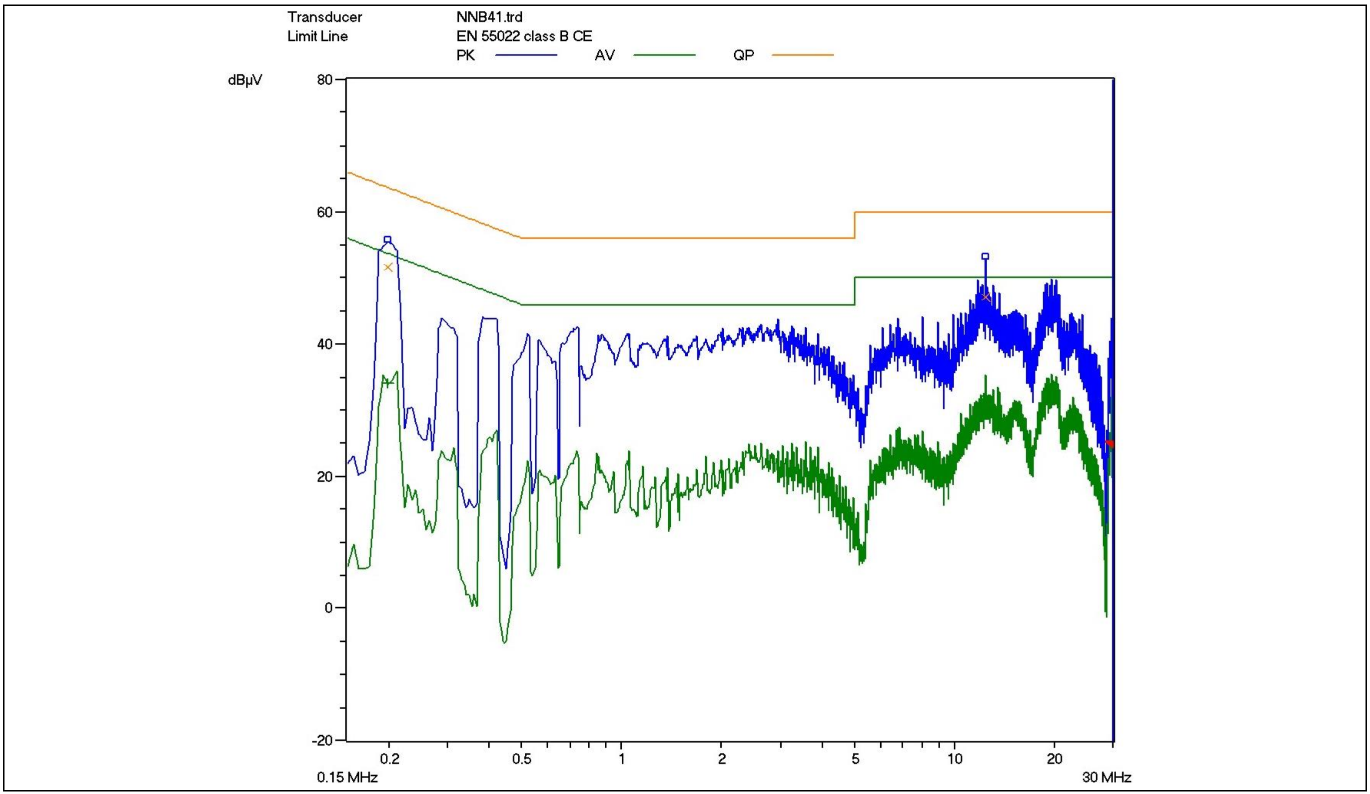


Figure 11 Conducted emissions (line) at 115 V AC and maximum load

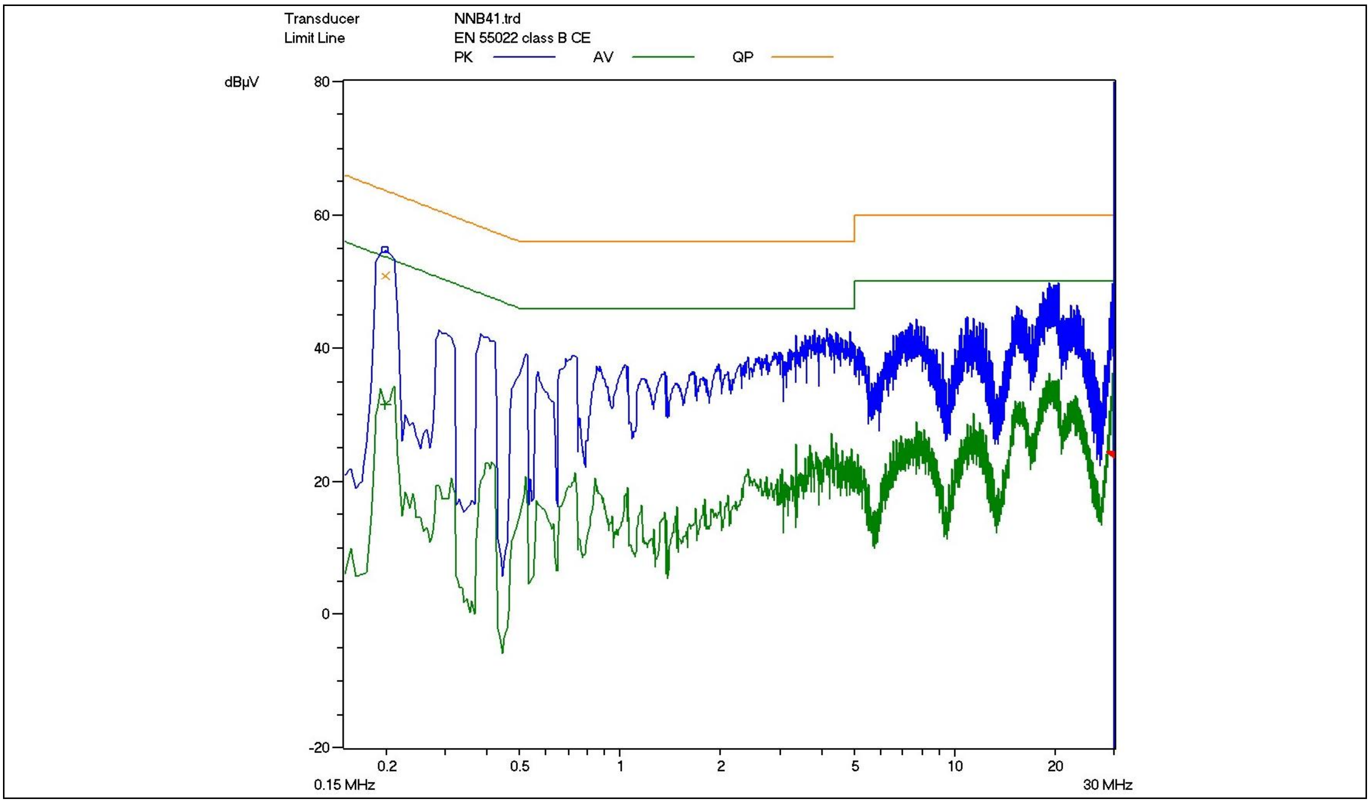


Figure 12 Conducted emissions (neutral) at 115 V AC and maximum load

Pass conducted emissions EN 55022 (CISPR 22) class B with 10 dB margin for quasi peak measurement at low-line (115 V AC).

Test results

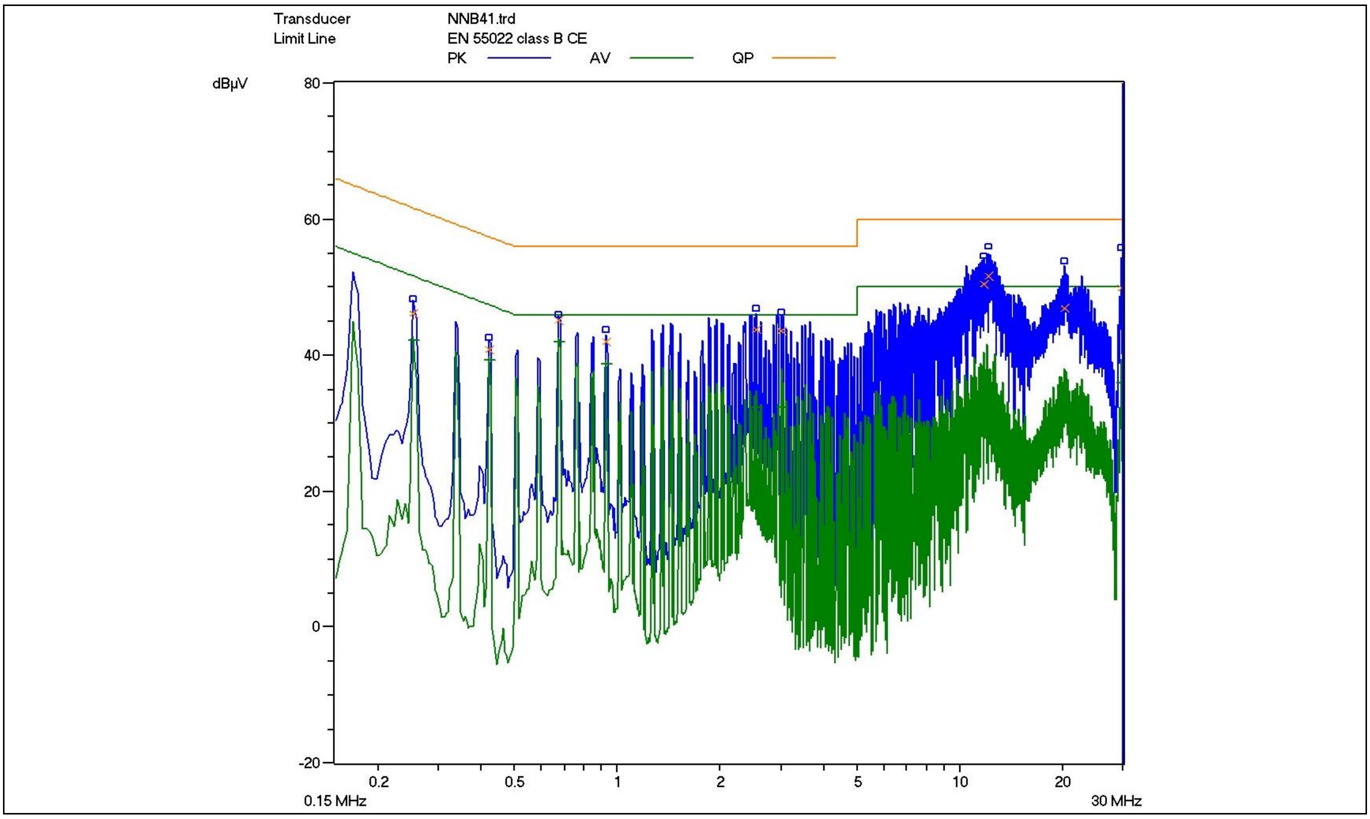


Figure 13 Conducted emissions (line) at 230 V AC and maximum load

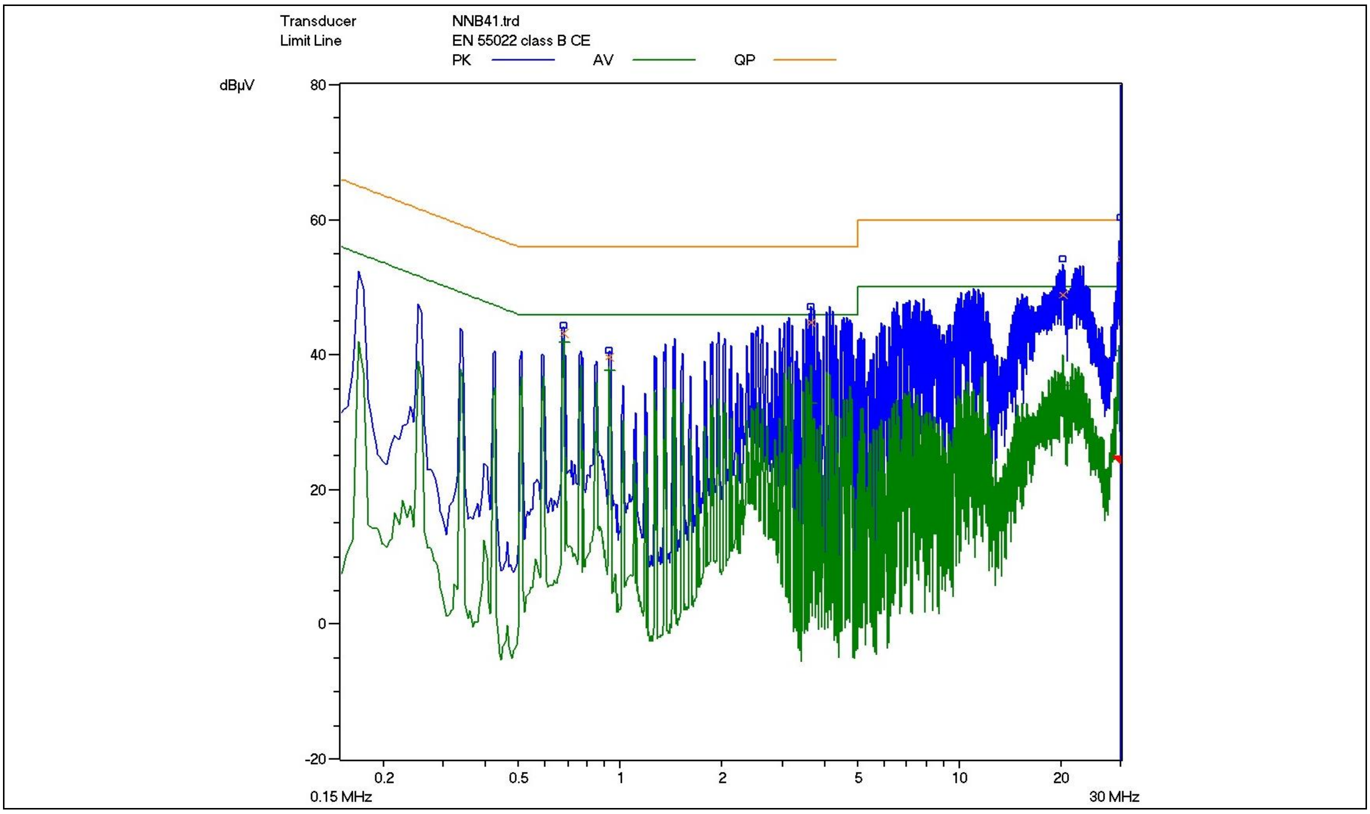


Figure 14 Conducted emissions (neutral) at 230 V AC and maximum load

Pass conducted emissions EN 55022 (CISPR 22) class B with 6 dB margin for quasi peak measurement at high-line (230 V AC).

10.9 Thermal measurement

The thermal test of the open-frame demo board was done using an infrared thermography camera (FLIR-T420) at an ambient temperature of 25°C. The measurements were taken after one hour running at full-load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	TR1 (transformer)	60.2	69.8
2	D21 (secondary diode)	77.0	77.9
3	IC11 (ICE5QR1680AG)	84.5	89.2
4	L11 (choke)	85.1	39.2
5	Ambient	25.0	25.0

85 V AC full-load and 25°C ambient **300 V AC full-load and 25°C ambient**

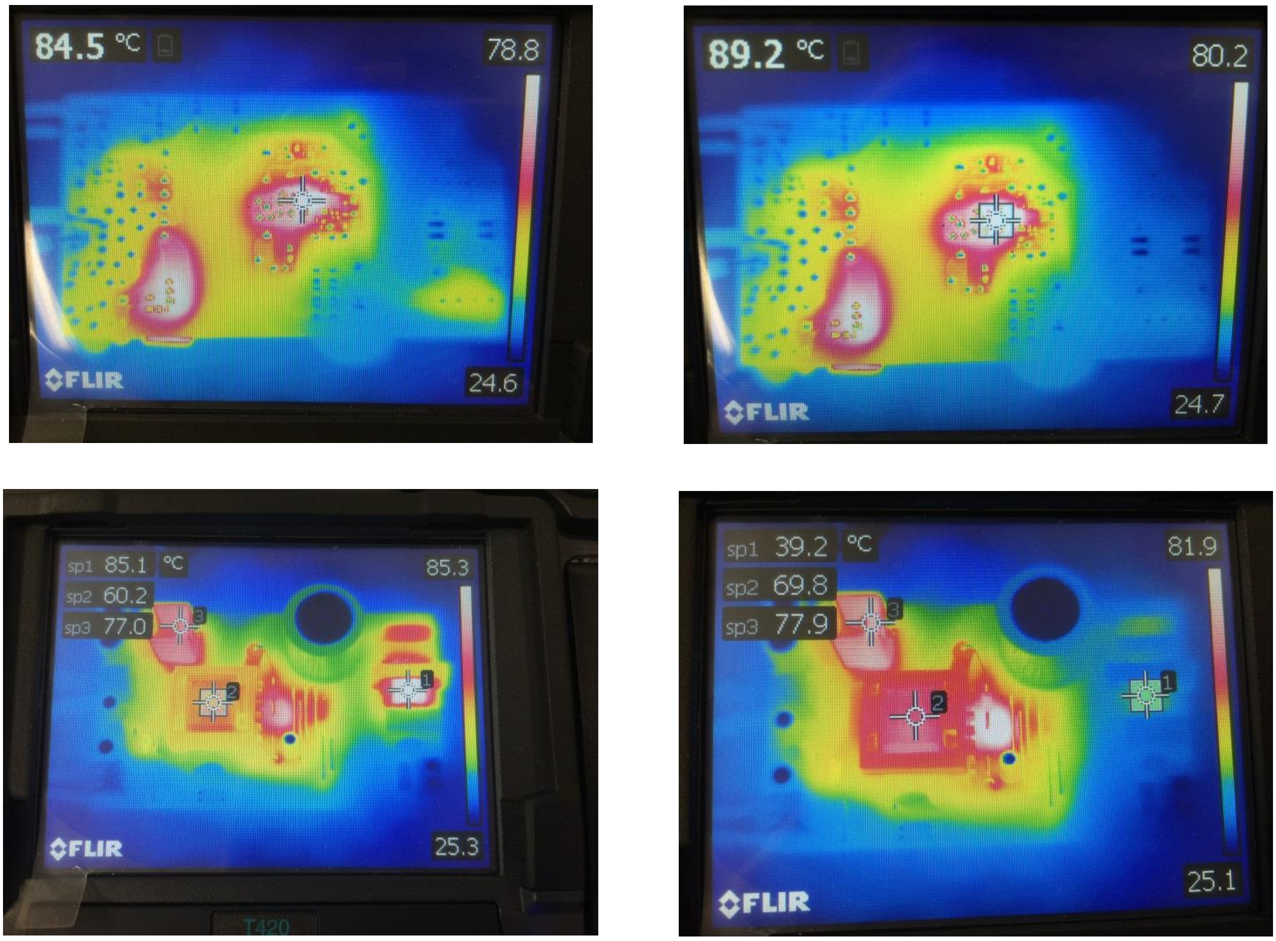


Figure 15 Infrared thermal image of DEMO_5QR1680AG_27W1

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a TELEDYNELECROY 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

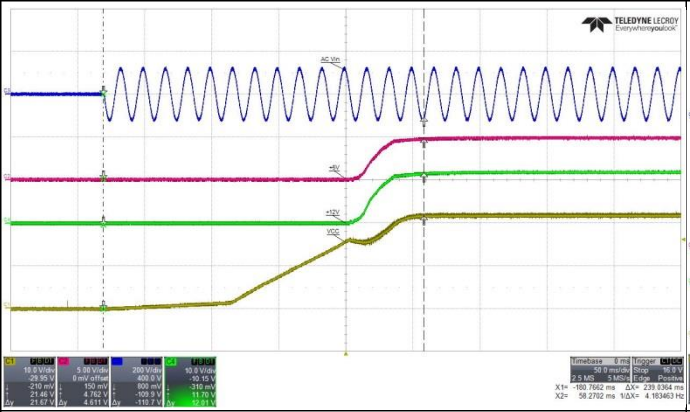
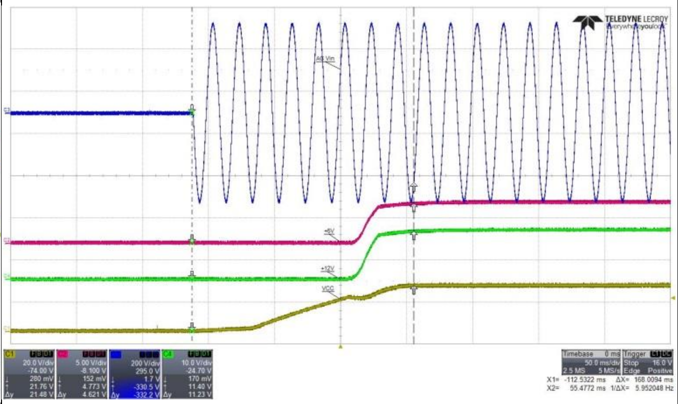
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : 5 V output voltage (V_{Out5}) C3 (blue) : AC-line voltage (AC_V_{IN}) C4 (green) : 12 V output voltage (V_{Out12})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : 5 V output voltage (V_{Out5}) C3 (blue) : AC-line voltage (AC_V_{IN}) C4 (green) : 12 V output voltage (V_{Out12})
Start-up time at 85 V AC and maximum load ≈ 239 ms	Start-up time at 300 V AC and maximum load ≈ 168 ms

Figure 16 Start-up

11.2 Soft-start

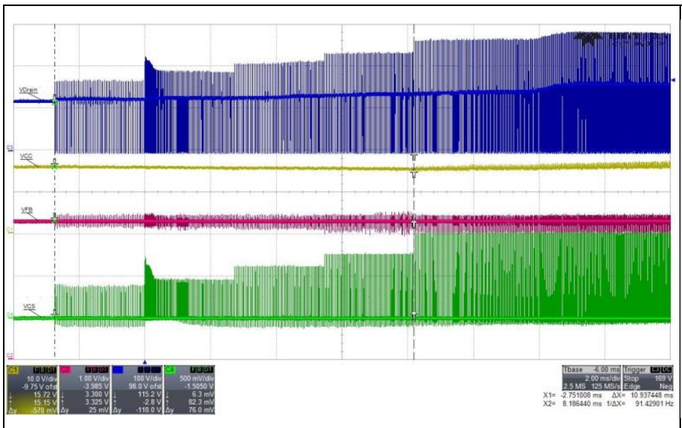
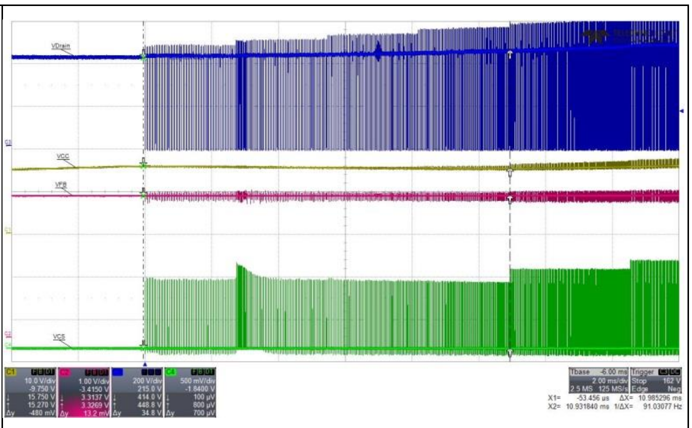
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Soft-start time at 85 V AC and maximum load ≈ 10.9 ms	Soft-start time at 300 V AC and maximum load ≈ 10.9ms

Figure 17 Soft-start

11.3 Drain and CS voltage at maximum load

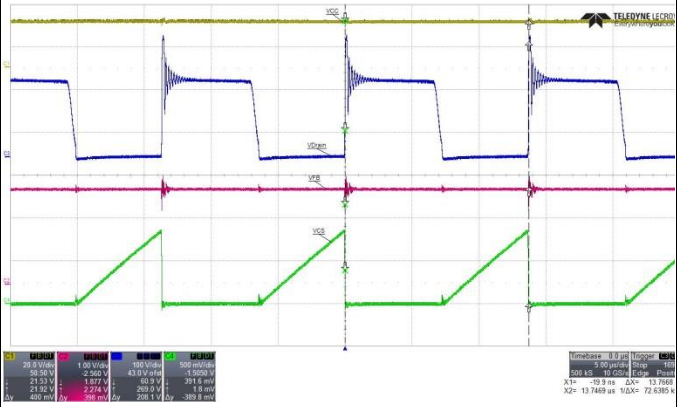
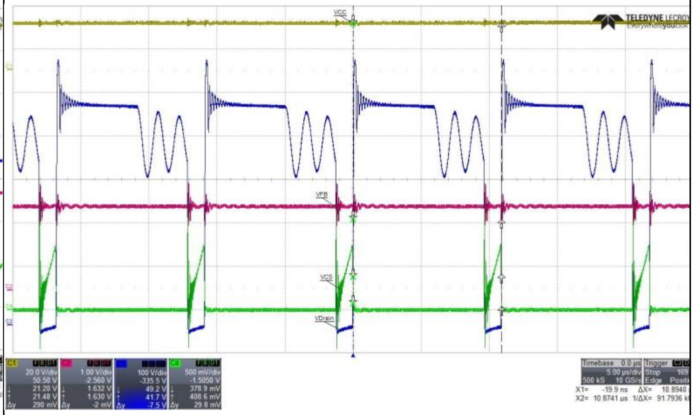
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
V_{Drain_peak} ≈ 278 V @ 85 V AC with 1st ZC and f_S ≈ 72.6 kHz	V_{Drain_peak} ≈ 610 V @ 300 V AC with 3rd ZC and f_S ≈ 91.8 kHz

Figure 18 Drain and CS voltage at maximum load

11.4 Zero crossing point during normal operation

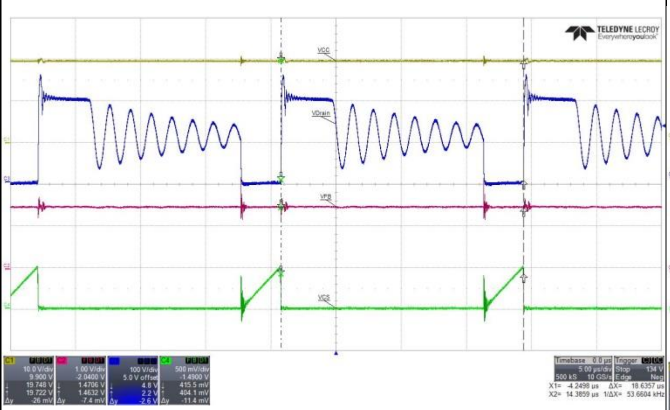
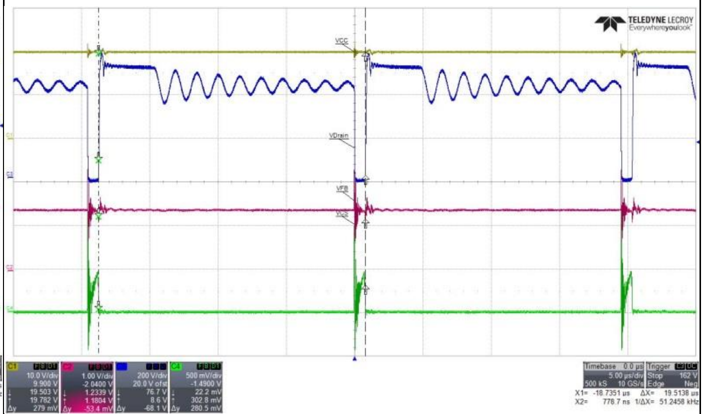
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
8th ZC at 85 V AC (ZC varies from 1~8 for low-line)	10th ZC at 300 V AC (ZC varies from 3~10 for high-line)

Figure 19 Zero crossing

11.5 Load transient response (dynamic load from 10% to 100%)

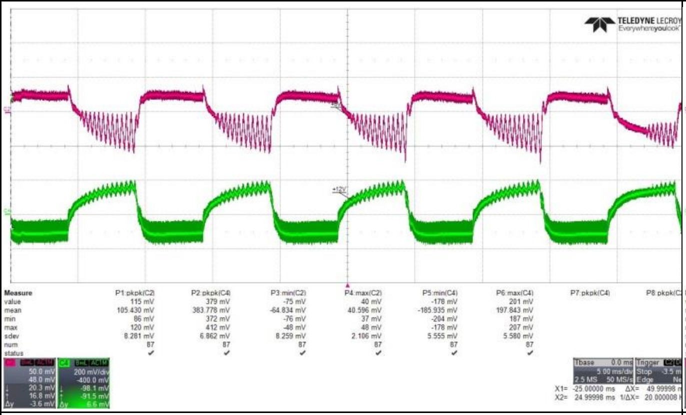
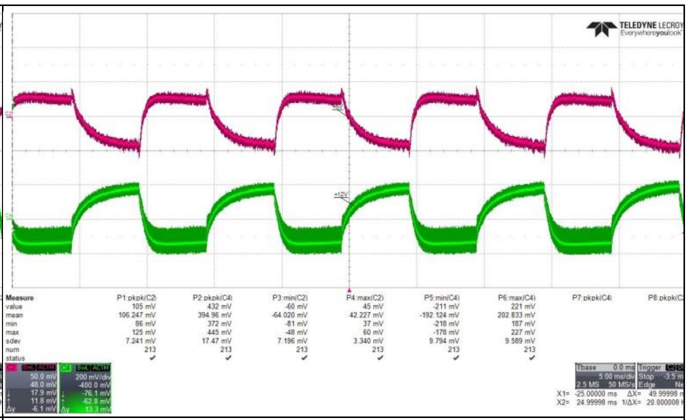
	
C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})	C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 115 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 379 mV (12 V load change from 10% to 100% and 5 V at 200 mA load at 85 V AC, 100 Hz, 0.4 A/μs slew rate) Probe terminal end with decoupling capacitor of 0.1 μF (ceramic) and 1 μF (electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 105 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 432 mV (12 V load change from 10% to 100% and 5 V at 200 mA load at 300 V AC, 100 Hz, 0.4 A/μs slew rate) Probe terminal end with decoupling capacitor of 0.1 μF (ceramic) and 1 μF (electrolytic), 20 MHz filter

Figure 20 Load transient response

11.6 Output ripple voltage at maximum load

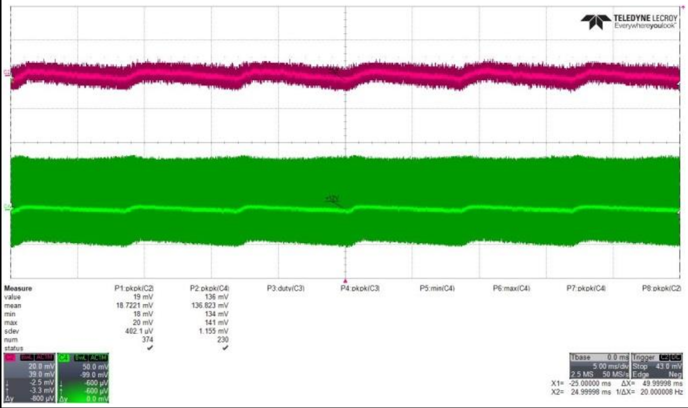
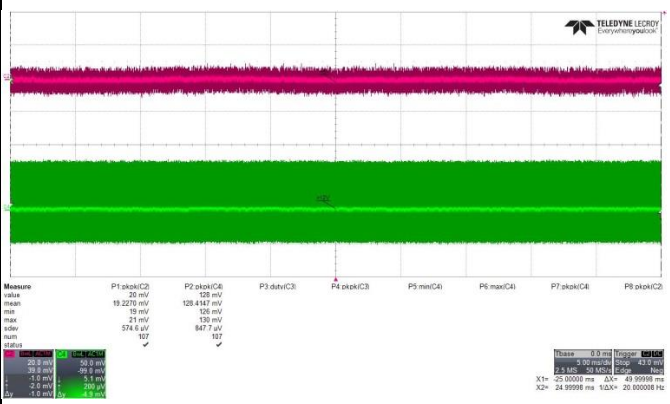
	
C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})	C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 19 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 136 mV Probe terminal end with decoupling capacitor of 0.1 μF (ceramic) and 1 μF (electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 20 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 128 mV Probe terminal end with decoupling capacitor of 0.1 μF (ceramic) and 1 μF (electrolytic), 20 MHz filter

Figure 21 Output ripple voltage at maximum load

11.7 Output ripple voltage at ABM 1 W load

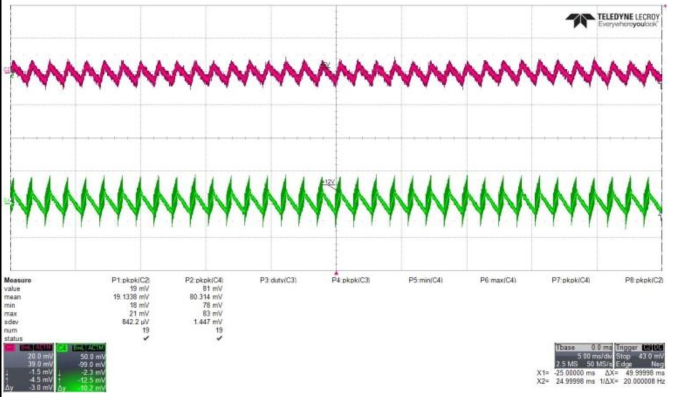
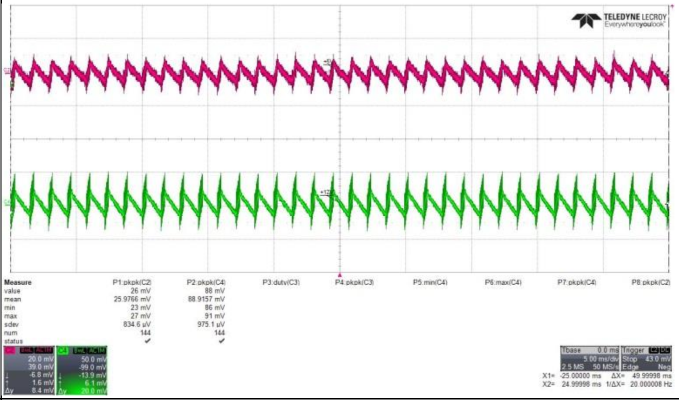
	
C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})	C2 (purple) : 5 V output ripple voltage (V_{Out5}) C4 (green) : 12 V output ripple voltage (V_{Out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 19 mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 81 mV Load: 5 V at 6 mA and 12 V at 80 mA Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 26 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 88 mV Load: 5 V at 6 mA and 12 V at 80 mA Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 22 Output ripple voltage at ABM 1 W load

11.8 Entering ABM

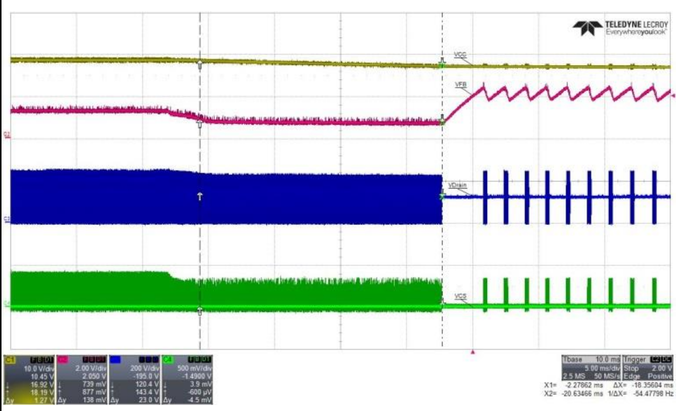
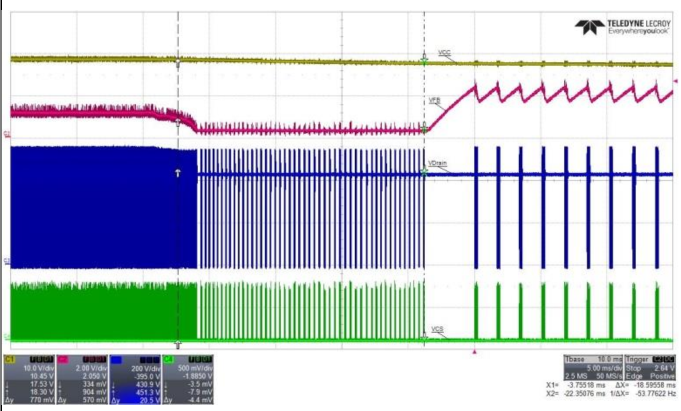
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Condition to enter ABM level 1: V_{FB} < 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms (Load change from 5 W to 0.5 W at 85 V AC)	Condition to enter ABM level 1 : V_{FB} < 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms (Load change from 5 W to 0.5 W at 300 V AC)

Figure 23 Entering ABM

11.9 During ABM

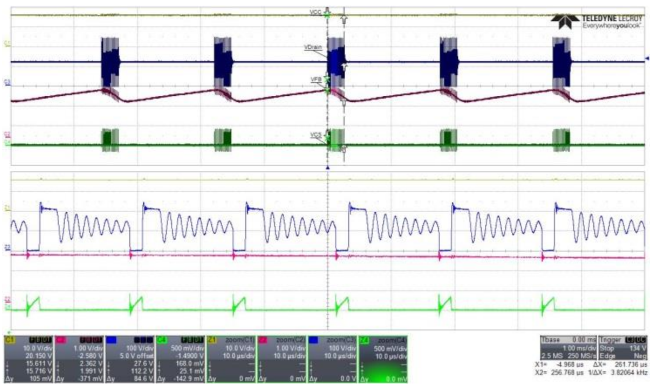
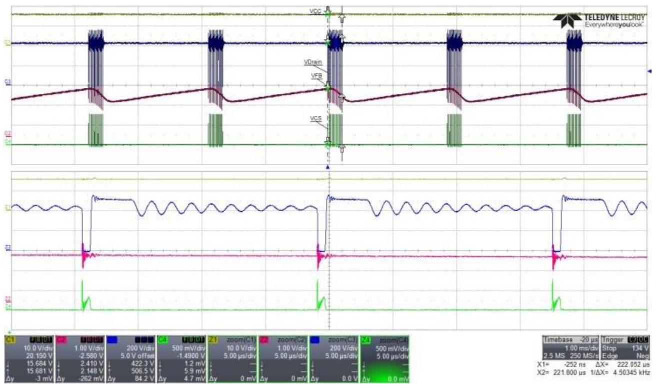
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
During ABM level 1: V_{FB_BOn} = 2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8 (0.5 W load at 85 V AC)	During ABM level 1: V_{FB_BOn} = 2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10 (0.5 W load at 300 V AC)

Figure 24 During ABM

11.10 Leaving ABM

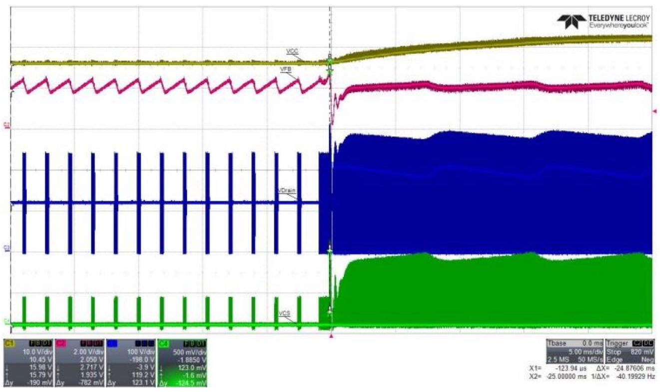
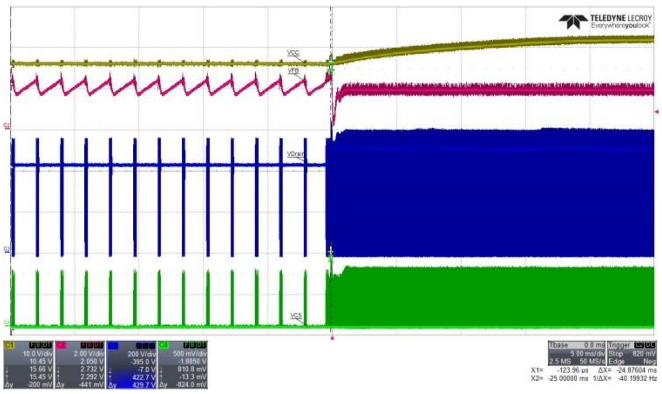
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Condition to leave ABM level 1: V_{FB} > 2.75 V (Load change from 0.5 W to full-load at 85 V AC)	Condition to leave ABM level 1: V_{FB} > 2.75 V (Load change from 0.5 W to full-load at 300 V AC)

Figure 25 Leaving ABM

11.11 Line OVP (non-switch auto restart)

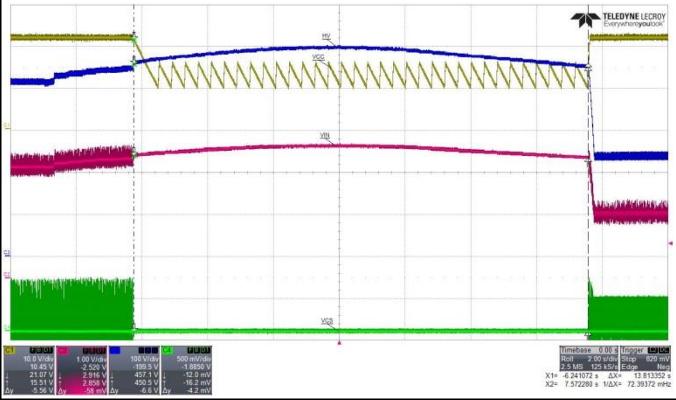
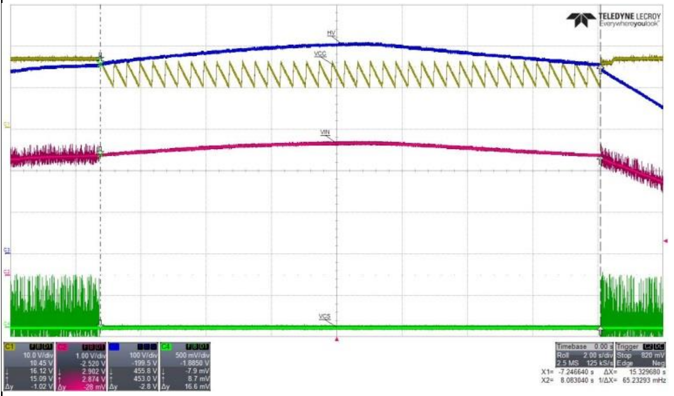
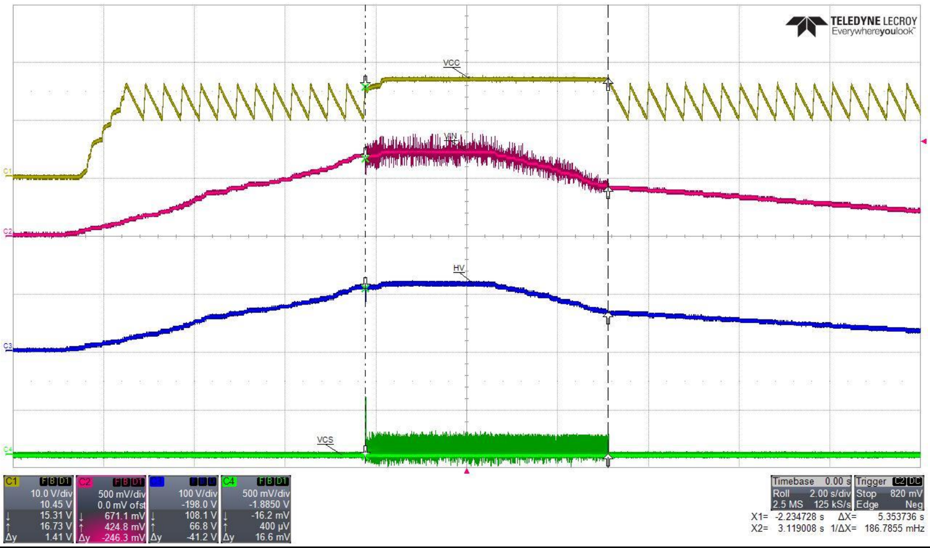
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : Bulk cap voltage (V_{Bulk}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : VIN voltage (V_{VIN}) C3 (blue) : Bulk cap voltage (V_{Bulk}) C4 (green) : CS voltage (V_{CS})
Condition to detect line OVP: V_{VIN} > 2.9 V Condition to reset line OVP: V_{VIN} < 2.9 V	
(Gradually increase AC-line voltage at full-load until line OVP detect and decrease AC-line until line OVP reset)	(Gradually increase AC-line voltage at 1 W load until line OVP detect and decrease AC-line until line OVP reset)

Figure 26 Line OVP

11.12 Brownout protection (non-switch auto restart)



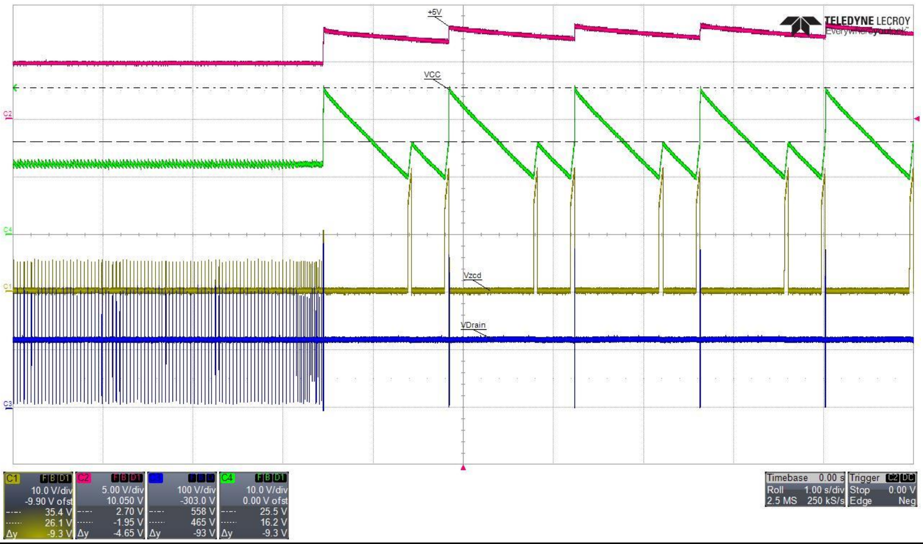
C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : V IN voltage (V_{VIN})
C3 (blue) : Bulk cap voltage (V_{Bulk})
C4 (green) : CS voltage (V_{CS})

Condition to reset brownout protection (brownin) : V_{VIN} > 0.66 V
Condition to detect brownout protection : V_{VIN} < 0.4 V

(Gradually increase AC-line voltage at 1 W load until system start and reduce the line until brownout detect)

Figure 27 Brownout protection

11.13 V_{CC} OVP (odd-skip auto restart)

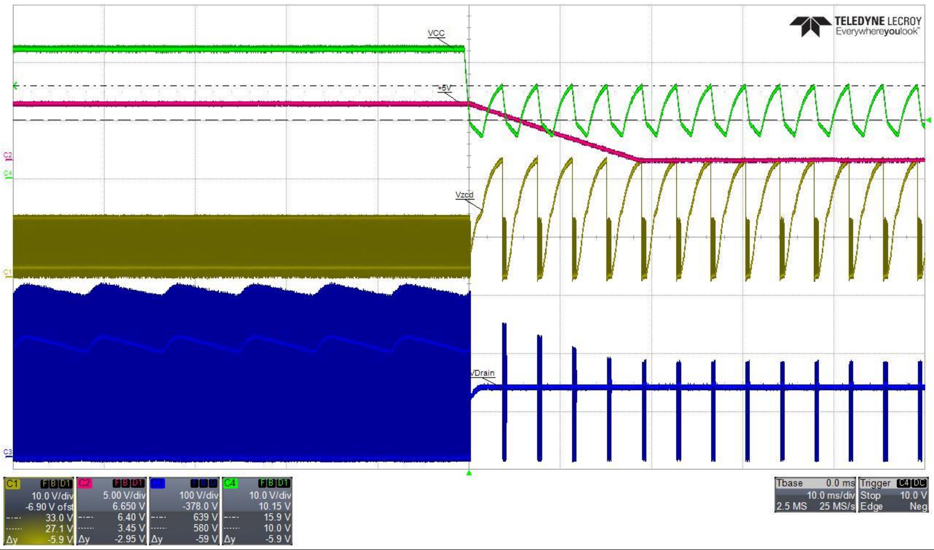


C1 (yellow) : ZCD voltage (V_{ZCD})
C2 (purple) : 5 V output ripple voltage (V_{Out5})
C3 (blue) : Drain voltage (V_D)
C4 (green) : Supply voltage (V_{VCC})

Condition to enter V_{VCC} OVP: V_{VCC} > 25.5 V
(85 V AC and disable ZCD pin output OVP detection, short R12A)

Figure 28 V_{CC} OVP

11.14 V_{CC} under-voltage protection (auto restart)

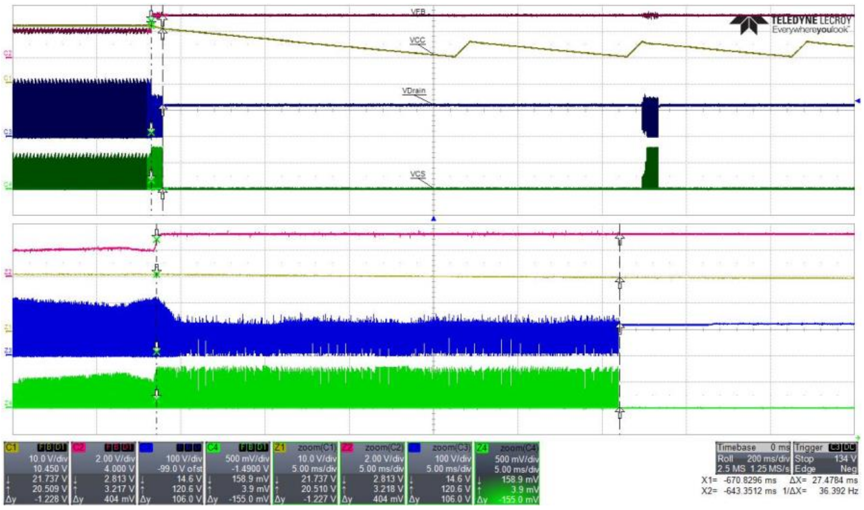


C1 (yellow) : ZCD voltage (V_{ZCD})
C2 (purple) : 5 V output ripple voltage (V_{Out5})
C3 (blue) : Drain voltage (V_D)
C4 (green) : Supply voltage (V_{VCC})

Condition to enter V CC under-voltage protection: V_{CC} < 10 V
(Remove R6 during normal operation @ 85 V AC)

Figure 29 V_{CC} under-voltage protection

11.15 Over-load protection (odd-skip auto restart)



C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : FB voltage (V_{FB})
C3 (blue) : Drain voltage (V_{D})
C4 (green) : CS voltage (V_{CS})

Condition to enter OVP: V_{FB} > 2.75 V and lasts for 30 ms blanking time
(12 V output load change from full-load to short at 85 V AC)

Figure 30 OVP

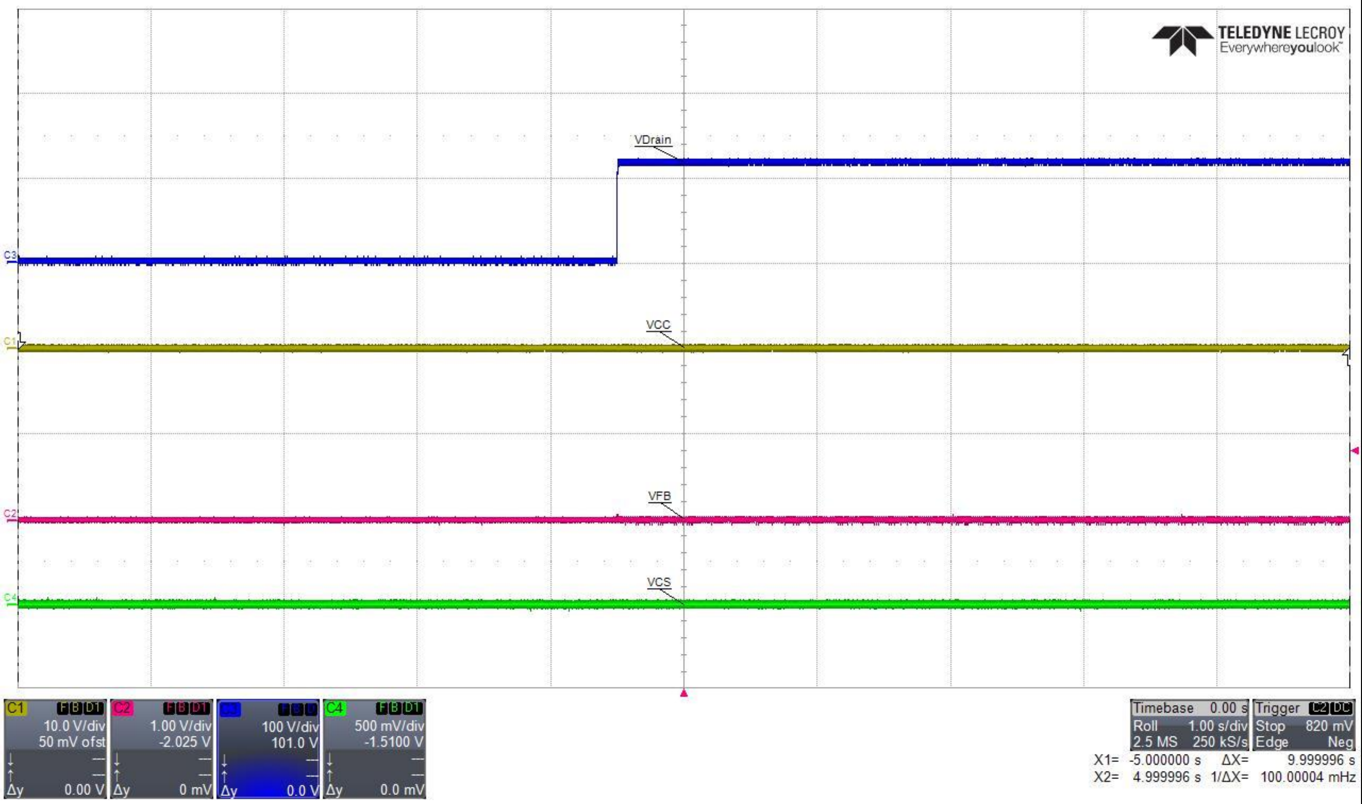
11.16 Output OVP (odd-skip auto restart)

C1 (yellow) : ZCD voltage (V_{ZCD})
C2 (purple) : 5 V output voltage (V_{O5})
C3 (blue) : Drain voltage (V_{D})
C4 (green) : 12 V output voltage (V_{O12})

Condition to enter output OVP: V_{O12} > 17 V, V_{O12} > 7 V (V_{ZCD} > 2 V)
(85 V AC, short R12A during system operation at no-load)

Figure 31 Output OVP

11.17 V_{CC} short-to-GND protection



C1 (yellow) : VCC voltage (V_{VCC})
C2 (purple) : FB voltage (V_{FB})
C3 (blue) : Drain voltage (V_D)
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} short-to-GND: if $V_{CC} < V_{VCC\_SCP} \rightarrow I_{VCC} = I_{VCC\_Charge1}$
(Short V_{CC} pin to GND by multimeter and measure the current, $I_{VCC} \approx 280$ µA and input power is ≈ 47 mW at 85 V AC and full-load)

Figure 32 V_{CC} short-to-GND protection

12 References

[1] ICE5QRxxxxAx datasheet, Infineon Technologies AG

[2] AN-201609_PL83_026-Fifth-Generation QR Design Guide

[3] Calculation Tool Quasi-Resonant CoolSET™ Generation 5

Revision history

Major changes since the last revision

Page or reference	Description of change
--	First release

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Email: erratum@infineon.com

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