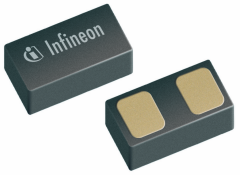
ESD101-B1-02 Series

Protection device

TVS (transient voltage suppressor)
Bi-directional, 5.5 V, 0.1 pF, 0201, 0402, RoHS and halogen free compliant

Features



- ESD/transient protection of high speed data lines according to:
  - IEC61000-4-2 (ESD): ±14 kV (air), ±12 kV (contact)
  - IEC61000-4-4 (EFT): ±1.5 kV/±30 A (5/50 ns)
  - IEC61000-4-5 (surge): ±2 A (8/20 µs)
- Bi-directional working voltage up to: V_{RWM} = ±5.5 V
- Extremely low capacitance C_L = 0.1 pF (typical) at f = 1 GHz
- Clamping voltage: V_{CL} = 30 V (typical) at I_{TLP} = 16 A with R_{DYN} = 1.5 Ω (typical)
- Very low reverse current: I_R < 0.1 nA
- Small form factor SMD sizes 0201 and 0402 low profile
- Bi-directional and symmetric I/V characteristics for optimized design/assembly

RoHS

Potential applications

Tailored for ESD protection of capacitance-susceptible application like:

- Super high speed interface
- RF antenna

For further application information please refer to application note AN327 ***[3]***.

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

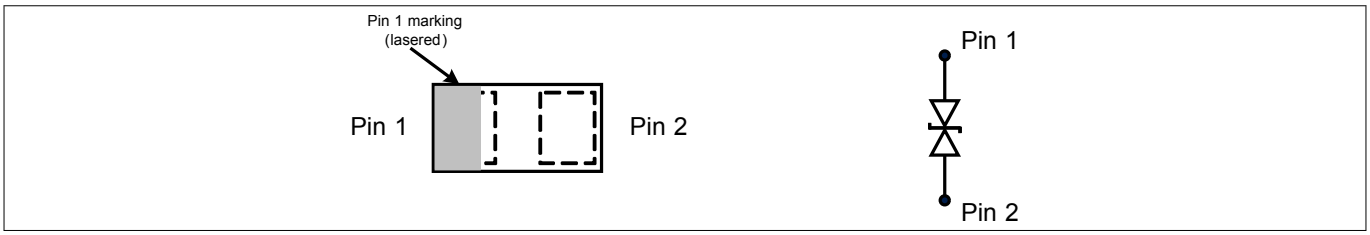


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD101-B1-02ELS	TSSLP-2-4	1 line, bi-directional	R
ESD101-B1-02EL	TSLP-2-20	1 line, bi-directional	R

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1 Maximum ratings

Note: T_A = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit	Note or test condition
ESD air discharge [1)]	V_{ESD}	±14	kV	–
ESD contact discharge [1)]		±12		
Peak pulse power	P_{PK}	30	W	–
Peak pulse current [2)]	I_{PP}	±2	A	–
Operating temperature	T_{OP}	-55 to 125	°C	–
Storage temperature	T_{stg}	-65 to 150	°C	–

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.***

1 V_{ESD} according to IEC61000-4-2
2 Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5

2 Electrical characteristics

Note: *T_A = 25 °C, unless otherwise specified.*
Device is electrically symmetrical.

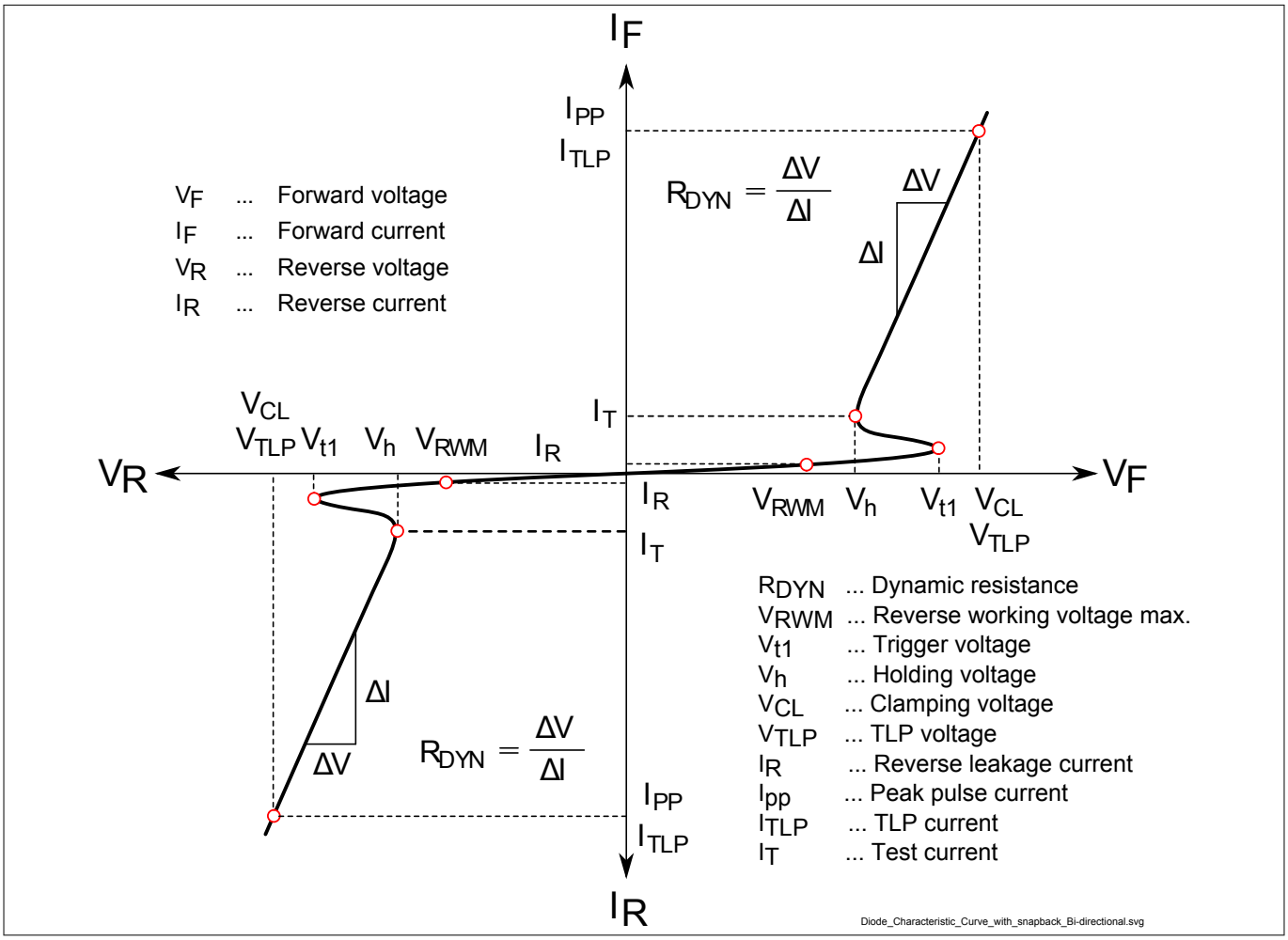

Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Reverse current	I_{RWM}	-5.5	–	5.5	V	
Trigger voltage [1)]	V_{t1}	6.1	–	–		
Holding voltage	V_h	6.1	7.3	8.2		I_T = 1 mA
		6.1	7.0	7.9		I_T = 10 mA
Reverse leakage current	I_R	–	<0.1	20	nA	V_R = 5.5 V

Table 4 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	–	0.2	pF	V_R = 0 V, f = 1 MHz
		–	0.1	–		V_R = 0 V, f = 1 GHz
Serie inductance	L_S	– –	0.2 0.4	– –	nH	ESD101-B1-02ELS ESD101-B1-02EL

Table 5 ESD and surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage [2)]	V_{CL}	–	18	–	V	I_{TLP} = 8 A, t_p = 100 ns
		–	30	–		I_{TLP} = 16 A, t_p = 100 ns
Clamping voltage[3)]		–	9	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	13	–		I_{PP} = 2 A, t_p = 8/20 µs
Dynamic resistance [2)]	R_{DYN}	– –	1.5	–	Ω	t_p = 100 ns

1 Verified by design
2 Please refer to application note AN210 [1], TLP parameters: Z_0 = 50 Ω , t_p = 100 ns, t_r = 300 ps
3 Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

3 Typical characteristic diagrams

Note: $T_A = 25\ °C$, *unless otherwise specified*

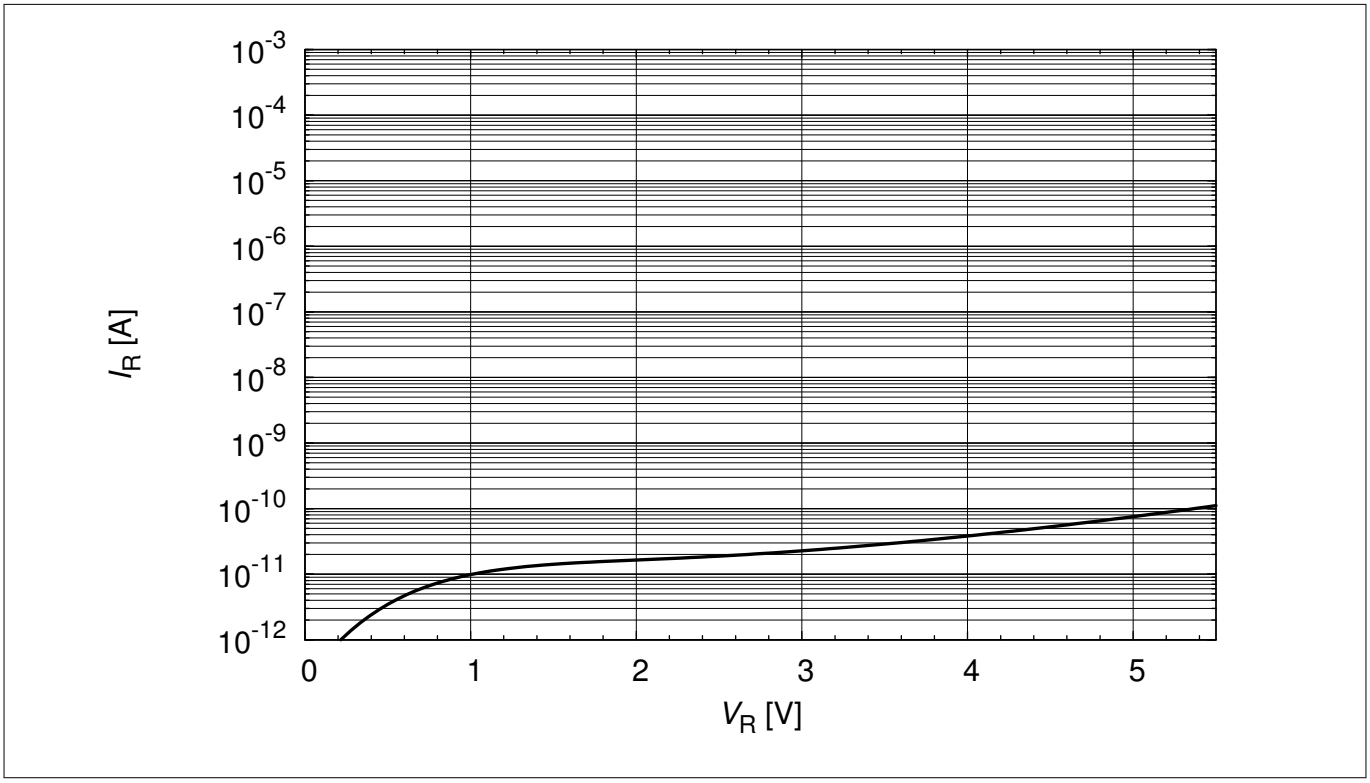

Figure 3 Reverse leakage current: $I_R = f(V_R)$

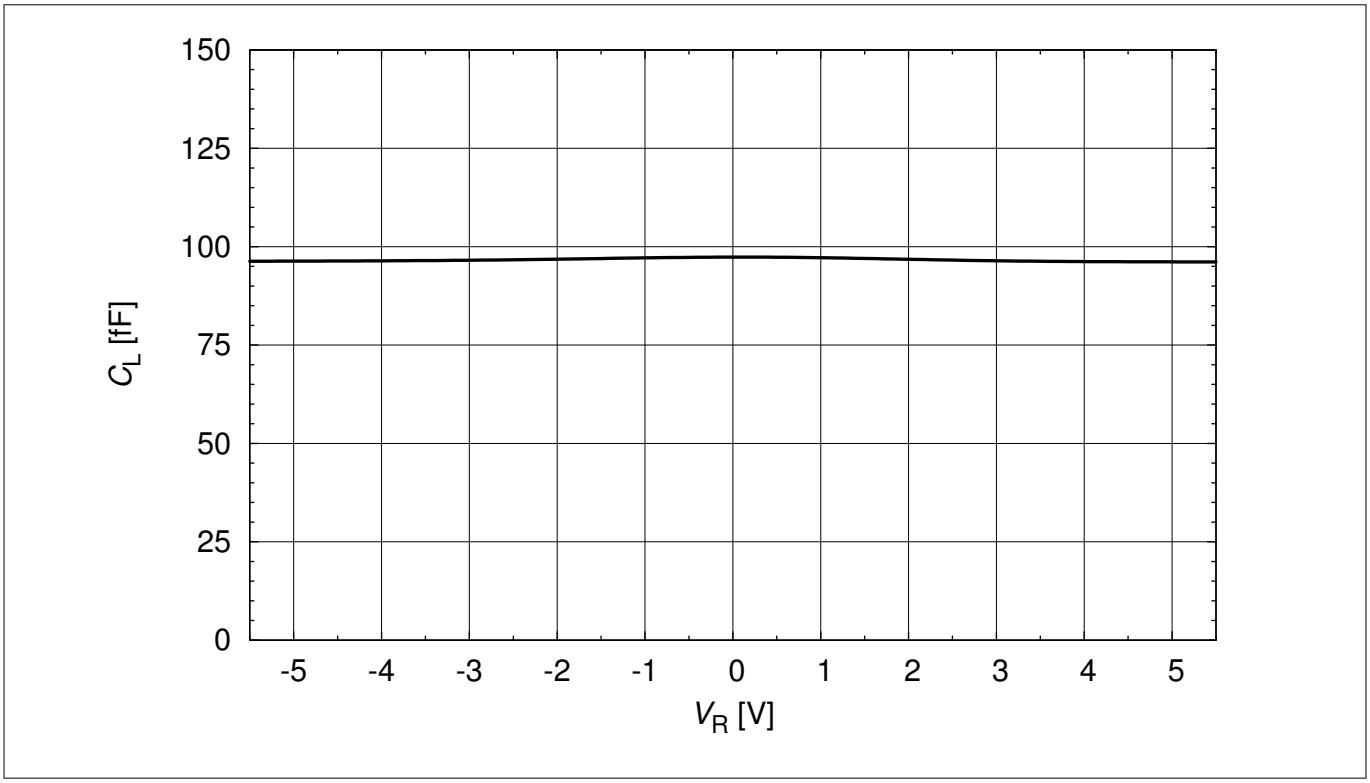

Figure 4 Line capacitance: $C_L = f(V_R)$, $f = 1$ GHz

Typical characteristic diagrams

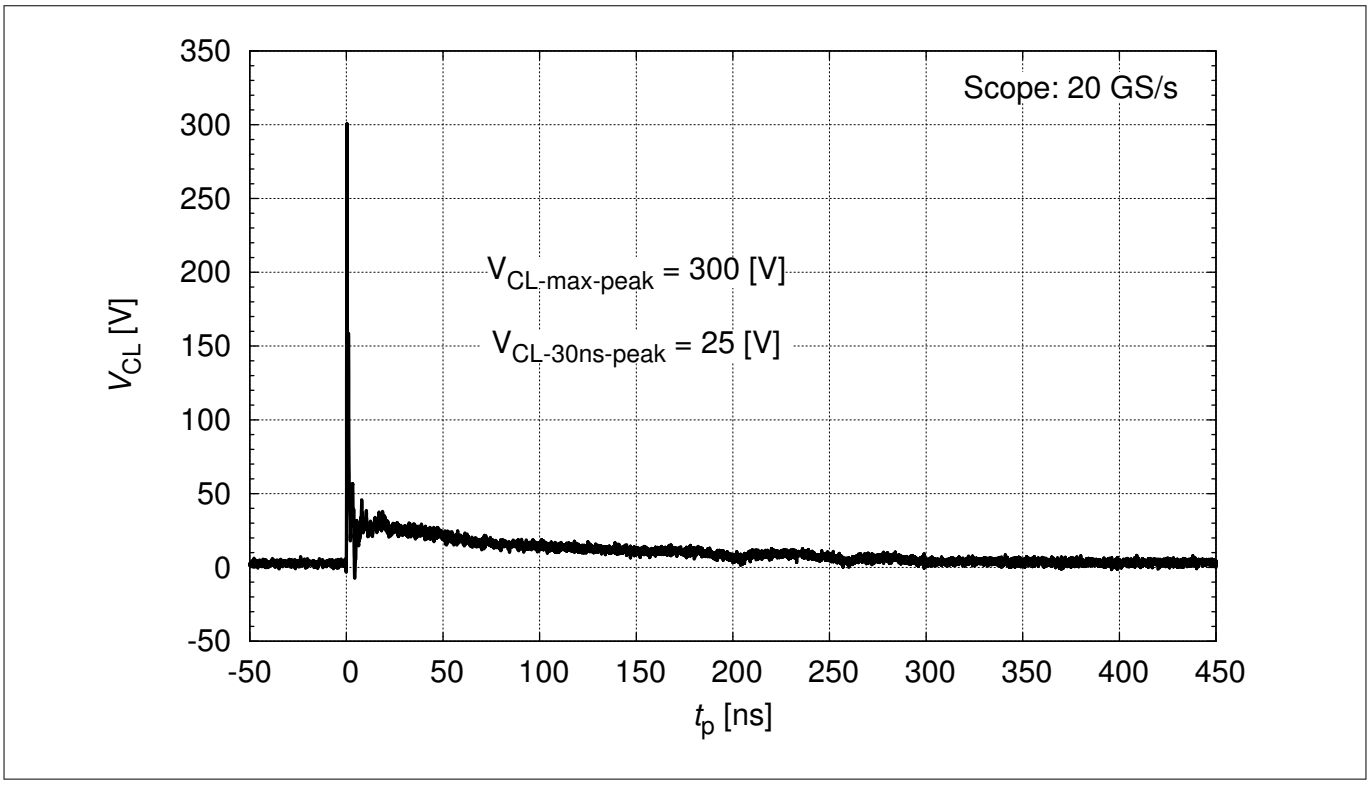

Figure 5 Clamping voltage (ESD): V_{CL}= *f(t)*, 8 kV positive pulse from pin 1 to pin 2

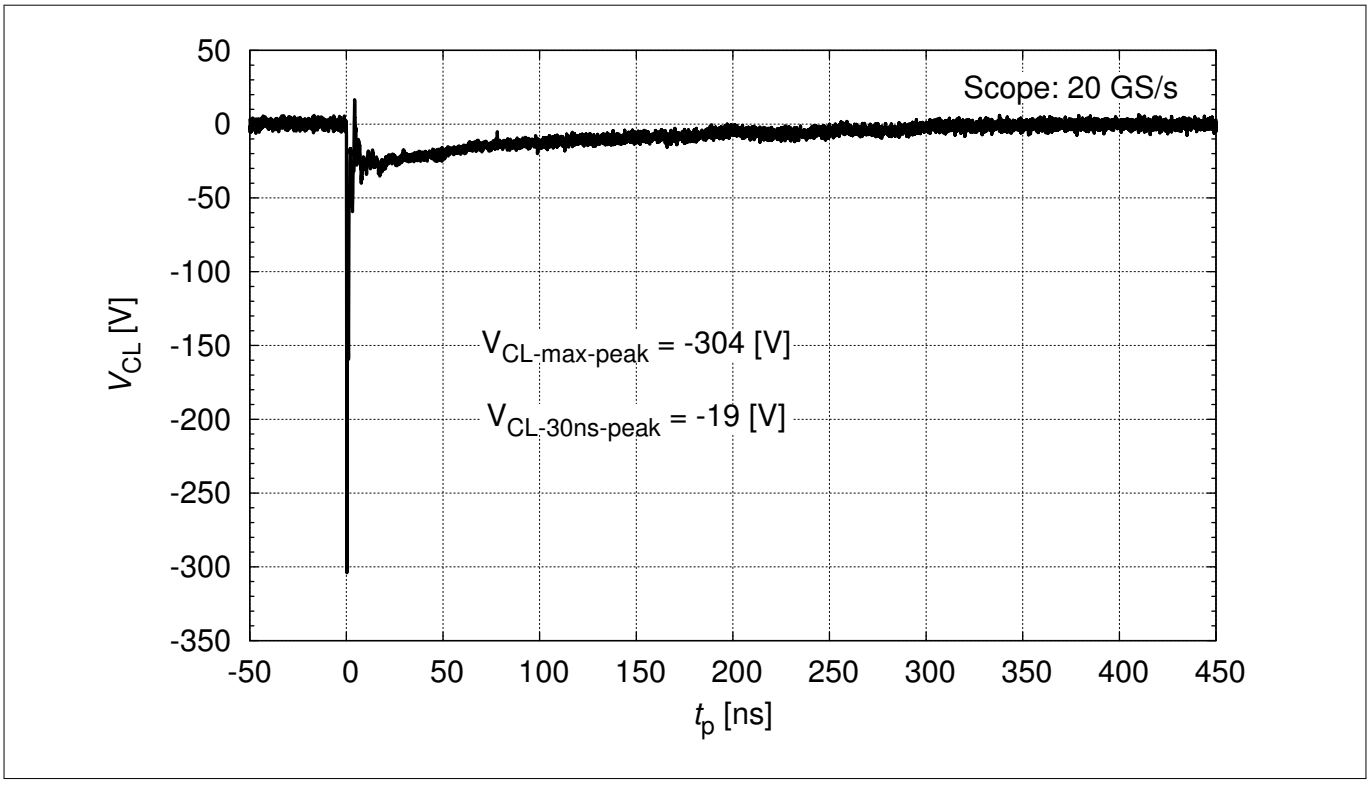

Figure 6 Clamping voltage (ESD): V_{CL} = *f(t)*, 8 kV negative pulse from pin 1 to pin 2

Typical characteristic diagrams

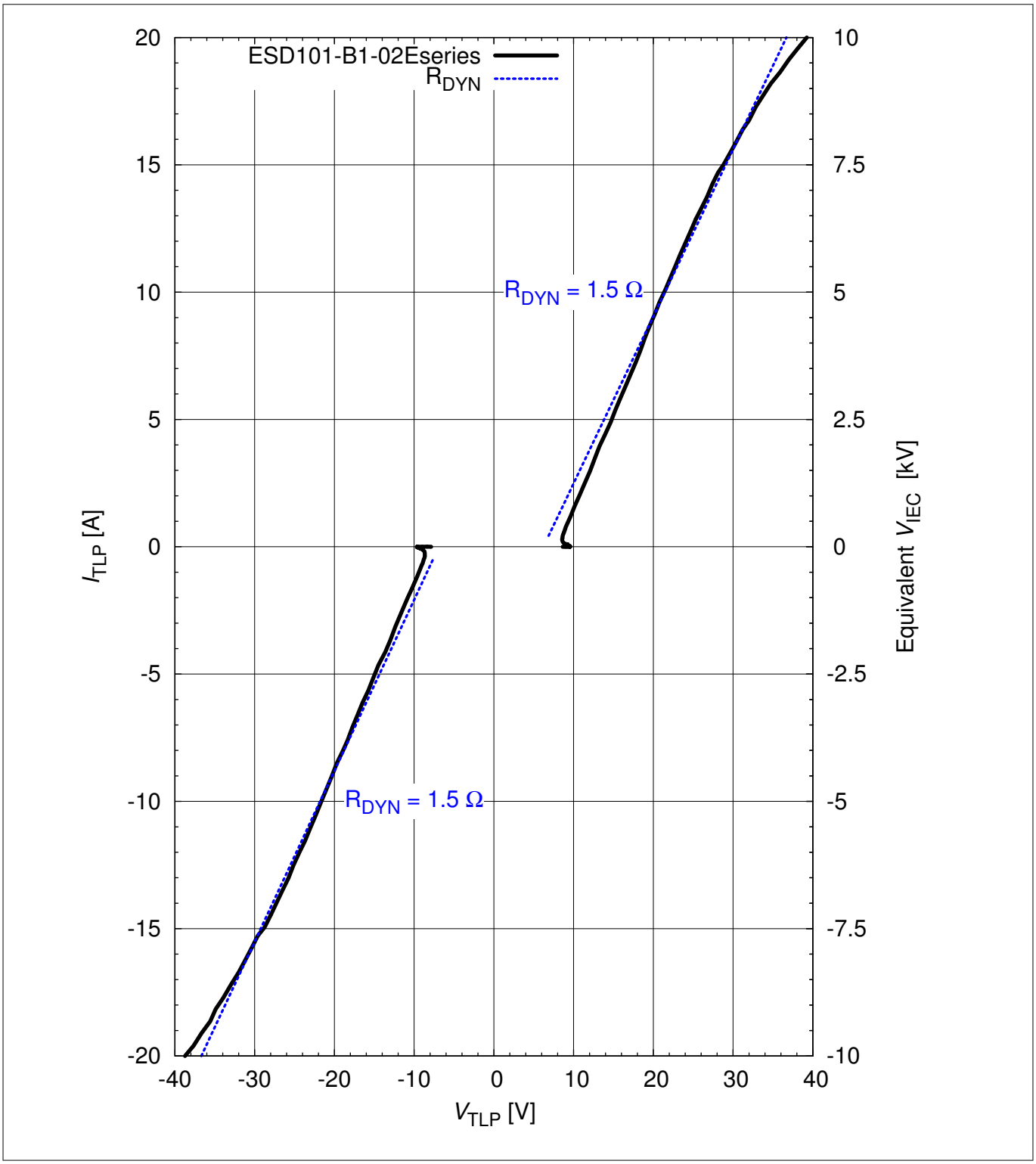

Figure 7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

Typical characteristic diagrams

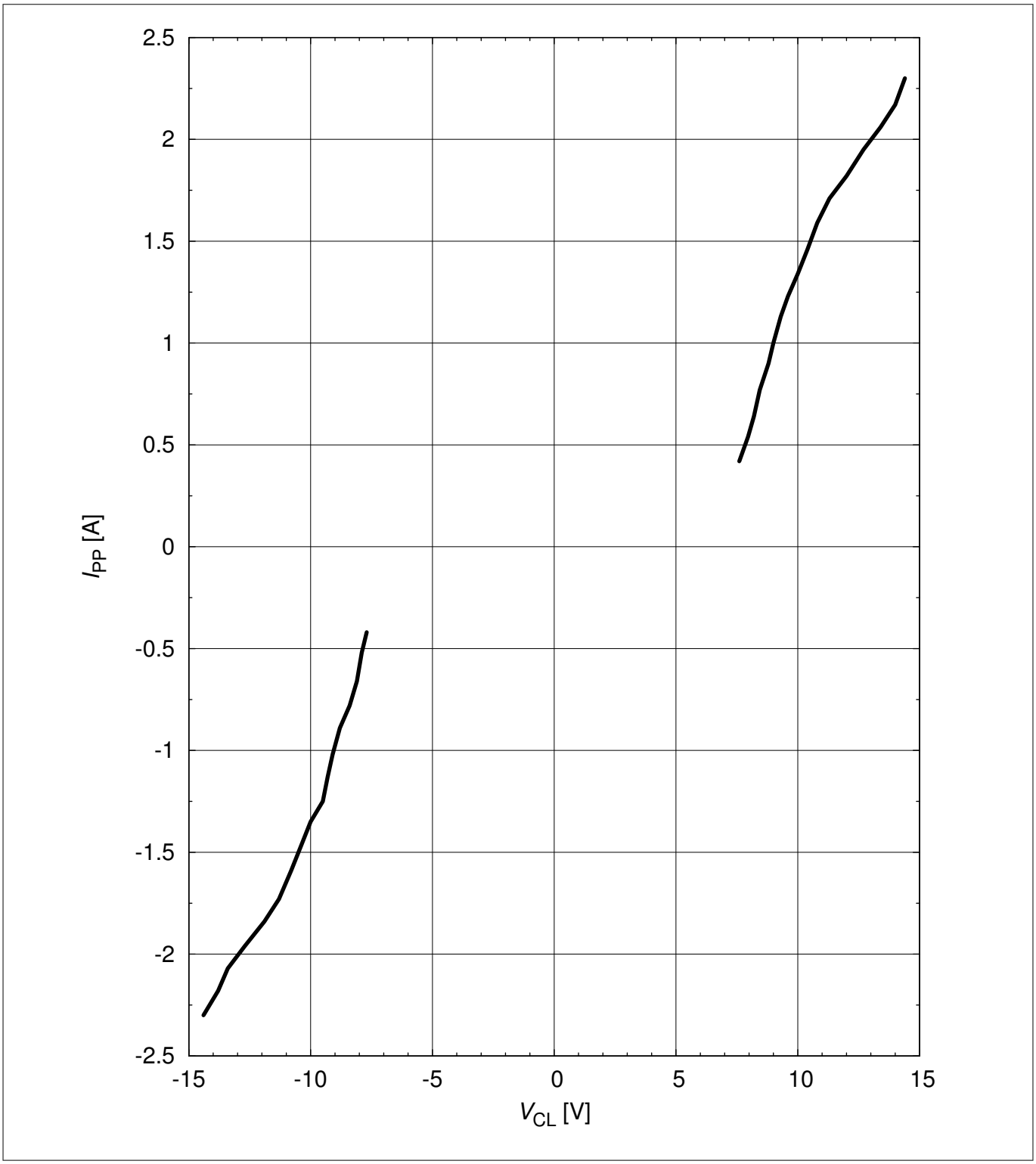

Figure 8 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1], pin 1 to pin 2

Typical characteristic diagrams

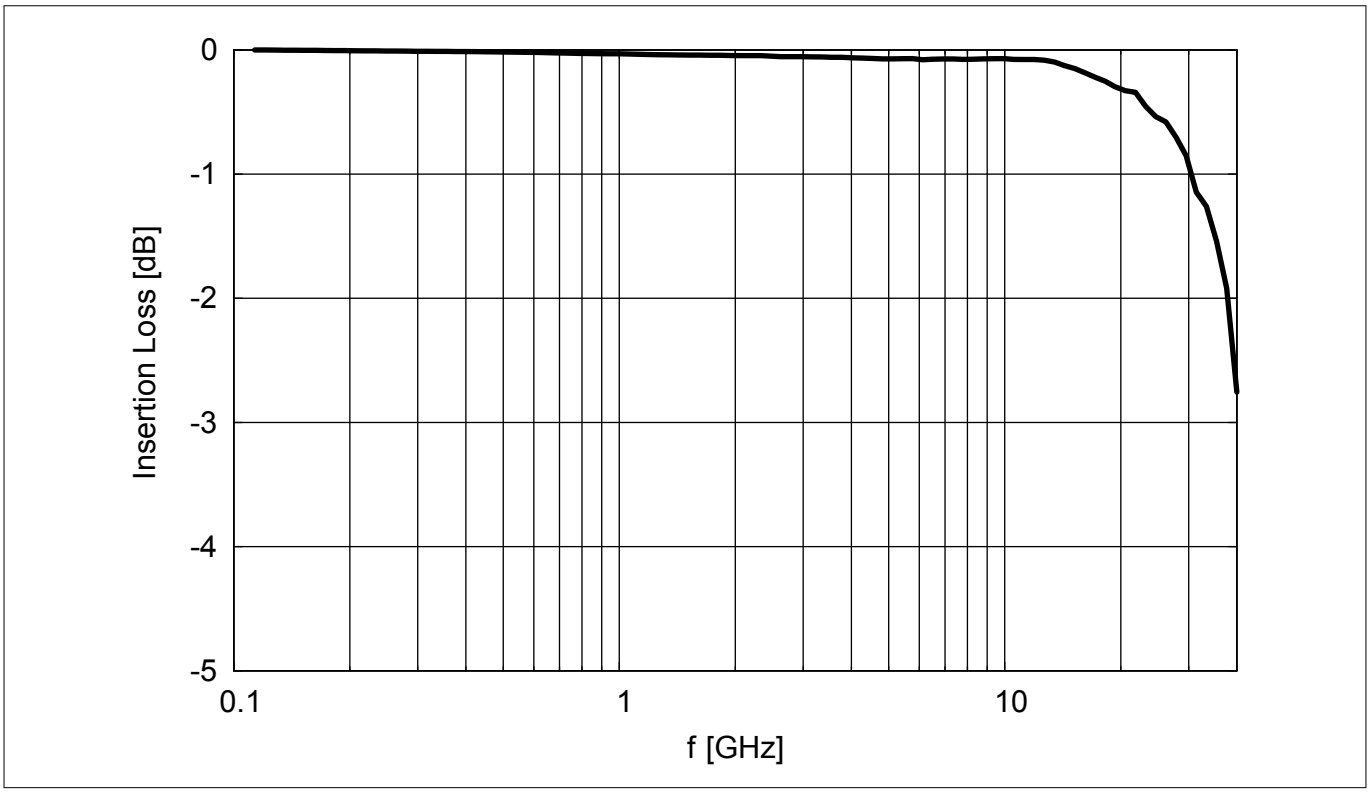

Figure 9 Insertion loss vs. frequency in a 50 Ω system

4 Package information

4.1 TSSLP-2-4

Note: *Dimension in mm*

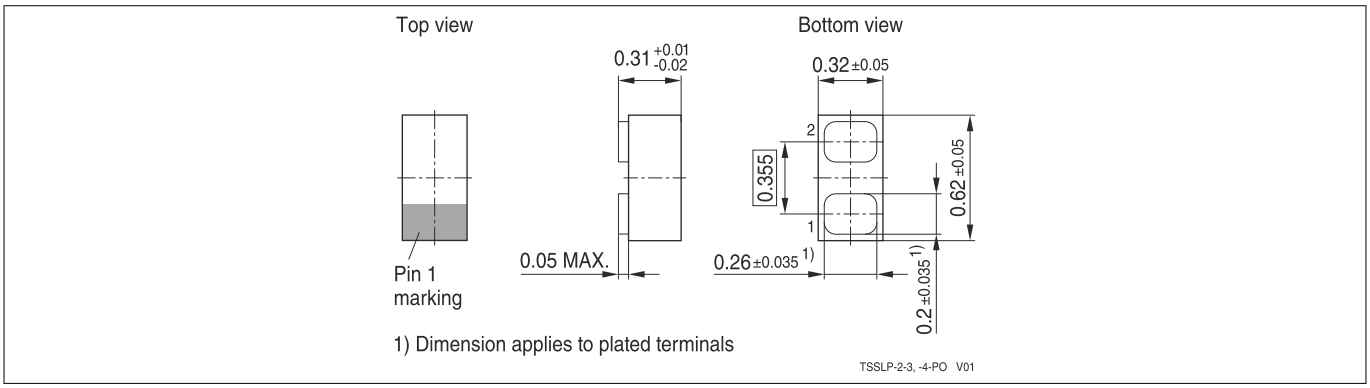

Figure 10 TSSLP-2-4 package outline

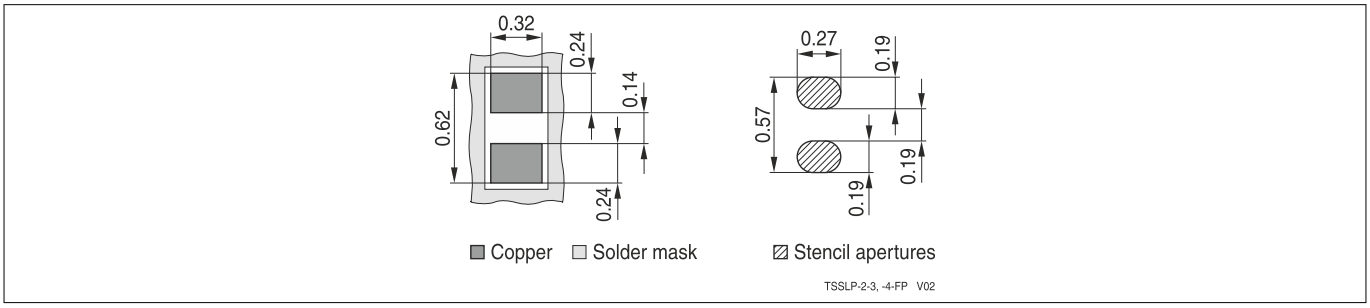

Figure 11 TSSLP-2-4 footprint

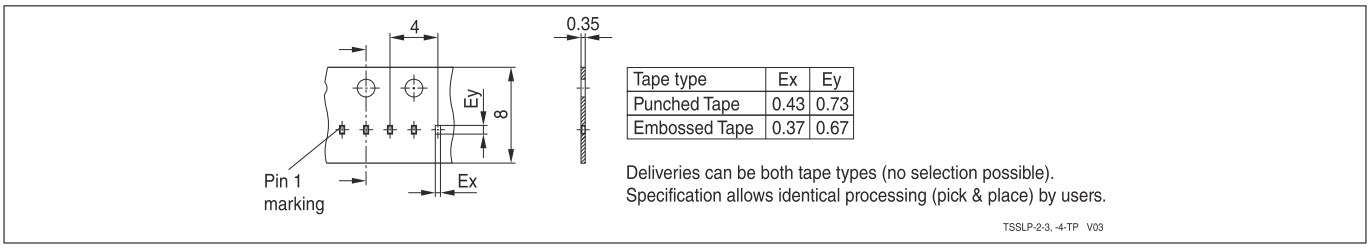

Figure 12 TSSLP-2-4 packing

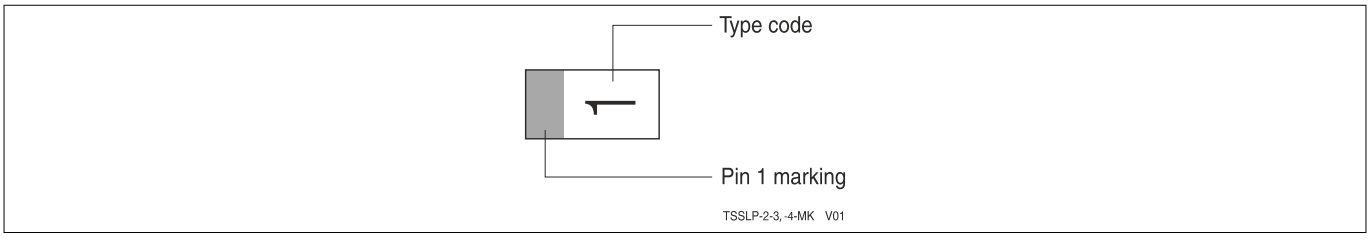

Figure 13 TSSLP-2-4 marking example

4.2 TSLP-2-20

Note: *Dimension in mm*

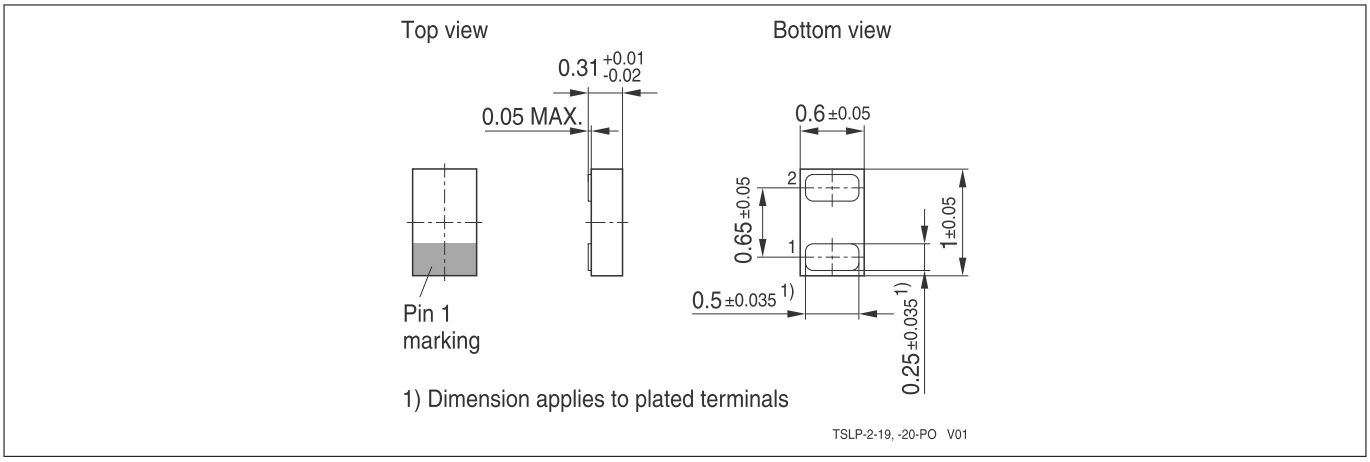

Figure 14 TSLP-2-20 package outline

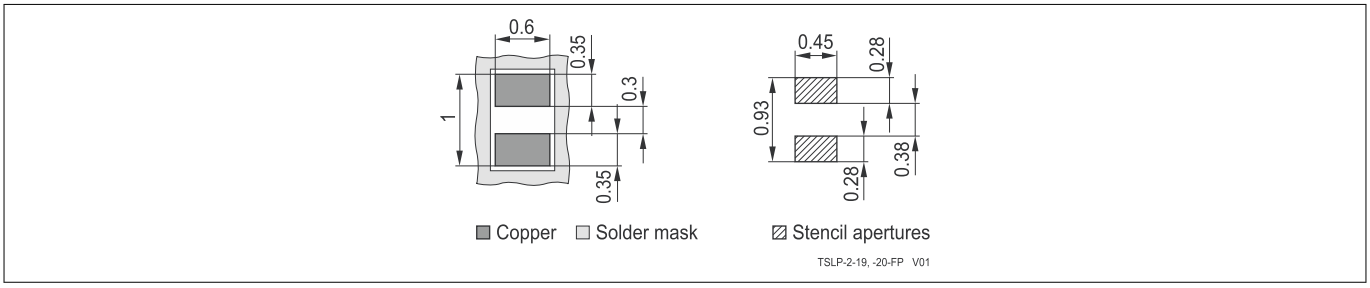

Figure 15 TSLP-2-20 footprint

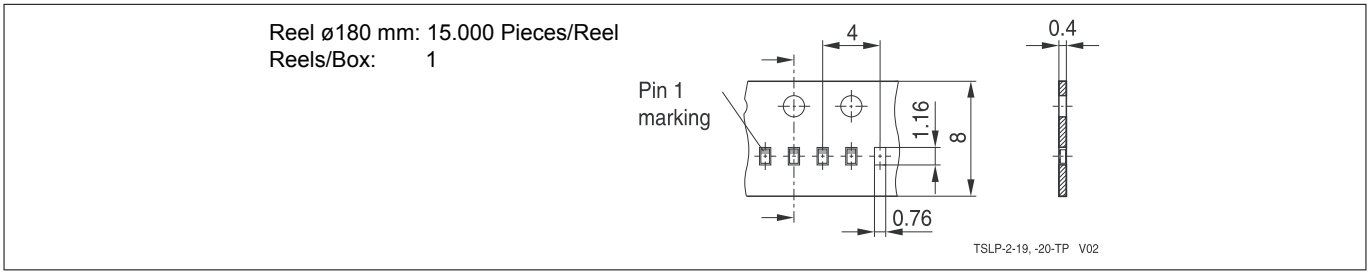

Figure 16 TSLP-2-20 packing

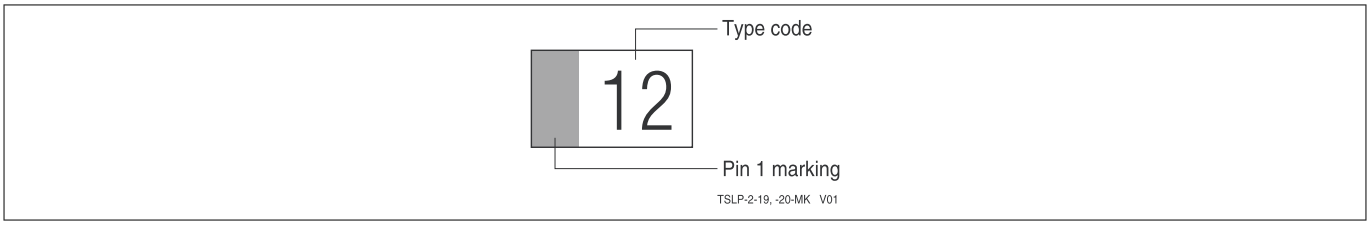

Figure 17 TSLP-2-20 marking example

5 References

[1] Infineon AG - **Application Note AN210**: Effective ESD protection design at system level using VF-TLP characterization methodology

[2] Infineon AG - ***Recommendations for PCB Assembly of Infineon TSLP/TSSLP/TSNP Packages***

[3] Infineon AG - **Application Note AN327**: ESD101-B1/ESD103-B1, Bi-directional Ultra Low Capacitance Transient Voltage Suppression Diodes for High Power RD Applications

Revision history

Revision history: Rev. 1.3. 2015-07-13	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.4, 2017-10-27	
All	Datasheet layout changed
	Table 3 updated

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Edition 2017-10-26

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-bvo1508924672557

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