

ESD119-B1-W01005

Protection device

TVS (transient voltage suppressor)

Bi-directional, 5.5 V, 0.2 pF, 01005, RoHS and halogen free compliant

Feature list

- ESD/transient protection of high speed data lines according to:
 - IEC61000-4-2 (ESD): ± 25 kV (air/contact discharge)
 - IEC61000-4-4 (EFT): ± 2.5 kV/ ± 50 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 2.5 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 5.5$ V
- Line capacitance: $C_L = 0.2$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 20$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.8 \Omega$ (typical)
- Very low reverse current: $I_R < 1$ nA (typical)
- Small form factor SMD size 01005, low profile (0.43 mm x 0.23 mm x 0.15 mm) [3]
- Bi-directional, symmetric I/V characteristic for optimized design and assembly, recommendations for PCB assembly see [2]



Potential applications

- USB 2.0/3.0, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI link, MDDI, MIPI, SWP/NFC

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

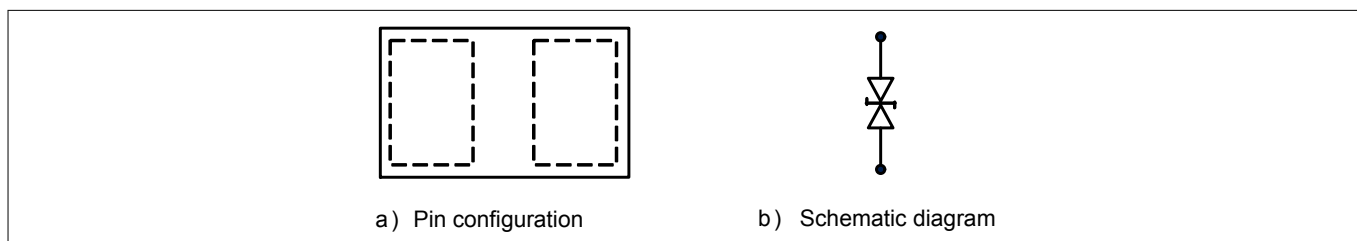


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD119-B1-W01005	WLL-2-2	1 line, bi-directional	C ¹⁾

¹ The device has no marking on the device backside. The marking code is on pad side.

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Maximum ratings

1 Maximum ratings

Note: $T_A = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	V
ESD (air/contact) discharge ¹⁾	V_{ESD}	±25	kV
Peak pulse power ²⁾	P_{PK}	35	W
Peak pulse current ²⁾	I_{PP}	±2.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

¹ V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)

² Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Electrical characteristics

2 Electrical characteristics

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified. Device is electrically symmetrical.

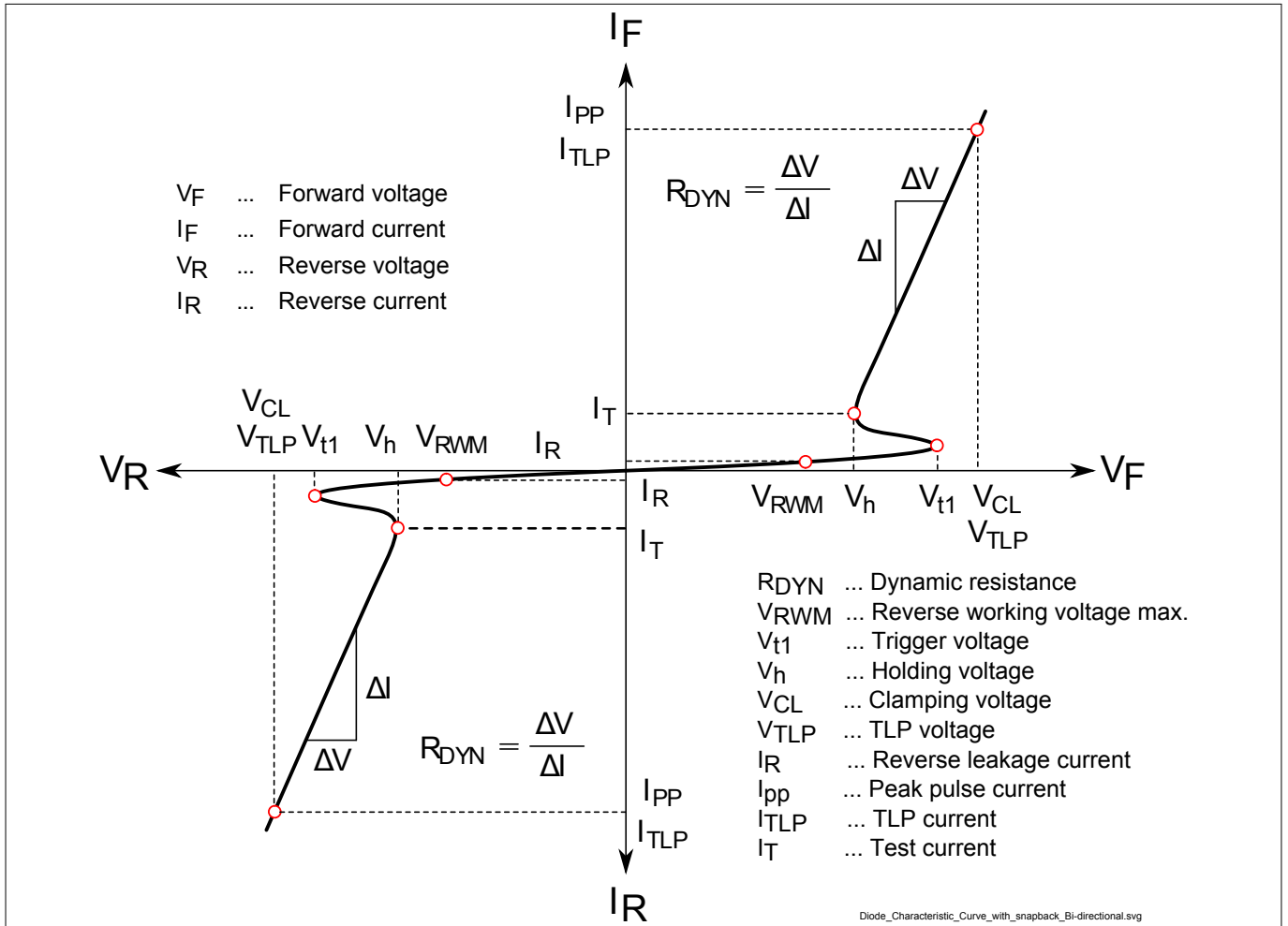


Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Trigger voltage ¹⁾²⁾	V_{t1}	6.1	9	10.5	V	–
Holding voltage ³⁾	V_h	6.1	7.5	9.5	V	$I_T = 10 \text{ mA}$
Reverse current	I_R	–	<1	20	nA	$V_R = 5.5 \text{ V}$

Table 4 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.2	0.3	pF	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$
		–	0.15	–		$V_R = 0 \text{ V}, f = 1 \text{ GHz}$

Table 5 ESD and Surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage ⁴⁾	V_{CL}	–	20	23	V	$I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$
		–	31	34		$I_{TLP} = 30 \text{ A}, t_p = 100 \text{ ns}$
Clamping voltage ⁵⁾		–	8	11		$I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{s}$
		–	11	14		$I_{PP} = 2.5 \text{ A}, t_p = 8/20 \mu\text{s}$
Dynamic resistance ⁴⁾	R_{DYN}	–	0.8	–	Ω	$t_p = 100 \text{ ns}$

1 Verified by design

2 Voltage forced

3 Current forced

4 Please refer to application note AN210 [1], TLP parameters: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$

5 Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

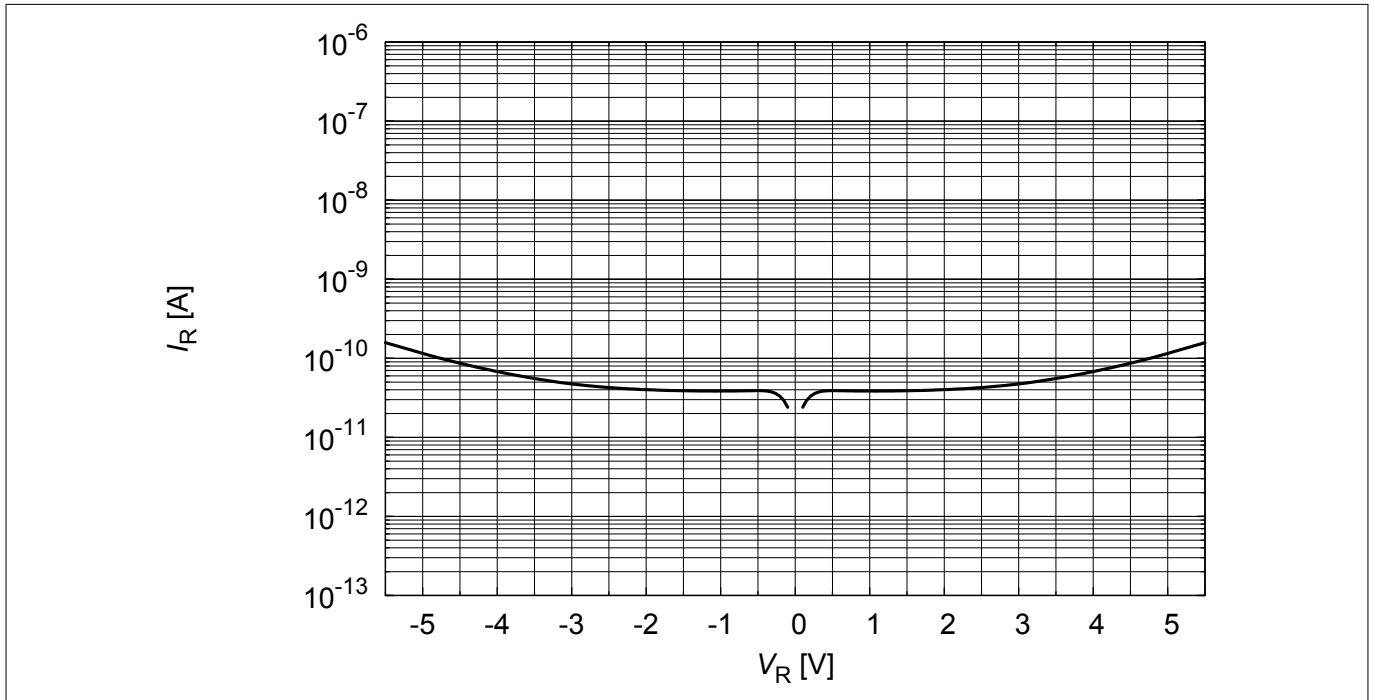


Figure 3 Reverse leakage current: $I_R = f(V_R)$

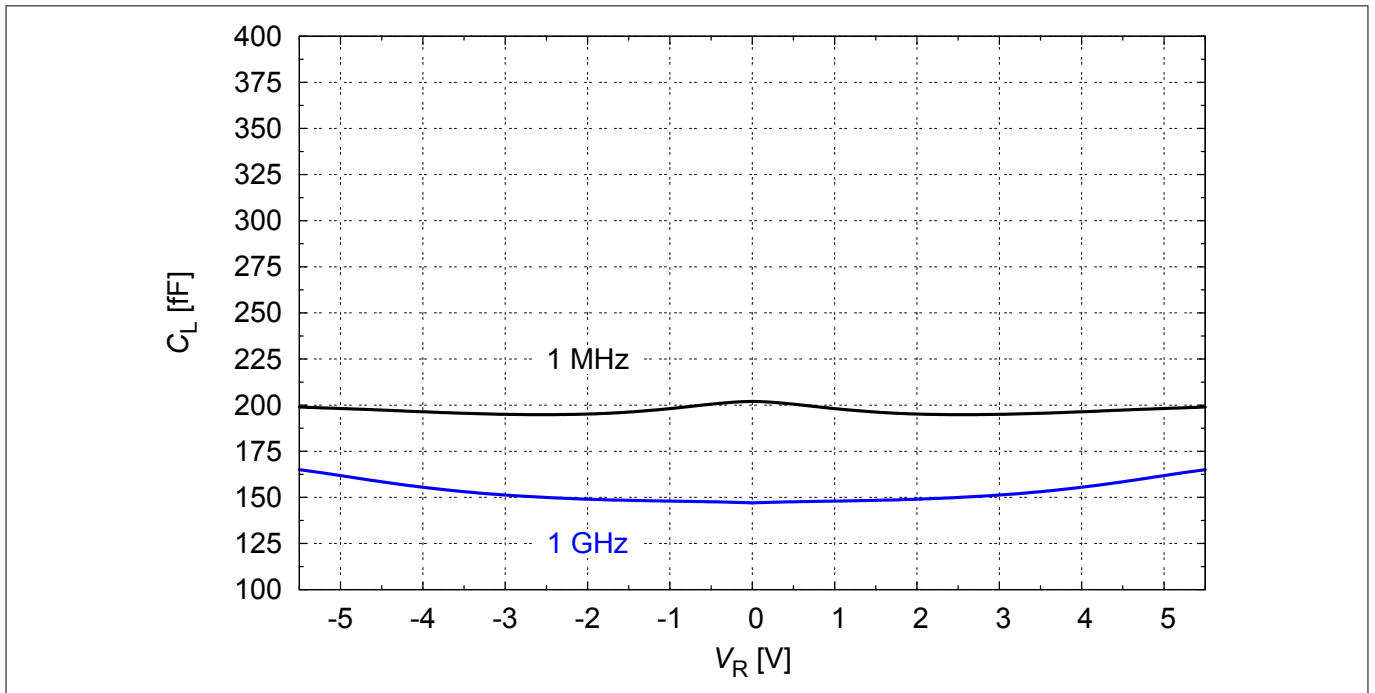


Figure 4 Line capacitance: $C_L = f(V_R)$, $f = 1\text{ MHz}, 1\text{ GHz}$

Typical characteristic diagrams

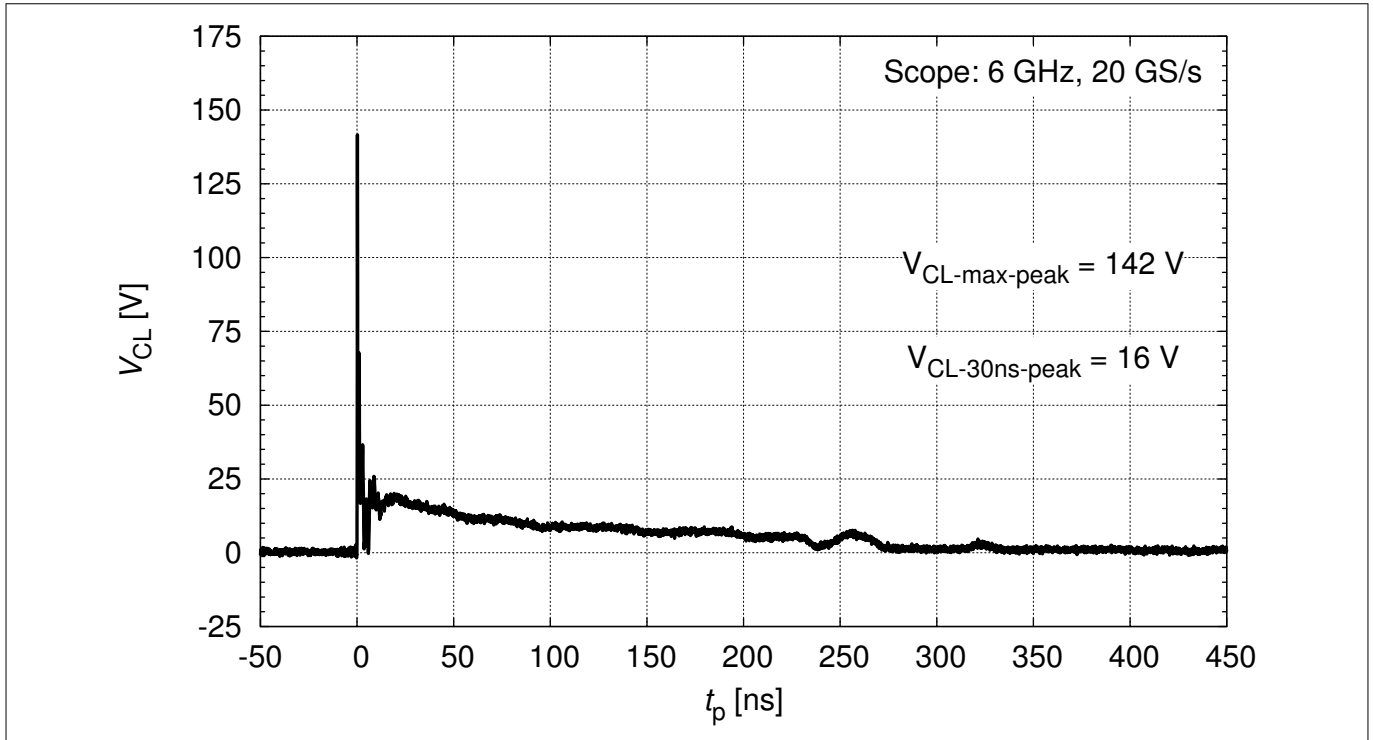


Figure 5 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse (according to IEC61000-4-2)

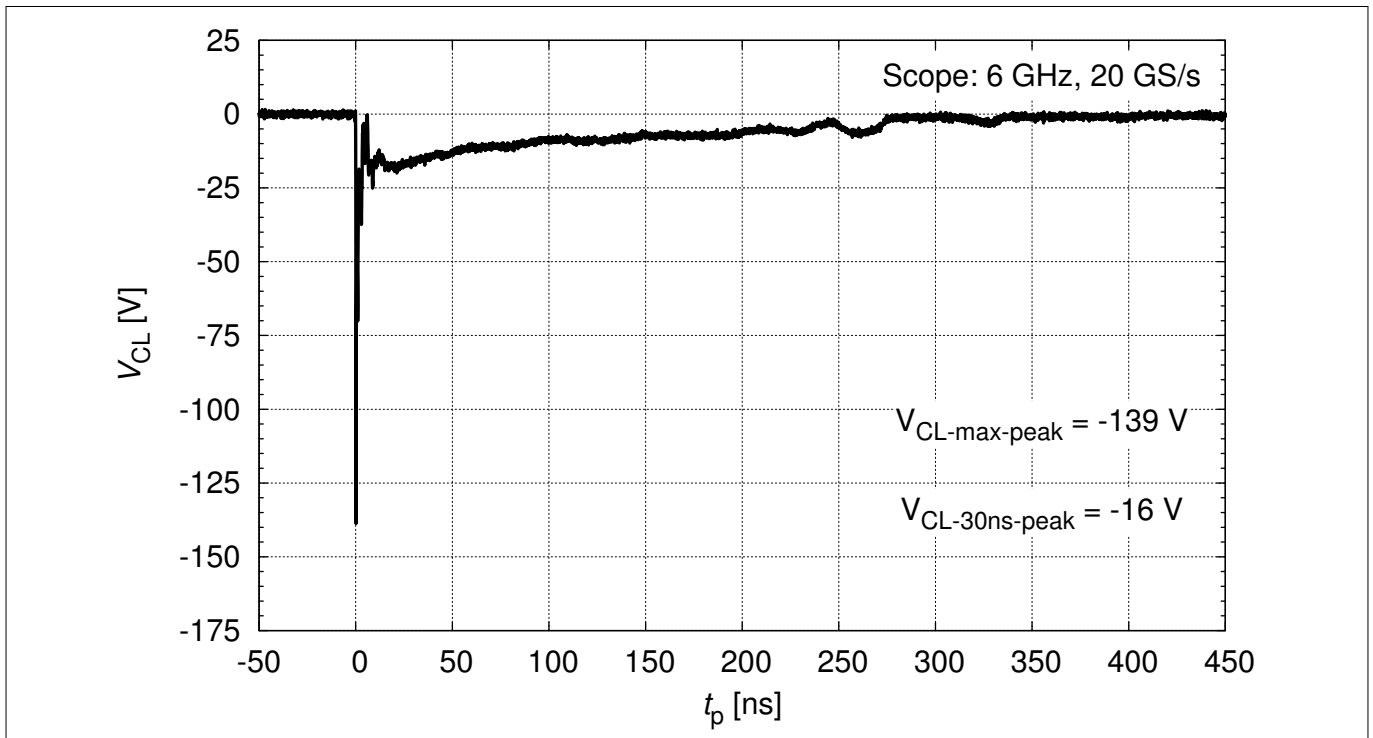


Figure 6 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse (according to IEC61000-4-2)

Typical characteristic diagrams

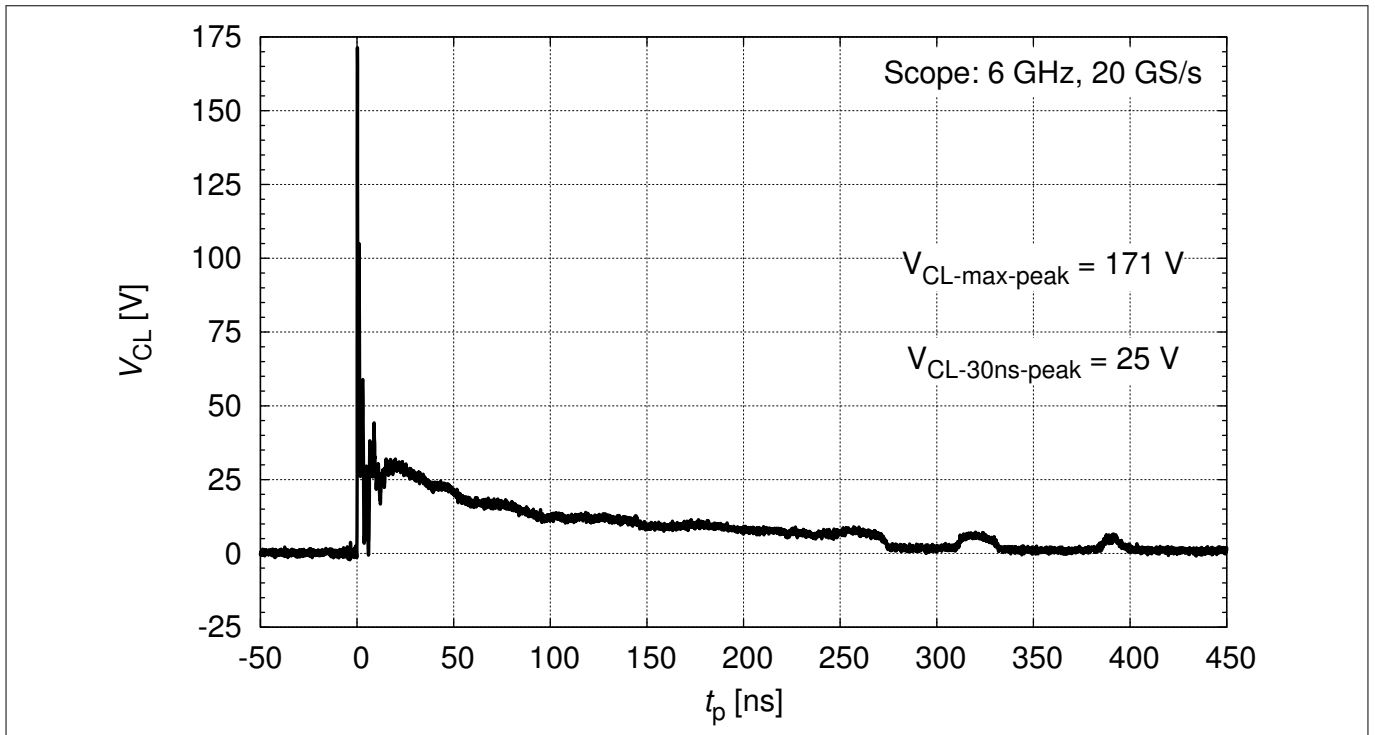


Figure 7 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positive pulse (according to IEC61000-4-2)

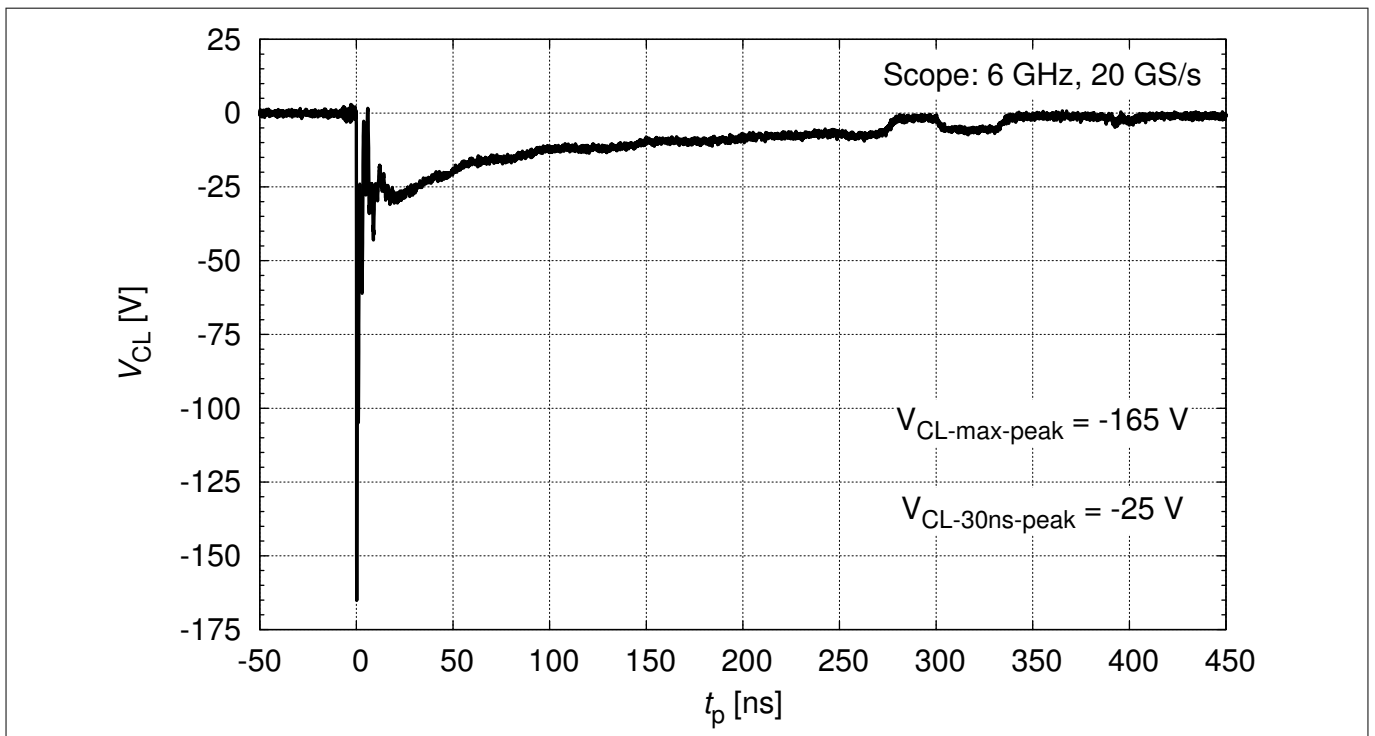


Figure 8 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negative pulse (according to IEC61000-4-2)

Typical characteristic diagrams

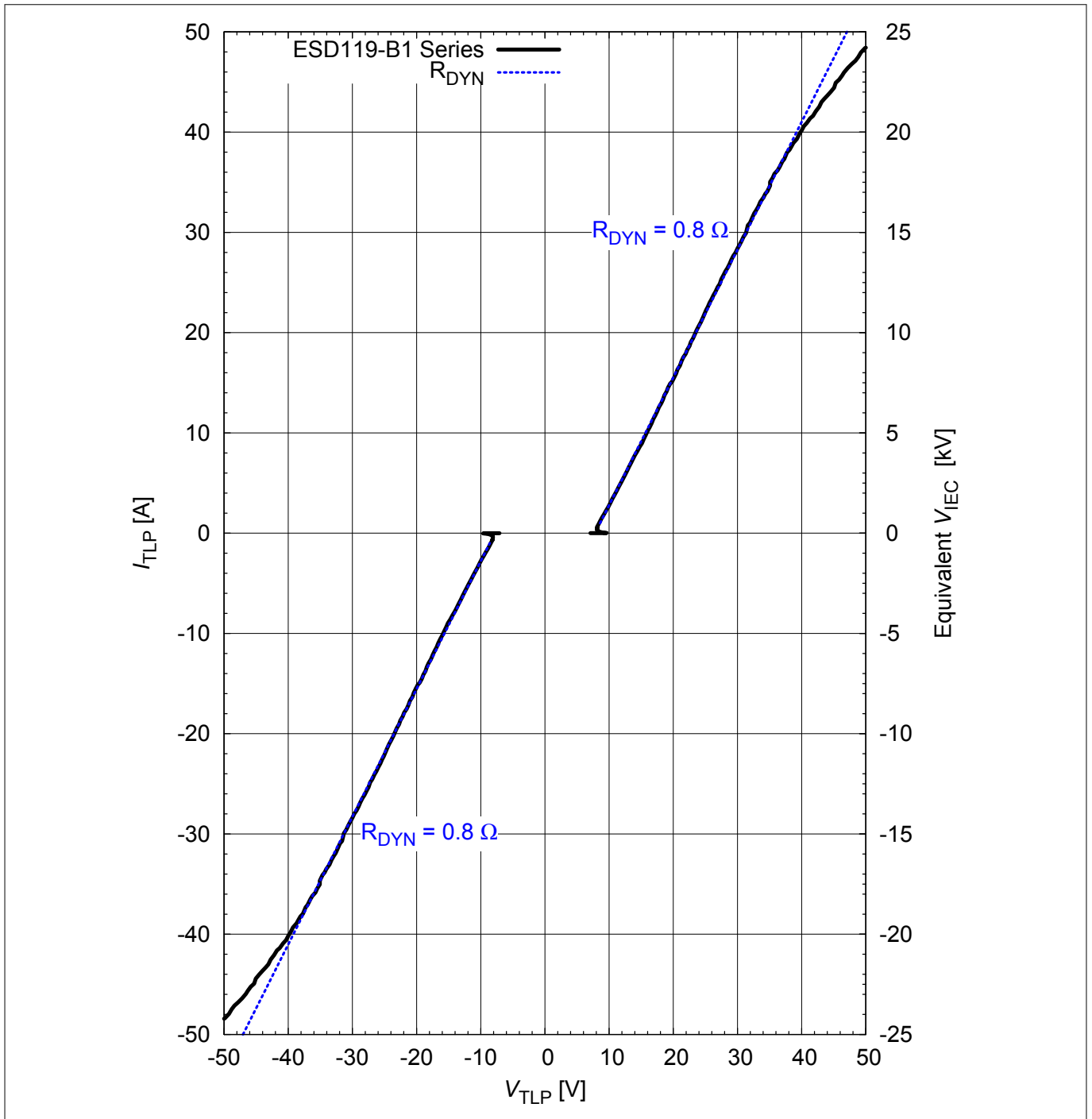


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

Typical characteristic diagrams

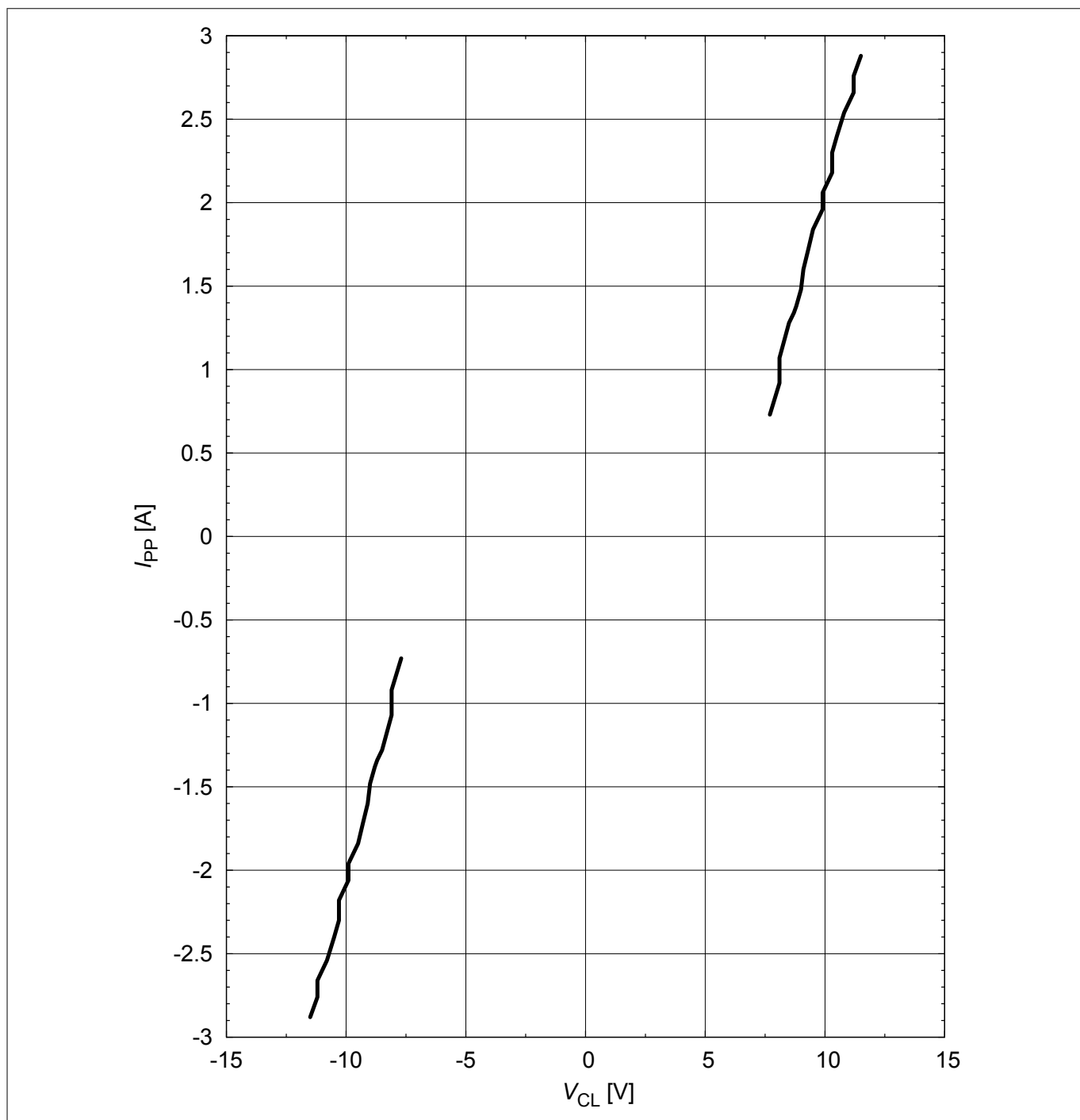


Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ (according to IEC61000-4-5) [1]

Typical characteristic diagrams

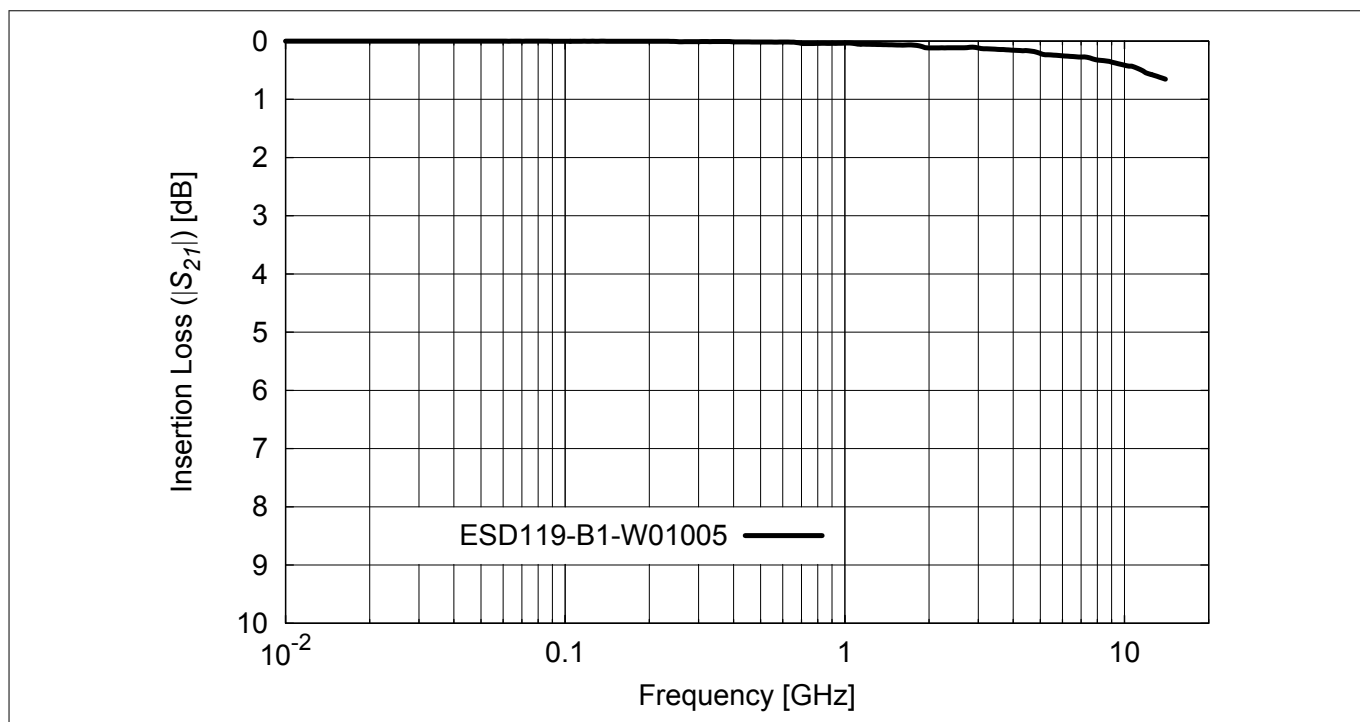


Figure 11 Insertion loss vs. frequency in a 50 Ω system

Package information

4 Package information

4.1 WLL-2-2 package

Note: Dimensions in mm.

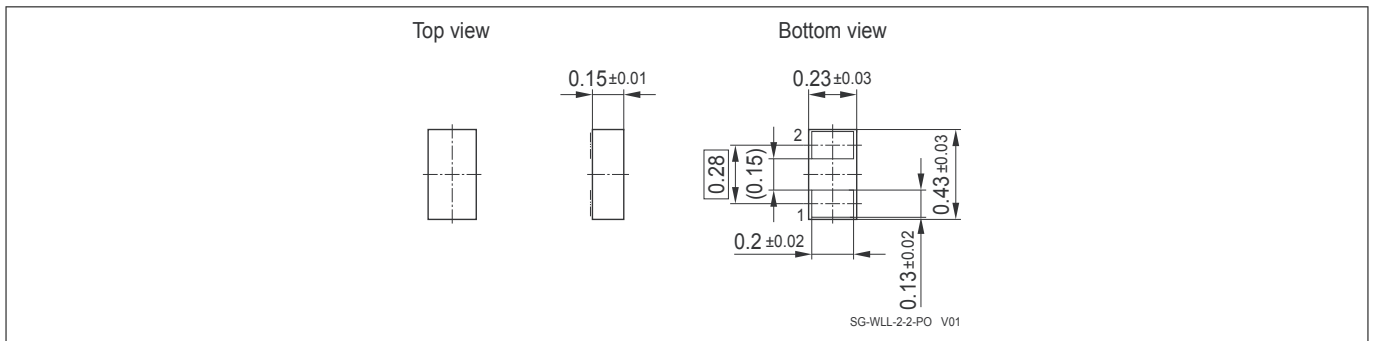


Figure 12 WLL-2-2 package outline

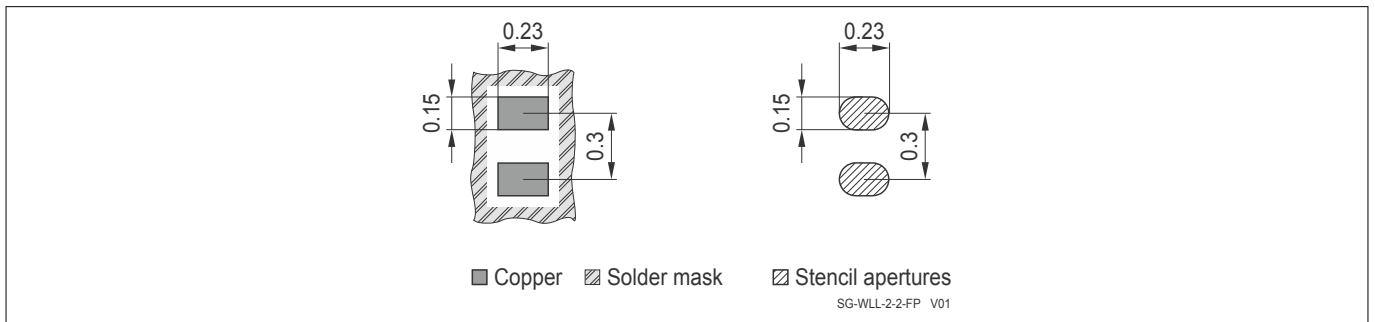


Figure 13 WLL-2-2 footprint

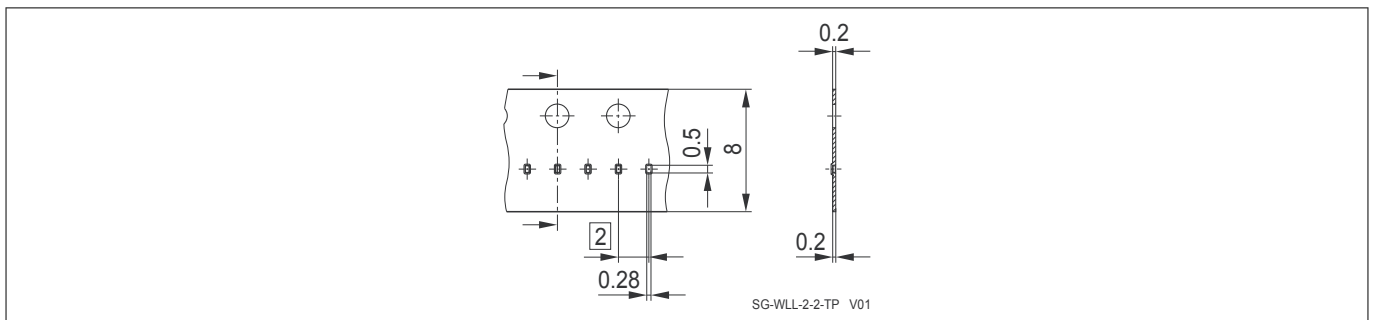


Figure 14 WLL-2-2 packing

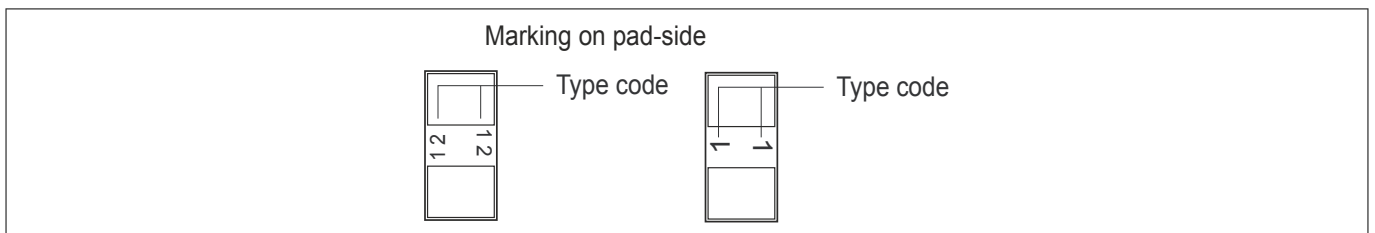


Figure 15 WLL-2-2 marking example (marking code see [Device information](#))

References

5 References

- [1] Infineon AG - **Application note AN210**: Effective ESD protection design at system level using VF-TLP characterization methodology
- [2] Infineon AG - **Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages**
http://www.infineon.com/Packageinformation_WLL
- [3] Infineon AG - **Application note AN392**: TVS diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Rev 1.3, 2017-10-17

Page or Item	Subjects (major changes since previous revision)
Revision 1.4, 2018-03-21	
Chapter 2	Max value of electrical parameter V_{t1} added
All	Minor editorial changes

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