

# Protection Device

TVS (Transient Voltage Suppressor)

## ESD205-B1 Series

Bi-directional, 5.5 V, 5 pF, 0201, 0402, RoHS and Halogen Free compliant

ESD205-B1-02ELS  
ESD205-B1-02EL

## Data Sheet

Revision 1.4, 2014-05-14  
Final

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# 1 Product Overview

## 1.1 Features

- ESD / transient protection of signal lines in low voltage applications according to:
  - IEC61000-4-2 (ESD):  $\pm 20$  kV (air / contact)
  - IEC61000-4-4 (EFT):  $\pm 2.5$  kV /  $\pm 50$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 2.5$  A (8/20  $\mu$ s)
- Bi-directional, working voltage up to  $V_{RWM} = \pm 5.5$  V
- Low capacitance:  $C_L = 5$  pF (typical)
- Low clamping voltage:  $V_{CL} = +10 / -12$  V (typical) at  $I_{TLP} = 16$  A
- Very low reverse current:  $I_R < 1$  nA (typical)
- Pb-free (RoHS compliant) and halogen free package



## 1.2 Application Examples

- Keypad, touchpad, buttons, convenience keys
- LCD displays, Camera, audio lines, mobile communication, Consumer products (E-Book, MP3, DVD, DSC...)
- Notebooks tablets and desktop computers and their peripherals

## 1.3 Product Description



Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD205-B1-02ELS	TSSLP-2-3	1 line, bi-directional	
ESD205-B1-02EL	TSLP-2-19	1 line, bi-directional	

## 2 Maximum Ratings

**Table 2-1 Maximum Ratings at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

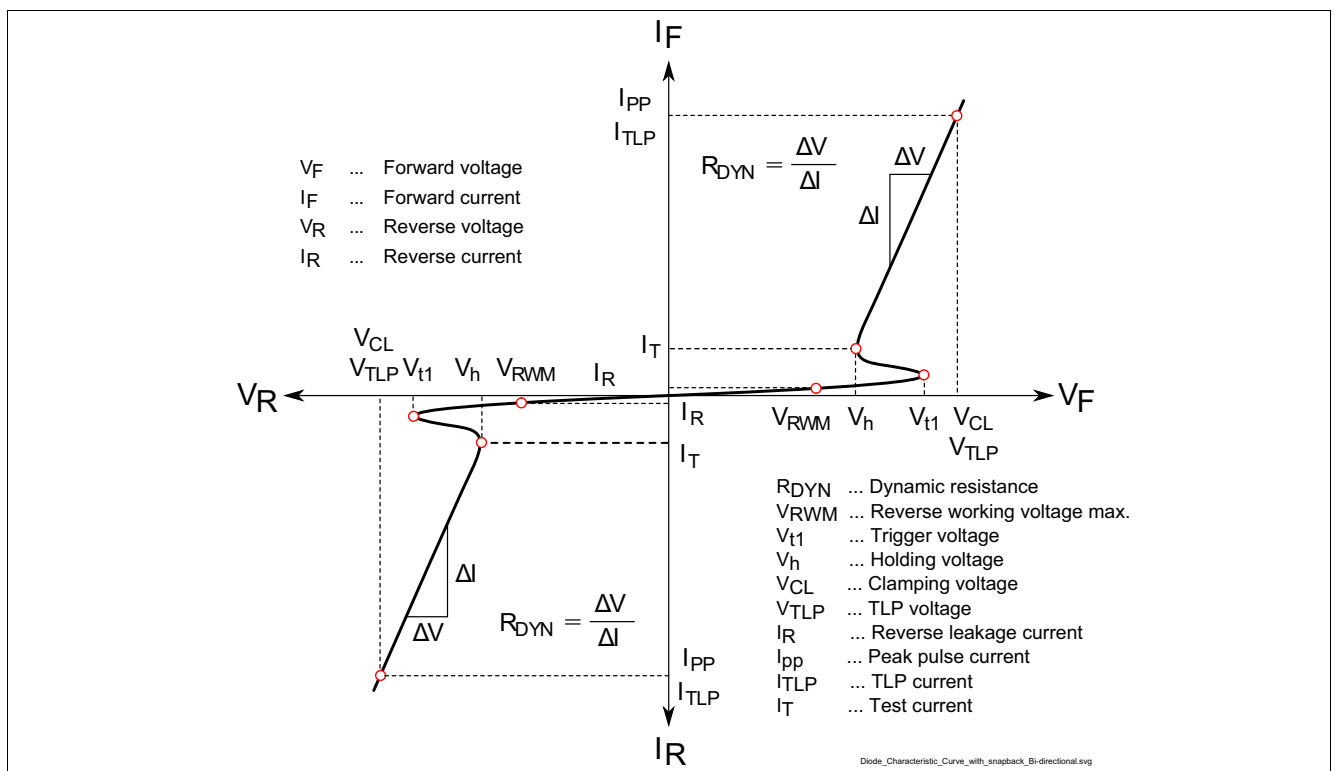
Parameter	Symbol	Values	Unit
ESD air discharge <sup>1)</sup>	$V_{ESD}$	$\pm 20$	kV
ESD contact discharge <sup>1)</sup>		$\pm 20$	
Peak pulse power <sup>2)</sup>	$P_{PK}$	30	W
Peak pulse current <sup>2)</sup>	$I_{PP}$	$\pm 2.5$	A
Operating temperature range	$T_{OP}$	-55 to 125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$

1)  $V_{ESD}$  according to IEC61000-4-2

2) Non-repetitive current pulse 8/20 $\mu\text{s}$  exponential decay waveform according to IEC61000-4-5

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## 3 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified



**Figure 3-1 Definitions of electrical characteristics**

**Electrical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Table 3-1 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	-5.5	–	5.5	V	
Trigger voltage	$V_{t1}$	6	–	–	V	
Holding voltage	$V_h$	6	8	10	V	$I_T = 1\text{ mA}$
Reverse current	$I_R$	–	<1	100	nA	$V_R = 5.5\text{ V}$

**Table 3-2 AC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	4 –	5 5	7 –	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$
Series inductance	$L_S$	– –	0.2 0.4	– –	nH	ESD205-B1-02ELS ESD205-B1-02EL

**Table 3-3 ESD and Surge Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>1)</sup>	$V_{CL}$	–	10	–	V	$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$ from Pin 1 to Pin 2
		–	13	–		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$ from Pin 1 to Pin 2
		–	12	–		$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$ from Pin 2 to Pin 1
		–	17	–		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$ from Pin 2 to Pin 1
Clamping voltage <sup>2)</sup>	$V_{CL}$	–	8	–	V	$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ from Pin 1 to Pin 2
		–	8.5	–		$I_{PP} = 2.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ from Pin 1 to Pin 2
		–	8	–		$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ from Pin 2 to Pin 1
		–	9	–		$I_{PP} = 2.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ from Pin 2 to Pin 1
Dynamic resistance <sup>1)</sup>	$R_{DYN}$	–	0.2	–	$\Omega$	Pin 1 to Pin 2
		–	0.3	–	$\Omega$	Pin 2 to Pin 1

1) Please refer to Application Note AN210[1]. TLP parameter:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$ .

2) Non-repetitive current pulse 8/20 $\mu\text{s}$  exponential decay waveform according to IEC61000-4-5

## 4 Typical Characteristics Diagrams

Typical characteristics diagrams at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

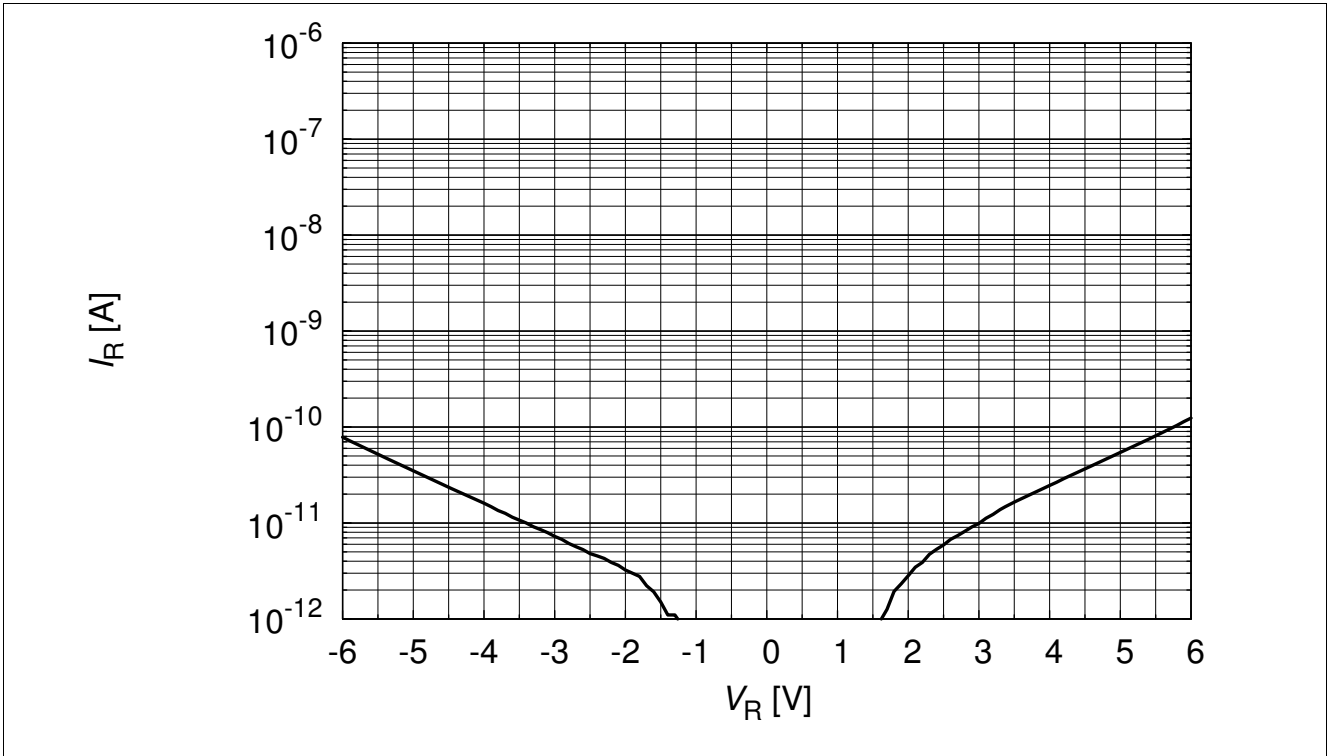


Figure 4-1 Reverse leakage current:  $I_R = f(V_R)$

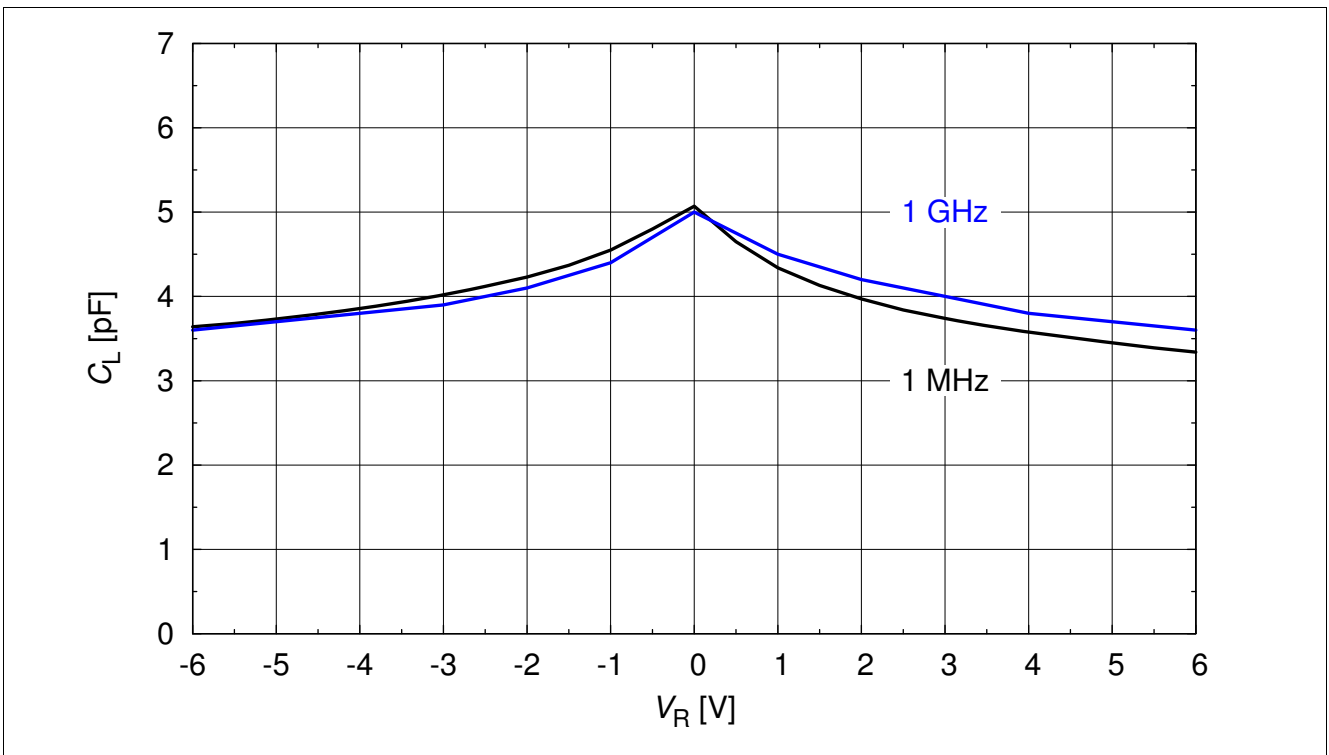


Figure 4-2 Line capacitance:  $C_L = f(V_R)$

Typical Characteristics Diagrams

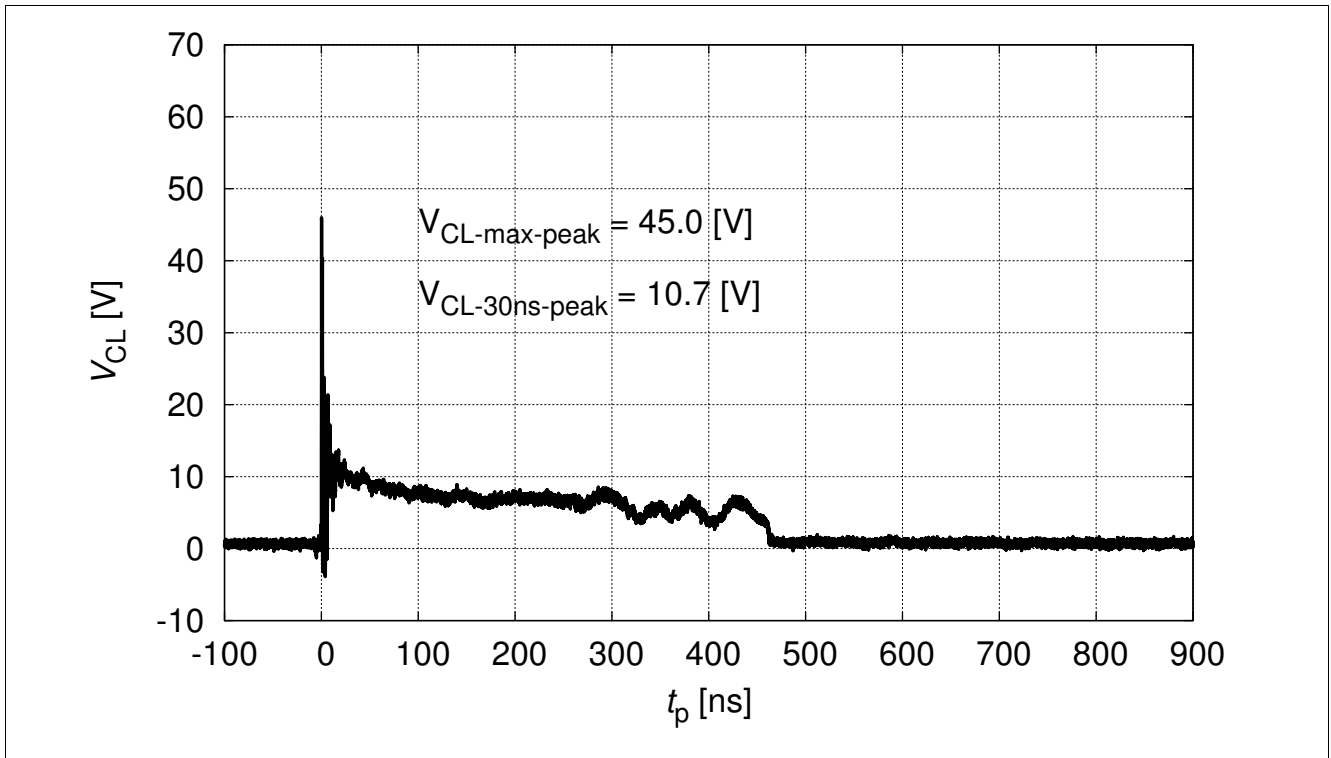


Figure 4-3 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positive pulse from pin 1 to pin 2

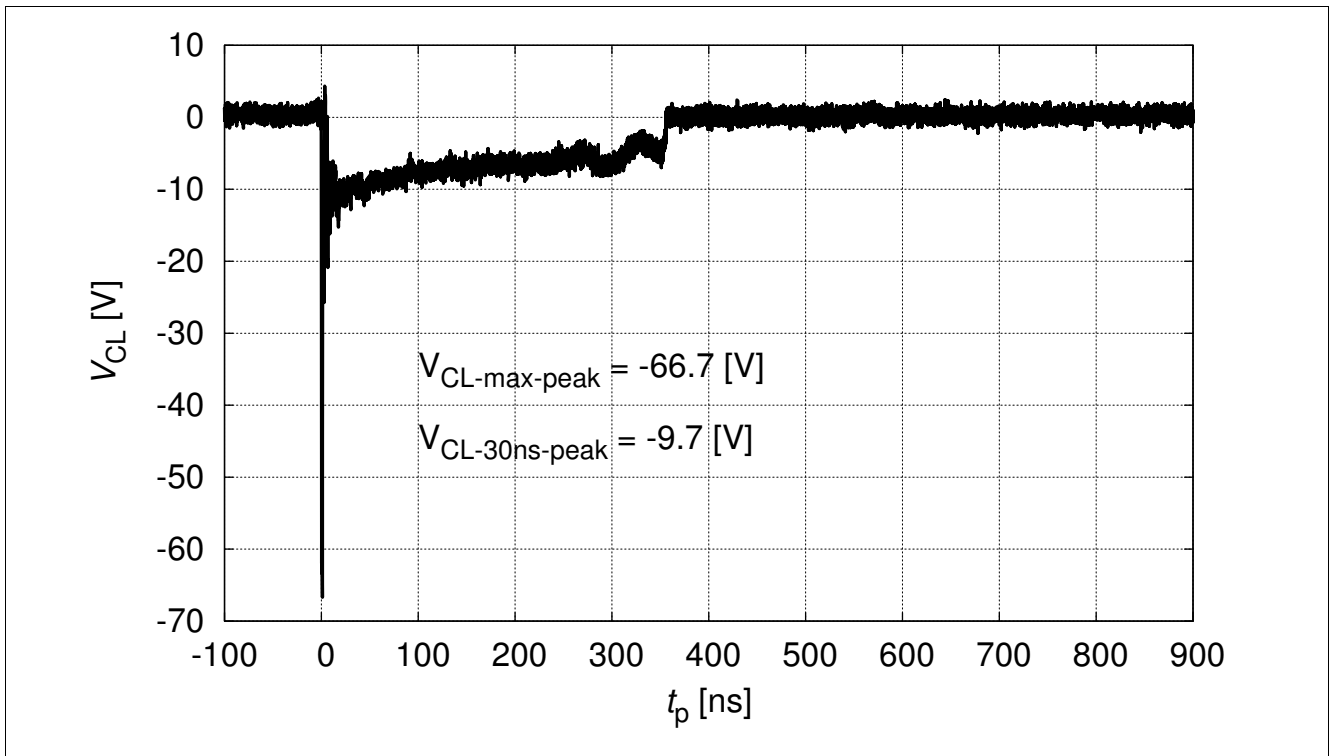


Figure 4-4 Clamping voltage (ESD)  $V_{CL} = f(t)$ , 8 kV negative pulse from pin 1 to pin 2

Typical Characteristics Diagrams

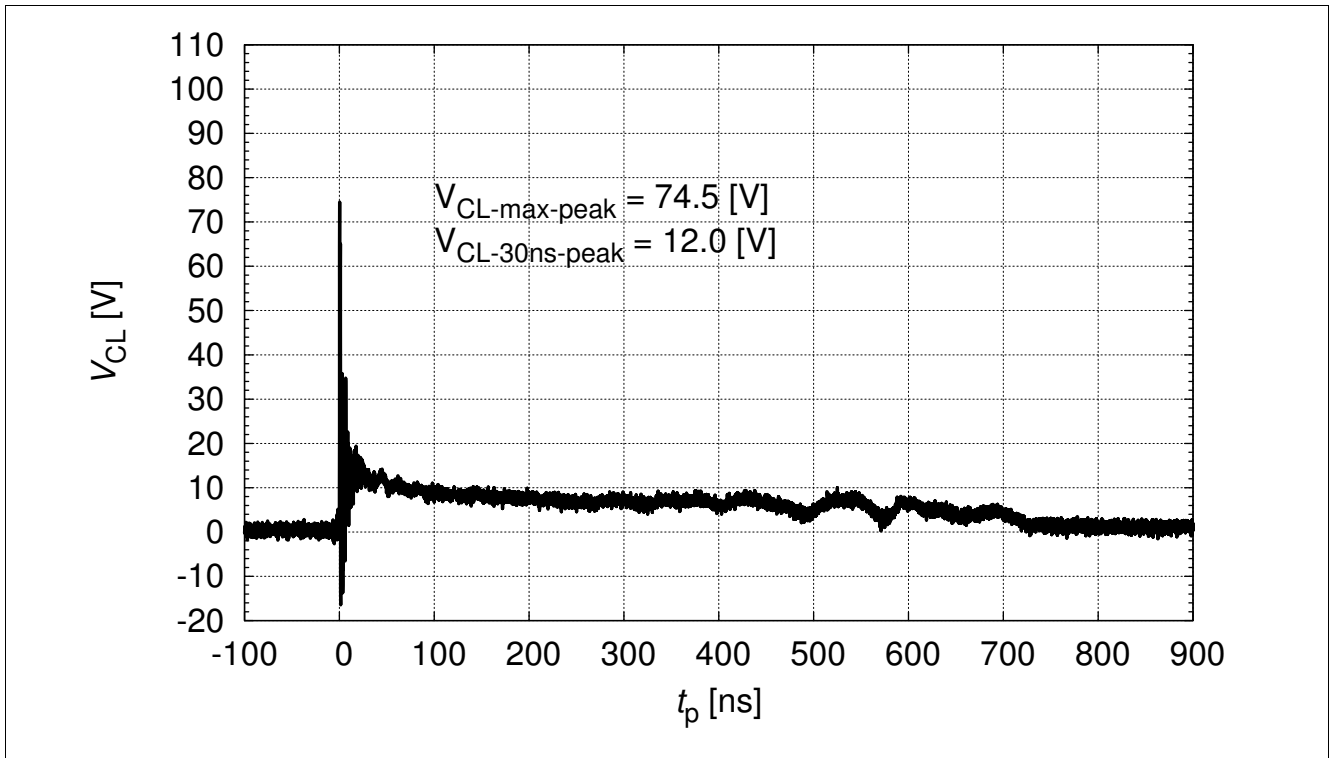


Figure 4-5 Clamping voltage (ESD)  $V_{CL} = f(t)$ , 15 kV positive pulse from pin 1 to pin 2

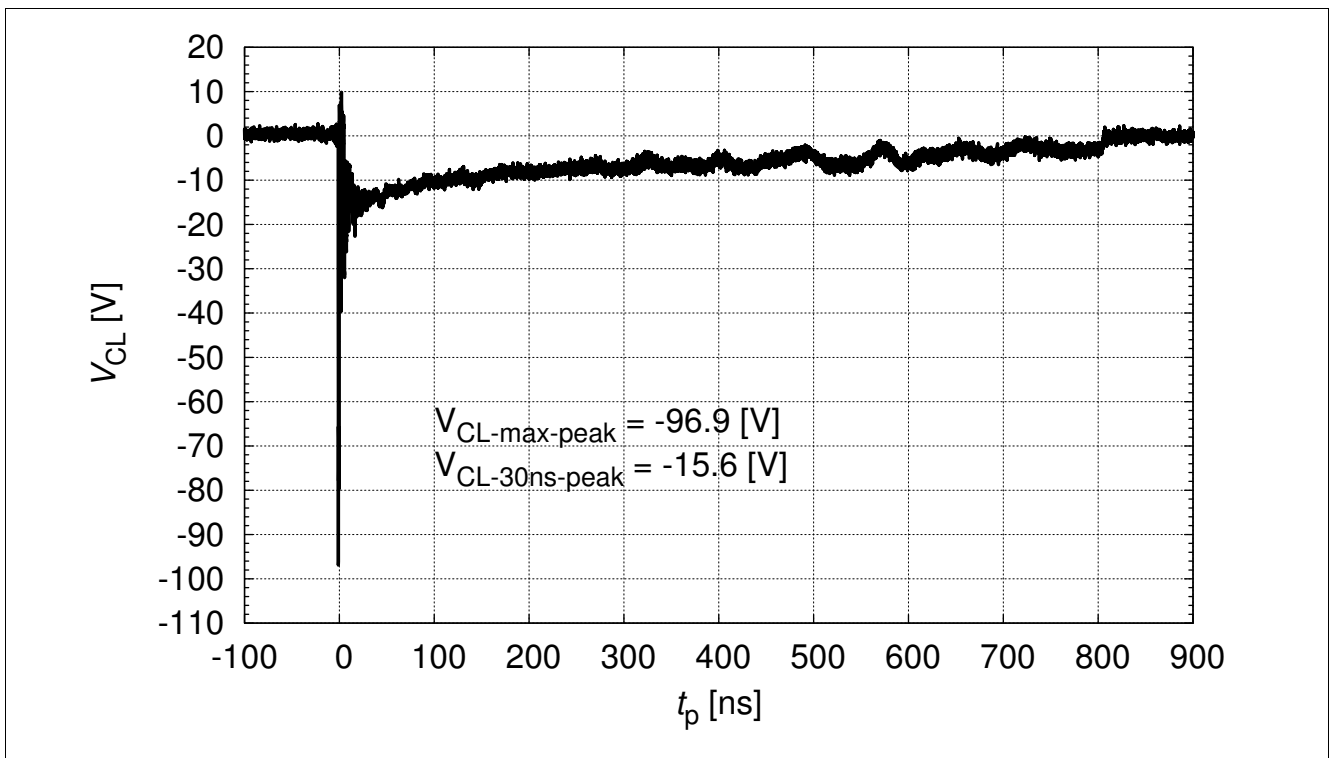


Figure 4-6 Clamping voltage (ESD)  $V_{CL} = f(t)$ , 15 kV negative pulse from pin 1 to pin 2



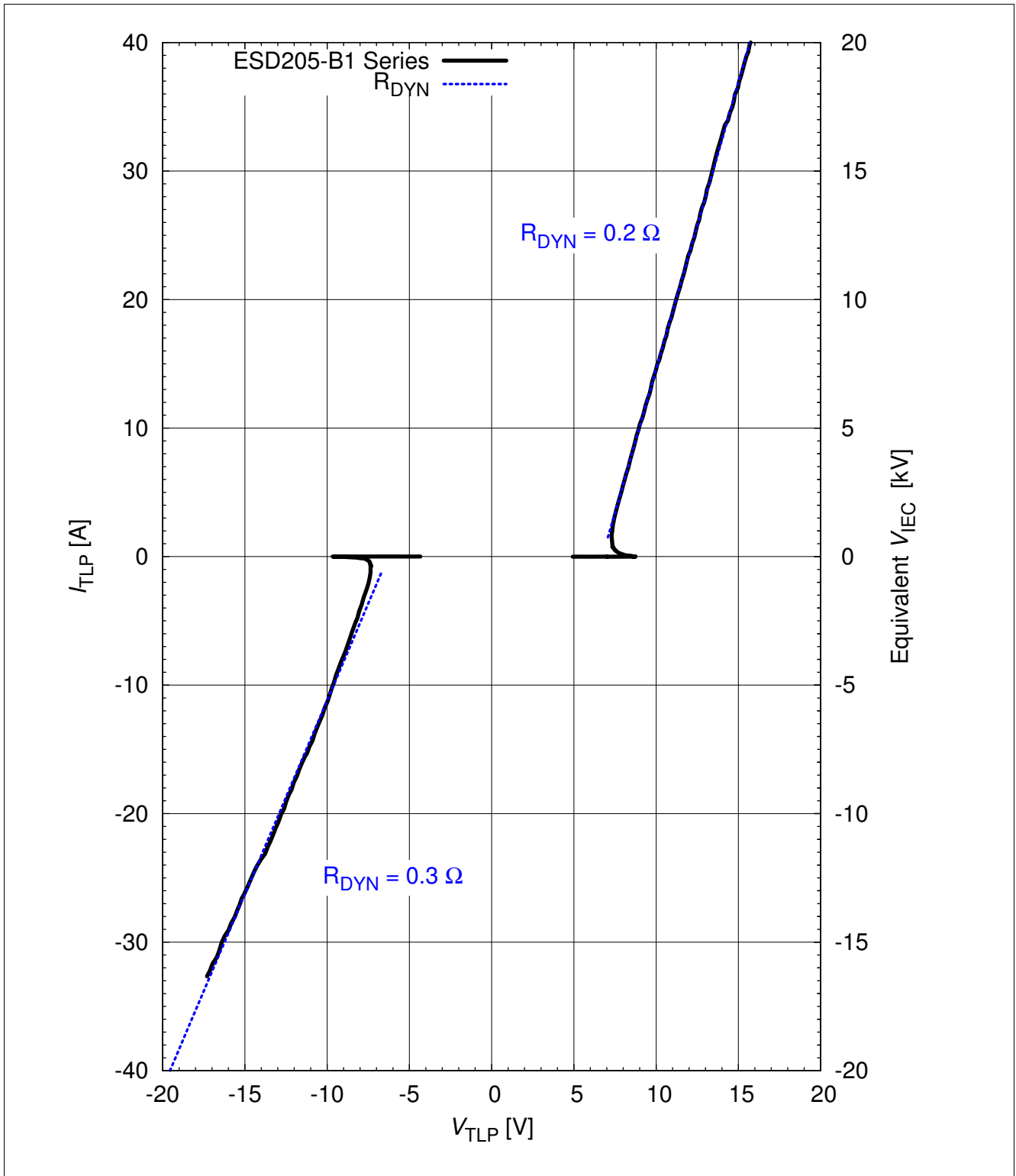


Figure 4-7 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

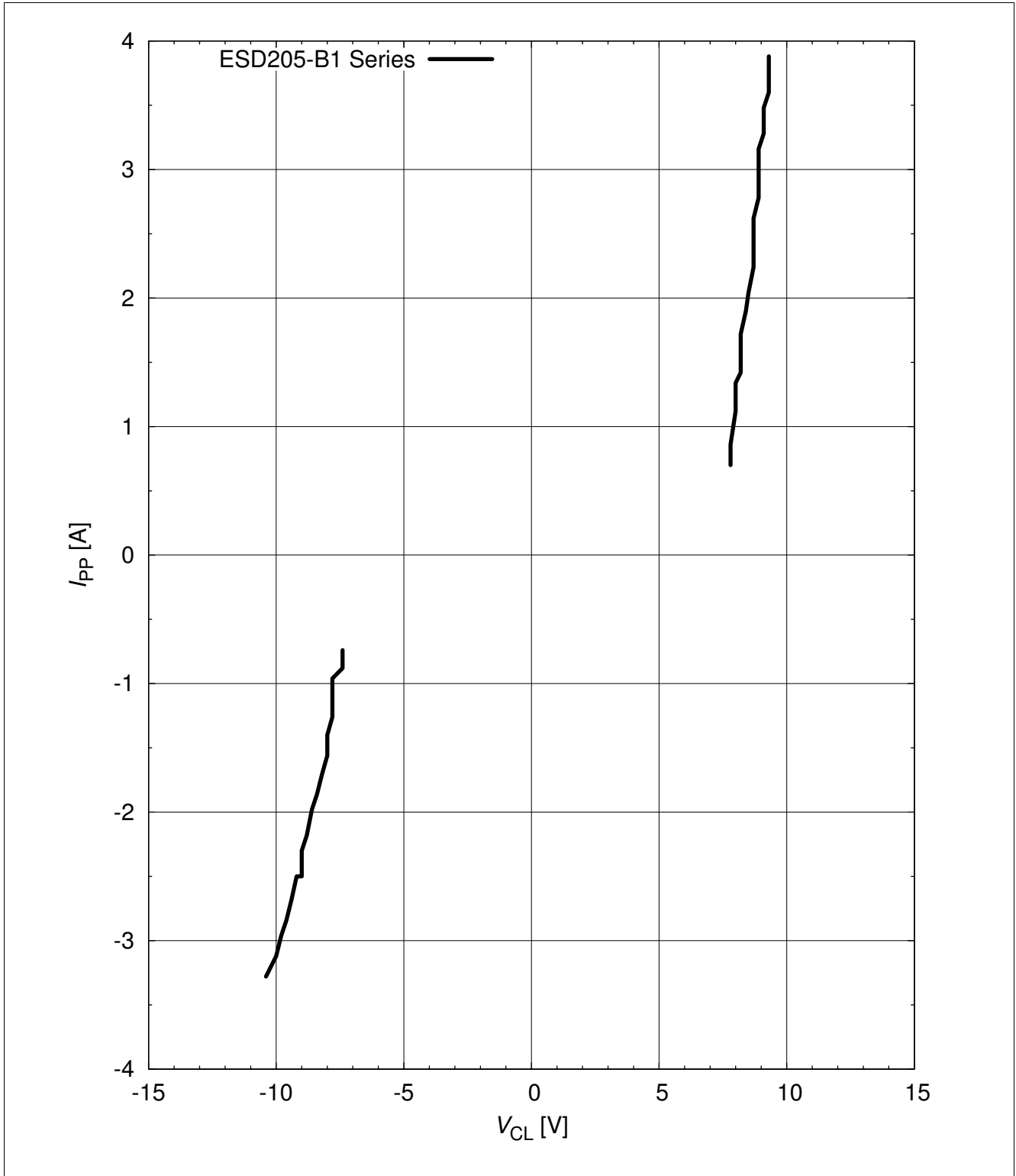


Figure 4-8 Clamping voltage (Surge):  $I_{PP} = f(V_{CL})$ [1], pin 1 to pin 2

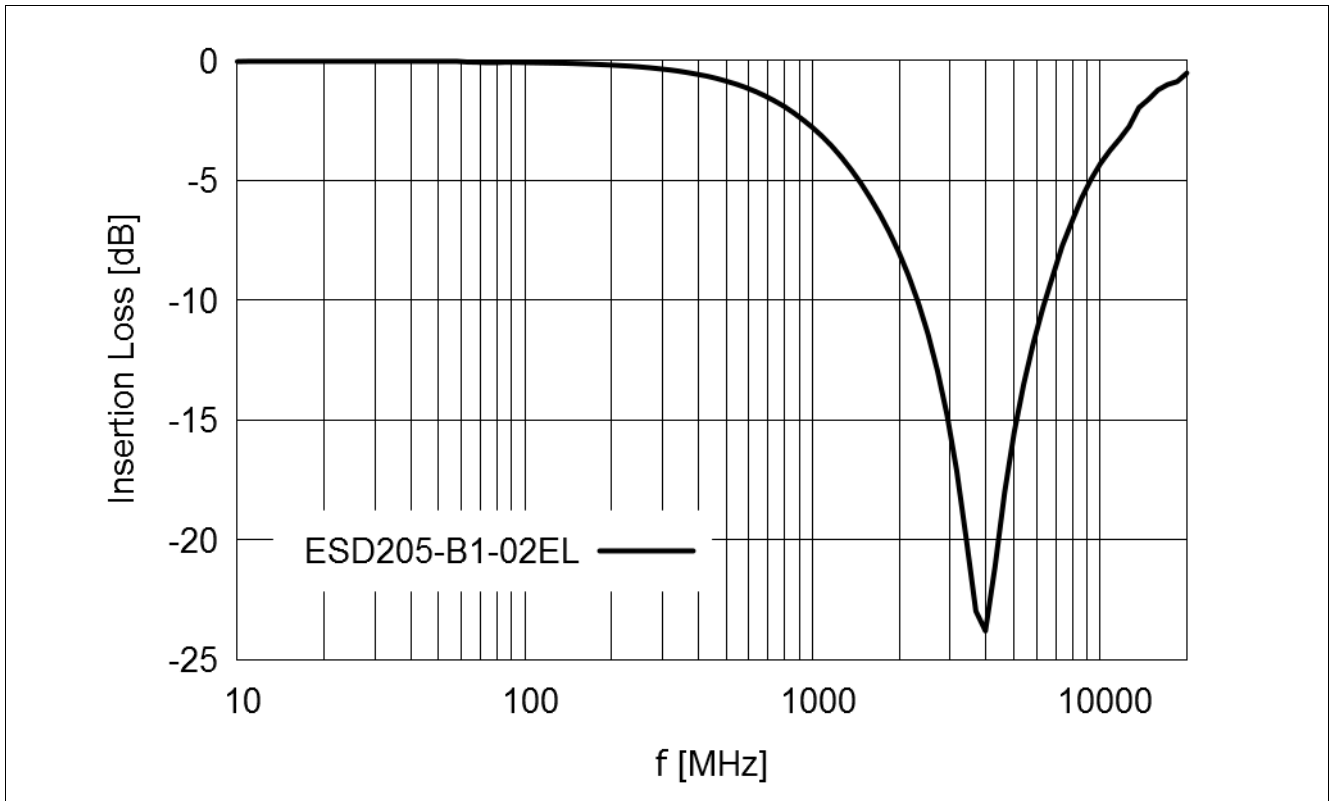


Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

## 5 Package Information

### 5.1 TSSLP-2-3

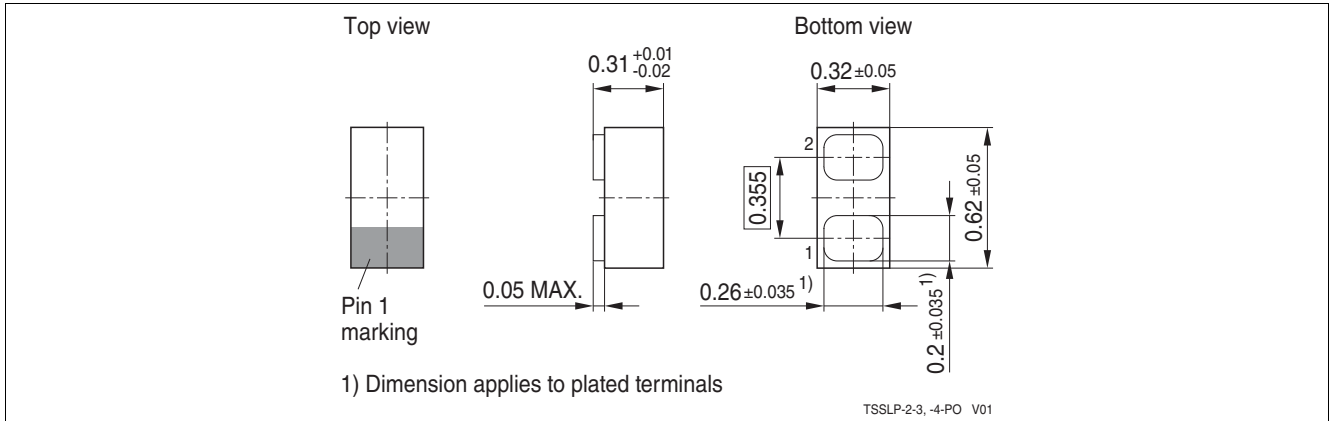


Figure 5-1 TSSLP-2-3 Package outline

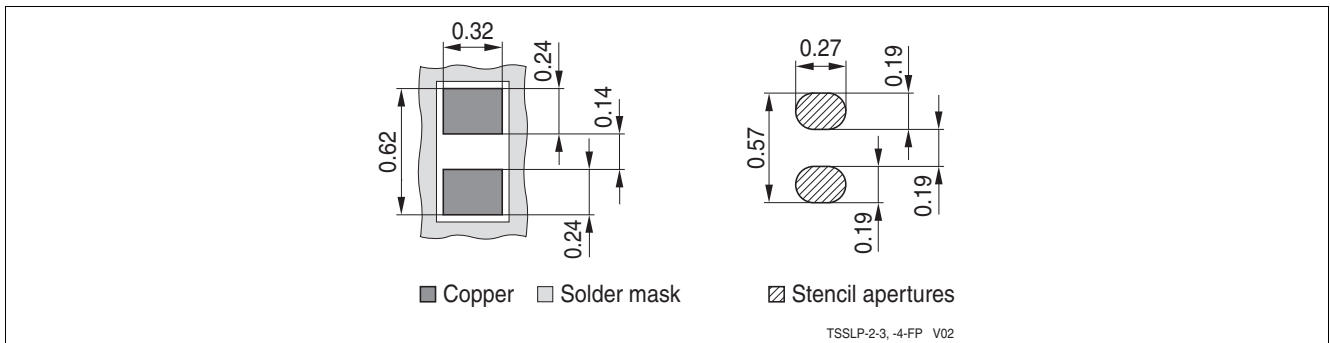


Figure 5-2 TSSLP-2-3 Footprint

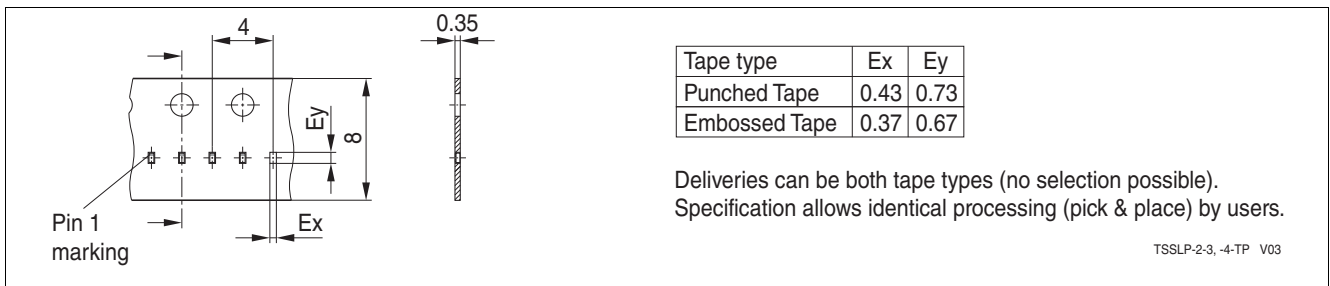


Figure 5-3 TSSLP-2-3 Packing

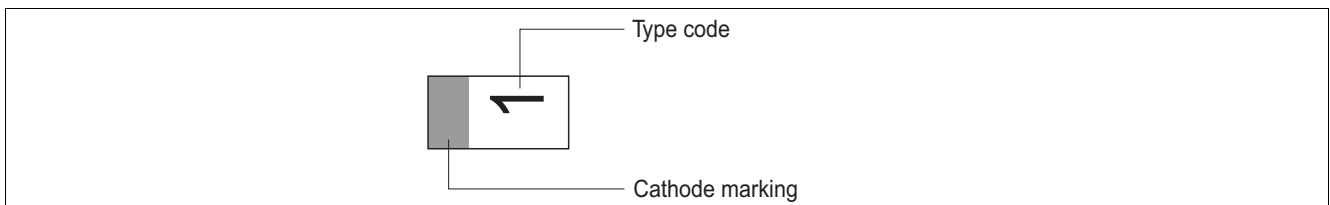


Figure 5-4 TSSLP-2-3 Marking example, Type code see: [Table 1-1 "Ordering Information" on Page 3](#)

5.2 TSLP-2-19

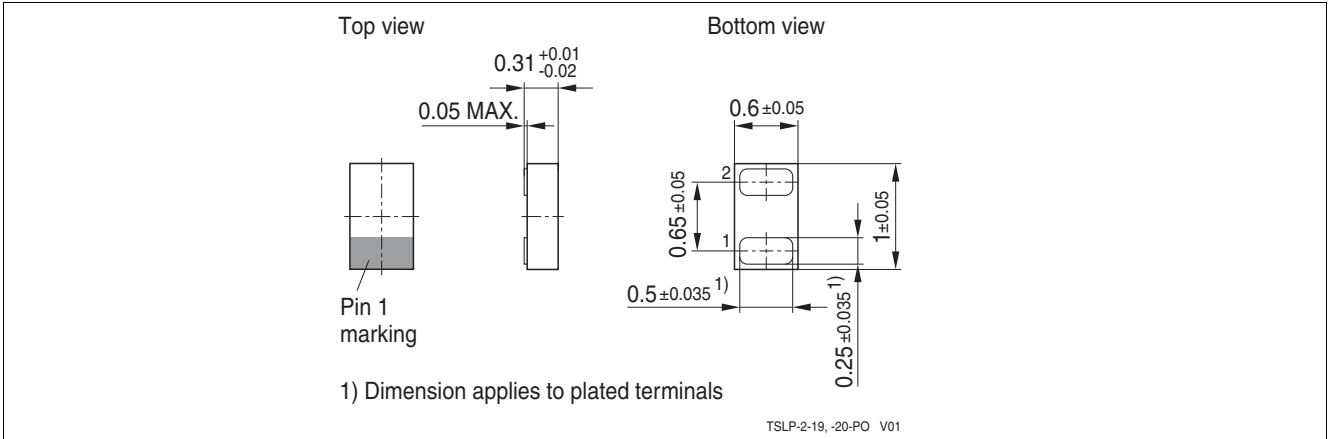


Figure 5-5 TSLP-2-19 Package outline

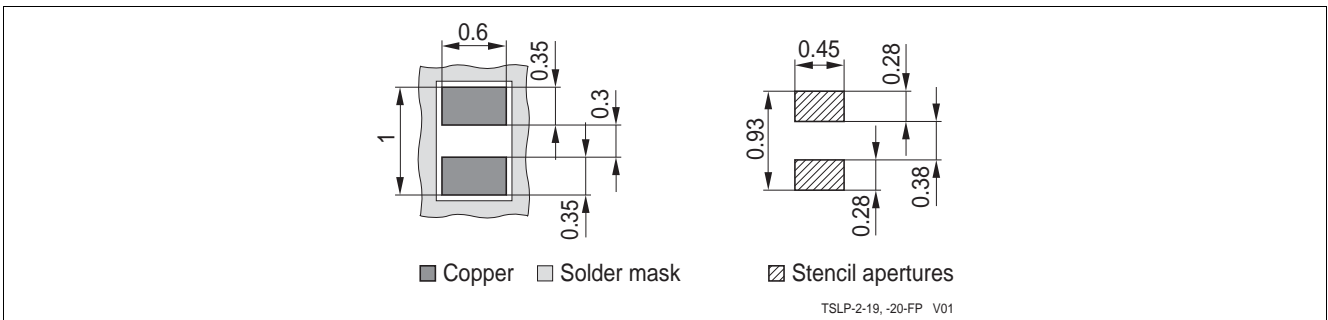


Figure 5-6 TSLP-2-19 Footprint

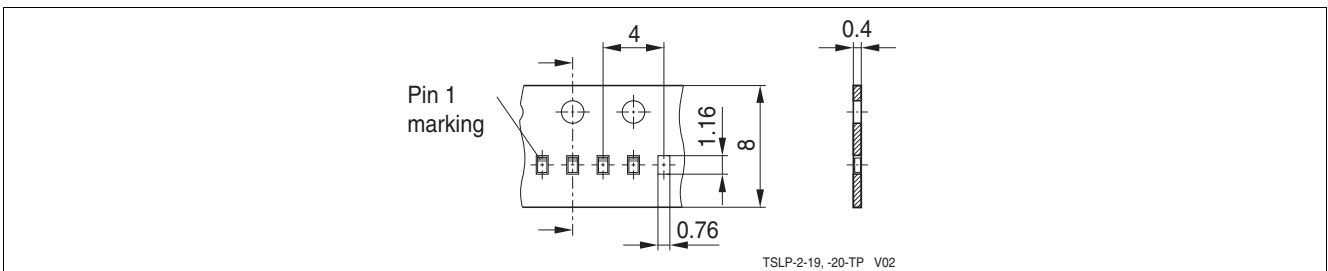


Figure 5-7 TSLP-2-19 Packing

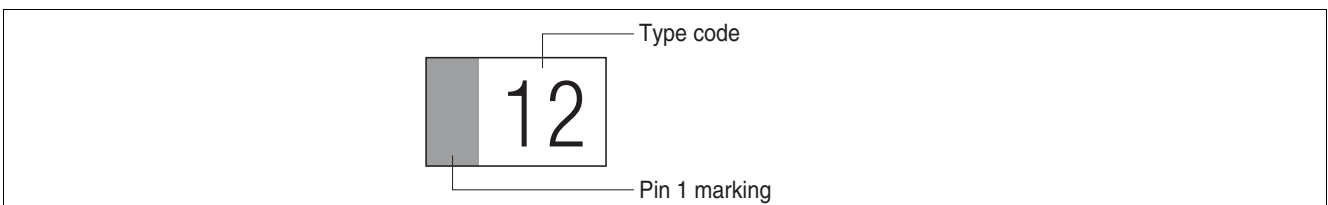


Figure 5-8 TSLP-2-19 Marking example, Type code see: [Table 1-1 “Ordering Information” on Page 3](#)

**References**

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

**Revision History: Revision 1.3,.2013-03-08**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.4, 2014-05-14</b>	
All	New type ESD205-B1-02EL inserted

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