

ESD242-B1-W01005

Protection Devices

TVS (Transient Voltage Suppressor)

Bi-directional, 3.3 V, 6 pF, 01005, RoHS and Halogen Free compliant

Feature list

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 18 kV (air / contact discharge)
 - IEC61000-4-4 (EFT): ± 2 kV / ± 40 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 4.5 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 3.3$ V
- Line capacitance: $C_L = 6$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 6$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.09 \Omega$ (typical)
- Very low reverse current: $I_R < 1$ nA (typical)
- Small form factor SMD size 01005 and low profile (0.43 mm x 0.23 mm x 0.15 mm); for further package information please refer to application note [\[3\]](#)
- Bi-directional and symmetric I/V characteristics for optimized design and assembly



Potential applications

- IC/ASICs in audio, headset
- Human digital interfaces, buttons, GPIO

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

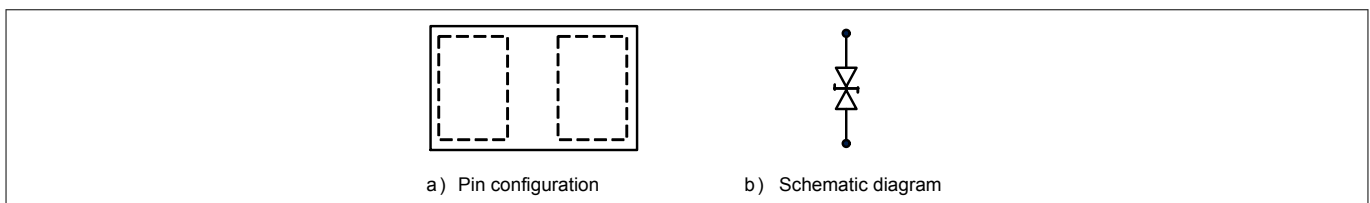


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD242-B1-W01005	WLL-2-2	1 line, bi-directional	AC ¹⁾

¹ The device has no marking on the device top. The marking code is on the pad side.

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Maximum ratings

1 Maximum ratings

Note: $T_A = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	± 3.3	V
ESD discharge ¹⁾	V_{ESD} (contact)	± 18	kV
	V_{ESD} (air)	± 18	
Peak pulse power ²⁾	P_{PK}	25	W
Peak pulse current ²⁾	I_{PP}	± 4.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

¹ V_{ESD} according to IEC61000-4-2 (R = 330 Ω , C = 150 pF discharge network)

² Stress pulse: 8/20 μ s current waveform according to IEC61000-4-5

Electrical characteristics

2 Electrical characteristics

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified. Device is electrically symmetrical.

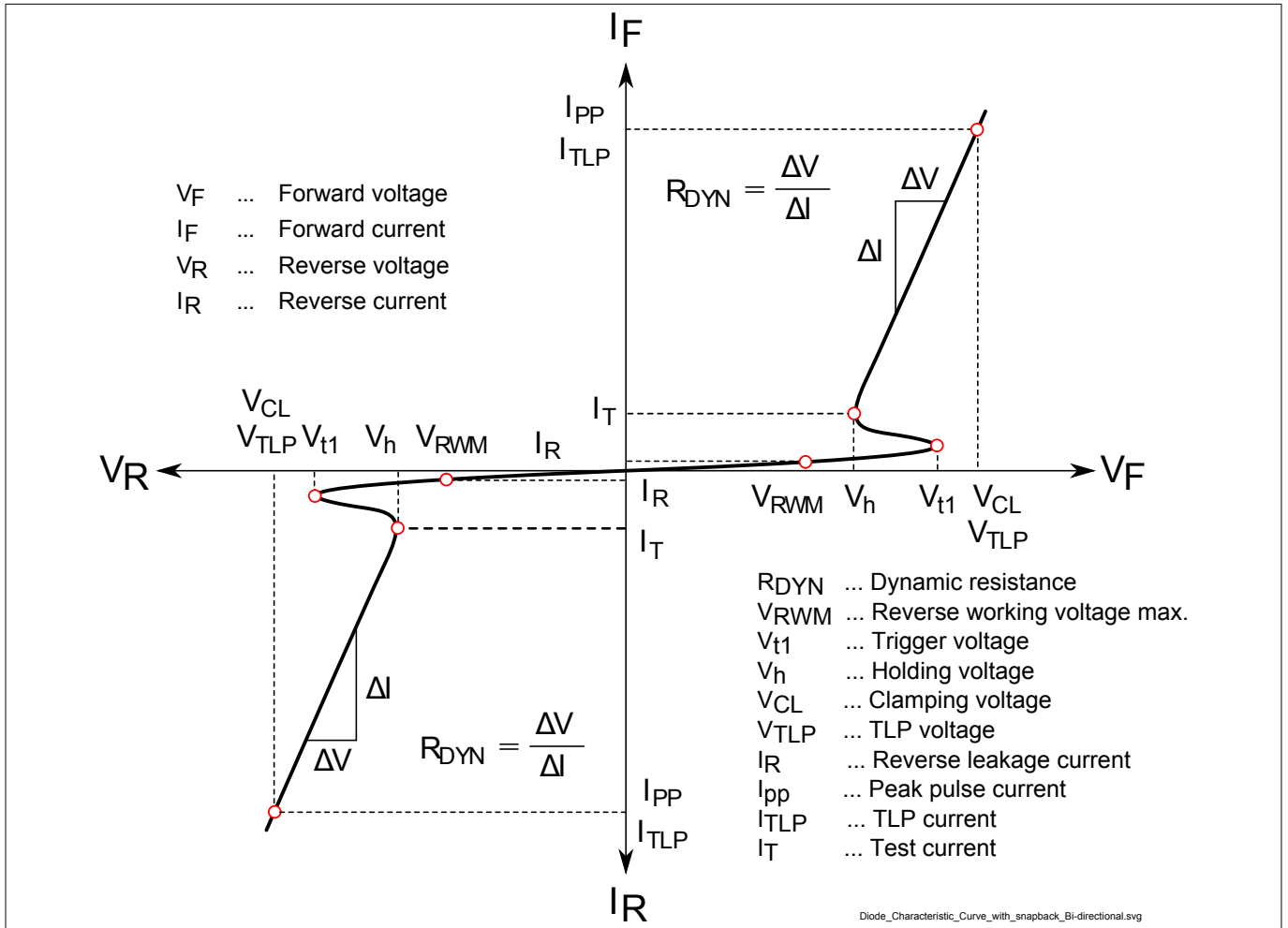


Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Trigger Voltage ¹⁾²⁾	V_{t1}	5	6	–	V	–
Holding voltage ³⁾	V_h	4	5.7	7.2	V	$I_R = 1 \text{ mA}$
Reverse current	I_R	–	1	30	nA	$V_R = 3.3 \text{ V}$

Table 4 AC characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	6	–	pF	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$
		–	6	–		$V_R = 0 \text{ V}, f = 1 \text{ GHz}$

Table 5 ESD and Surge characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage ⁴⁾	V_{CL}	–	6	–	V	$I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$
		–	7	–		$I_{TLP} = 30 \text{ A}, t_p = 100 \text{ ns}$
Clamping voltage ⁵⁾		–	5	–		$I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{s}$
		–	6	–		$I_{PP} = 4 \text{ A}, t_p = 8/20 \mu\text{s}$
Dynamic resistance ⁴⁾	R_{DYN}	–	0.09	–	Ω	$t_p = 100 \text{ ns}$

1 Verified by design

2 Voltage forced

3 Current forced

4 Please refer to Application Note AN210 [1]. TLP parameters: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$.

5 Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

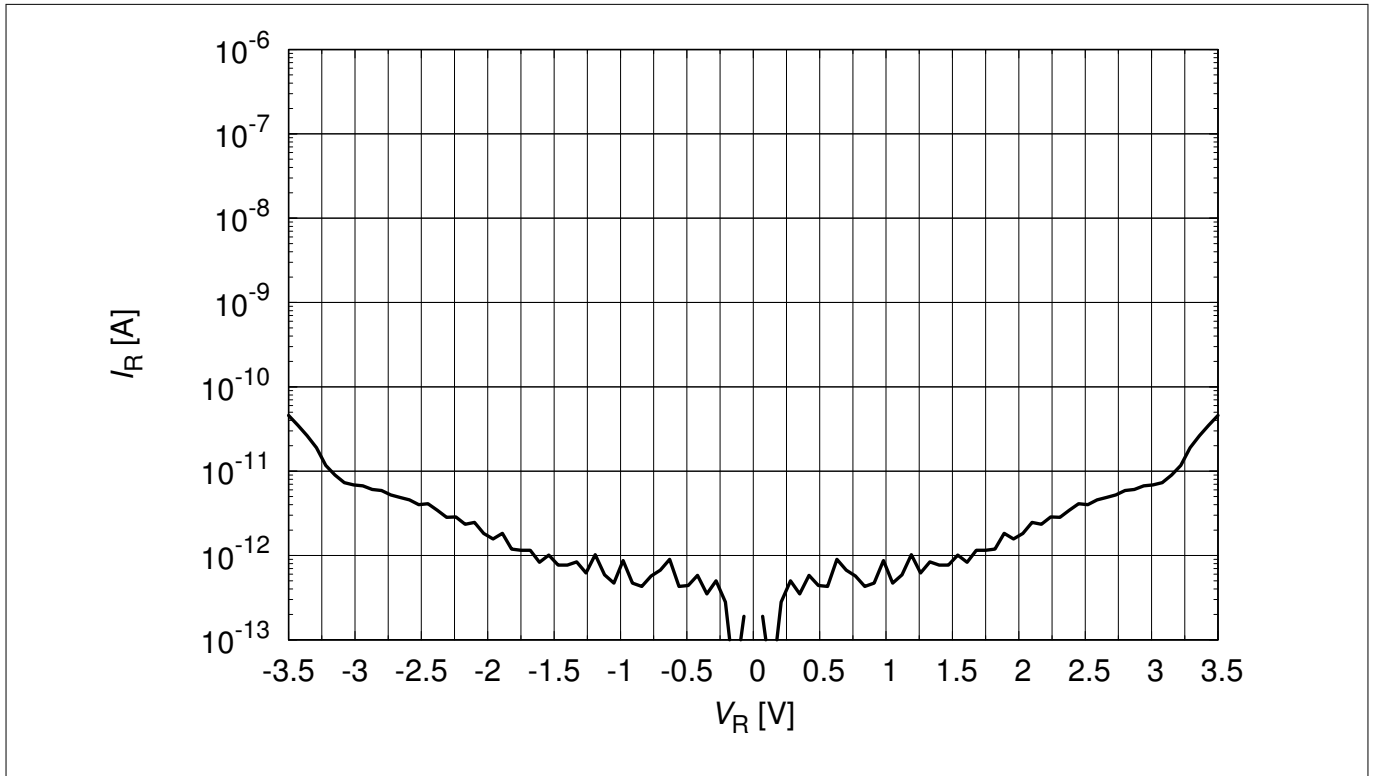


Figure 3 Reverse leakage current: $I_R = f(V_R)$

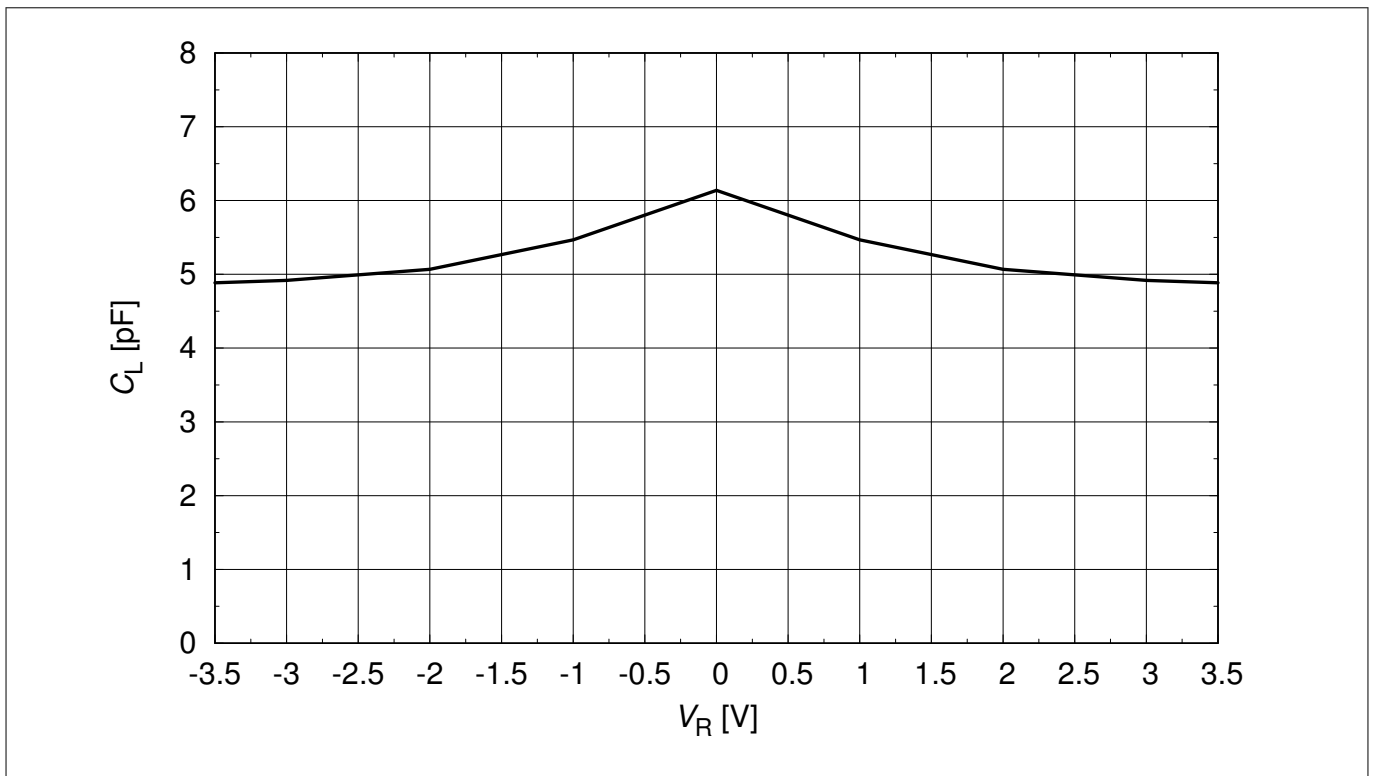


Figure 4 Line capacitance: $C_L = f(V_R)$, $f = 1\text{ MHz}$

Typical characteristic diagrams

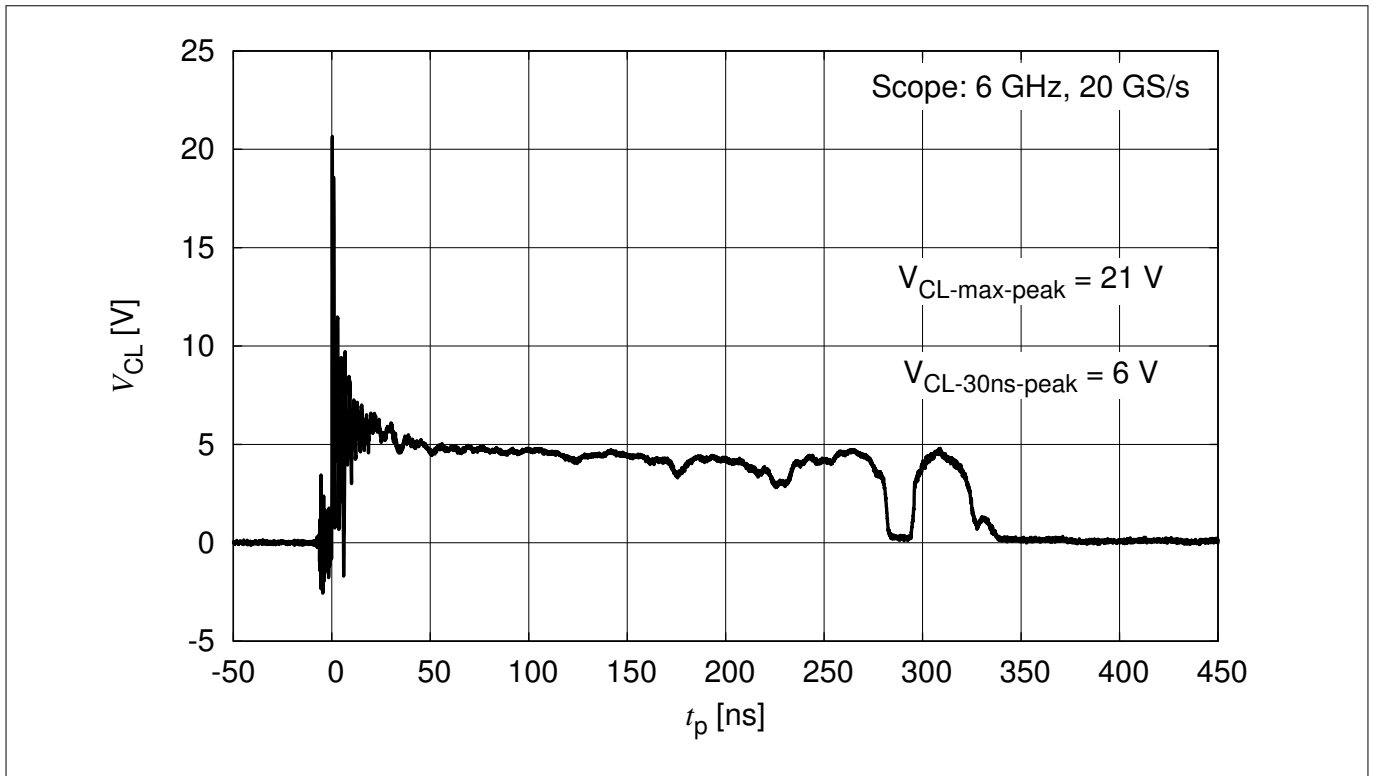


Figure 5 Clamping voltage (ESD): $V_{CL} = f(V_t)$, 8 kV positive (according to IEC61000-4-2)

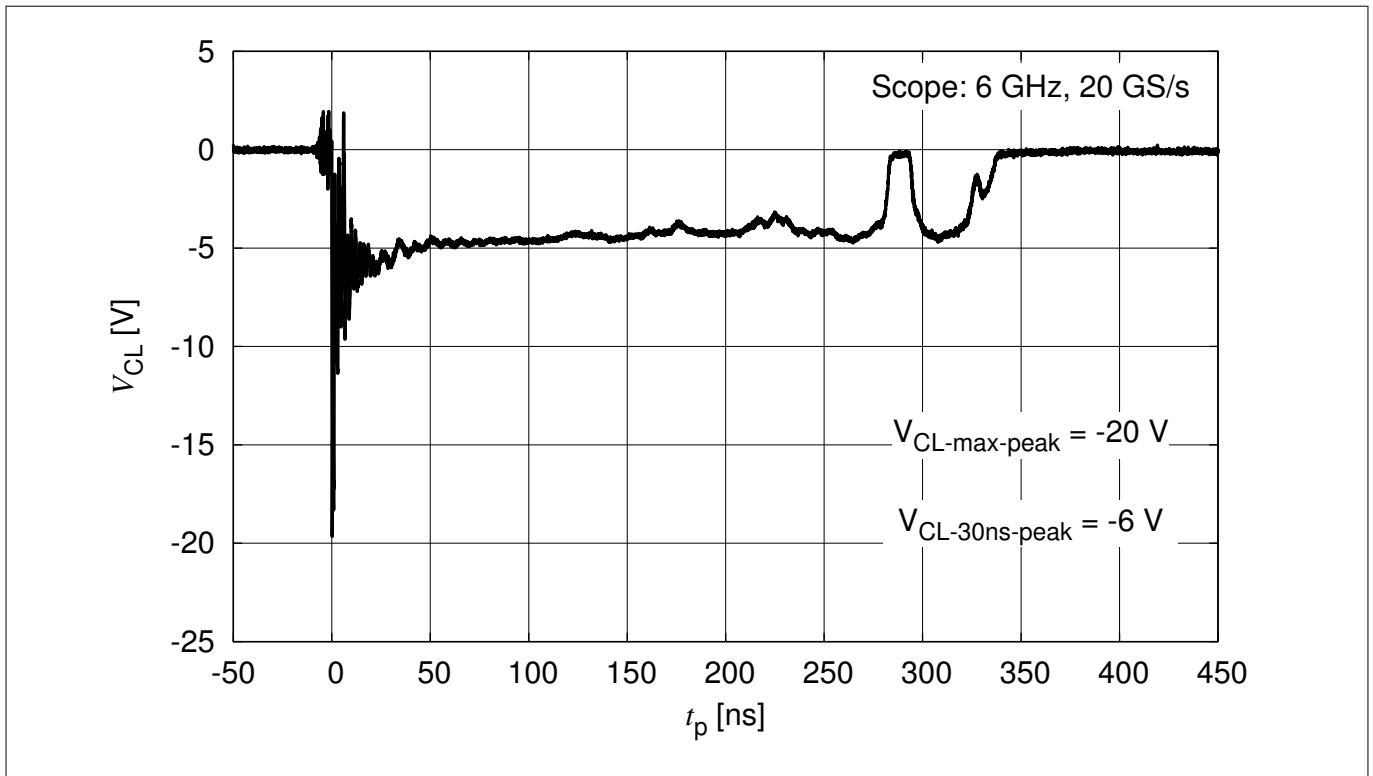


Figure 6 Clamping voltage (ESD): $V_{CL} = f(V_t)$, 8 kV negative (according to IEC61000-4-2)

Typical characteristic diagrams

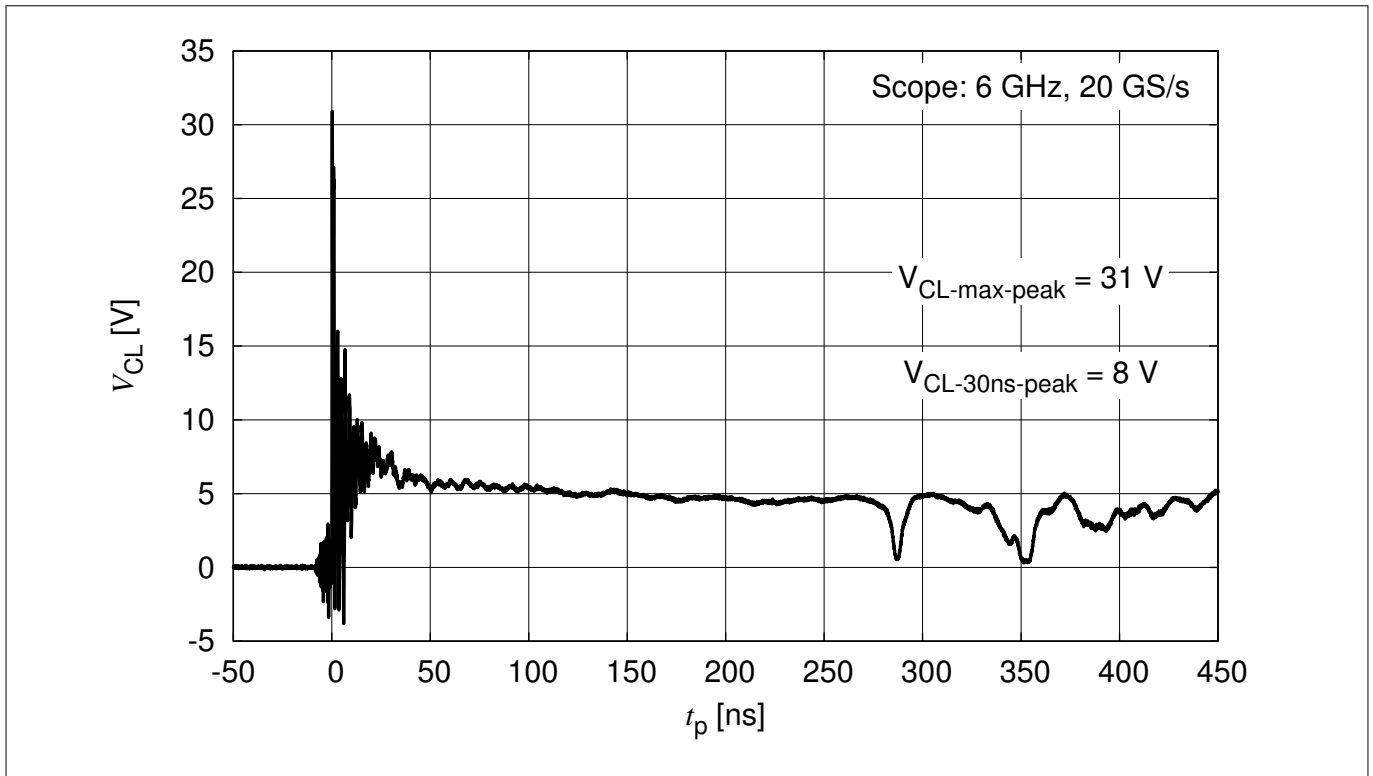


Figure 7 Clamping voltage (ESD): $V_{CL} = f(V_t)$, 15 kV positive (according to IEC61000-4-2)

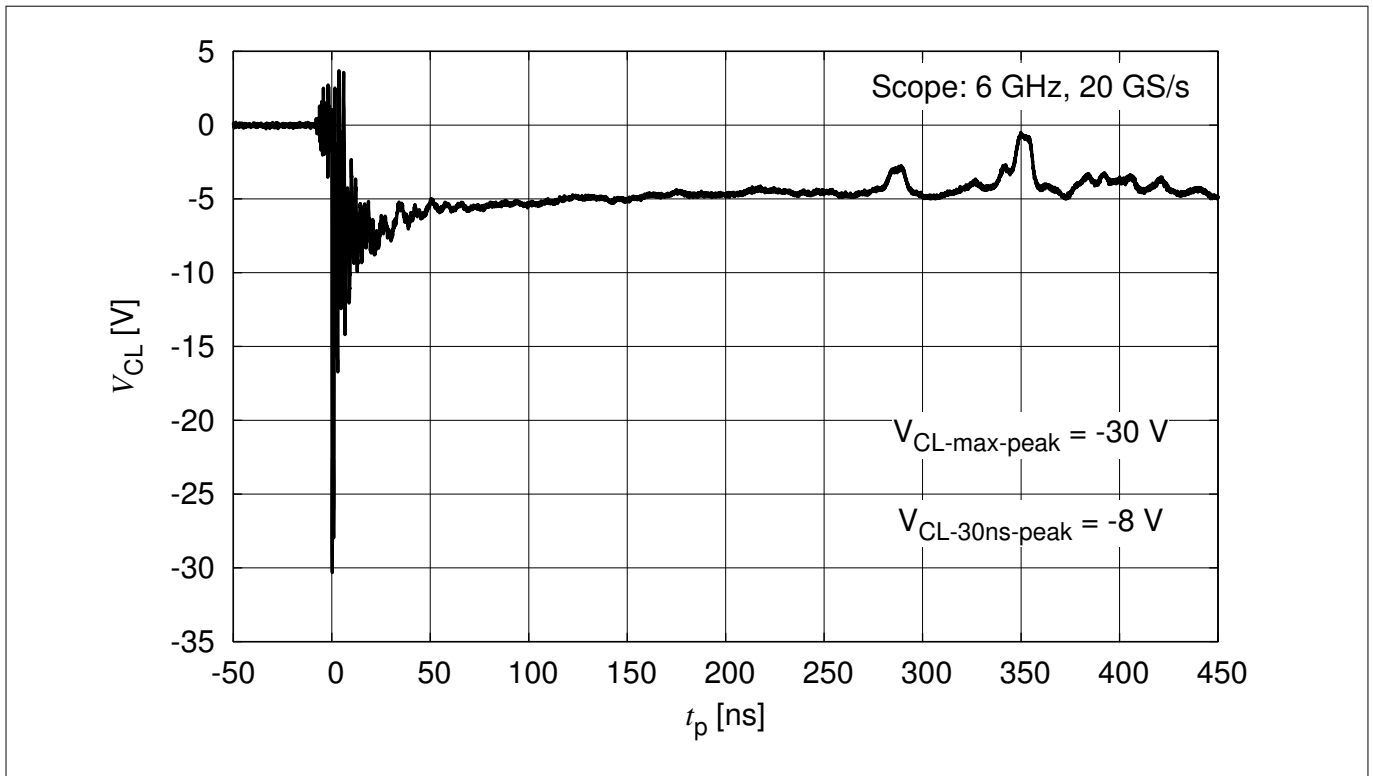


Figure 8 Clamping voltage (ESD): $V_{CL} = f(V_t)$, 15 kV negative (according to IEC61000-4-2)

Typical characteristic diagrams

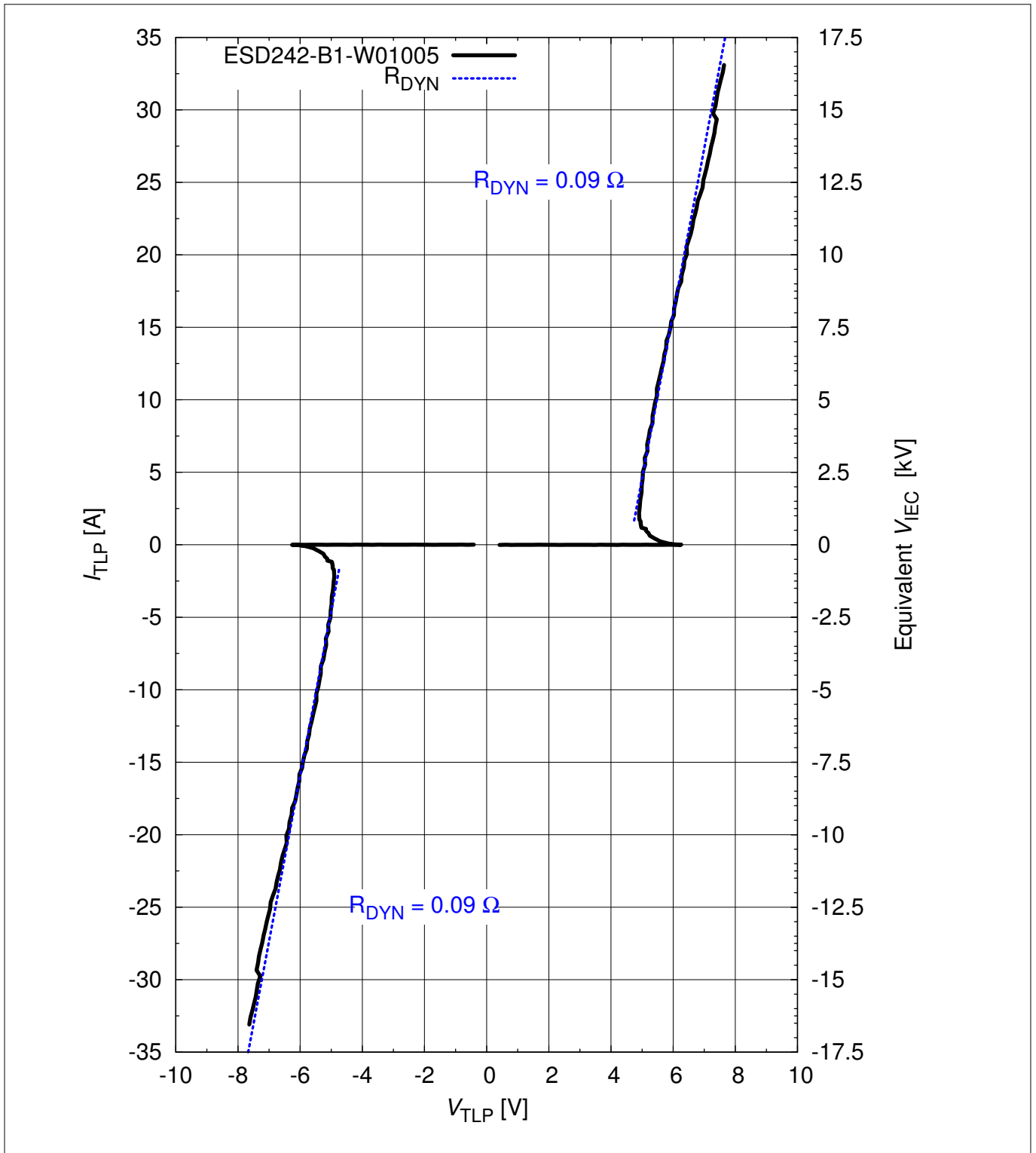


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

Typical characteristic diagrams

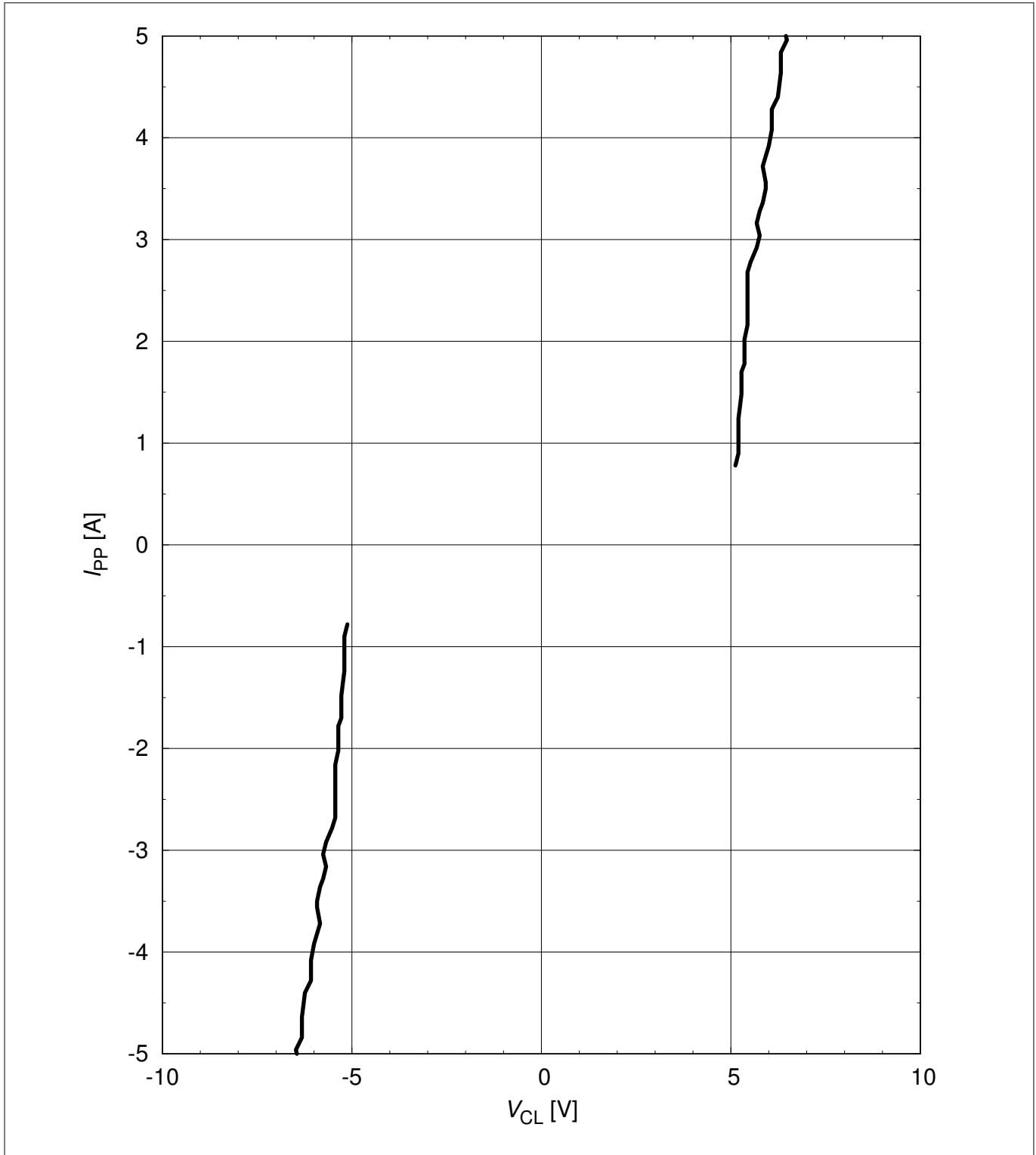


Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ (according to IEC61000-4-5) [1]

Package information

4 Package information

4.1 WLL-2-2 package

Note: Dimensions in mm

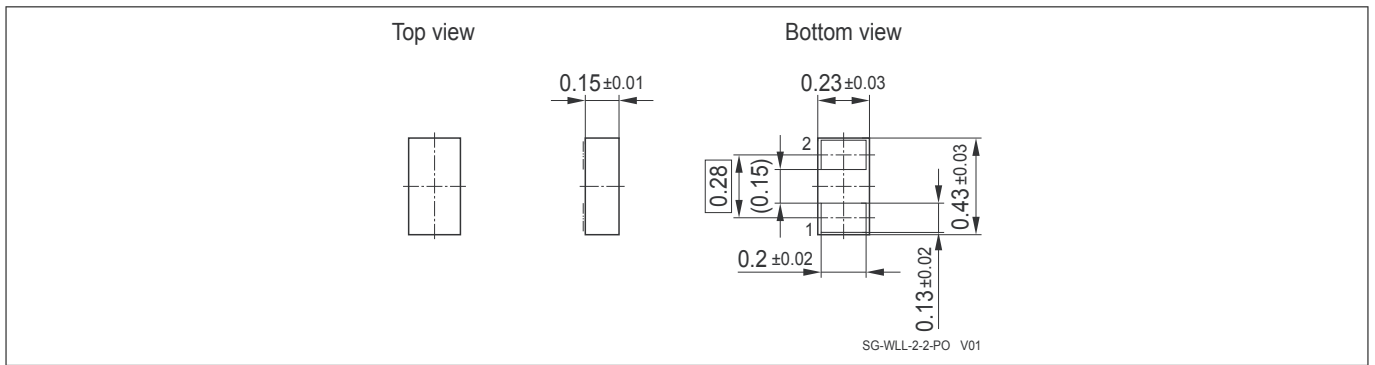


Figure 11 WLL-2-2 package outline

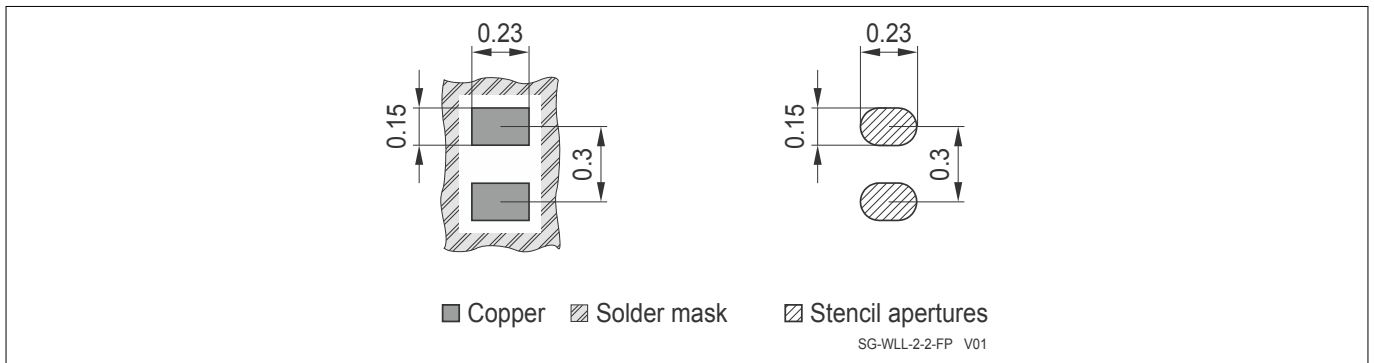


Figure 12 WLL-2-2 footprint (recommendation for Printed Circuit Board assembly see [2])

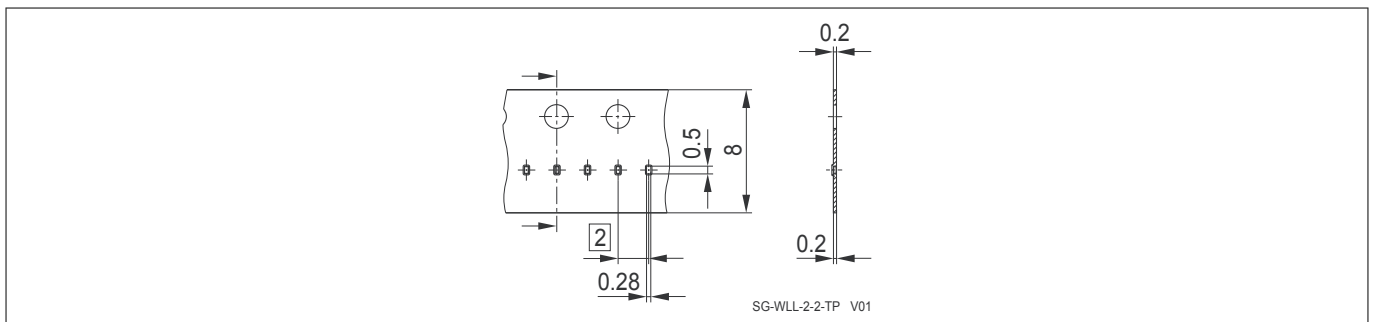


Figure 13 WLL-2-2 packing

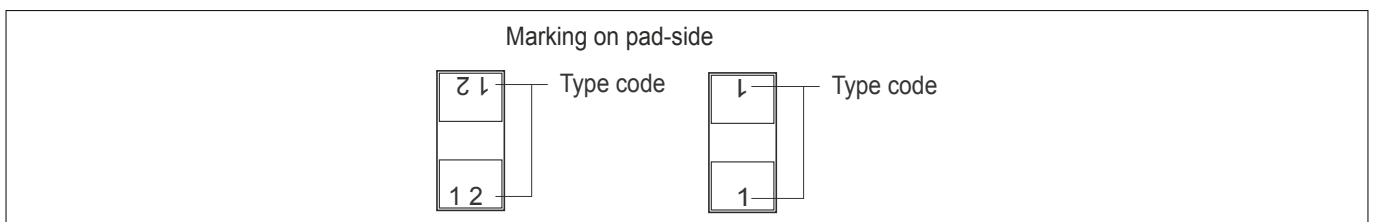


Figure 14 WLL-2-2 marking example (see [Device information](#))

References

5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Rev. 1.0, 2017-06-26

Page or Item	Subjects (major changes since previous revision)
Revision 1.1, 2017-11-27	
Chapter 3	ESD pulse curves (IEC61000-4-2) added
	Minor editorial changes

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