CCM PFC demo board with 600 V CoolMOS™ S7 for active-line rectification and inrush current control

2400 W 65 kHz high-efficiency and high power density design

About this document

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Scope and purpose

This document is an application note describing the design and operation of a complete Infineon Technologies AG system solution for a 2400 W Continuous Conduction Mode (CCM) Power Factor Correnction (PFC) converter with active-line rectification and solid-state relay solutions based on the 600 V CoolMOS™ S7.

The demo board presented in this document, later named as **EVAL_2K4W_ACT_BRD_S7**, has two additional features compared to a standard boost PFC:

1. **Use of 600 V CoolMOS™ S7 for the active-bridge rectification to increase efficiency**
2. **Replacement of inrush current relay with 600 V CoolMOS™ S7 to increase power density**

This document describes the converter hardware (shown in Figure 1) and the test results of the full Infineon solution, focusing on the main benefits of using the 600 V CoolMOS™ S7 for active-line rectification and relay replacement.

The main Infineon components used in the 2400 W active-bridge CCM PFC are described as follows:

Active bridge:

- 600 V CoolMOS™ S7 Superjunction (SJ) MOSFET
- IR11688S dual Synchronous Rectification (SR) control IC (Smartrectifier™)
- 2EDF7275F fast dual-channel functional isolated gate driver (EiceDRIVER™)

PFC:

- 600 V CoolMOS™ C7 SJ MOSFET
- 650 V CoolSiC™ Schottky diode
- Medium-power Schottky diode BAT165
- ICE3PCS01G standalone CCM PFC control IC
- 1EDN8550B single-channel with true differential inputs non-isolated gate driver (EiceDRIVER™)

Pre-charge:

- 600 V CoolMOS™ S7 SJ MOSFET

Bias supply:

- 950 V CoolMOS™ P7 SJ MOSFET
- ICE5QSAG CoolSET™ Quasi Resonant (QR) Flyback controller

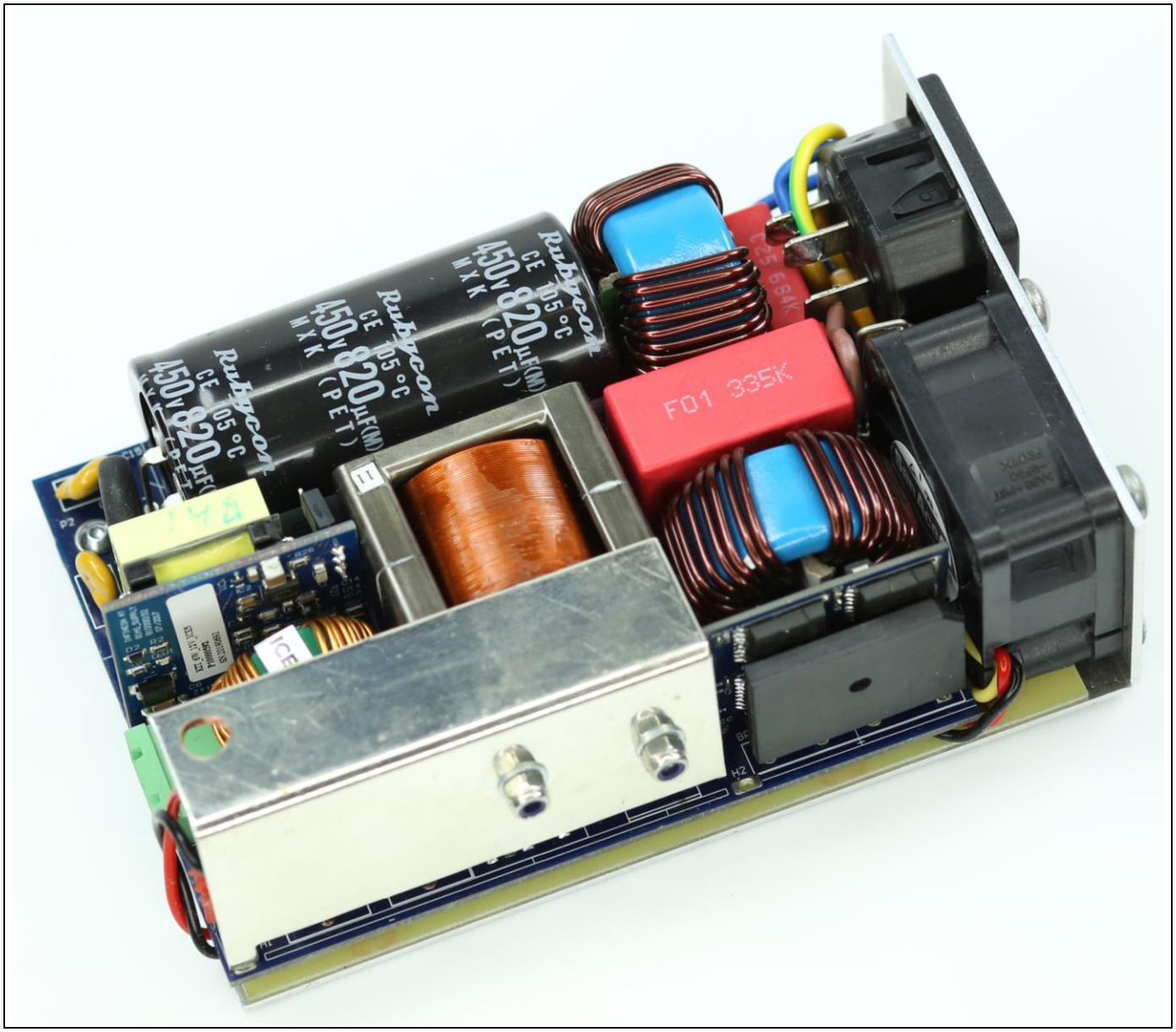

Figure 1 2400 W active-bridge CCM PFC based on 600 V CoolMOS™ S7

Intended audience

This document is intended for power supply designers, application engineers, students and anyone who wants to quickly improve the whole power range efficiency of a SMPS to achieve higher efficiency, such as that required by 80 PLUS Titanium, or to improve the thermal performance of power devices in high power density power supply units.

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1 Introduction

1.1 Background and motivation

Table 1 80 PLUS Titanium efficiency requirements classification

80 PLUS efficiency requirement	115 V internal non-redundant (percent)				230 V internal non-redundant (percent)			
Load percentage	*10*	*20*	*50*	*100*	*10*	*20*	*50*	*100*
80 PLUS Platinum		90	92	89		90	94	91
80 PLUS Titanium	90	92	94	90	90	94	96	91

In recent years, the trend for SMPS has been to increase both efficiency and power density at the same time with optimized cost.

A variety of efficiency requirements, such as 80 PLUS or EuP, are defined for various SMPS. Table 1 shows two examples of efficiency requirements for non-redundant internal power supplies, i.e. the 80 PLUS Platinum and the 80 PLUS Titanium PSU classes. In the Platinum class the PSU must have a peak efficiency above 94 percent at high-line and 92 percent at low-line, while for a Titanium design these values increase to 96 percent and 94 percent, respectively. In addition, some customers may define stricter efficiency requirements based on system operating conditions.

It is obvious that the overall efficiency of the PSU depends on both efficiency levels of the PFC and of DC-DC stages. For a fixed efficiency target of the PSU, if we are able to increase PFC performance than we can relax the requirements of the DC-DC converter and vice versa. Of course, this will impact the overall cost of the system. The question of every PSU manufacturer would be: what is the optimum balance between the two stages?

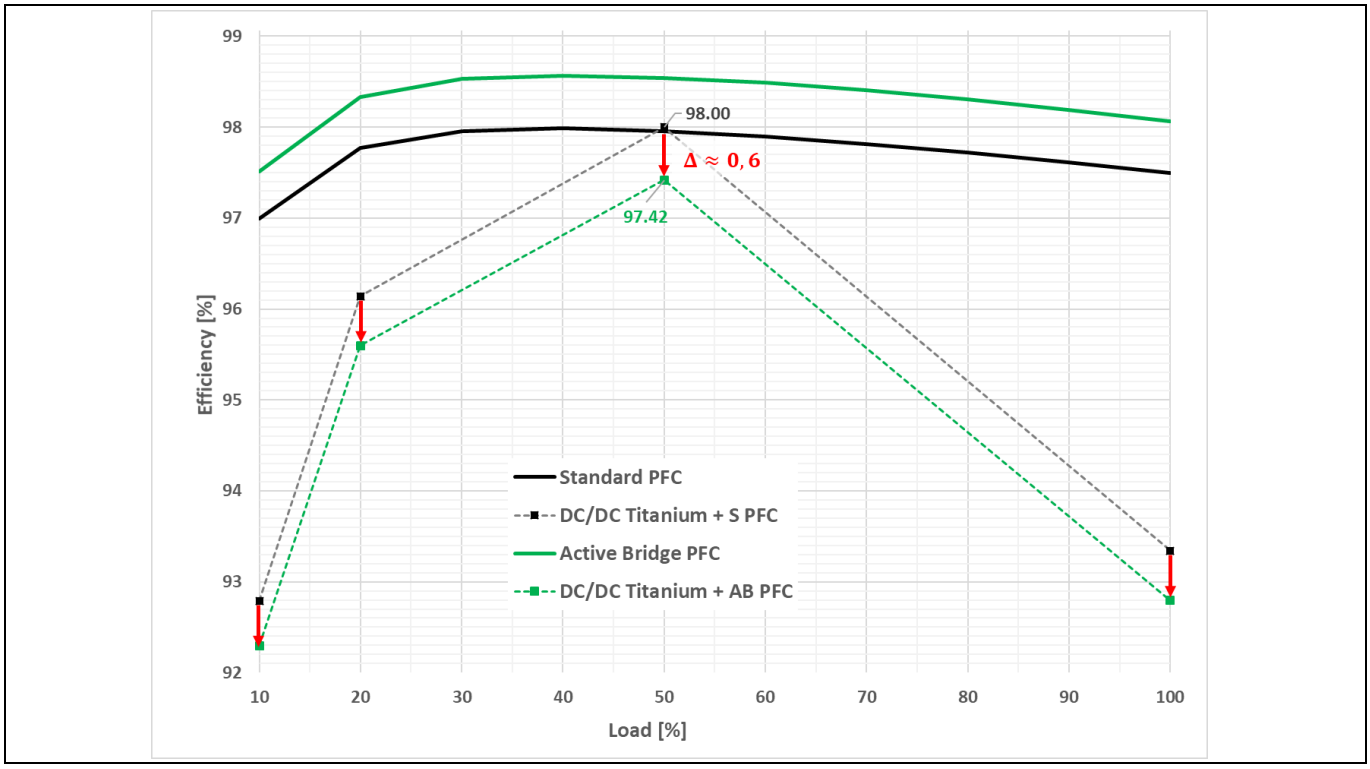


Figure 2 Reduction of DC-DC efficiency requirements for a PLUS Titanium design thanks to the active bridge (at 230 V_{AC})

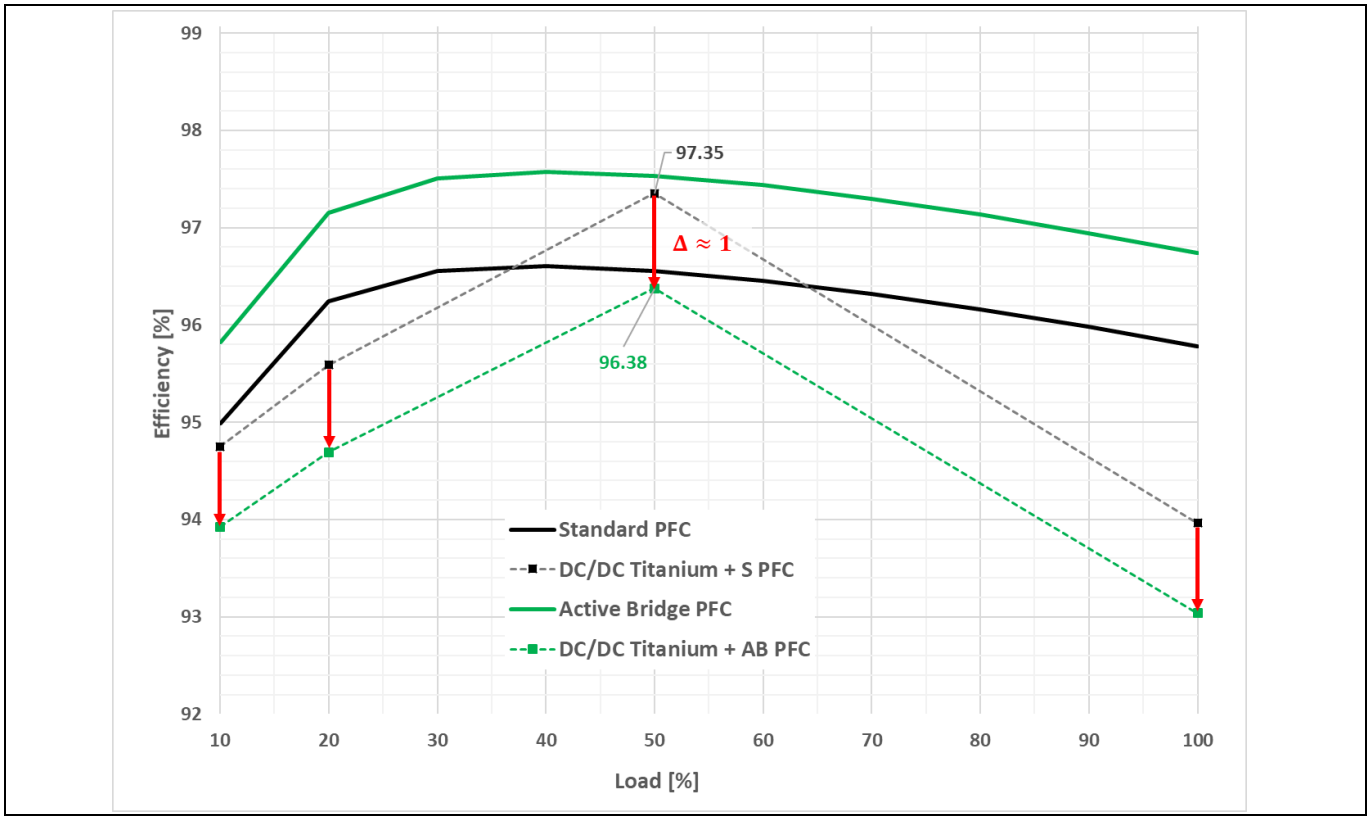


Figure 3 Reduction of DC-DC efficiency requirements for an 80 PLUS Titanium design thanks to the active bridge (at 115 V_{AC})

An easy and effective way of improving the PFC efficiency across the whole load and voltage range, without a big design impact, or increasing complexity and PFC cost, is to simply replace the classic diode bridge with an active bridge based on 600 V CoolMOS™ S7.

Figure 2 and Figure 3 clearly show the benefit of the active-bridge utilization in a standard CCM PFC. Targeting 80 PLUS Titanium efficiency, the simple replacement of the diode bridge with an active one, implemented with 22 mΩ 600 V CoolMOS™ S7, will reflect in a huge reduction of the peak efficiency that the DC-DC stage must guarantee in order to comply with Titanium class. A reduction of 0.6 percent can be seen at high-line and a reduction of 1 percent at low-line, meaning a potential increase of power density and reduction of the cost for the DC-DC stage.

The 800 W PFC developed by Infineon [1] is a good example of the achievable efficiency levels, for an 80 PLUS Platinum server design. However, if higher power is needed with the same form factor (thus increasing the power density) and even higher efficiency is required in order to achieve 80 PLUS Titanium level, the above mentioned design will no longer reach the targets.

This document introduces a 2400 W CCM PFC with active-bridge solution based on the new 600 V CoolMOS™ S7. The demo board has the same form factor as the one described in [1], meaning that the power density is three times higher. At the same time the efficiency is improved thanks to the replacement of the diode bridge with the active one. A full description of the prototype and experimental results will be presented in the following sections.

1.2 System overview

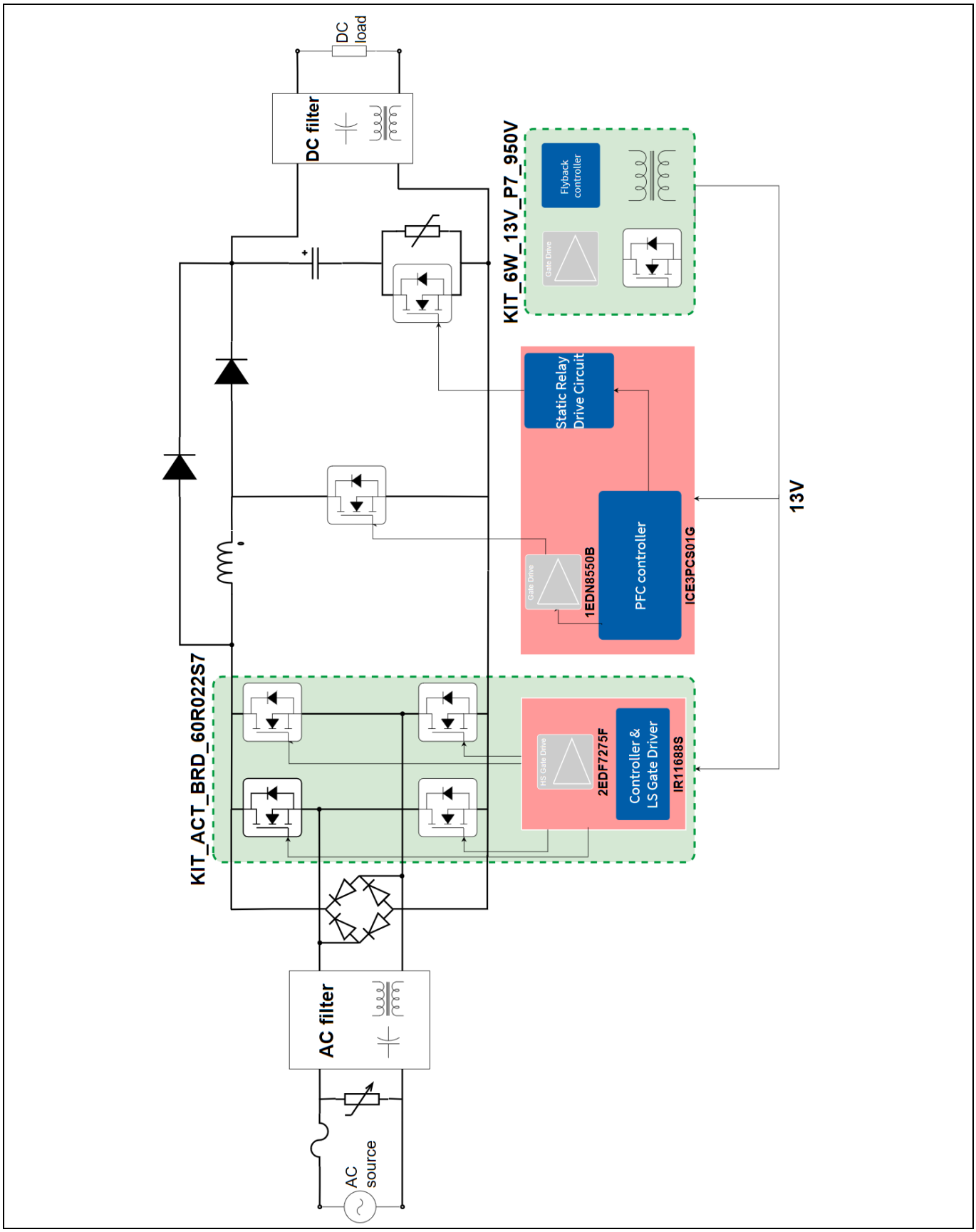


Figure 4 **2400 W active-bridge CCM PFC (EVAL_2K4W_ACT_BRD_S7) – simplified diagram showing the topology and the Infineon semiconductors used**

The simplified circuit diagram of the **EVAL_2K4W_ACT_BRD_S7** demo board is shown in Figure 4. The AC-DC converter is a 2400 W standard boost PFC working in CCM with two added features:

- Active-bridge line rectification for efficiency improvement
- Replacement of the Electro-Magnetic (EM) relay with a solid-state relay for power density increase

The active-line rectification is realized with a plug-in daughter card, named as **KIT_ACT_BRD_60R0xxS7** in Figure 4, based on the 600 V CoolMOS™ S7 in a TOLL package.

The classic bulky EM relay is replaced with a 600 V CoolMOS™ S7 (also in a TOLL package) in series with the bulk capacitor and parallelized with a NTC resistor for inrush current limitation.

The PFC stage is operated at both low-line (90 Vrms minimum, 120 Vrms nominal) and high-line (230 Vrms nominal, 265 Vrms maximum) in CCM with a 65 kHz fixed switching frequency. The bulk capacitance is designed to comply with typical hold-up time of 20 ms. The PFC controls the input AC current to a sinusoidal shape and the output DC voltage to a fixed DC value (around 390 V) by means of an easy-to-use analog controller.

The other daughter card, named as **KIT_6W_12V_P7_950V**, is employed to derive the 12 V power supply for the PFC controller, for the driving stage of the PFC switch and the solid-state relay. Finally, it is also used to supply the active-bridge daughter card.

The power supply has been designed to comply with the requirements of a data center server PFC stage targeting 80 PLUS Titanium effiency and exceeding 80 W/in^3 of power density.

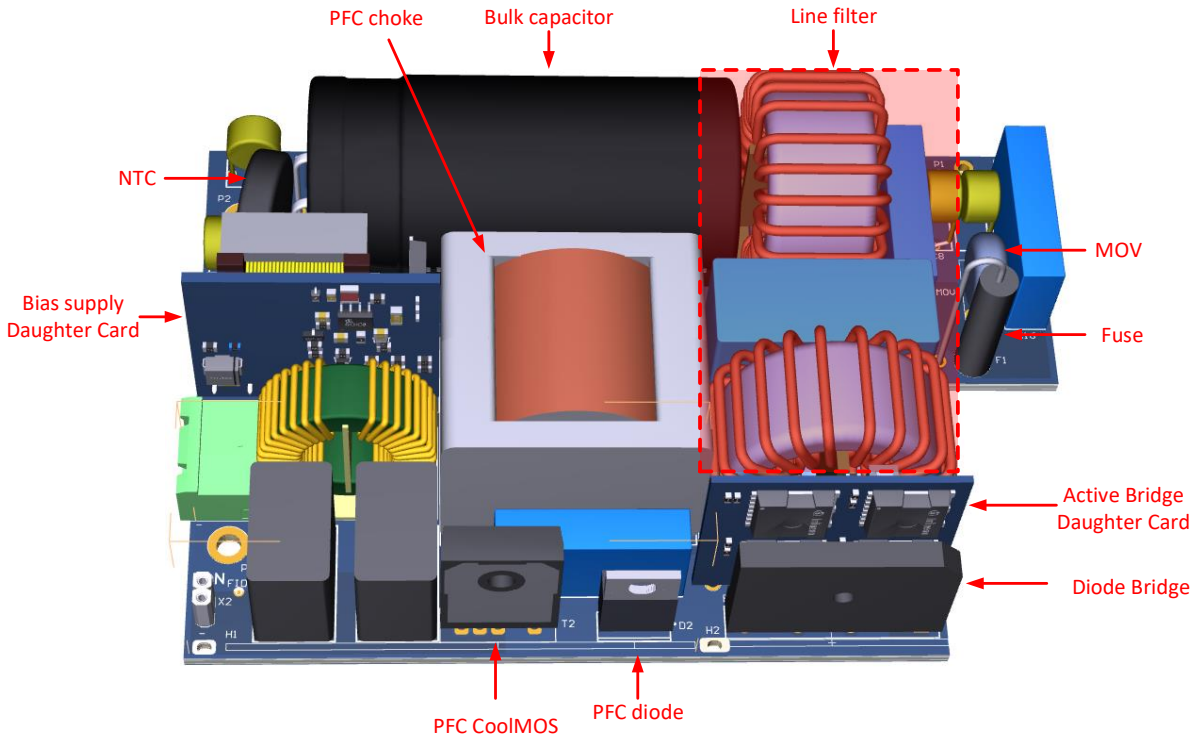
1.3 Main board description

A 3D overview of **EVAL_2K4W_ACT_BRD_S7**, highlighting the main components, is reported in Figure 5. The board is 127 mm long, with a width of 85 mm and a height of 44 mm, thus complying with the target power density.

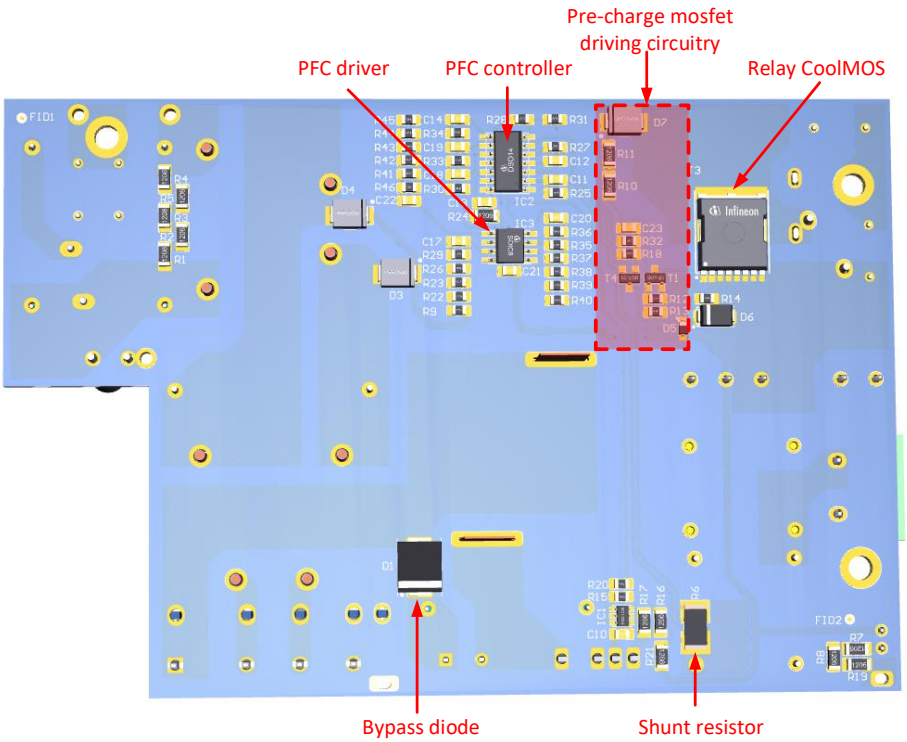
As shown by the demo board top view in Figure 5a, the design is highly compact as the placement of each component has been carefully optimized. All the Through-Hole Technology (THT) components are located on the top layer of the main PCB. The bias supply and active-bridge daughter cards can also be considered THT components.

Starting from the upper right side of Figure 5a, after the AC input connector (not visible in the 3D model), the fuse and the surge-protection Metal-Oxide Varistor (MOV) are placed together. They are followed by a two-stage EMI line filter. As already metioned in the introduction, no input EM relay is employed for the inrush current limitation circuit, because in this demo board it is realized with a different concept. The removal of the bulky relay helps to increase the power density of the system. In the lower right side of the board, the active-bridge daughter card is soldered in parallel with the diode bridge. The latter is active only during high current transients, such as inrush current and surge conditions, while during normal PFC operation it is bypassed by the active bridge. The demo board is without heatsink on the diode bridge, as shown in Figure 1, as the diode bridge is not conducting continuous current. The user anyway has the possibility to mount the bridge heatsink in case the **EVAL_2K4W_ACT_BRD_S7** is tested with unplugged active bridge for efficiency comparison purposes. In the center part of the board we can find the PFC choke followed by the PFC diode (650 V CoolSiC™ Schottky G6) and PFC MOSFET (600 V CoolMOS™ C7). These two devices are instead cooled through a proper heatsink (removed for simplicity in Figure 5a but visible in Figure 1). Moving to the upper left side, the bulk capacitor is positioned horizontally in order to maximize component density. In series to it we find the NTC resistor, used for inrush current limitation. The bias supply daughter card is placed together witht the output EMI filter and DC connector (element in green).

The bias converter generates the required supplies for the driving and control circuitries. Furthermore, it offers the possibility of supplying the fan externally, not visible in Figure 5a. All the SMD components are located on the bottom layer, as shown in Figure 5b.



a) Top view



b) Bottom view

Figure 5 Placement of the different components in the 2400 W active-bridge CCM PFC with Infineon 600 V CoolMOS™ S7 MOSFET

Starting from the upper right side of Figure 5b, the solid-state relay, implemented with a 600 V CoolMOS™ S7 in a TOLL package, is placed together with its driving circuitry. The latter will be discussed in detail in the surge pulse section, because it has been optimized for that condition. After the relay circuit, we can find the PFC analog controller (ICE3PCS01G) and the PFC MOSFET driver (1EDN8550B). On the bottom of Figure 4b, another two important elements are highlighted: the shunt resistor, used for PFC current control, and the bypass diode, active during surge transients.

1.4 Daughter card description

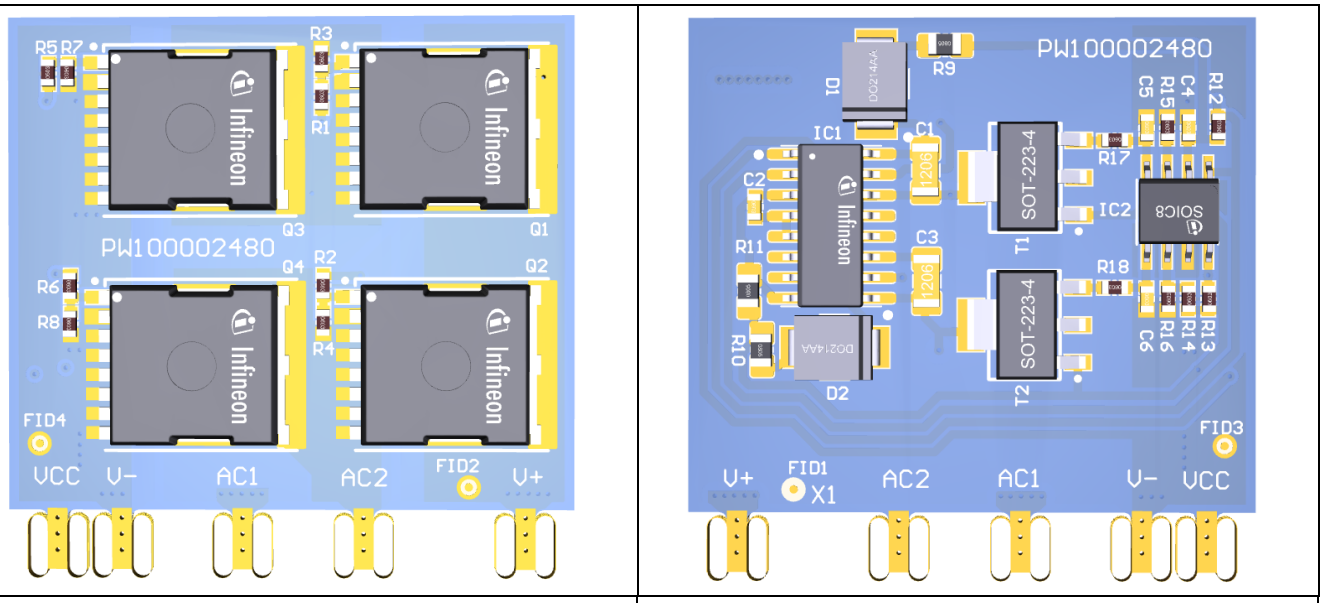
1.4.1 Active bridge

The active bridge daughter board is presented in Figure 6. The board is 35 mm long, with a width of 6 mm and a height of 30 mm, comparable to the size of a standard diode bridge rectifier (20 mm x 30 mm x 4.6 mm). This daughter board has five pins:

- Line (AC1) and neutral (AC2) alternate inputs
- Positive (V+) and negative (V-) rectified outputs
- Bias supply input (V_{CC})

The bias supply voltage of 12 V is provided by the PFC main board or by an external power supply, considering that the same V_{CC} is also used to supply PFC control and driving stages .

The daughter card integrates the power devices, the control and the driving components, thus enabling a high power density design. The power devices in a TOLL package are placed on the top side together with the gate resistors, as shown in Figure 6a. Furhter srink of the board size is limited by safety distances among traces and components. On the bottom side, the controller (IR11688S) and the high-side MOSFETs driver (2EDF7275F) are placed as shown in Figure 6b. Additional components are: bootstrap R-C-D networks for high-side MOSFET driving and small-signal transistor in SOT-223 for extending the voltage capability of the controller. Wihout any additional transistor, the IR11688S drain voltage sense capability would be limited to 200 V. More details about the control of the active bridge will be discussed in the next subsection.



a) b)

Figure 6 Placement of the different components in the active-bridge daughter card with Infineon 600 V CoolMOS™ S7 MOSFET: a) top view and b) bottom view

1.4.1.1 Control method of the active-bridge line rectifier

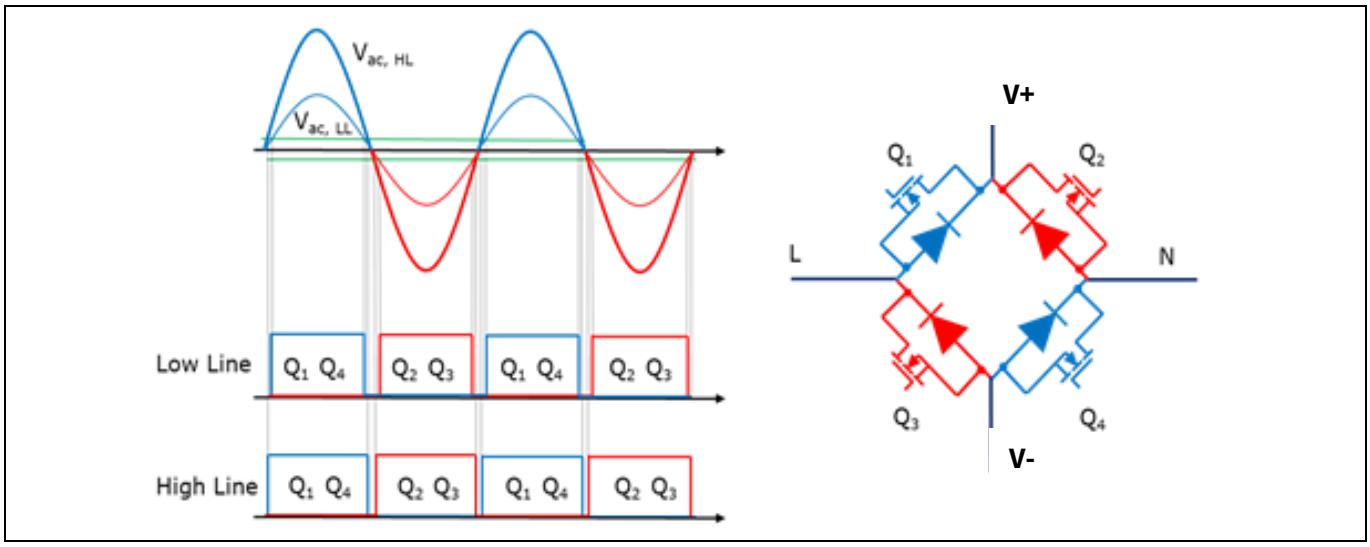


Figure 7 Control concept of the active-bridge line rectification

Control of an active bridge for line rectification is intuitive. As shown in Figure 7, during the positive half-cycle of the mains, Q1 and Q4 are supposed to be switched on, while the others are kept off. Instead, during the negative half-cycle of the AC-grid, Q3 and Q2 are supposed to conduct, while the others are off.

It's important to highlight that all the MOSFETs are always conducting in the so-called "reverse mode" or "diode mode", with a positive current flowing from the source to the drain. In fact, the active bridge's purpose is to take over the conduction of the diode in order to achieve better efficiency, since MOSFET conduction losses are lower than those from diodes.

There are two possible ways of controlling the active-bridge switches:

1. By measuring the input voltage V_{AC}
2. By sensing the voltage drop across the MOSFET V_{DS}

In the *first method*, the control signal for each MOSFET of the active bridge is obtained by comparing the instantaneous input voltage (properly scaled down through a resistive divider) with a fixed reference voltage threshold (Figure 8). The voltage divider resistance should be high enough to minimize the quiescent loss, especially at high-line input. With this method, the on-time of the control signal at each cycle strongly depends on the input voltage level. This means that a shorter on-time is obtained at low-line input and vice versa.

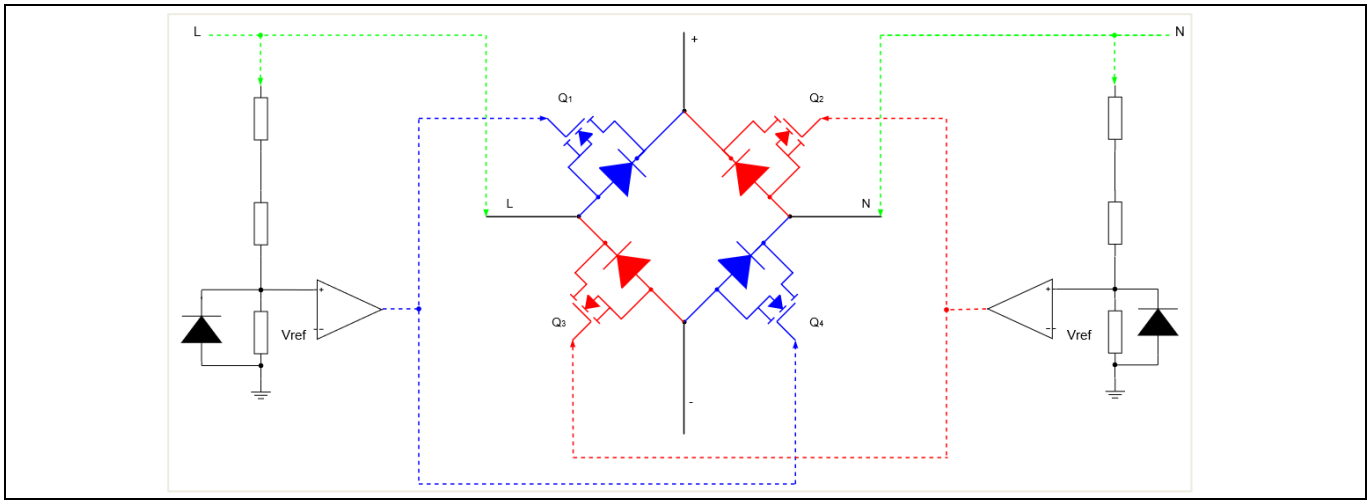


Figure 8 First control method based on measuring the input voltage

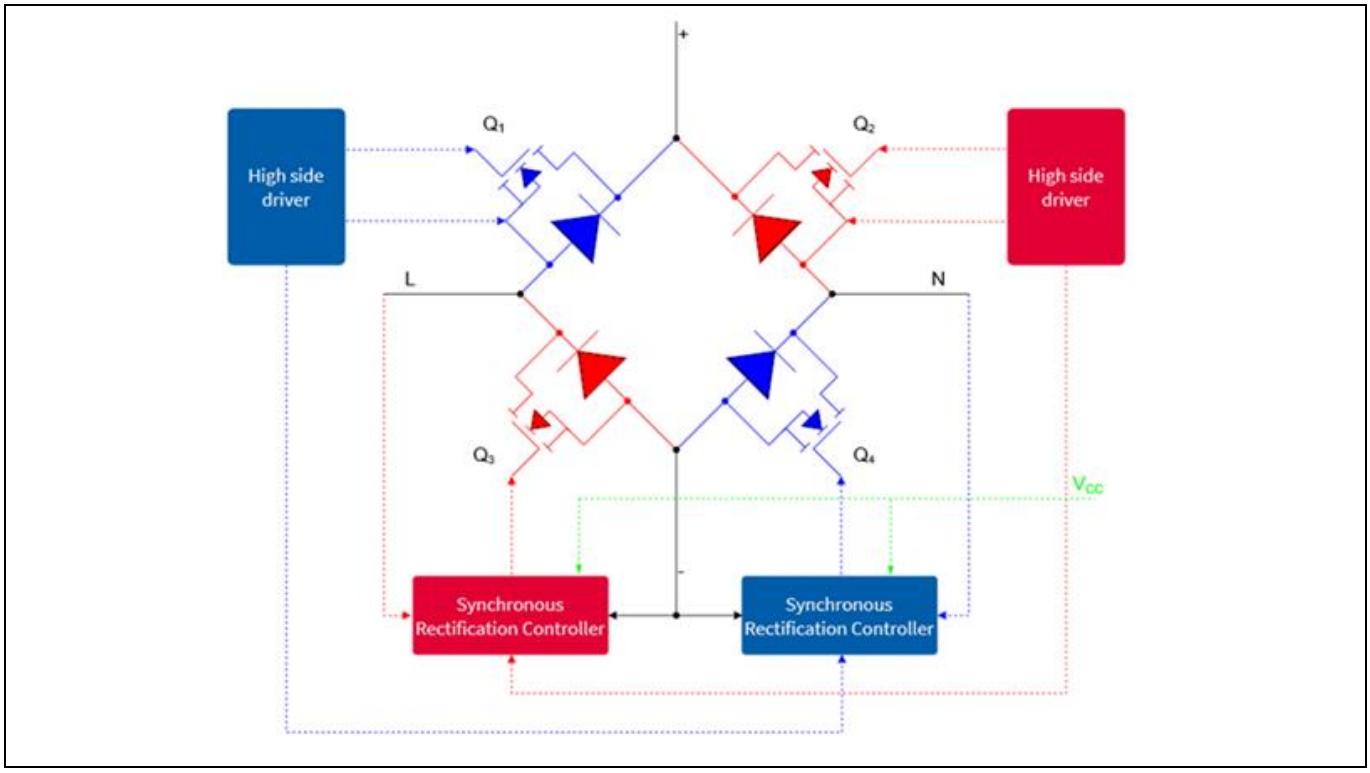


Figure 9 Second approach based on the SR controller

The *second approach* exploits the information of the current flowing through each low-side MOSFET by sensing the V_{DS} across the MOSFETs, as shown in Figure 9. This method is commonly used in the secondary-side SR controllers. Such a solution is already available in the market and is widely used in high-efficiency step-down DC-DC converters, for example for driving the SR of an LLC resonant converter.

This second method is the one employed in the proposed active-bridge daughter card by using Infineon controller IR11688S, as shown in Figure 10.

The IR11688S is a dual smart secondary-side controller IC optimized to drive two N-channel power MOSFETs configured for SR in resonant converter applications, with drain voltage sensing capability up to 200 V. Small-signal transistors T1 and T2 in Figure 10 are added to further extend the voltage capability of the controller, matching the high-line PFC application.

The drain-to-source voltage of the low-side MOSFET (Q3, Q4) of the active bridge is sensed through the VD1 and VD2 pins to determine the source-to-drain current and consequently turn on/off each gate rapidly at the start/end of each conduction cycle. The drain-to-source voltages are compared to different thresholds to precisely control the gates, as shown in Figure 11a.

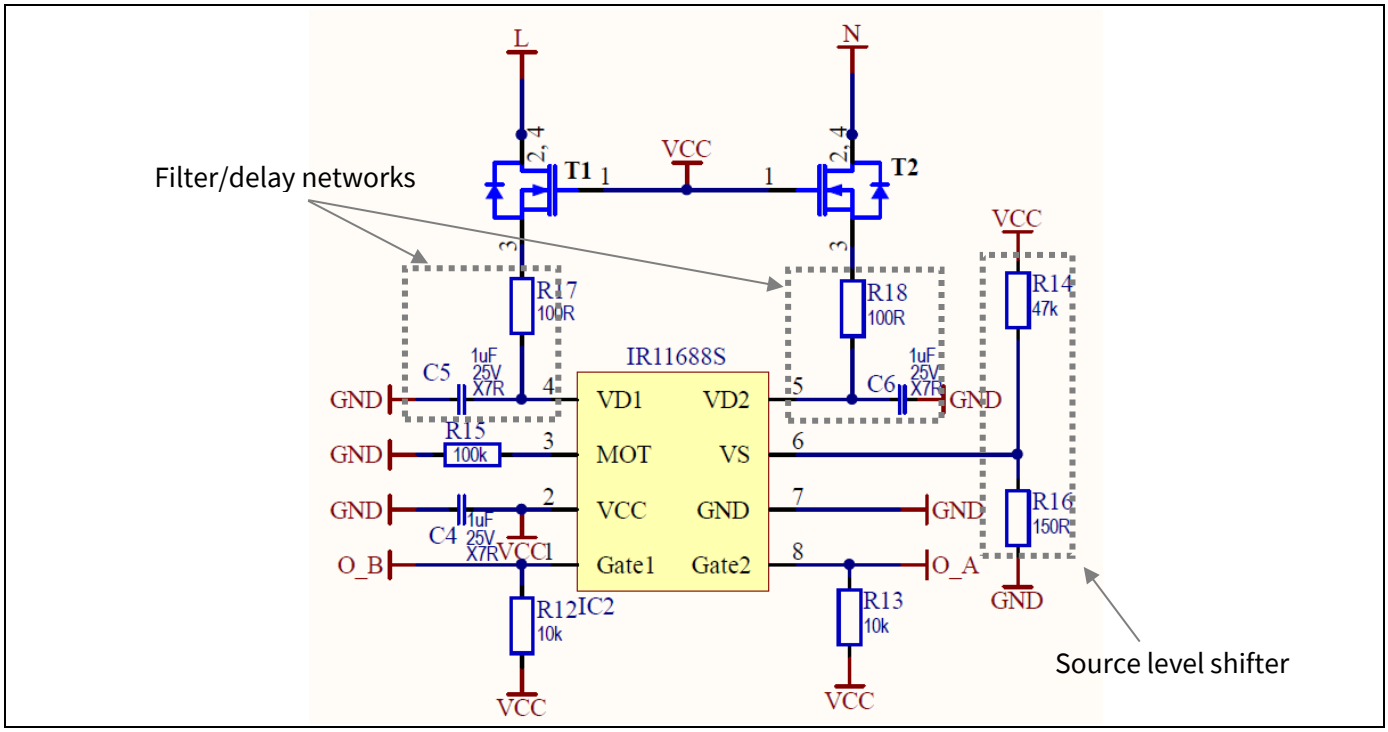


Figure 10 Adaptation of IR11688S for active-line rectification

Turn-on blanking time

When the conduction phase of each active full-bridge MOSFET begins, the active MOSFET is still off, therefore the current starts to flow through the body diode, producing a negative V_{DS} voltage across it, as shown by the blue line in Figure 11b. The body diode's voltage drop is sufficient to trigger the turn-on threshold VTH2 (≈-230 mV). If V_{DS} remains below VTH2 for more than T_{Don} (≈150 ns), the gate of the corresponding active MOSFET is driven high, which causes V_{DS} to reduce rapidly to $I_D * R_{DS,ON}$. The internal delay timer will be reset if V_{DS} rises above VTH2 before T_{Don} times out. This turn-on blanking time represents the body diode conduction time and helps to avoid mis-firing that could be triggered by high-frequency ringing in Discontinuous Conduction Mode (DCM) operation. For fixed-frequency 50/60 Hz PFC applications this means very high duty cycle for the active bridge, regardless of working at low- or high-line.

Minimum on-time

The voltage drop at the gate turn-on is usually accompanied by some amount of ringing, which could potentially trigger the input comparator to turn off the gate drive very quickly. However, the Minimum On-Time (MOT) blanking period prevents this. For fixed-frequency 50/60 Hz PFC applications the MOT is rather to be set to the highest possible value, through the value of R15 of Figure 10. This results in $T_{MOT} = R_{MOT} * 2 * 10^{-11} + 20ns \approx 2us$.

Regulation phase

At the end of the MOT, the gate output is no longer driven high and reverts to a high impedance state. When V_{DS} is below the regulation threshold V_{THR} (≈-40 mV), a weak pull-down gradually discharges the gate voltage held by the active-bridge MOSFET input capacitance. As the gate voltage drops, the MOSFET channel resistance increases as it enters the linear region. This causes V_{DS} to once again exceed V_{THR} so that weak pull-down will cease until the conduction current falls to the point where V_{DS} again drops below V_{THR}.

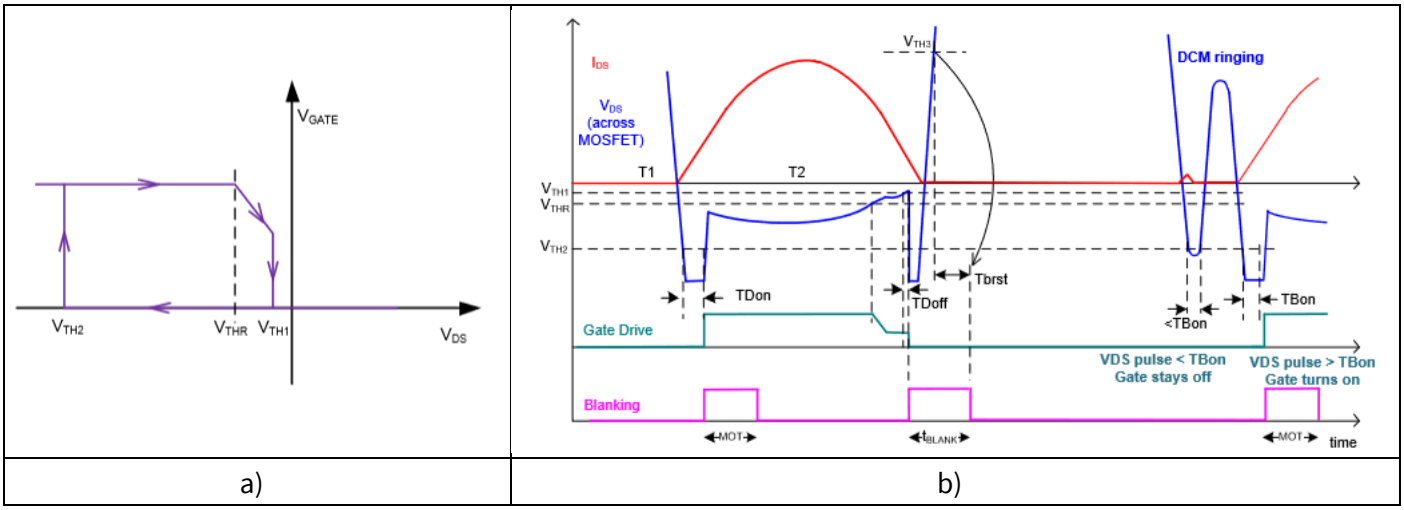


Figure 11 Behavior of IR11688S: a) input comparator thresholds and b) example of waveforms

This regulating process continues so that the conduction period is extended until the current has fallen to a very low level. In this way premature turn-off, which can arise due to parasitic inductances in PCB traces and the MOSFET package, is prevented. This period of conduction through the SR MOSFET body diodes is thereby reduced to a minimum, improving overall system efficiency.

Turn-off and reset

At the end of the switching cycle the conduction rectifier current reduces to zero so the V_{DS} voltage will cross the turn-off threshold VTH1 (≈-4 mV). When this happens the gate is driven low to switch off the SR MOSFET. Any residual current will again start flowing through the body diode, causing a negative step in V_{DS}. When this occurs V_{DS} could potentially trigger turn-on once again by crossing VTH2. To prevent this possibility, turn-on is blanked for a time period t_{DBLANK} (≈15 µs) after turn-off has occurred. The blanking time is internally set and can be reset only when V_{DS} crosses the positive threshold VTH3 (≈1.18 V). Reset occurs only when V_{DS} remains higher than VTH3 for more than the reset blanking time, t_{BRST} (≈400 ns). This protects against false triggering due to ringing after the turn-off phase. Once reset the IR11688S is re-armed so that turn-on may be triggered for the next conduction cycle.

Reset VTH3 and regulation VTHR thresholds are referenced to GND (see [3]), therefore they cannot be changed by any circuit modification. On the other hand, turn-on VTH2 and turn-off VTH1 thresholds are referenced to VS, thus giving the designer freedom to change them by adapting the resistor-divider (named as “Source level shifter” in Figure 10). In our example we are shifting the VS voltage of around 40 mV. This VS offset has to be adapted depending on the MOSFET $R_{DS,ON}$ and the application.

The IR11688S has very low quiescent current when the gate drivers are not switching to offer minimal power consumption in standby mode (less than 500 µA).

1.4.1.2 Active-bridge steady-state waveforms

Figure 12 shows the steady-state waveforms of active-bridge low-side complementary driving signals during PFC operation at high-line.

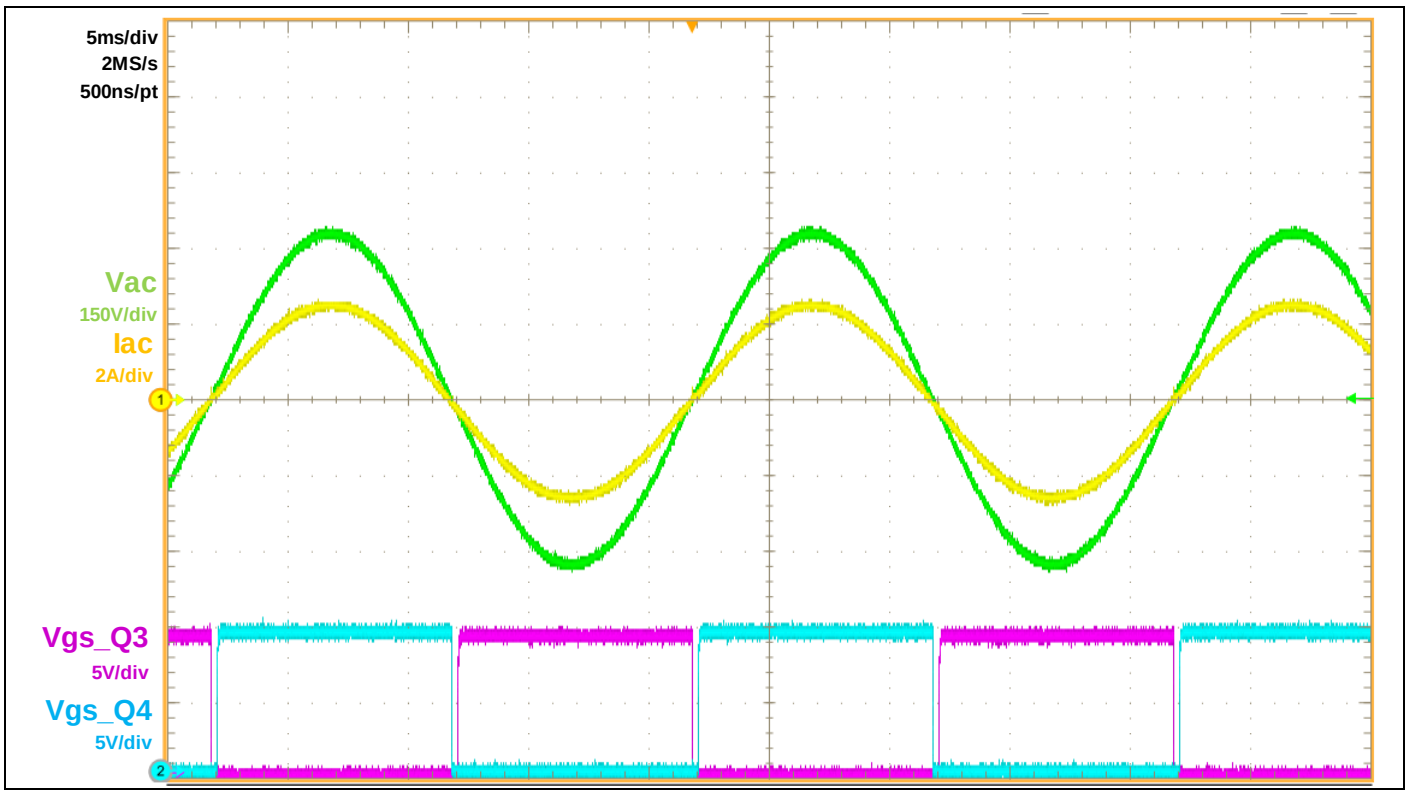


Figure 12 Steady-state waveforms of active-bridge low-side complementary driving signals (magenta and light blue lines), input current and voltage (yellow and green lines) and PFC output voltage (light blue line) at 230 V_{AC}

1.4.2 Bias power supply

For details of the bias power supply daughter card please refer to [2].

1.5 Board specification

Table 2 presents the specification of the 2400 W active-bridge PFC developed using the 600 V CoolMOS™ S7 in a TOLL package.

Table 2 Summary of specifications and test conditions for the 1600 W PSU

Parameter	Condition	Specification
Input voltage range		90 to 265 Vrms
Nominal input voltage at low-line		115 Vrms
Nominal input voltage at high-line		230 Vrms
AC-line frequency range		45 to 65 Hz
Max. ambient temperature		40°C
Max. input current	90 V_{AC}/1200 W	14 Arms
Inrush current	230 Vrms, 50 Hz/60 Hz, measured on the first AC cycle	I_{in_peak} less than 30 A
Power Factor (PF)	More than 20 percent of load	More than 0.95
Hold-up time	P_{out_max} = 1800 W/V_{out_min} = 311 V	10 ms
Nominal output voltage		390 V
Max. output power	230 V_{AC}	2400 W
Peak efficiency at high-line	230 V_{AC}	More than 98.6 percent
Peak efficiency at low-line	115 V_{AC}	More than 97.6 percent

2 PFC efficiency increase with active bridge

2.1 Theoretical efficiency improvement with active bridge

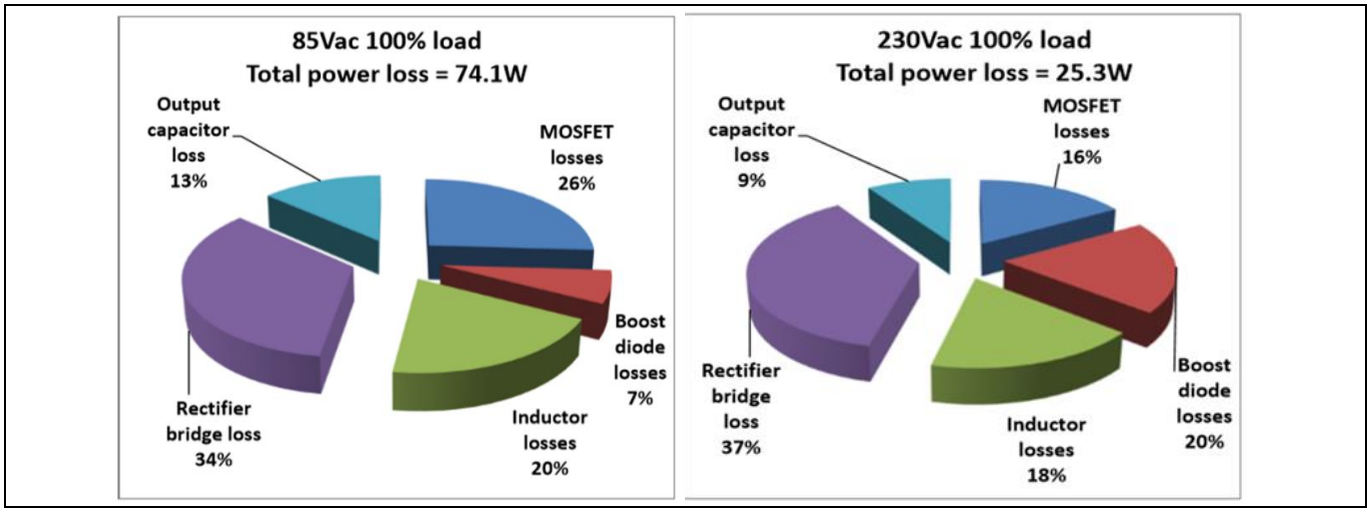


Figure 13 Power dissipation of power devices with a 1000 W PFC circuit at 85 V_{AC} and 230 V_{AC}

A SMPS, with traditional PFC and an efficient enough DC-DC converter, can quite easily meet the 80 PLUS Platinum efficiency requirements. In order to achieve greater efficiency, such as 80 PLUS Titanium, maintaining the same circuit structure with some efficiency improvements will not be sufficient. By only replacing the power components with better ones, for example using a MOSFET with lower $R_{DS,ON}$ or an inductor with less core material loss, it is almost impossible to achieve adequate efficiency improvements in the whole voltage and load range.

Figure 13 shows the power losses of main components in a 1000 W standard PFC circuit. The bridge rectifier's power dissipation dominates among power losses, regardless of low-line or high-line input voltage.

Reducing the power dissipation of a bridge rectifier is the simplest and most effective way to improve efficiency. In the following section, a comparison between conduction losses of diodes and active bridges is described in detail.

2.1.1 Formula for calculating the conduction loss of bridge diodes and MOSFETs

The advantage of active-bridge line rectification for power supply is not only to improve the efficiency from light load to full load, but also to reduce the temperature of the power device. To estimate the efficiency improvement achieved by active-bridge line rectification, the power dissipation of a bridge rectifier and power MOSFET needs to be calculated first.

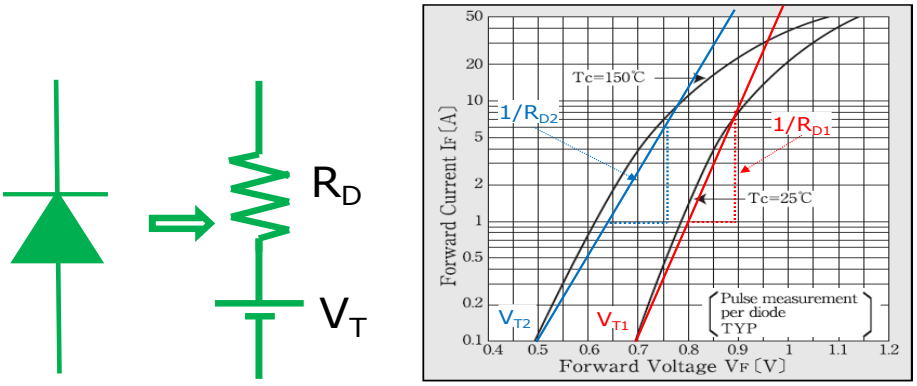
The equivalent diode circuit is derived as a DC potential, V_T, in series with an equivalent resistance, R_D, as shown in Figure 14. The formula for conduction loss of the diode is:

$$P_{con} = V_T \times I_{D,avg} + I_{D,rms}^2 \times R_D(@specified\ T_J)$$

Where $I_{D,avg}$ and $I_{D,rms}$ is the average current and effective current of the diode, respectively.

Moreover, the MOSFET can be modeled as a resistance, which is the $R_{DS,ON}$ at a specified junction temperature. The conduction loss of the MOSFET can be calculated by:

$$P_{con} = I_{D,rms}^2 \times R_{DS,ON}(@specified\ T_J)$$

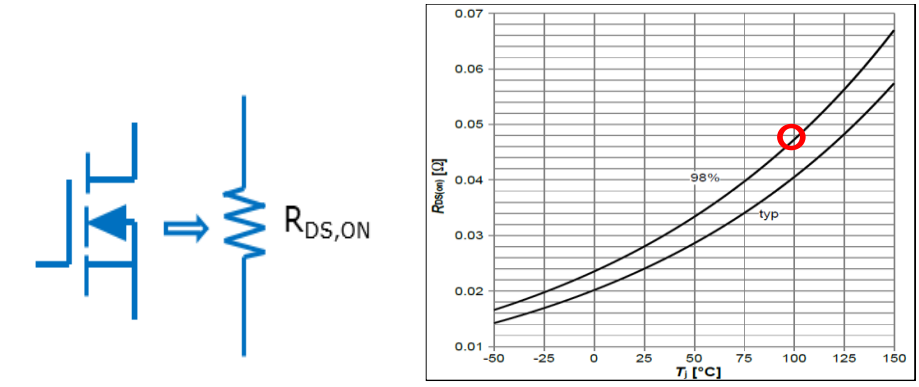


$$P_{con,diode} = V_T \times I_{D,avg} + I_{D,rms}^2 \times R_D(@specified\ T_J)$$

Figure 14 The equivalent circuit and the conduction loss of the diode

Theoretically, it is simple to calculate the power loss improvement by subtracting the power dissipation of the MOSFET from that of the bridge rectifier. The efficiency improvement can be obtained from the power loss reduction at different load conditions. However, it is not simple in real calculations for the following reasons:

a. The equivalent circuit of diode power dissipation is considered as DC potential in series with an equivalent resistance. However, these two parameters are not fixed and change along with the temperature and current of the diode. The curves at all of the possible temperatures are not provided by the manufacturers. In most cases, only curves at 25°C and 150°C are found in the data sheet.
b. The $R_{DS,ON}$ of the MOSFET varies along with its junction temperature and current. However, the PCB parasitic resistance cannot be ignored when using an extremely low $R_{DS,ON}$ device (such as 10 mΩ), which makes it difficult to estimate the power dissipation on active-bridge line rectification.



$$P_{con} = I_{D,rms}^2 \times R_{DS,ON}(@specified\ T_J)$$

Figure 15 The equivalent circuit and the conduction loss from $R_{DS,ON}$ of the power MOSFET

2.1.2 PFC efficiency estimation with active bridge

Figure 16 and Figure 17 present the efficiency simulated curves as a function of the output load for a standard PFC with active-line rectification at high- and low-line respectively. Moreover, an efficiency comparison is done between the PFC solution without and with active bridge using different $R_{DS,ON}$, i.e. 22 mΩ, 40 mΩ and 65 mΩ. Estimation of bridge losses is done using the formula described in previous subsection. Simulation results can then be compared to experimental measurements of the next section in order to understand the limits of the model.

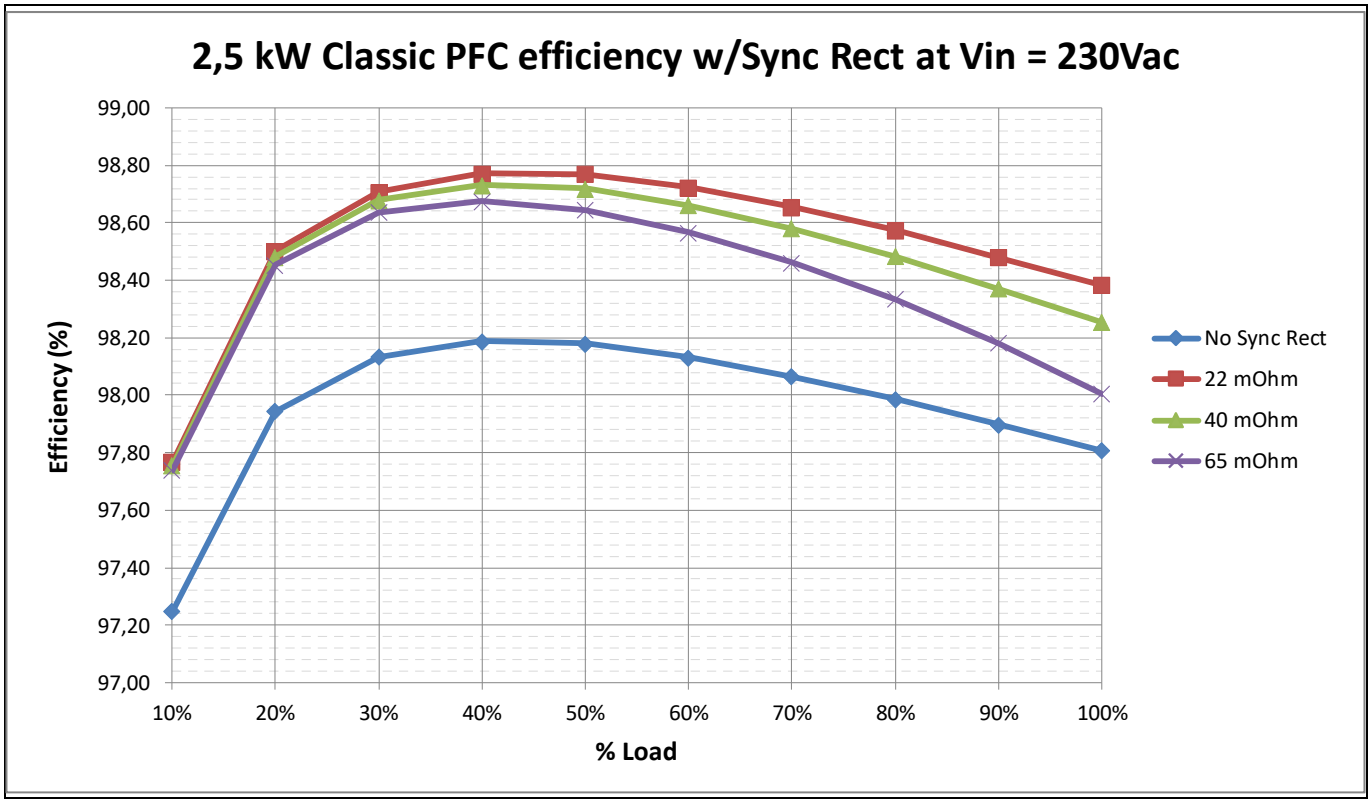


Figure 16 **Simulation results with (22 mΩ, 40 mΩ, 65 mΩ) and without active-bridge line rectification at high-line**

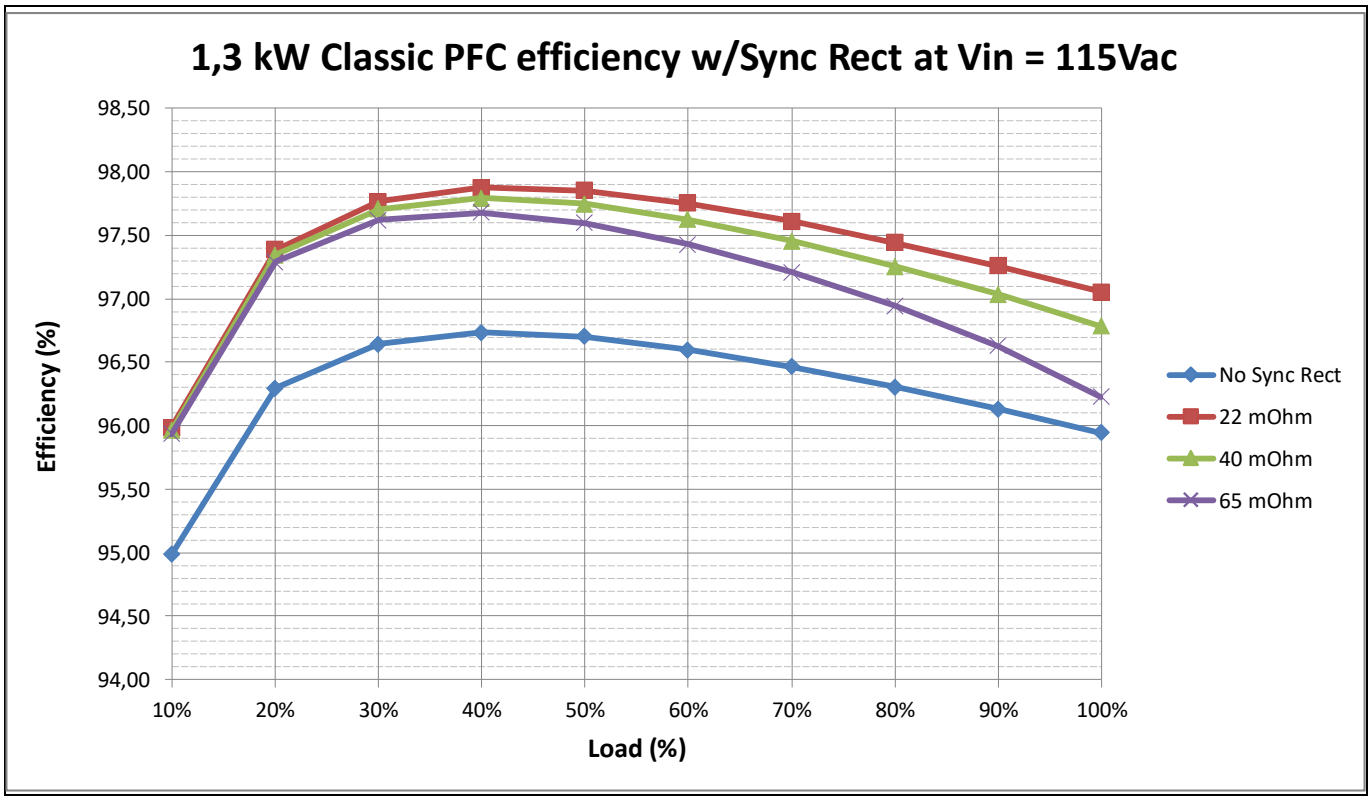


Figure 17 **Simulation results with (22 mΩ, 40 mΩ, 65 mΩ) and without active-bridge line rectification at low-line**

2.2 PFC efficiency measurements with active bridge

The efficiency measurements are performed on the **EVAL_2K4W_ACT_BRD_S7** using active-bridge daughter cards with different $R_{DS,ON}$, i.e. 22 mΩ, 40 mΩ and 65 mΩ, and without any heatsink attached to the bridge (even in the case that the active bridge is not plugged in). Load is changed through a DC electronic load and the output voltage is kept constant by the PFC at around 390 V_{DC}. The fan is supplied internally by the board. As a result its consumption is included in the efficiency measurements.

Results at nominal high-line voltage (230 V_{AC}) are shown in Figure 18. A peak efficiency of 98.6 percent is reached with 22 mΩ active bridge at around half load. From Figure 18 it is also evident that the PFC efficiency with the 22 mΩ active bridge is above 98 percent in almost all the load conditions, keeping a constant delta compared to the diode solution in the range of 0.4 to 0.5 percent. The 40 mΩ active bridge keeps a constant delta compared to the diode solution in the range of 0.4 percent up to half of the maximum load. The 65 mΩ active bridge is close to the one reached with the diode bridge only when the output power is around 2400 W. This means that the major benefit of this kit is given below: 50 percent of the output power.

Measurements at nominal low-line voltage (115 V_{AC}) are reported in Figure 19. A peak efficiency of 97.6 percent is reached with 22 mΩ active bridge at around half load. Similar behavior is experienced compared to high line.

Finally, Figure 20 presents the efficiency gain using the active bridges a) at high-line and b) at low-line.

A peak efficiency improvement of 1.3 percent is reached at low-line with an active-bridge line rectification of 22 mΩ MOSFET. At high-line the delta efficiency peak is around 0.7 percent.

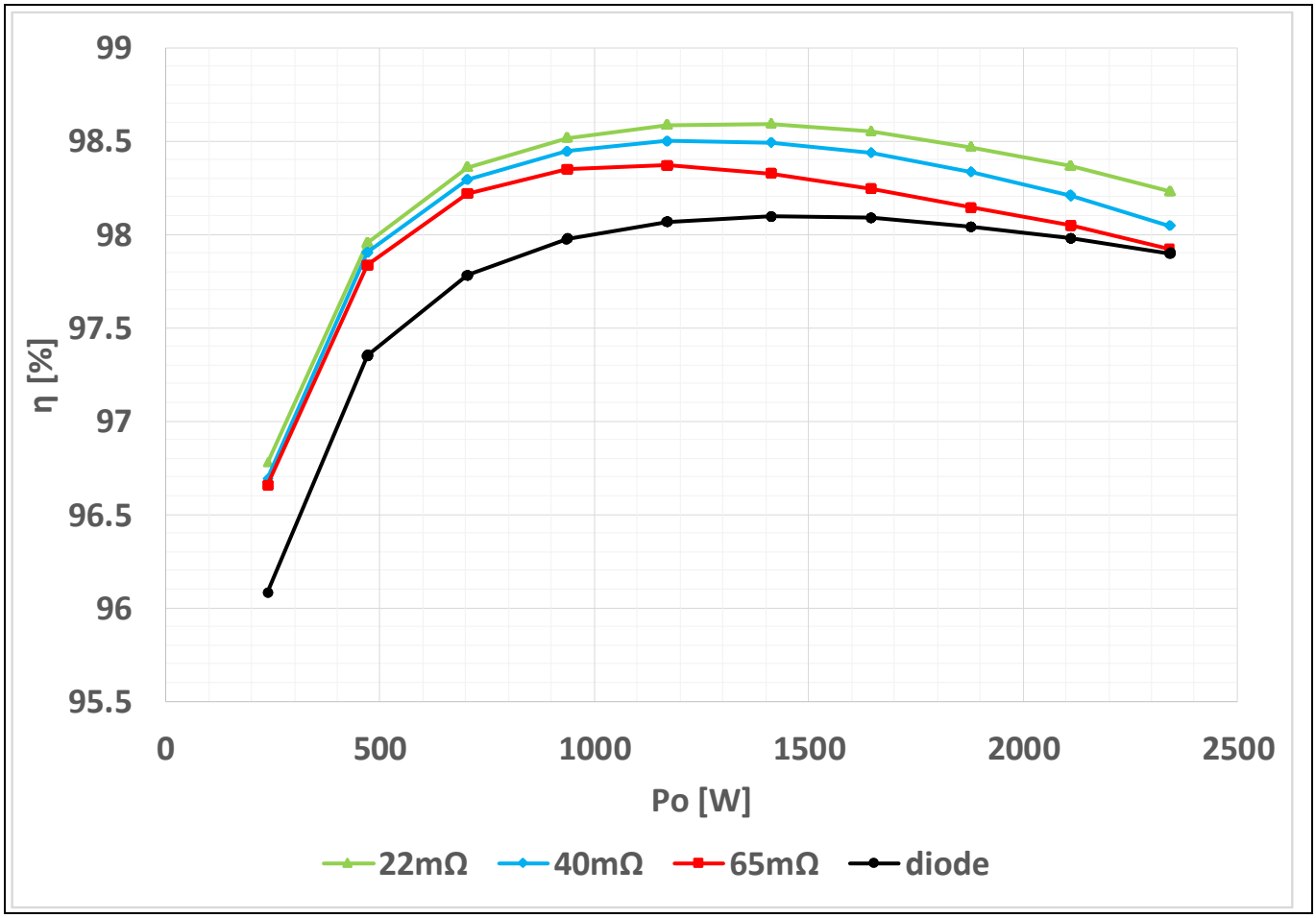


Figure 18 Efficiency test result of EVAL_2K4W_ACT_BRD_S7 with 22 mΩ (green line), 40 mΩ (light blue), 65 mΩ (red) active-bridge line rectification and with only the diode bridge (black) at 230 V_{AC}

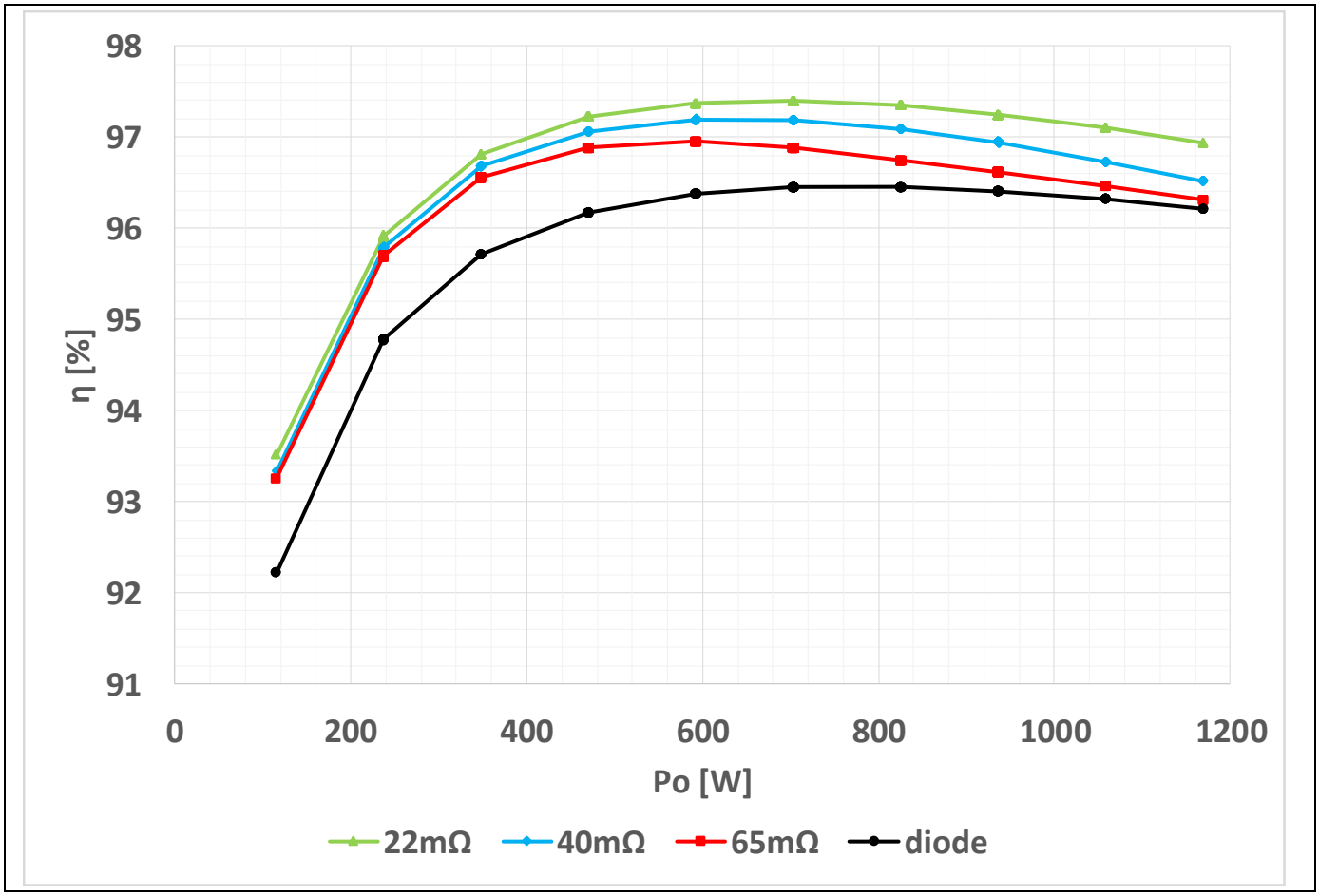
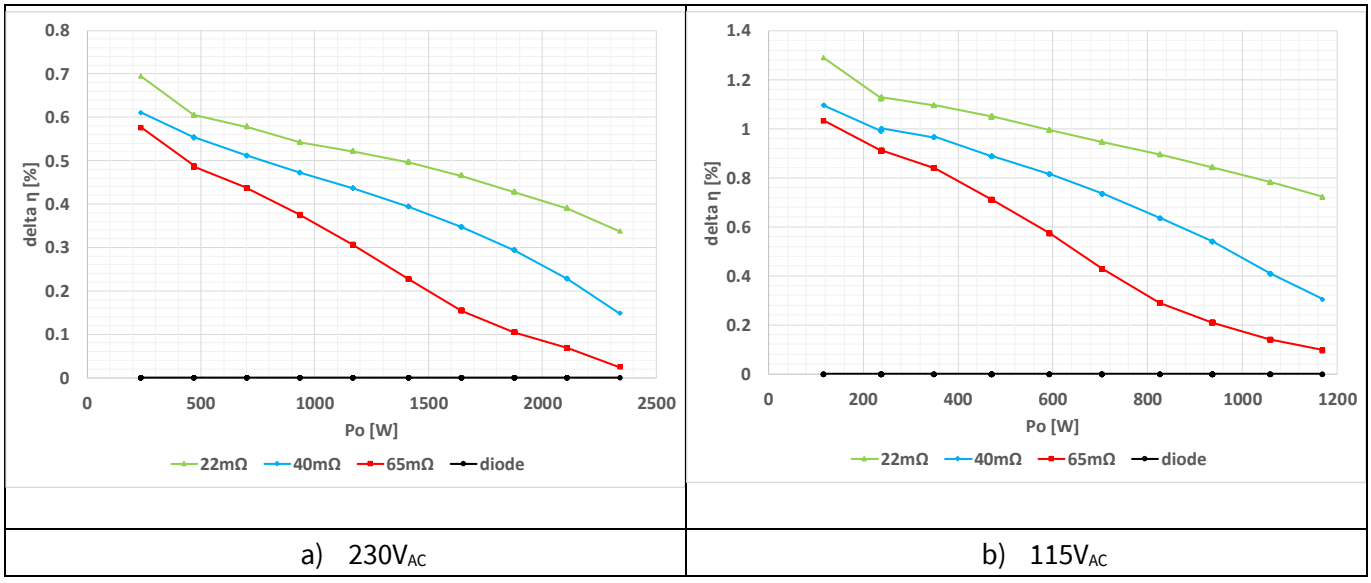


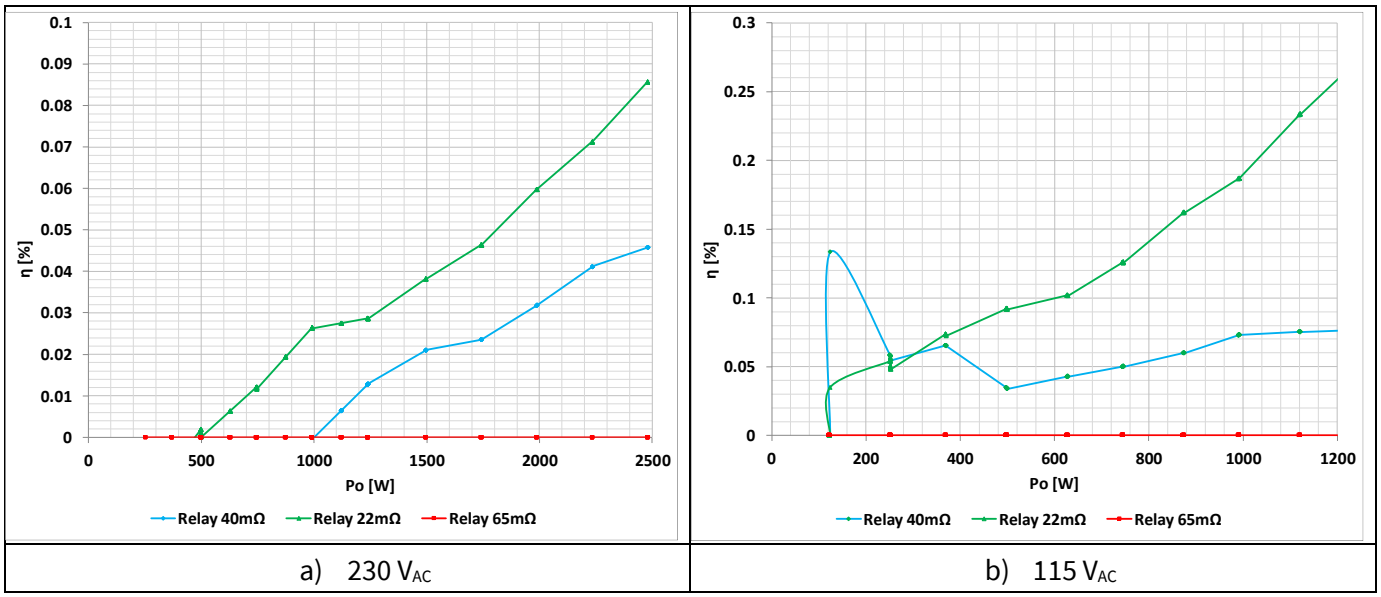
Figure 19 **Efficiency test result of EVAL_2K4W_ACT_BRD_S7 with 22 mΩ, 40 mΩ, 65 mΩ full-wave active-bridge line rectification and without active bridge (passive) at 115 V_{AC}**



a) 230V_{AC} b) 115V_{AC}

Figure 20 **Delta efficiency test result of EVAL_2K4W_ACT_BRD_S7: comparison between passive and active bridge at different $R_{DS,ON}$**

2.3 Relay MOSFET impact on PFC efficiency



a) 230 V_{AC} b) 115 V_{AC}

Figure 21 Delta efficiency test result of EVAL_2K4W_ACT_BRD_S7: comparison of relay MOSFETs with different $R_{DS,ON}$

Figure 21 shows the impact of the different solid-state relay MOSFETs on the overall PFC efficiency. Three different $R_{DS,ON}$ 600 V CoolMOS™ S7s are compared in terms of delta efficiency (taking as reference the 65 mΩ results). The experiment in Figure 21 demonstrates that, at high-line, there is a gain of around 0.08 percent of efficiency at full load by using a 22 mΩ device. The gain decreases to 0.04 percent when the device instead has 40 mΩ. At low-line, the advantage of using a lower $R_{DS,ON}$ becomes more evident: 0.25 percent increase with 22 mΩ and 0.08 percent with 40 mΩ.

Furthermore, the benefit of lower-ohmic devices is not limited to efficiency gain, but is also related to a higher current capability during transients and surges with a clear advantage for system reliability.

2.4 Temperature measurements

A long-run test has been performed with thermocouples attached to the main devices of the **EVAL_2K4W_ACT_BRD_S7** board. The test has been run for nominal input voltage (230 Vrms) as well as the minimum input voltage (90 Vrms), which is the worst case for PFC operation. The tested unit was enclosed and the fan was controlled by the bias Flyback supplied from the output voltage of the PFC. Therefore, the results presented in this section provide the thermal performance of the 2400 W active-bridge PFC with S7 MOSFETs introduced in this document at room temperature.

The monitored parts in the thermal test are:

- Ambient temperature
- Diode bridge
- Active bridge
- Heatsink: where both PFC MOSFET and diode are thermally connected to
- PFC choke
- Solid-state relay MOSFET

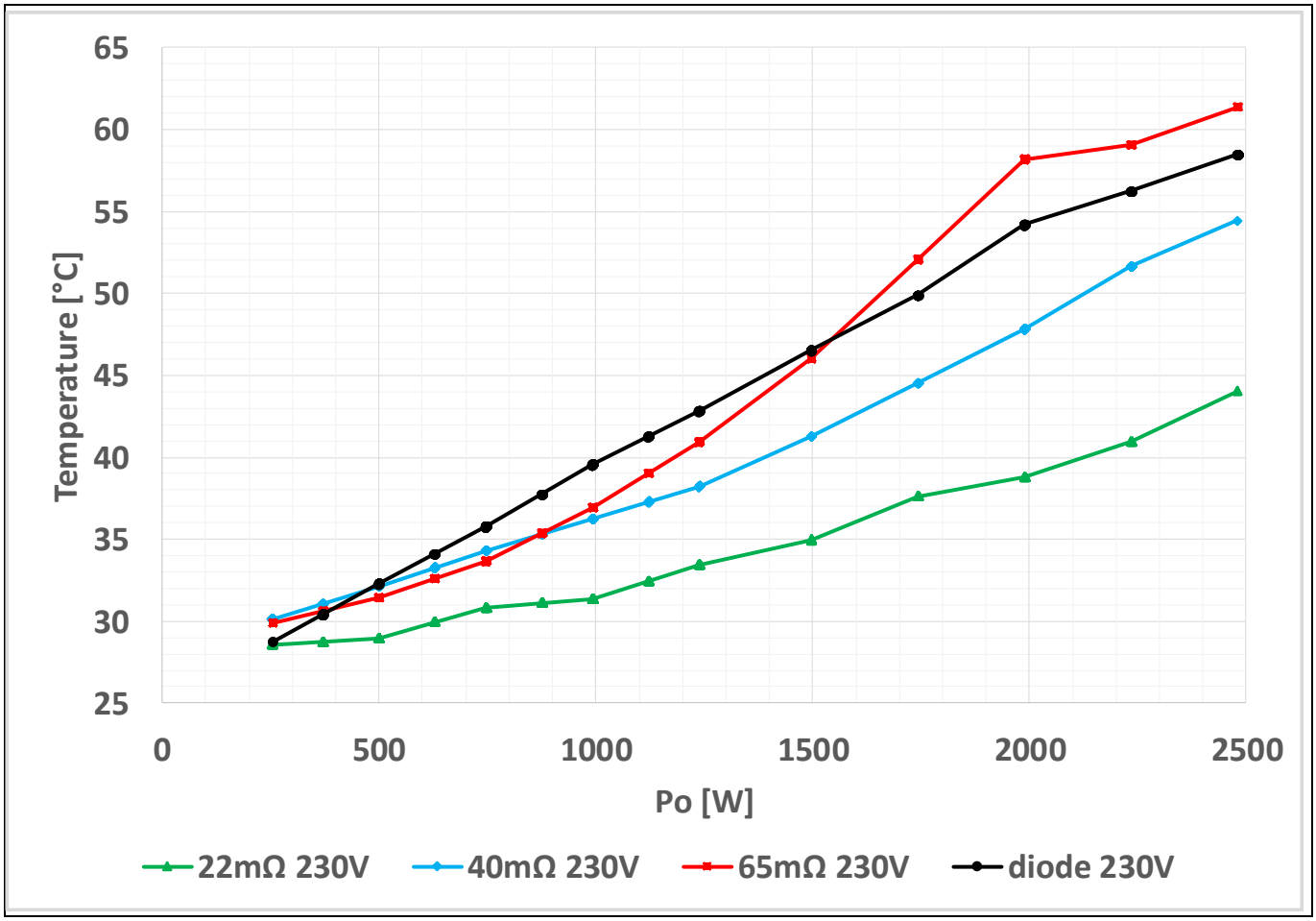


Figure 22 Bridge temperature measurements of EVAL_2K4W_ACT_BRD_S7 at nominal high-line

Figure 22 shows the temperature evolution of the bridge (passive or active) from 10 percent to 100 percent of the output power at high-line (230 Vrms). With a 22 mΩ 600 V CoolMOS™ S7, the active-bridge temperature reaches a maximum of 43°C at full power (2400 W) and room temperature. In the same conditions, 40 and 65 mΩ devices reach 54°C and 63°C respectively. These results justify the removal of the heatsink for the bridge cooling and eventually the employment of a less powerful fan. Moreover, there is enough margin in case the ambient temperature increases.

Figure 23 presents the temperature results at low-line (120 Vrms). With a 22 mΩ 600 V CoolMOS™ S7, the active-bridge temperature reaches a maximum of 55°C at 1200 W. In the same conditions, 40 and 65 mΩ devices reach 63°C and 64°C respectively. When the active bridge is removed, the temperature of the diode bridge is around 73°C.

For completeness, Figure 24 and Figure 25 report the temperature measured on the other main PFC components both at high- and low-line.

Finally, Figure 26**Error! Reference source not found.** shows an acquisition with the thermocamera at 2400 W.

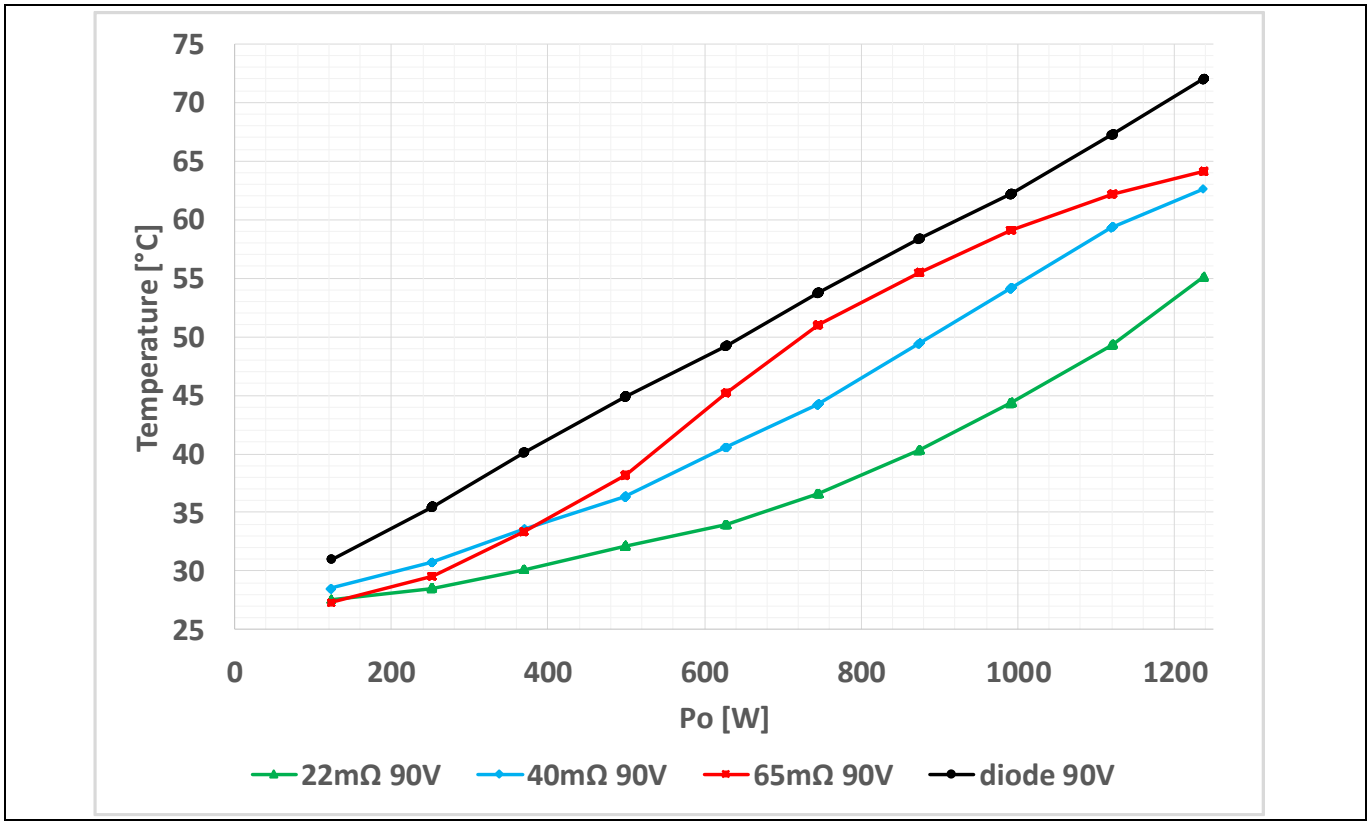


Figure 23 Bridge temperature measurements of EVAL_2K4W_ACT_BRD_S7 at minimum low-line

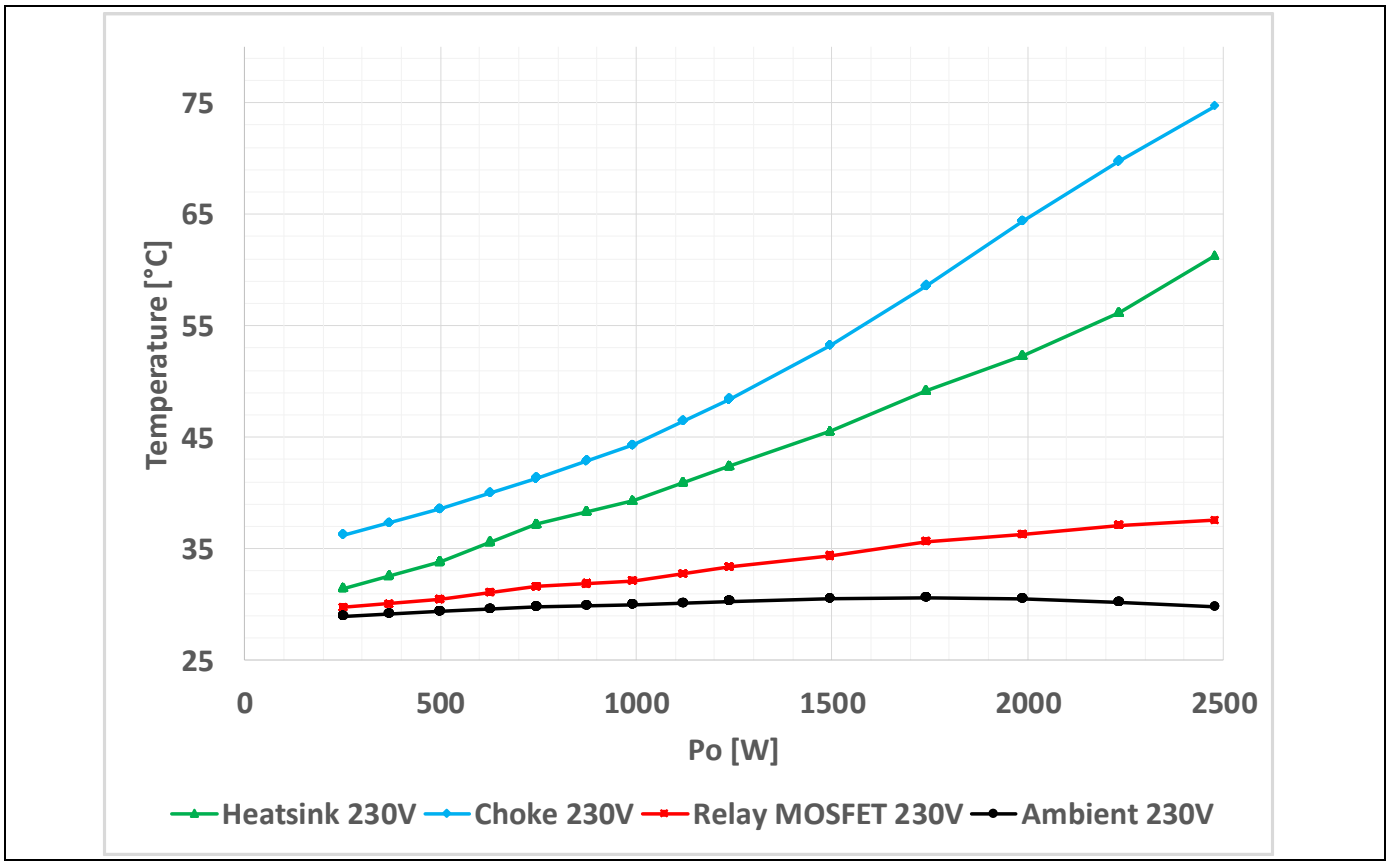


Figure 24 Other PFC devices temperature measurements of EVAL_2K4W_ACT_BRD_S7 at nominal high-line

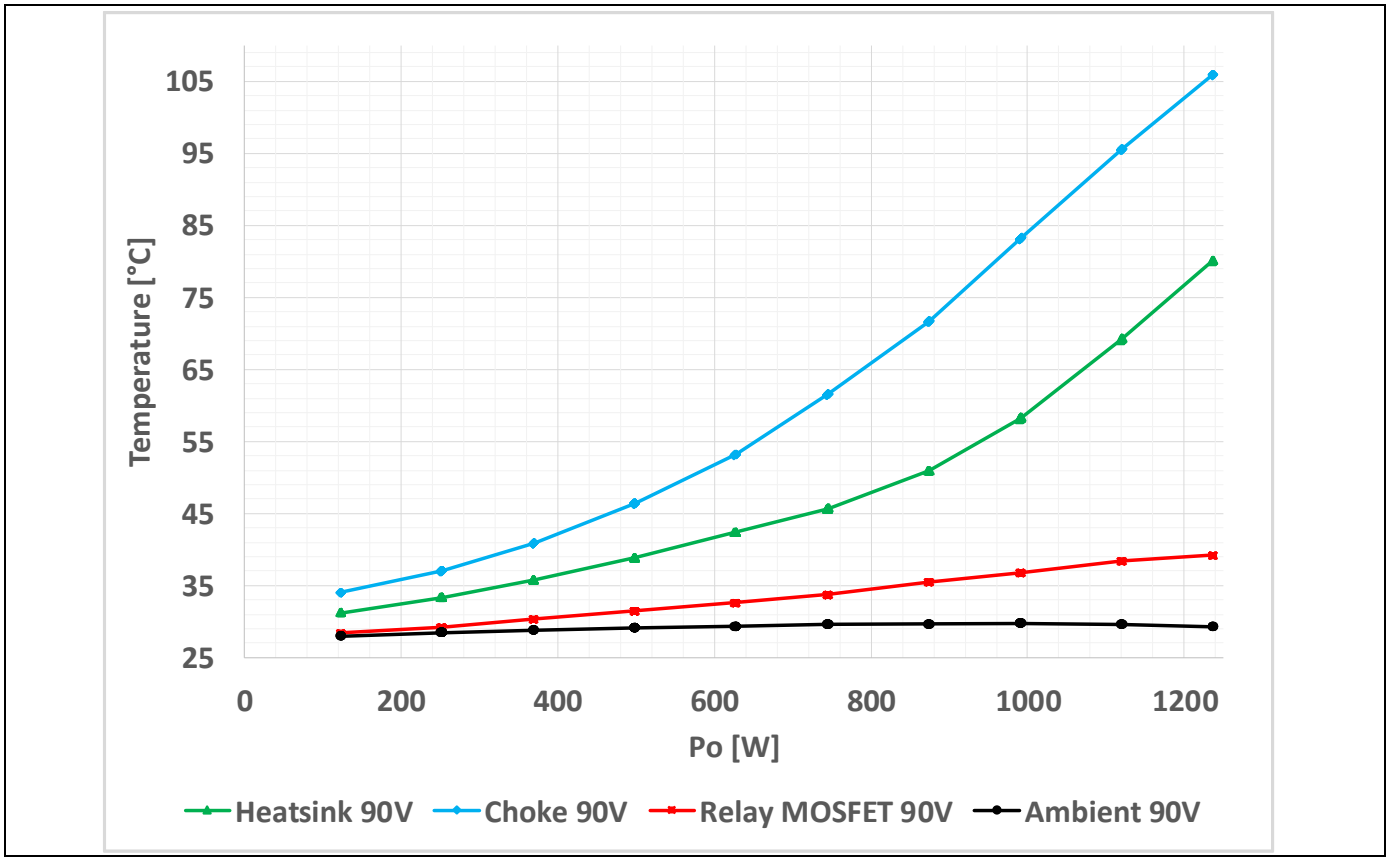


Figure 25 Other PFC devices temperature measurements of EVAL_2K4W_ACT_BRD_S7 at minimum low-line

3 DC-link pre-charge and PFC start-up

3.1 Relay replacement introduction

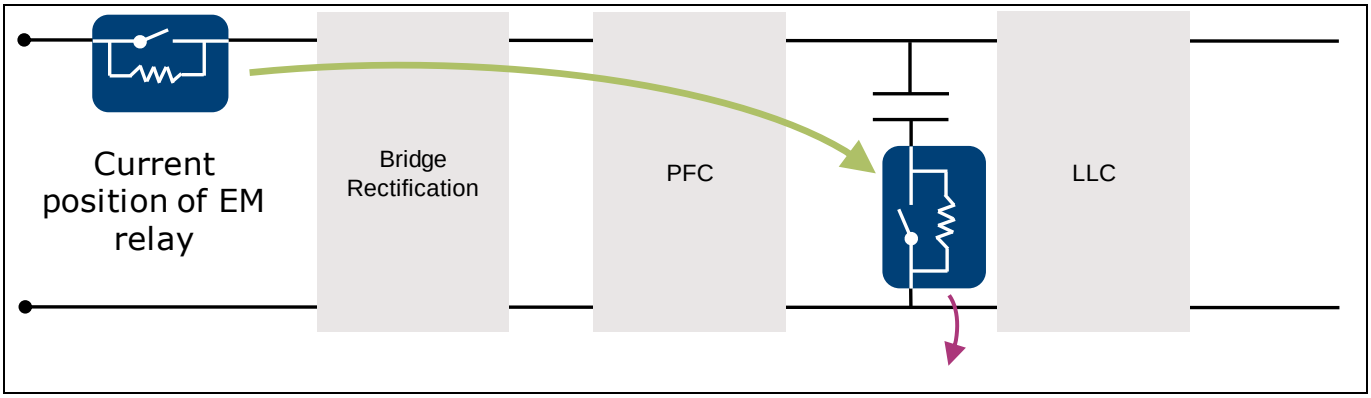
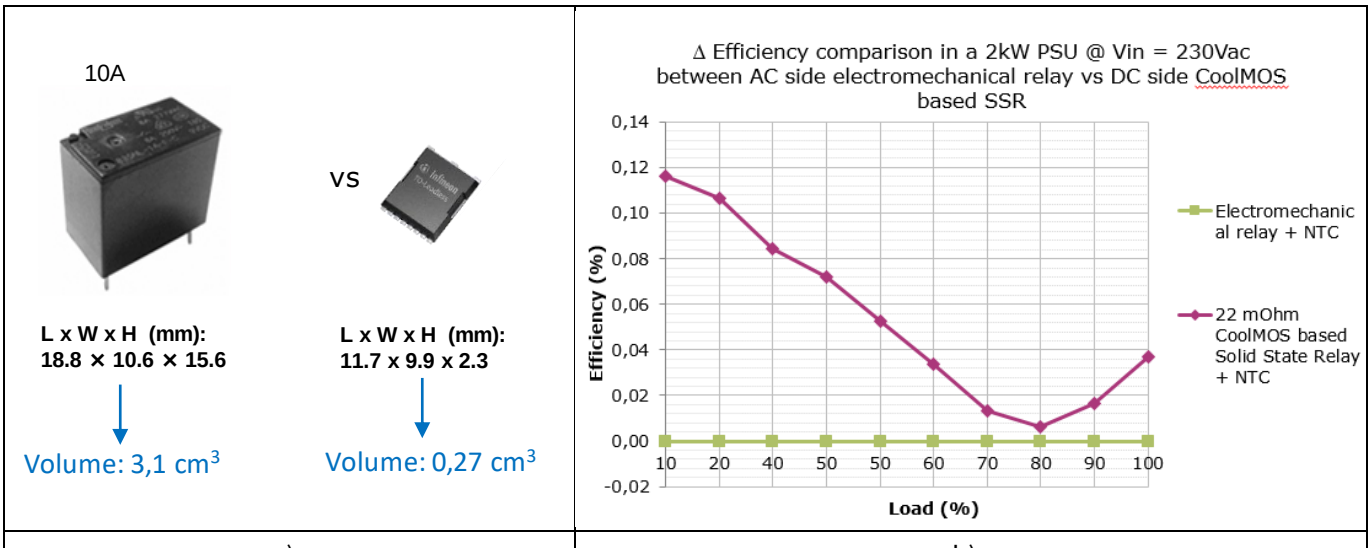


Figure 26 Inrush current device from AC-side to DC-link side

One of the major trends in the power supplies market is increasing power density. One way of achieving higher density is by removing the EM relay and replacing it with a MOSFET.

It is more convenient to move the pre-charge circuit, switching device plus PTC/NTC/power resistor, from the AC-side to the DC-link side (in series with the bulk capacitor), as shown in Figure 26. In this way, not only is the RMS current flowing through the switching device lower, but also the driving circuit can be implemented much more simply, without the need for an isolated driver or bootstrap circuitry.

Moreover, MOSFETs have less volume and weight impact compared to relays. Figure 27a presents a size comparison between a typical EM relay used for PFC applications and a CoolMOS™-based solution in a TOLL package. By using MOSFETs, the volume reduction is around 91 percent. In addition, relays are much heavier: a PCB relay is in the range of 10 g, while a smart switch is in the range of 1 g or even below for small packages [5]. In terms of efficiency (Figure 27b), the advantage of using MOSFETs is more evident at light load (+0.12 percent at 10 percent load), when the coil losses of the relay become significantly dominant compared to the driving losses of the MOSFET. At heavy loads the MOSFET still slightly outperforms the relay if the right $R_{DS,ON}$ is chosen.



a) b)

Figure 27 Size (a) and efficiency (b) comparison between standard mechanical relay at AC-side and CoolMOS™-based solution at DC-side

In summary, the major benefits of using MOSFETs in place of relays are:

- Increased power density
- Improved system reliability and robustness
- Improved power dissipation (especially in terms of control losses [5])
- Better EMI behavior during switch-on/off
- Removal of the relay acoustic noise (attractive for TV applications)
- Easier implementation of the diagnosis (relevant for automotive and high-safety applications)

Nevertheless, there are still same challenges to be addressed and solved in the case of employing a pre-charge MOSFET: i.e. device protection in the event of high voltage surge pulse and cost optimization of the solution at overall application level.

3.2 Pre-charge control strategy

The active-bridge CCM PFC demo board implements the inrush current limitation circuit at the DC-link side, for reasons discussed previously. The circuit is composed of a 22mΩ 600 V CoolMOS™ S7 in parallel with a 30 Ω NTC resistor and limits the turn-on inrush current.

When the AC-line is connected to the PFC, the DC-link capacitor starts to be charged with a maximum current limited by the NTC resistance value and after a few hundreds of ms reaches a DC voltage slightly below the peak of the AC voltage. In the meantime the bulk voltage rises, and the bias power supply starts up and provides the 12 V supply to the PFC controller, turning it on.

The control signal for activating the pre-charge MOSFET is realized by an “OR” between two analog signals coming from the Infineon PFC controller ICE3PCS01G: the VB_OK and the PWM signals as shown in Figure 28. VB_OK becomes high once the bulk voltage reaches 95 percent of the rated PFC output voltage while the PWM is the control signal of the main PFC MOSFET. The pre-charge MOSFET is kept high as long as the bulk capacitor is charged at a proper voltage level or the PWM signal is commutating, thus meaning that the PFC is active and boosting the voltage to the target value.

The only VB_OK signal is not enough since it becomes high too late during start-up, leading to additional stress on the pre-charge MOSFET during the start-up phase.

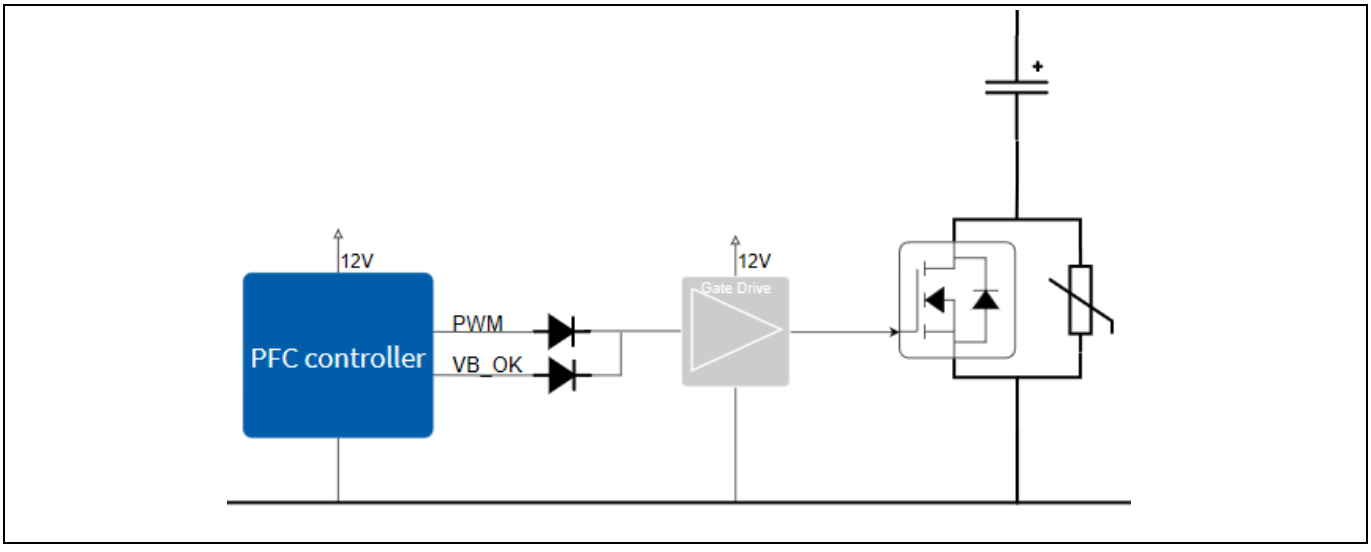


Figure 28 Control network of the pre-charge MOSFET

3.3 Pre-charge and start-up experimental results

Figure 29 and Figure 30 present the PFC pre-charge and start-up sequence for both high- and low-line respectively. One can see that the inrush CoolMOS™, used in place of the relay, is switched on when the PFC is starting to modulate the PWM signal. During start-up, as long as the bulk voltage is less than 95 percent of the rated one, the internal voltage loop output (current reference) increases from an initial value under soft-start control. This results in a controlled linear increase of the output from 0 A, thus reducing the stress on the external components. Once 95 percent is reached, the soft-start control is released to achieve good regulation and dynamic response.

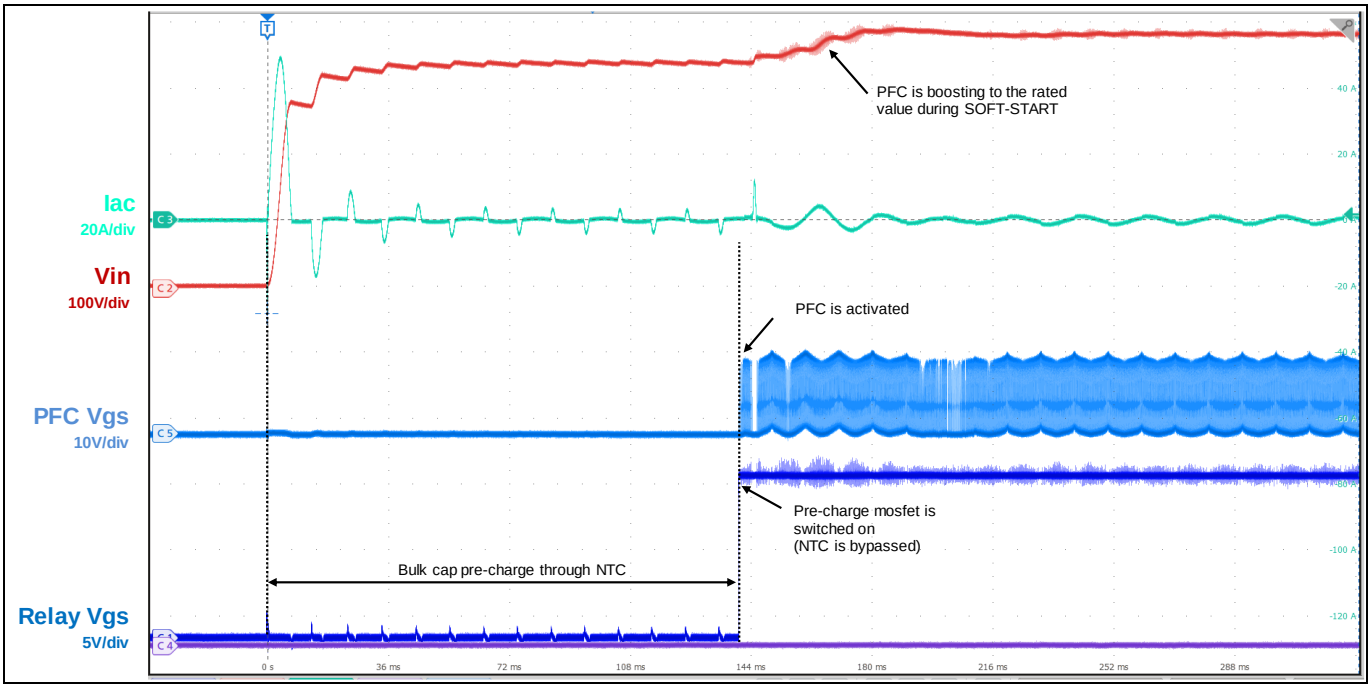


Figure 29 Pre-charge and PFC start-up at 250 V_{AC}

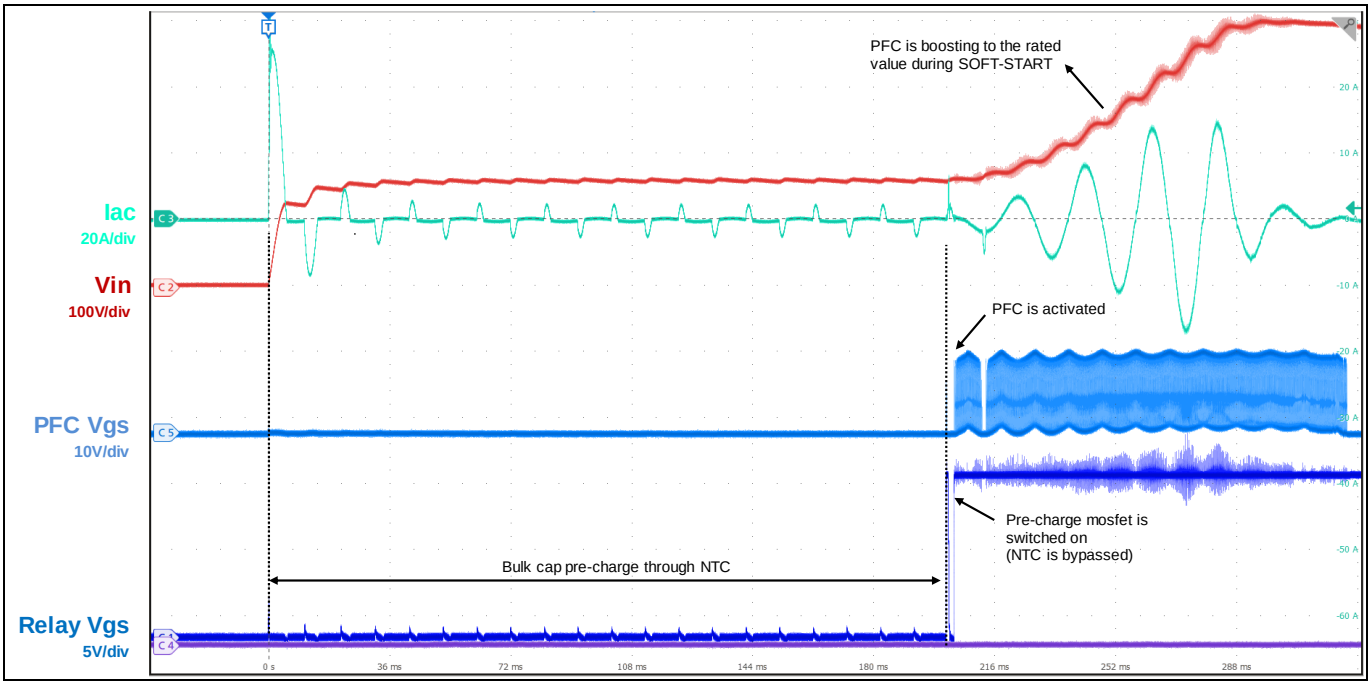


Figure 30 Pre-charge and PFC start-up at 120 V_{AC}

4 AC-Line Drop-Out (ACLDO)

4.1 Test-bench

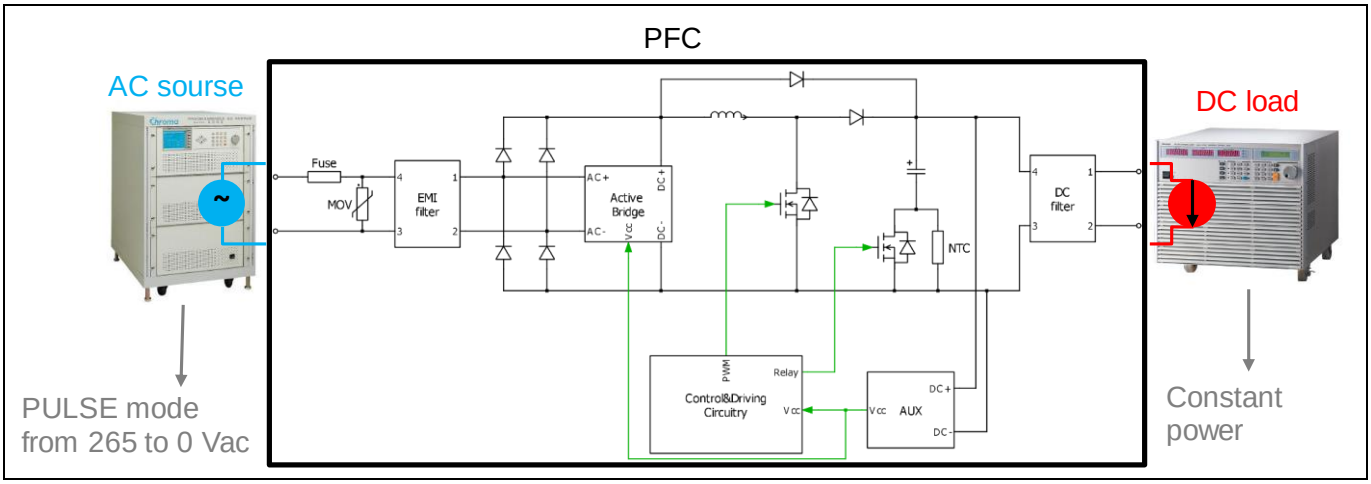


Figure 31 Test-bench for voltage drop-out emulation

The robustness of the active-bridge PFC against AC-Line Drop-Out (ACLDO) events is tested in the worst operating conditions, i.e. AC voltage from 265 V to 0 V during 10/20 ms happening at 90 degrees or 270 degrees, and using a DC electronic load demanding partial or full load at constant power. Test bench is shown in Figure 31.

4.2 Experimental results

Figure 32 shows the results of a 20 ms ACLDO at 75 percent of the load power, where a minimum bulk voltage of 272 V is reached.

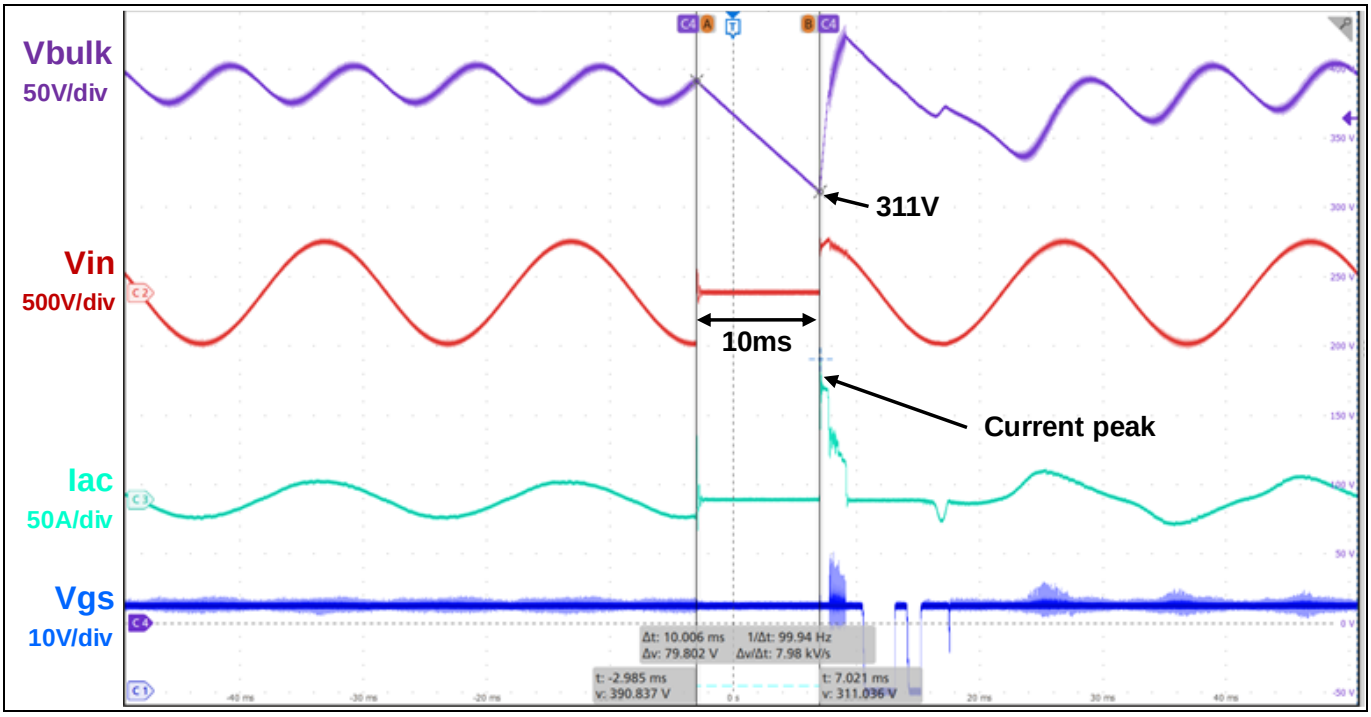


Figure 32 Voltage drop of 20 ms at 1800 W

The detail of Figure 33 shows that at the time the AC-line comes back the pre-charge MOSFET is still driven high and it experiences a current peak around 110 A with a pulse duration around 2 µs.

Figure 34 shows the results of a 10 ms ACLDO at full-load power, where a minimum bulk voltage of 311 V is reached.

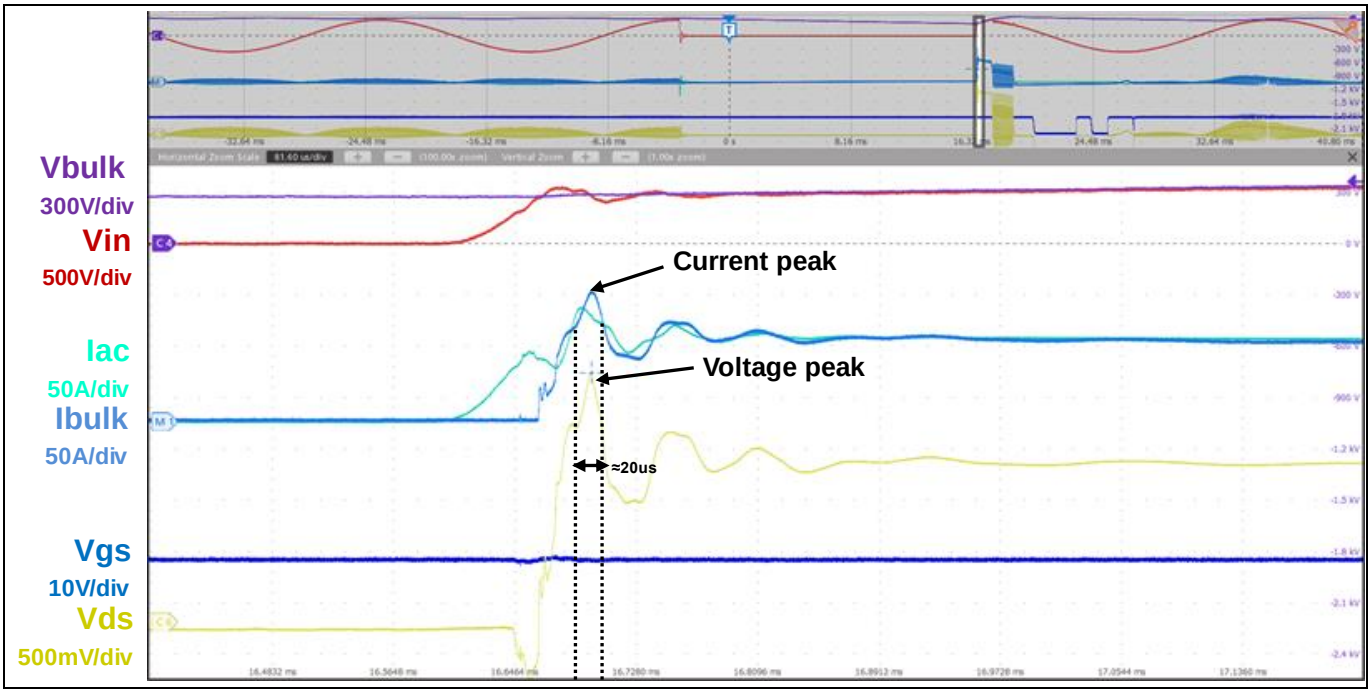


Figure 33 Zoom: voltage drop of 20 ms at 1800 W

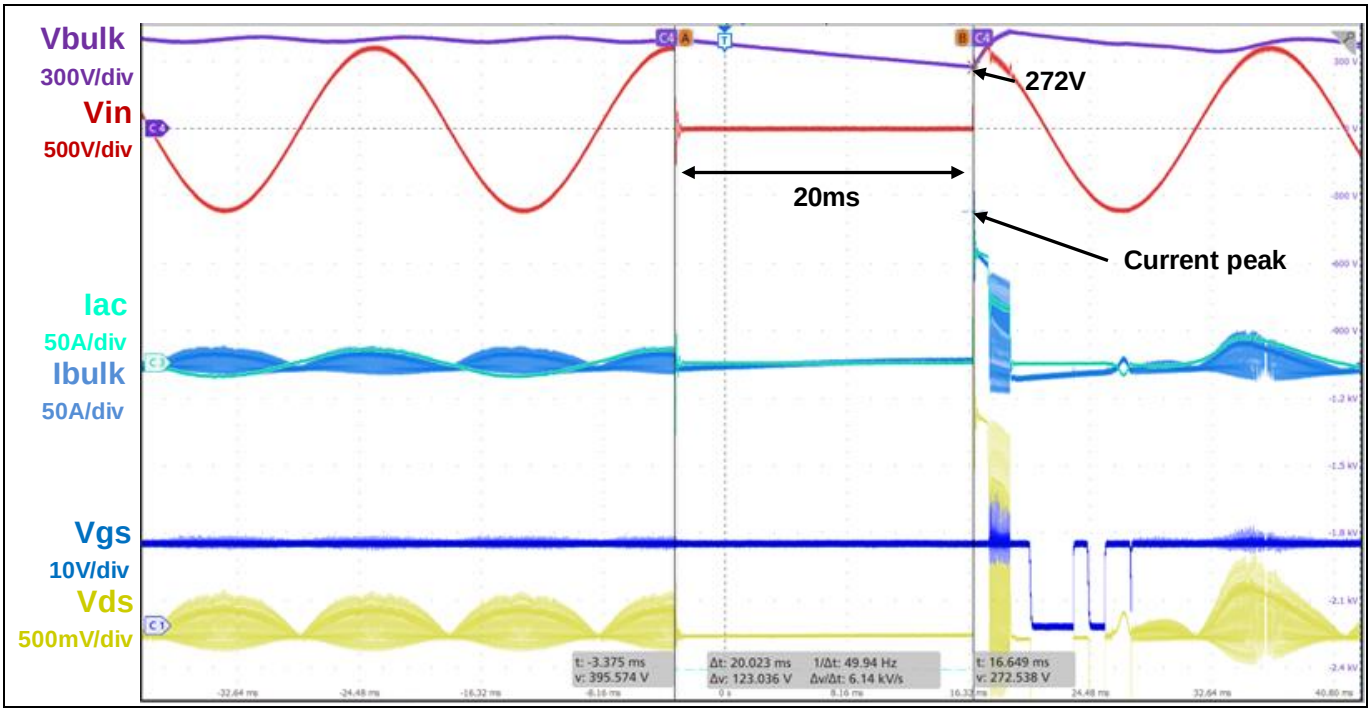


Figure 34 Voltage drop of 10 ms at 2400 W

4.3 Simulation of body diode conduction during ACLDO

Test results in the previous section clearly show that during ACLDO pre-charge MOSFET is kept high by the controller and thus is still conducting during the return of the AC voltage. In case the MOSFET is switched off, the CoolMOS™ body diode will conduct during the hold-up time, while the bulk capacitor is fully supplying the load.

In the simulation test of Figure 35, the body diode of the pre-charge MOSFET is conducting during the 20 ms hold-up time with an output constant current of 8 A. In the worst case of case temperature of 140°C the delta temperature between case and junction is below 2°C, confirming low thermal stress for the device. As long as the AC voltage is back, the load current will be supplied by the PFC and only the bulk capacitor ripple current will flow through the pre-charge MOSFET.

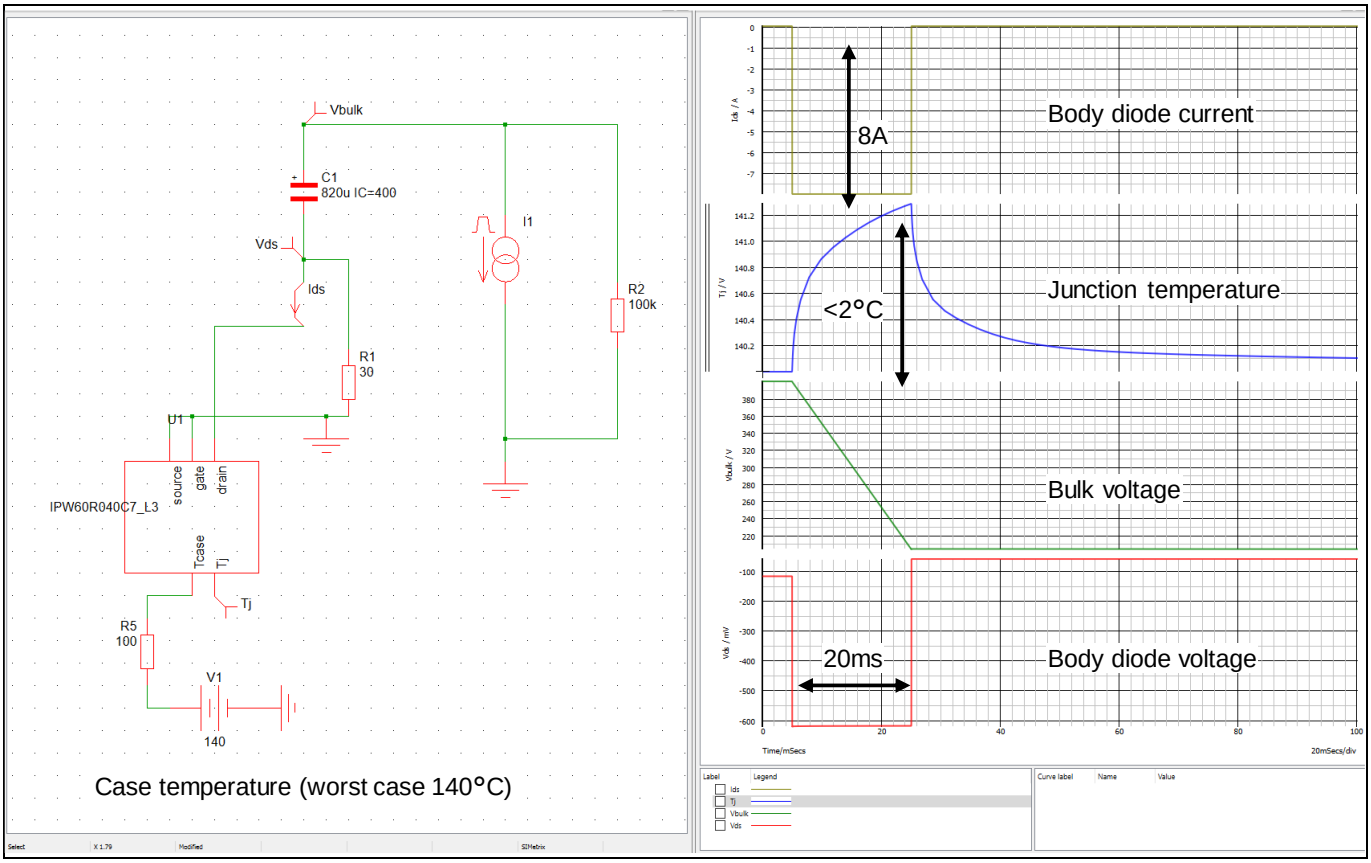


Figure 35 Simulation in case of relay CoolMOS™ body diode conducting during voltage drop-out

5 Surge immunity test

5.1 Surge specification from the standards

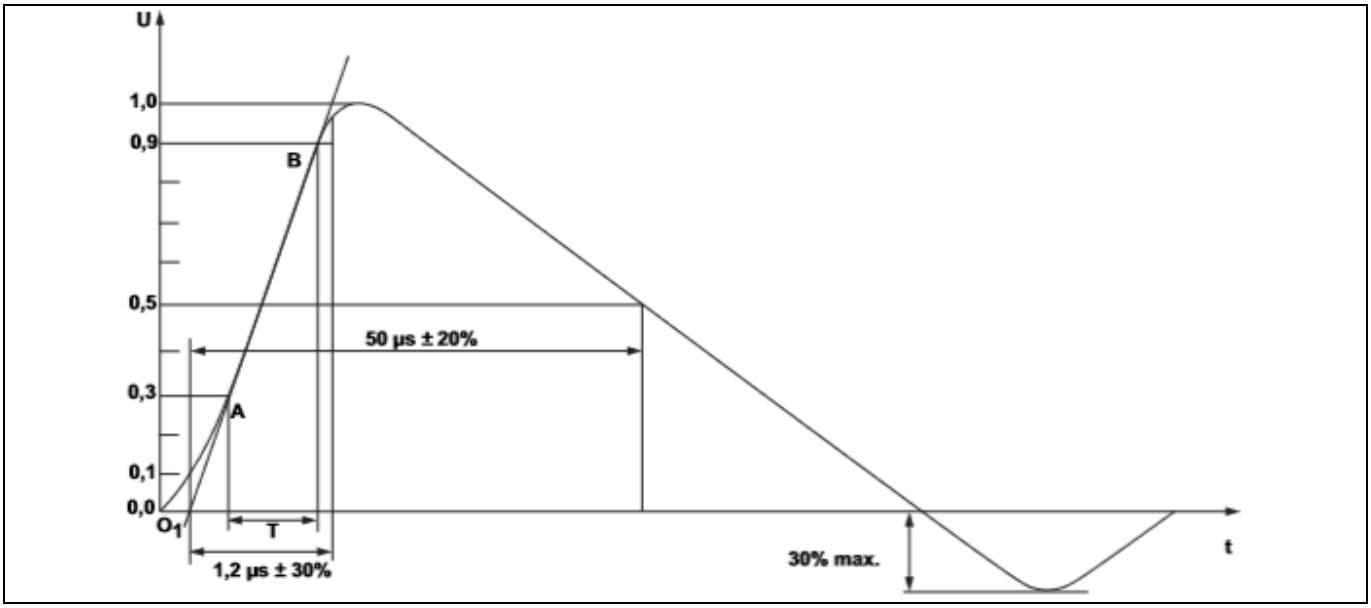


Figure 36 Surge voltage waveform according to IEC 61000-4-5

Power-line surges are caused by lightning strikes, load switching, capacitor bank switching, equipment faults, etc.

The methodology for surge testing is well developed and is described by the IEC 61000-4-5 standard [4], which specifies the surge generator output into both open- and short-circuits.

The open-circuit voltage-surge waveform shown in Figure 36 is called the Combination Wave Generator (CWG) 1.2/50 µs waveform. Another aspect is the number of surge strikes needed for the test. The VDE 0884-11 standard specifies the application of 50 surge strikes, of which 25 are of polarity one, followed by 25 of polarity two.

The ability of devices to withstand such surges is important, because it has a significant impact on field-reliability. In PFC circuits, much of the line surge is attenuated by other components, like spark gaps, MOVs, EMI filters and bus capacitances. The residual surge energy reaching the power MOSFET is dissipated by means of avalanche, making the avalanche rating of the device important, or it can be dissipated by means of current, making the maximum pulse current rating of the device fundamental.

Traditional surge testing for silicon-based power supply applications involves firing surge strikes at specified voltages from 0.5 kV up to 4 kV, depending on the desired rating level. The power supply is typically designed with surge protection components like spark gaps and MOVs that attenuate and dissipate the surge strike. In addition, other components like EMI filters and power-supply capacitances further attenuate the surge voltage. The residual surge waveform reaching the FET is thereby power supply design dependent. In addition, the surge strike can cause system-level failures by stressing other components such as bypass diodes and capacitors.

5.2 Surge pulse test bench

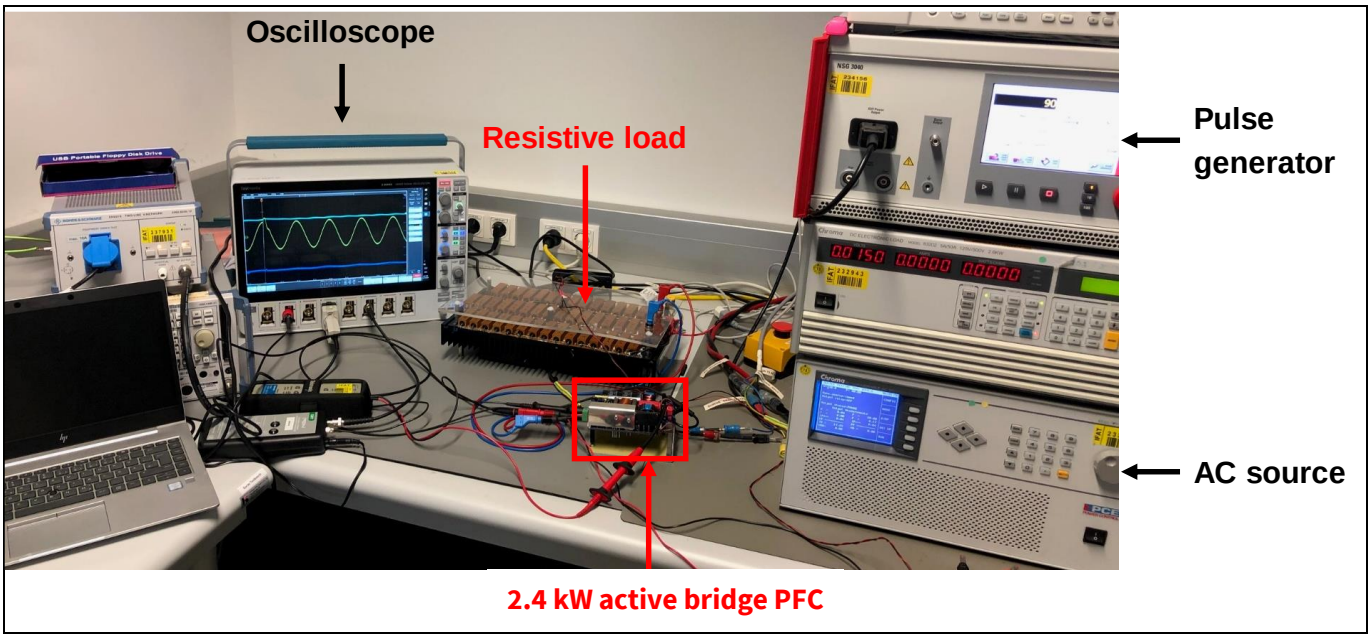


Figure 37 Surge pulse test bench

The test bench for surge pulse testing is the one presented in Figure 37. The surge generator NSG 3040 is coupled with a standard AC soruce. CWG of 1.2/50 µs with a series resistor of 2 Ω is applied by the surge generator to the Line and Neutrals conductors. Only differential mode surge is considered in this application note. The load is a fixed resistor of 120 Ω. Rogowski Coils are used for current measurements.

5.3 Surge pulse with AC-line

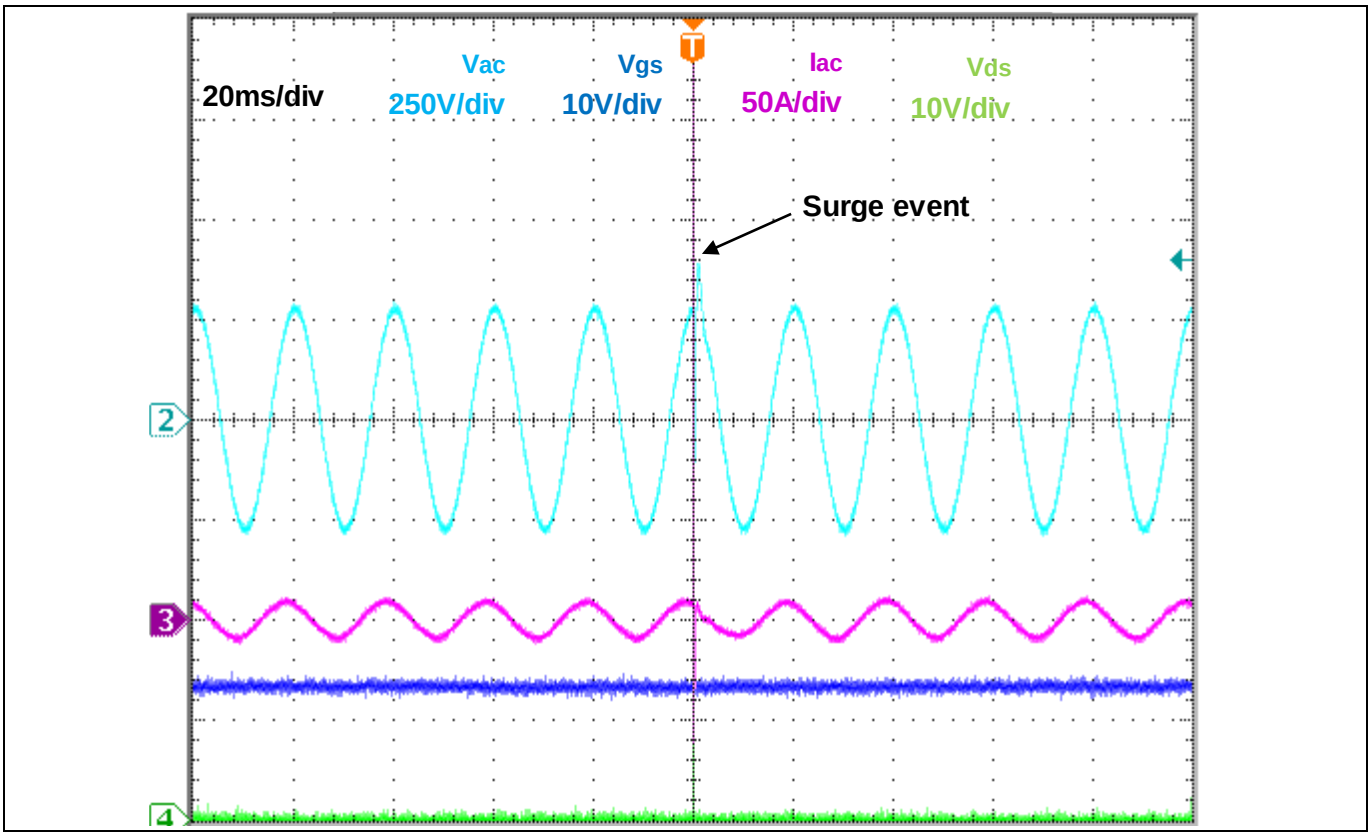


Figure 38 PFC running during surge event

The surge pulse is applied during the positive peak of the AC voltage (at 90° of the sinusoide), as shown by Figure 38, with a pulse amplitude from a minimum of 200 V to a maximum of 4 kV. The Vds (green line) and Vgs (blue) of Figure 38 are related to the pre-charge MOSFET. Input voltage (light blue) and input current (magenta) are captured before the EMI filter.

5.3.1 Without active bridge

Figure 39 and Figure 40 show the results with surge pulse voltage at 1 kV and 2 kV respectively. The active bridge was remopved from the **EVAL_2K4W_ACT_BRD_S7** and the only diode bridge was present. No falilure has been reported on the board. During the surge pulse the pre-charge MOSFET is always kept on, otherwise all the current would flow through the NTC resistor with the consequence of rising the bulk voltage.

In Figure 39 and Figure 40, the Vds (green line) and Vgs (blue) are related to the pre-charge MOSFET, input voltage (light blue) and input current (magenta) are captured before the EMI filter.

Surge current is completely flowing through the diode rectifier since the active bridge is not present. At 1 kV surge the input current peak is aroud 300 A. At 2 kV surge the input current peak is around 700 A. Similarly, it happens for the pre-charge MOSFET. At 2 kV surge, the current exeeds the maximum pulse current written in the datasheet of the components. In this case, paralleling of 2 devices could be an option, unless the PFC manufacturer takes the risk of operating the device above the datasheet limits.

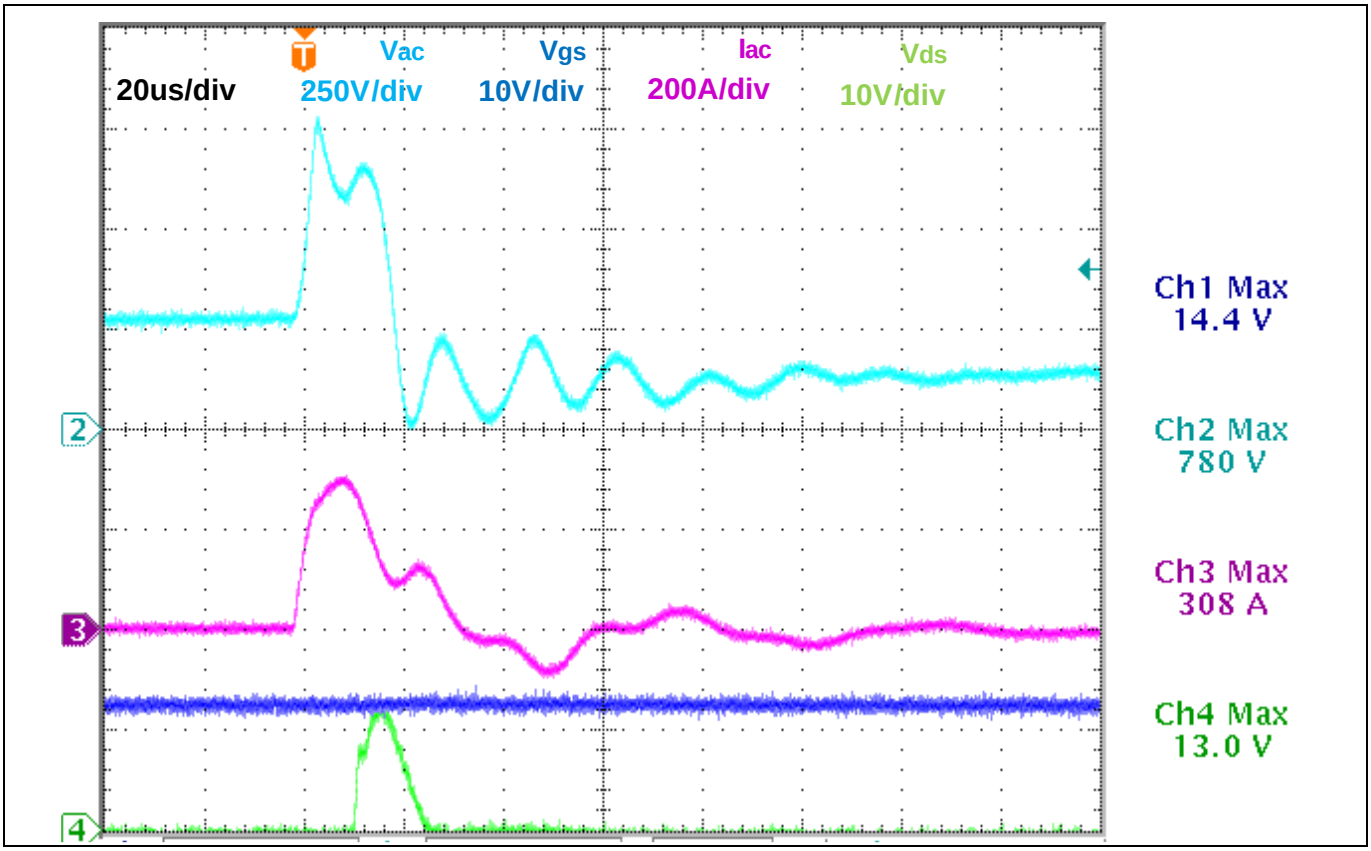


Figure 39 Experimental results of 1 kV surge without active bridge

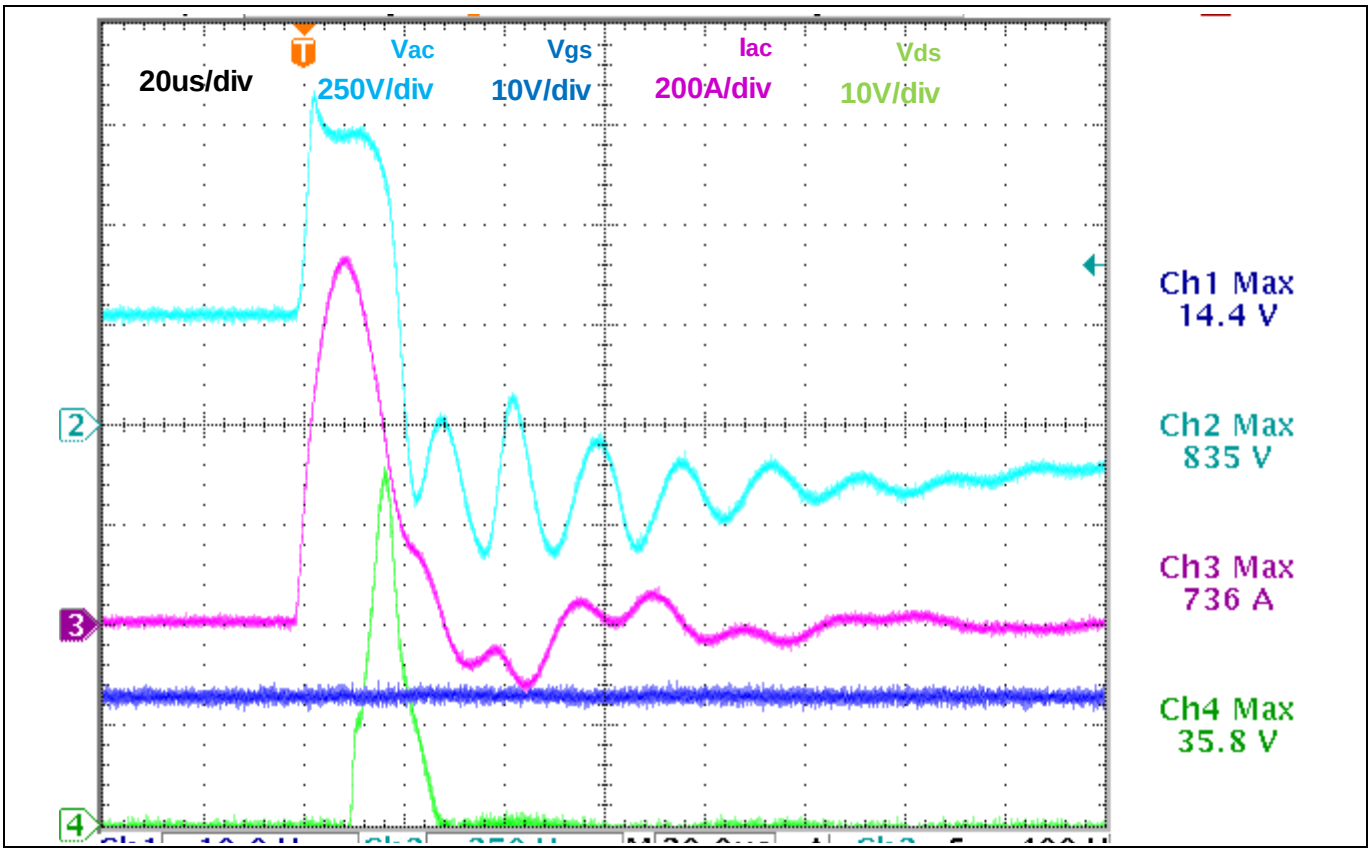


Figure 40 Experimental results of 2 kV surge without active bridge

5.3.2 With active bridge

Figure 41 and Figure 42 show the results with surge pulse voltage at 1 kV and 2 kV respectively. The active bridge is plugged in the **EVAL_2K4W_ACT_BRD_S7** and it is parallel with the diode bridge rectifier. No failure has been reported on the board. During the surge pulse the pre-charge MOSFET is always kept on, otherwise all the current would flow through the NTC resistor with the consequence of rising the bulk voltage.

In Figure 41 and Figure 42, the Vds (green line) and Ids (blue) are related to the low-side active bridge MOSFET, input voltage (light blue) and diode bridge current (magenta) are also captured.

Surge current is distributed between active and diode bridge. The active bridge experiences more current than the diode bridge, around 60 percent of the total current. At 1 kV surge the active bridge current peak is aroud 250 A and the diode bridge one is around 200 A. At 2 kV surge the active bridge current peak is aroud 350 A and the diode bridge one is around 270 A. As a result, the current doesn't exeed the maximum pulse current of the active bridge MOSFET even at 2 kV.

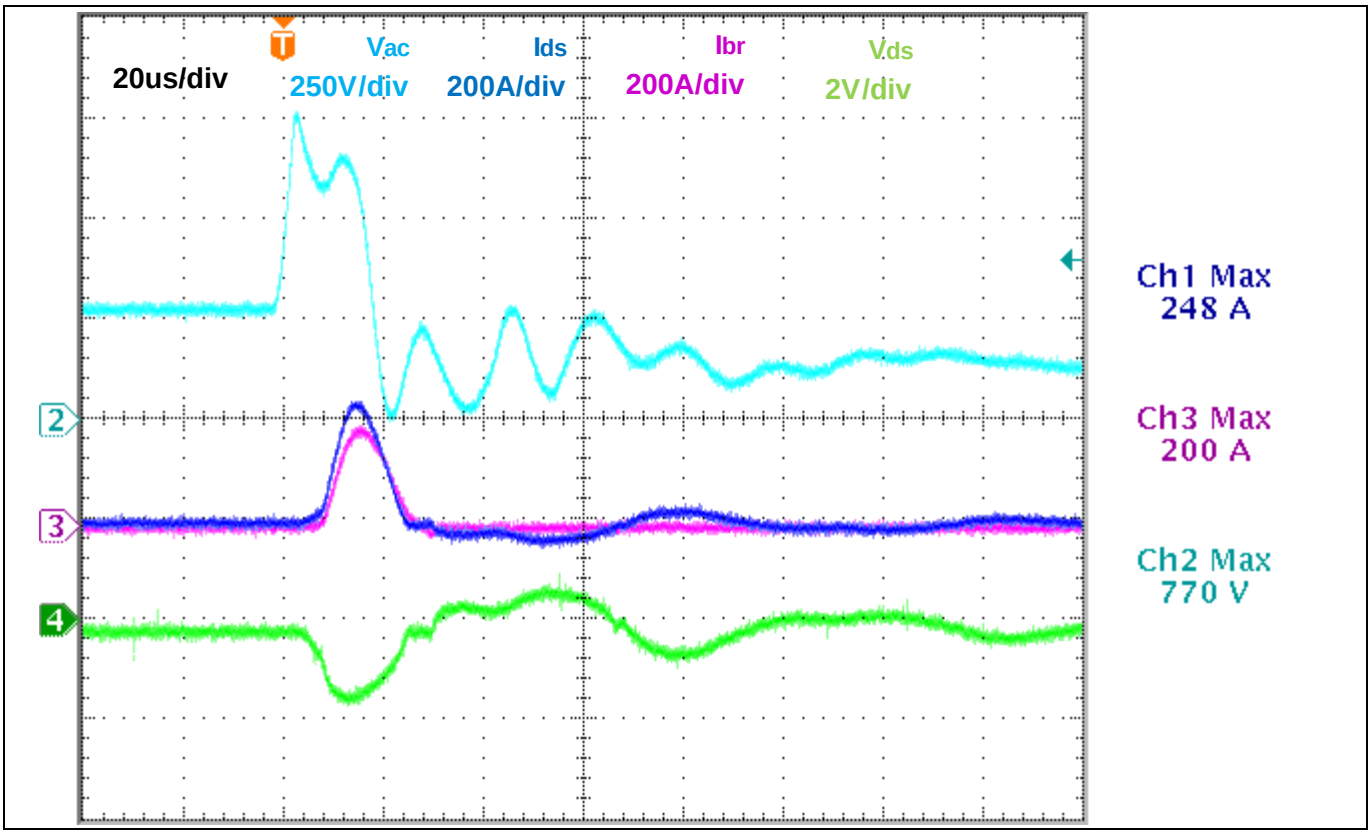


Figure 41 Experimental results of 1 kV surge with active bridge

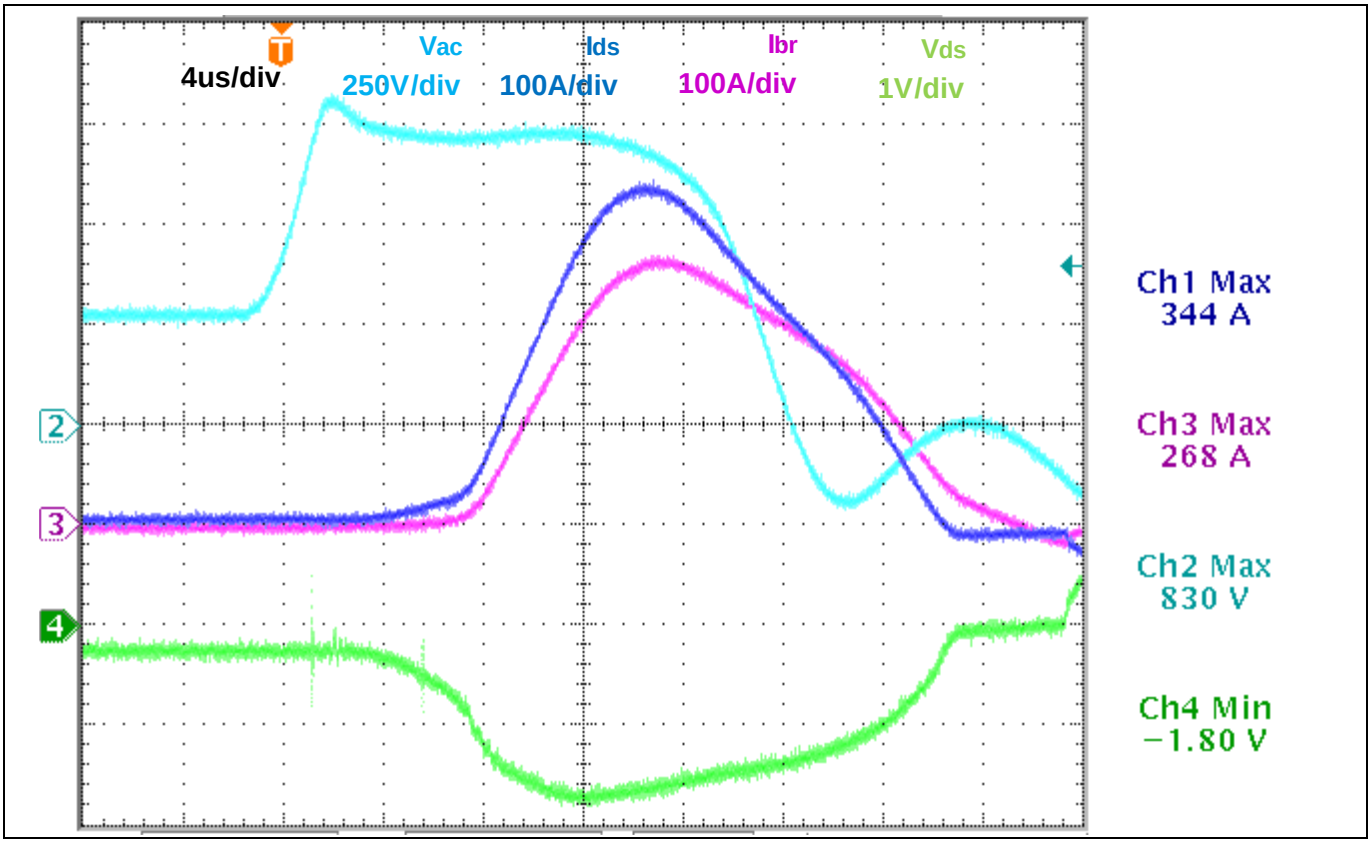
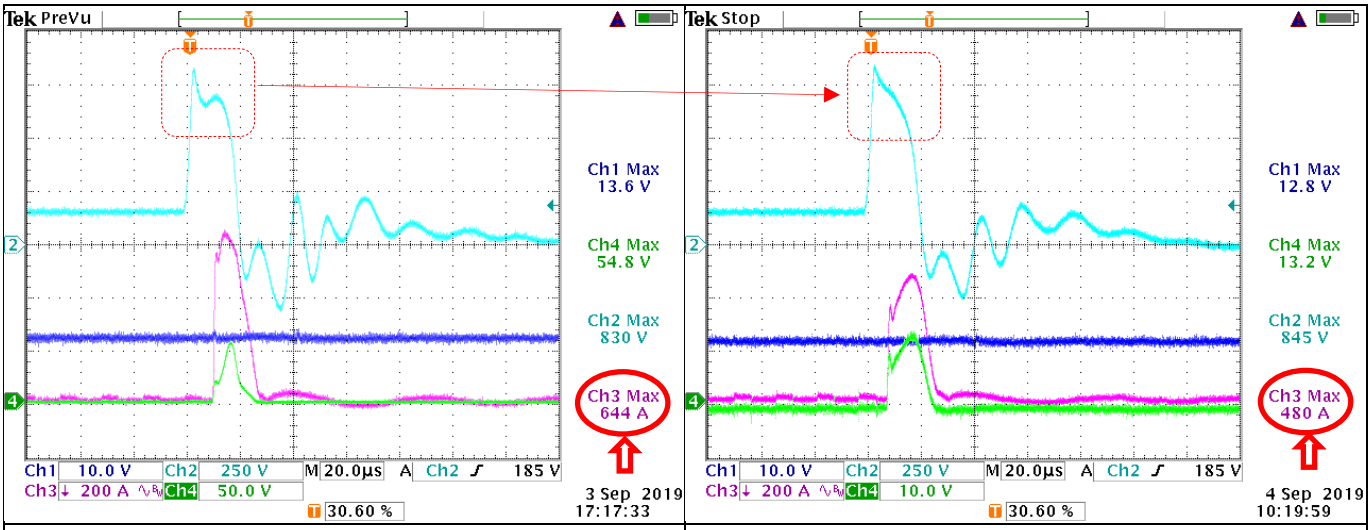


Figure 42 Experimental results of 2 kV surge with active bridge

5.4 Influence of EMI filter on surge behavior

EMI filter values influence surge pulse response of the PFC converter. In particular, resonance between differential inductance of the common mode choke and X capacitor might affect the surge current peak.

Figure 43 shows the 2 kV surge pulse response with and without X capacitor C4 (the one between the two common mode chokes). The Vds (green line) of the and Vgs (blue) are related to, input voltage (light blue) and bulk capacitor current (magenta) are reported. With the removal of C4 there is a 200 A decrease in the current.



With C4 mounted on PCB	Without C4 mounted on PCB

Figure 43 2 kV surge pulse BULK current

6 Summary

Active-bridge line rectification is a circuit that can improve the efficiency within entire power ranges for high efficiency and high power density in SMPS. It demonstrates a flexible design with different daughter board MOSFET $R_{DS,ON}$ for various efficiency requirements of different applications without any other circuit modification. For high power density adapters with burst mode control and convection cooling, but without internal auxiliary power, active-bridge line rectification does reduce the power loss and temperature of power devices. For server power supplies, active-bridge line rectification helps improve the efficiency and extend the power range with at least 94 percent efficiency. The total power loss reduction and efficiency improvement can be estimated by the simple formulas provided in this application note.

For best performance, the MOSFET $R_{DS,ON}$ plays an important role in this application. Considering the mechanical outline, space and thermal conduction inside power supplies, various MOSFET packages are the key to achieving flexibility for such applications. Infineon provides the lowest MOSFET $R_{DS,ON}$ within the same package and MOSFETs with new top-side cooling SMD packages.

Taking into consideration abnormal conditions and EMC tests, solutions for surge voltage and surge current are necessary for MOSFETs. These are also discussed in this application note. Even when active-bridge line rectification acts as a bridge rectifier, a bridge rectifier is still needed, as when they are used in parallel, higher surge current capabilities are possible for abnormal conditions.

Efficiency improvement results with active-bridge line rectification are demonstrated in a 2400 W PFC.

A schematic of a reference circuit is provided in this application note, so that readers can design and manufacture an active-bridge line rectification board following the concept.

7 Schematics

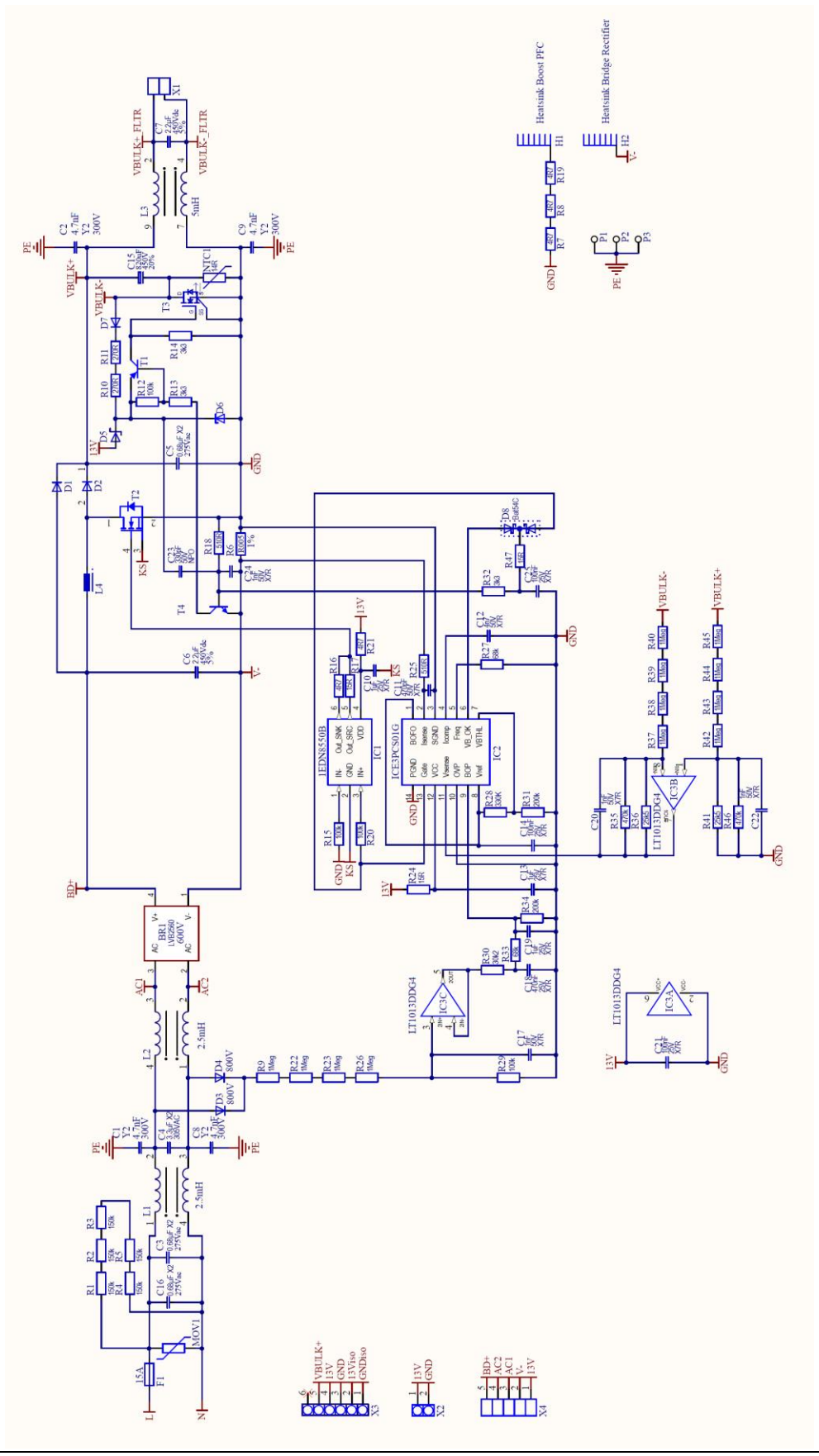


Figure 44 2400 W CCM PFC main board schematic

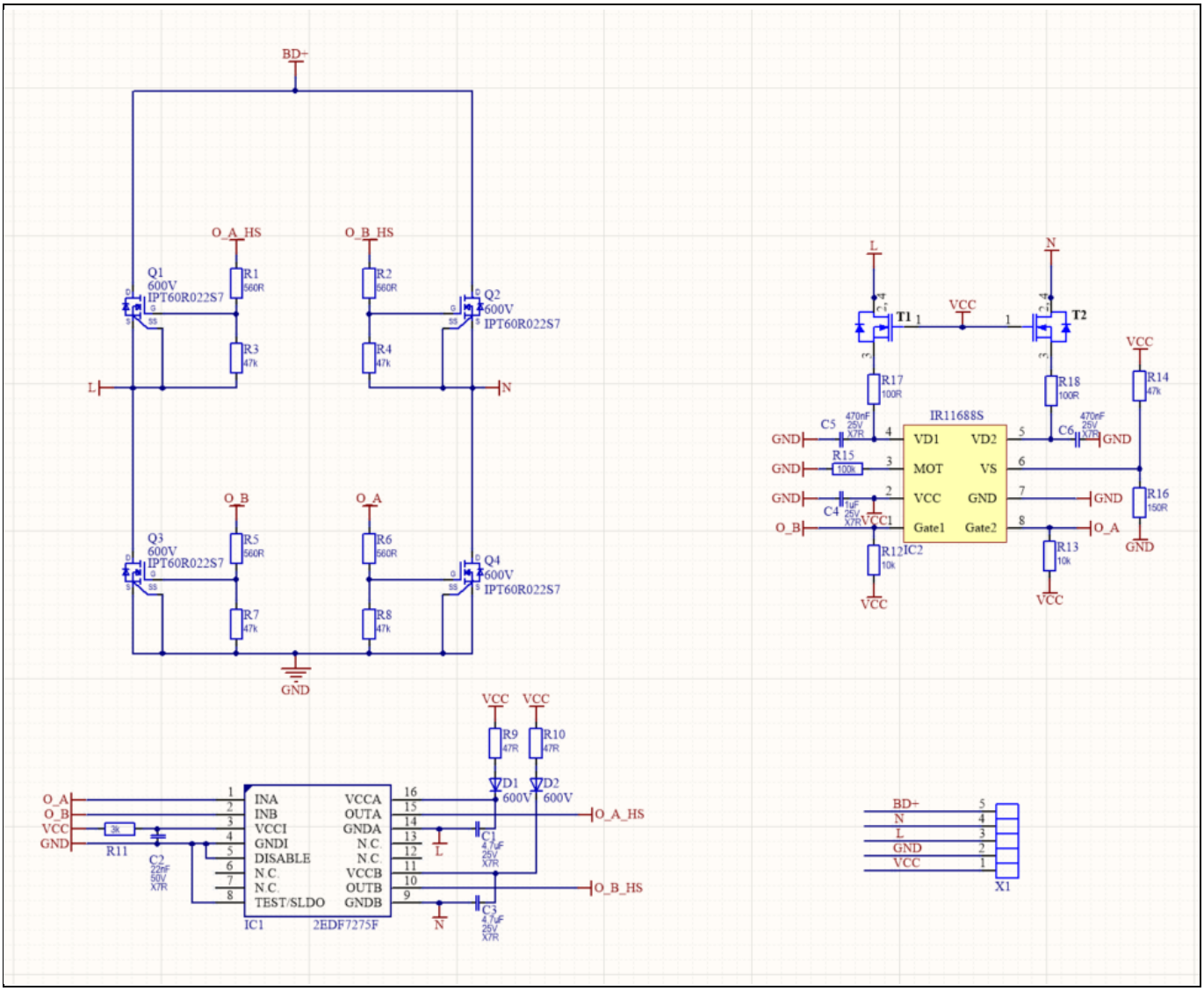


Figure 45 Active-bridge daughter card schematic

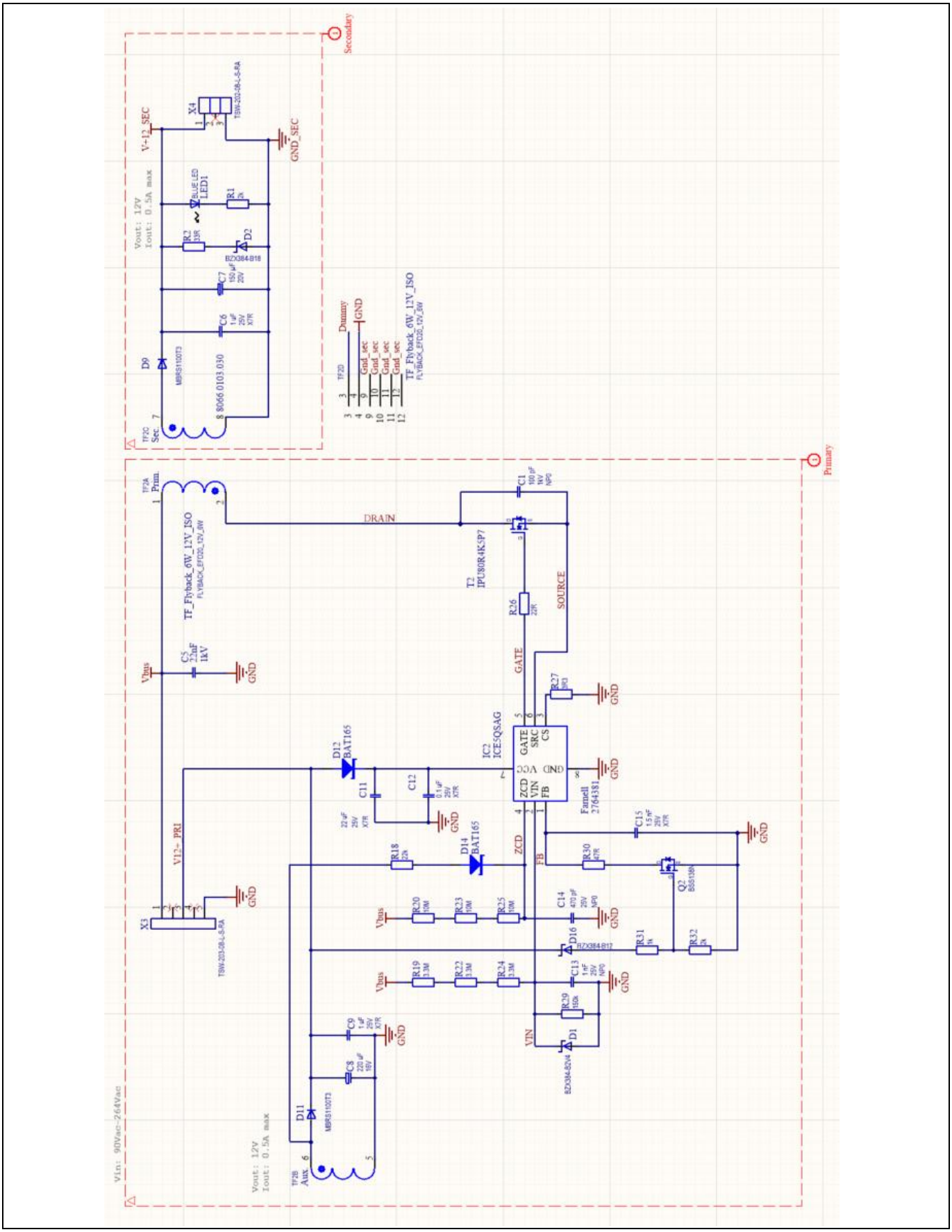


Figure 46 Bias power supply daughter card schematic

8 Bill of Materials (BOM)

Table 3 Main board components

Designator	Comment	Value	Tolerance	Voltage	Description
X1	THT	MKDS 5/3-6, 35-1714955			Connector
T4	SMD	BC817-40		45 V	NPN-transistor
T3	SMD	IPT60R022S7		600 V	N-channel MOSFET
T2	THT	IPZ60R040C7		600 V	N-channel MOSFET
T1	SMD	BC807-40		45 V	PNP-transistor
R36, R41	SMD	25k5	1 percent		Resistor
R35, R46	SMD	470 k	1 percent		Resistor
R31, R34	SMD	200 k	1 percent		Resistor
R30	SMD	30k2	1 percent		Resistor
R28	SMD	330 k	1 percent		Resistor
R27, R33	SMD	68 k	1 percent		Resistor
R18, R25	SMD	510 R	1 percent		Resistor
R17, R24	SMD	15 R	1 percent		Resistor
R13, R14, R32	SMD	3k3	1 percent		Resistor
R12, R15, R20, R29	SMD	100 k	1 percent		Resistor
R10, R11	SMD	270 R	1 percent		Resistor
R9, R22, R23, R26, R37, R38, R39, R40, R42, R43, R44, R45	SMD	1 Meg	1 percent		Resistor
R7, R8, R16, R19, R21	SMD	4R7	1 percent		Resistor
R6	SMD	R005	1 percent		Shunt resistor
R1, R2, R3, R4, R5	SMD	150 k	1 percent		Resistor
NTC1	THT	30 R	±20 percent		NTC resistor
MOV1	THT	V320LA20AP			Varistor
L4	THT	MG10000850			Inductor
L3	THT	5 mH			Common-mode choke
L1, L2	THT	2.5 mH			Common-mode choke
IC3	SMD	LT1013DDG4			Dual-precision

Bill of Materials (BOM)

Designator	Comment	Value	Tolerance	Voltage	Description
					operational amplifier
IC2	SMD	ICE3PCS01G			Standalone CCM PFC controller
IC1	SMD	1EDN8550B			Gate-driver IC
H2	THT	HT100002000			Heatsink
H1	THT	HT200002000			Heatsink
F1	THT	15 A			Fuse
D6	SMD	18 V		18 V	Zener diode
D5	SMD	BAT165		40 V	Schottky diode
D3, D4, D7	SMD	MURS360BT3G		600 V	Standard diode
D2	THT	IDH12G65C6		650 V	SiC diode
D1	SMD	S8KCDICT		800 V	Standard diode
C18	SMD	470 nF	X7R	25 V	Ceramic capacitor
C17, C20, C22, C23	SMD	1 nF	X7R	50 V	Ceramic capacitor
C15	THT	820 µF	20 percent	450 V	Polarized capacitor
C14, C21	SMD	100 nF	X7R	25 V	Ceramic capacitor
C12	SMD	4n7	X7R	50 V	Ceramic capacitor
C11	SMD	470 pF	X7R	50 V	Ceramic capacitor
C10, C13, C19	SMD	1 µF	X7R	25 V	Ceramic capacitor
C6, C7	THT	2.2 µF	5 percent	450 V_{DC}	Foil capacitor
C4	THT	3.3 µF x2	10 percent	305 V_{AC}	Foil capacitor
C16	THT	0.33 µF x2*	20 percent	275 V_{AC}	Foil capacitor
C3, C5	THT	0.68 µF x2	20 percent	275 V_{AC}	Foil capacitor
C1, C2, C8, C9	THT	4.7 nF	Y2	300 V	Ceramic capacitor
BR1	THT	LVB2560		600 V	

**Capacitance value of C16 has been decreased due to mechanical constraints. In order to have better EMI performace, consider increasing this value.*

Table 4 Active-bridge daughter card components

Designator	Comment	Value	Tolerance	Voltage	Description
C1, C3	SMD	4.7 µF	X7R	25 V	Ceramic capacitor
C2	SMD	22 nF	X7R	50 V	Ceramic capacitor
C4, C5, C6	SMD	1 µF	X7R	25 V	Ceramic capacitor
D1, D2	SMD	MURS360BT3G		600 V	Standard diode
IC1	SMD	2EDF7275F			Integrated circuit
IC2	SMD	IR11688S			Integrated circuit
Q1, Q2, Q3, Q4	SMD	IPT60R040S7		600 V	N-channel MOSFET
R1, R2, R5, R6,	SMD	560 R	1 percent		Resistor
R12, R13	SMD	10 k	1 percent		Resistor
R3, R4, R7, R8, R14	SMD	47 k	1 percent		Resistor
R9, R10	SMD	47 R	1 percent		Resistor
R11	SMD	3 k	1 percent		Resistor
R15	SMD	100 k	1 percent		Resistor
R16	SMD	150 R	1 percent		Resistor
R17, R18	SMD	100 R	1 percent		Resistor
T1, T2	SMD	BSP300H6327XUSA1		800 V	N-channel MOSFET
R9, R22, R23, R26, R37, R38, R39, R40, R42, R43, R44, R45	SMD	1 Meg	1 percent		Resistor

Table 5 Bias power supply daughter card components

Designator	Qty	Description	Manufacturer	Part number
C1	1	Ceramic capacitor, 10 pF, 1 kV, NP0, CAP1206	Kemet	1702125
C5	1	Ceramic capacitor, 22 nF, 1 kV, CAP1210	Murata	2456116
C6, C9	2	Ceramic capacitor, 1 µF, 25 V, X7R, CAP1206		

Designator	Qty	Description	Manufacturer	Part number
C7	1	Electrolytic capacitor, 150 µF, 20 V	Kemet	
C8	1	Electrolytic capacitor, 220 µF, 16 V	Kemet	1793863
C11	1	Ceramic capacitor, 22 µF, 25 V, X7R, CAP1210		
C12	1	Ceramic capacitor, 0.1 µF, 25 V, X7R, CAP0805		
C13	1	Ceramic capacitor, 1 nF, 25 V, NP0, CAP0805		
C14	1	Ceramic capacitor, 470 pF, 25 V, NP0, CAP0805		
C15	1	Ceramic capacitor, 1.5 nF, 25 V, X7R, CAP0805		
D1	1	Schottky diode, BZX384-B2V4, SOD323	Nexperia	1727-3647-1-ND
D2	1	Schottky diode, BZX384-B18, SOD323	Nexperia	
D9, D11	2	Standard diode, MBRS1100T3, SMB/DO-214AA		2317670
D12, D14	2	Medium-power AF Schottky diode, BAT165, S0D250X125X110-2N	Infineon	1056502
D16	1	Schottky diode, BZX384-B12, SOD323	Nexperia	
IC2	1	QR Flyback controller, ICE5QSAG, SOIC8	Infineon	ICE5QSAG
LED1	1	LED, 2.9 V, LED-0603R	Rohm	2762564
Q2	1	N-channel MOSFET, BSS138N, SOT23R	Infineon	2432717
R1	1	Resistor, 2 k, RES0805W	Vishay	1469884
R2	1	Resistor, 33 R, RES0805R	Vishay	1738939
R18	1	Resistor, 22 k, RES0805W	Vishay	1469896
R19, R22, R24	3	Resistor, 3.3 M, RES0805W		
R20, R23, R25	3	Resistor, 10 M, RES0805W		
R26	1	Resistor, 22 R, RES0805W		
R27	1	Resistor, 3R3, RES0805W	Vishay	2413965
R29	1	Resistor, 150 k, RES0805W		
R30	1	Resistor, 47 R, RES0805W		
R31	1	Resistor, 1 k, RES0805W		

Bill of Materials (BOM)

Designator	Qty	Description	Manufacturer	Part number
R32	1	Resistor, 10 k, RES0805W		
T2	1	MOSFET, 950 V CoolMOS™ P7	Infineon	IPU95R3K7P7
TF2	1	Flyback transformer		8066.0103.030
X3	1	Pin header, 5-pin	Samtec	2041577
X4	1	Pin header, 3-pin	Samtec	2041576

9 References

[1] “PFC demo board based on CoolMOS™ P7 600 V: 800 W 65 kHz platinum server design”, AN_201703_PL52_016.

[2] “6 W bias supply using the new 950 V CoolMOS™ P7, ICE5QSAG QR Flyback controller, and snubberless Flyback for improved auxiliary power supply efficiency and form-factor”, AN_1801_PL52_1803_160336

[3] “Data sheet – IR11688S”, from Infineon

[4] “Design notes control IC SmartRectifier™ IR11688”, application note from Infineon

[5] “Relay replacement within automotive power distribution. Smart switch versus relay: detailed comparison”, application note Z8F65515545

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