

Automotive MOSFET

OptiMOS™-5 Power-Transistor



Features

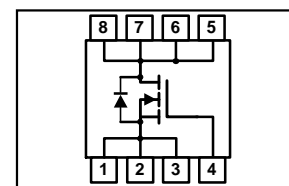
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

V_{DS}	60	V
$R_{DS(on)}$	10.2	mΩ
I_D (chip limited)	47	A

Type	Package	Marking
IAUC41N06S5N102	PG-TDSON-8-33	5N06N102



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	47	A
		$V_{GS}=10\text{V}$, DC current	41	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	13	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	121	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=20\text{ A}$	37	mJ
Avalanche current, single pulse	I_{AS}	–	41	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	42	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	3.6	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	–	–	25.6	–	

Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	60	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=13\text{ }\mu\text{A}$	2.2	2.8	3.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	–	–	1	μA
		$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$	–	–	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$, $I_D=10\text{ A}$	–	9.8	11.8	m Ω
		$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$	–	8.4	10.2	
Gate resistance ²⁾	R_G	–	–	1.28	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics²⁾						
Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	-	855	1112	pF
Output capacitance	C_{oss}		-	184	239	
Reverse transfer capacitance	C_{rss}		-	12	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=20\text{ A}, R_G=3.5\ \Omega$	-	2.8	-	ns
Rise time	t_r		-	1.4	-	
Turn-off delay time	$t_{d(off)}$		-	3.9	-	
Fall time	t_f		-	2.0	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=30\text{ V}, I_D=20\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	4.1	5.3	nC
Gate to drain charge	Q_{gd}		-	2.7	4.1	
Gate charge total	Q_g		-	12.5	16.3	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	41	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ }^\circ\text{C}, t_p=100\ \mu\text{s}$	-	-	121	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30\text{ V}, I_F=41\text{ A}, di_f/dt=100\text{ A}/\mu\text{s}$	-	30.0	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	22.7	-	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

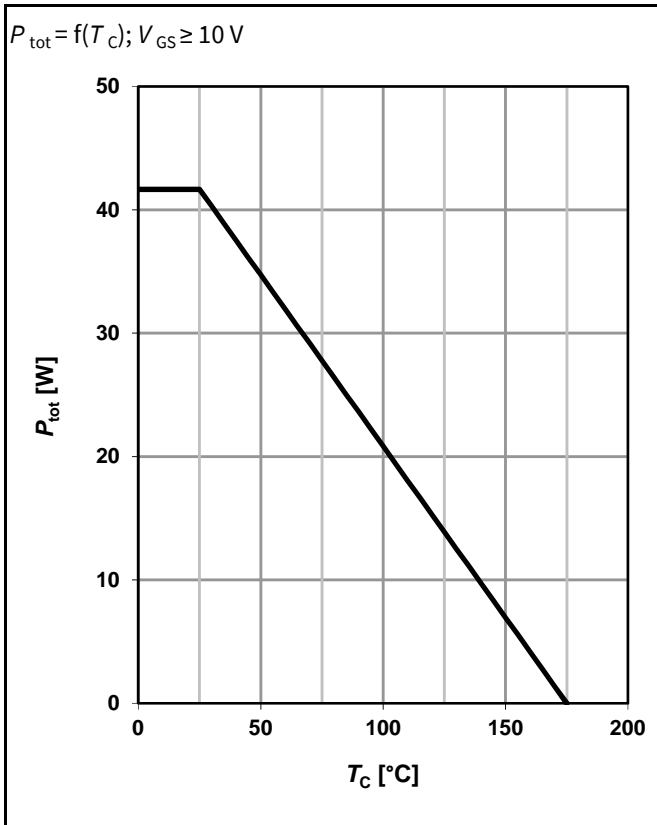
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Current is limited by the package.

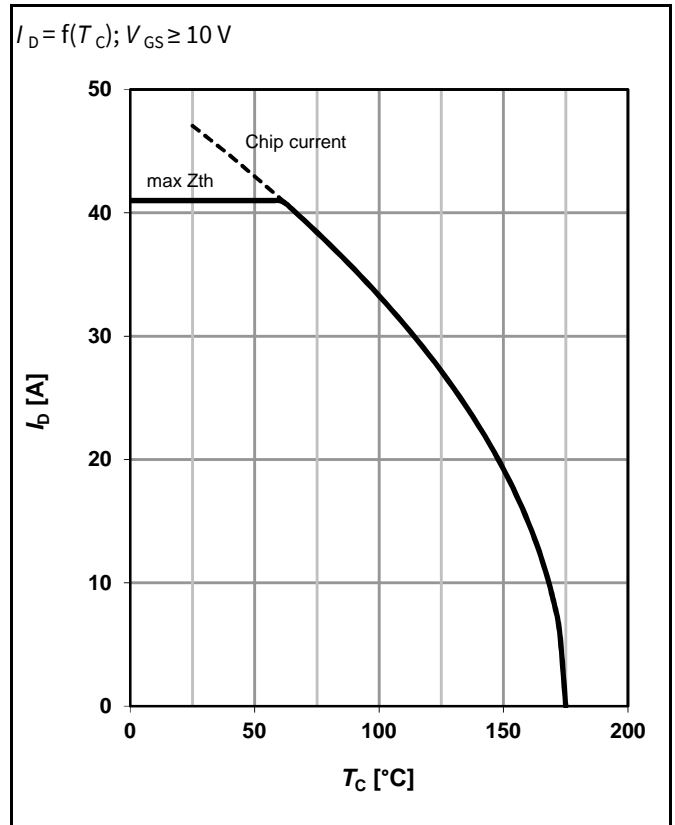
⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

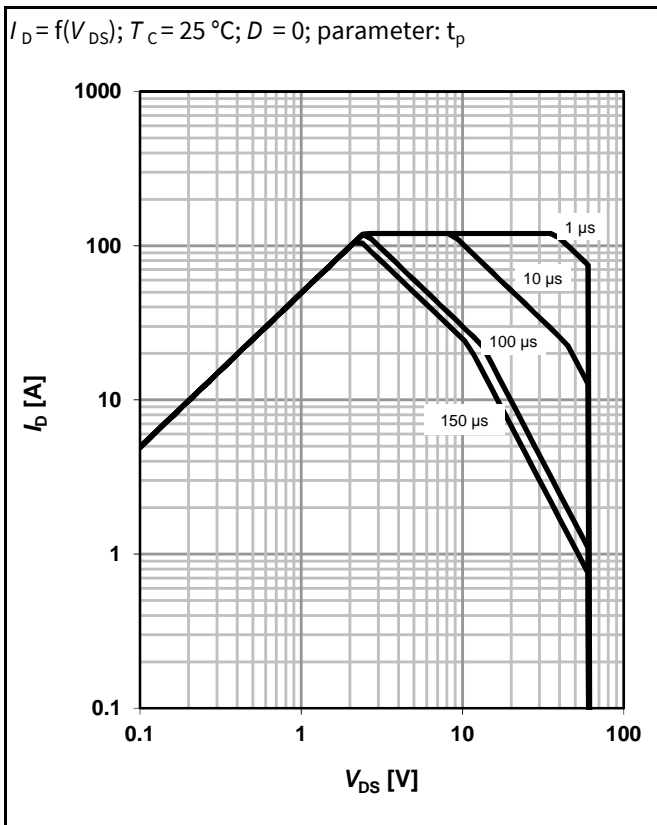
1 Power dissipation



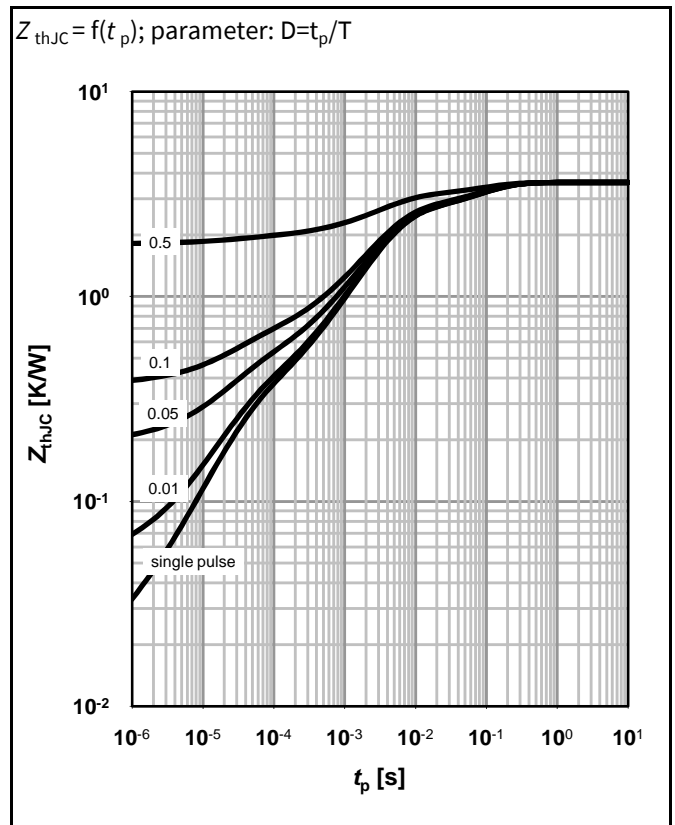
2 Drain current



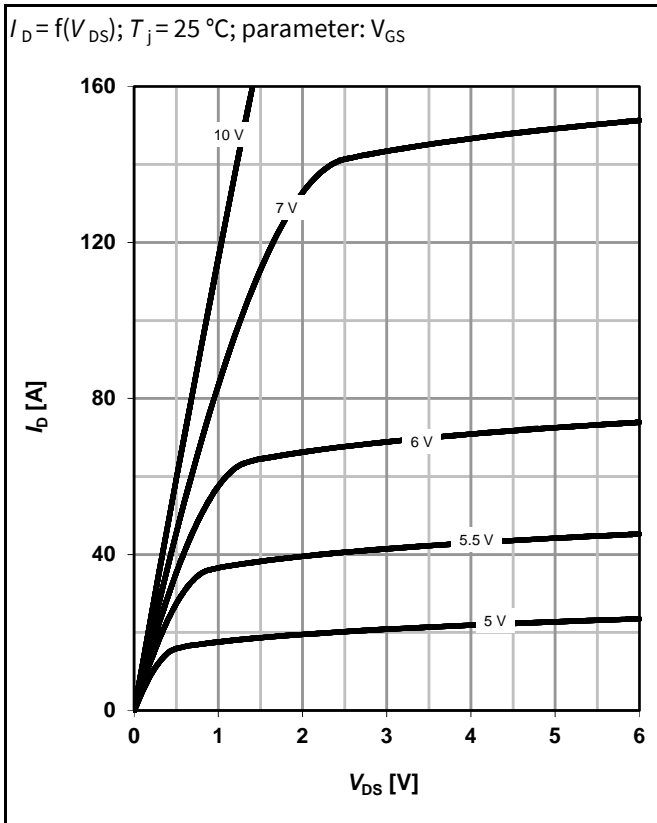
3 Safe operating area



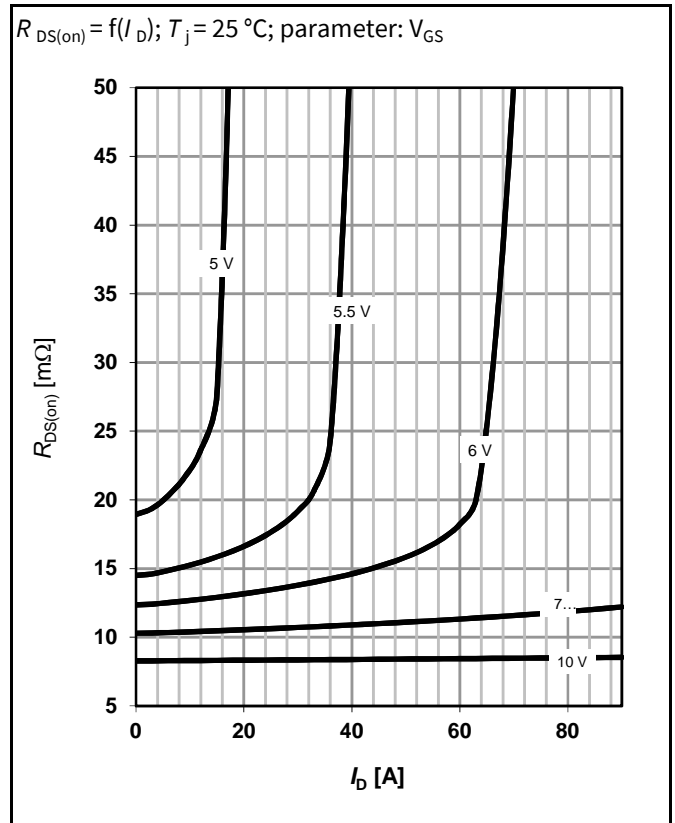
4 Max. transient thermal impedance



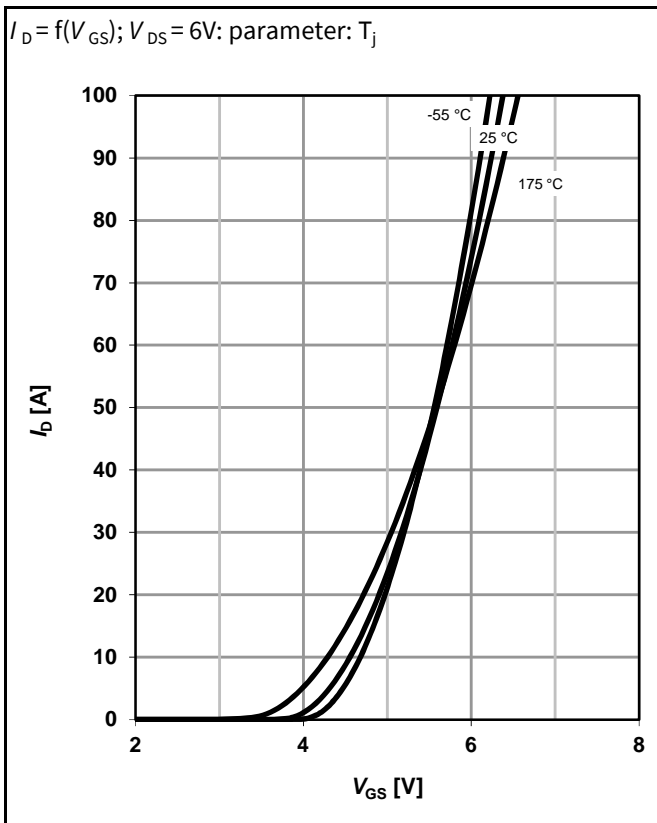
5 Typ. output characteristics



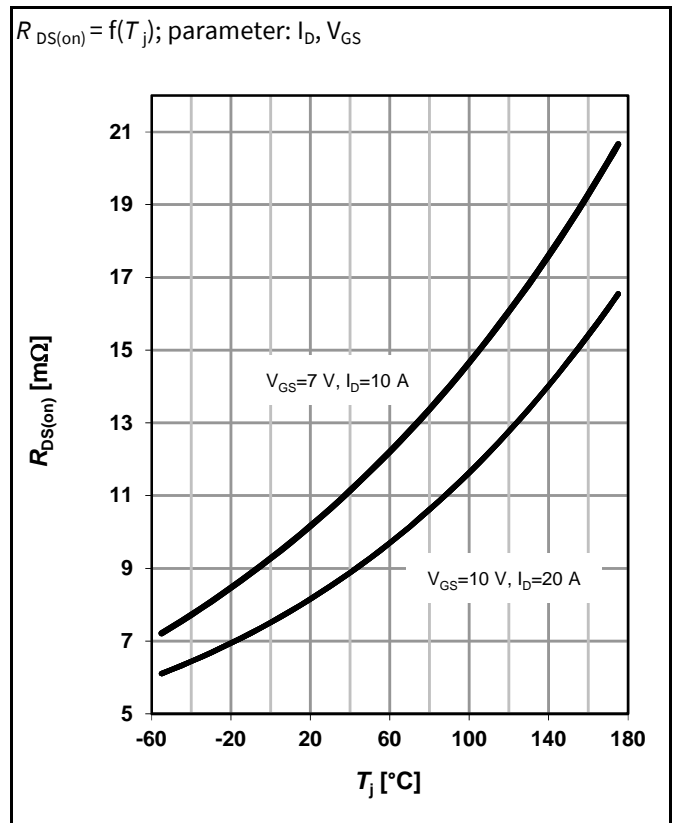
6 Typ. drain-source on-state resistance



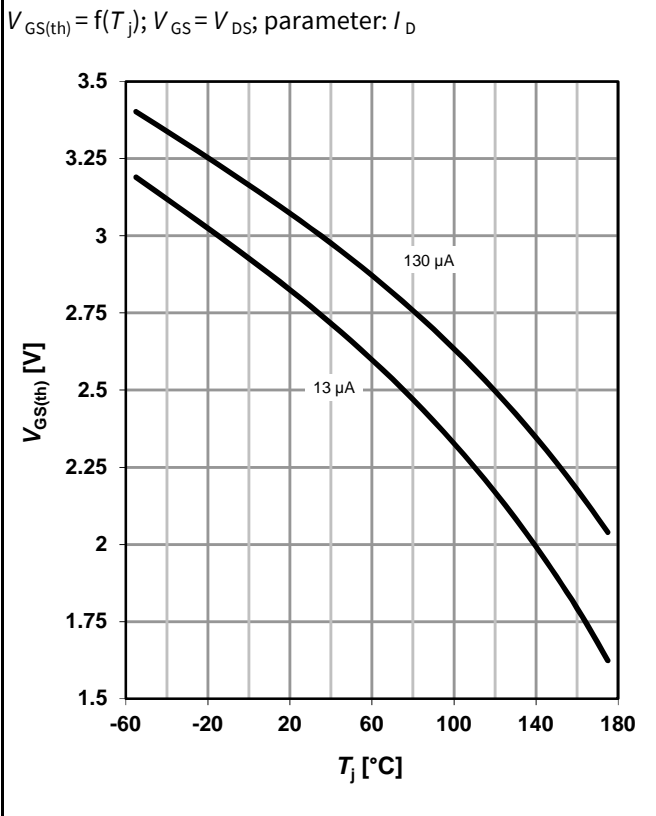
7 Typ. transfer characteristics



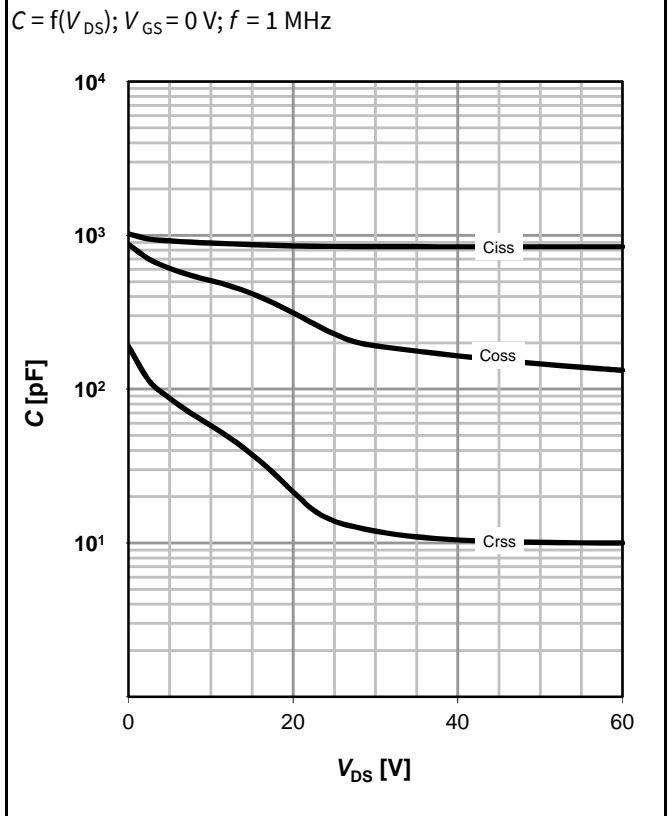
8 Typ. drain-source on-state resistance



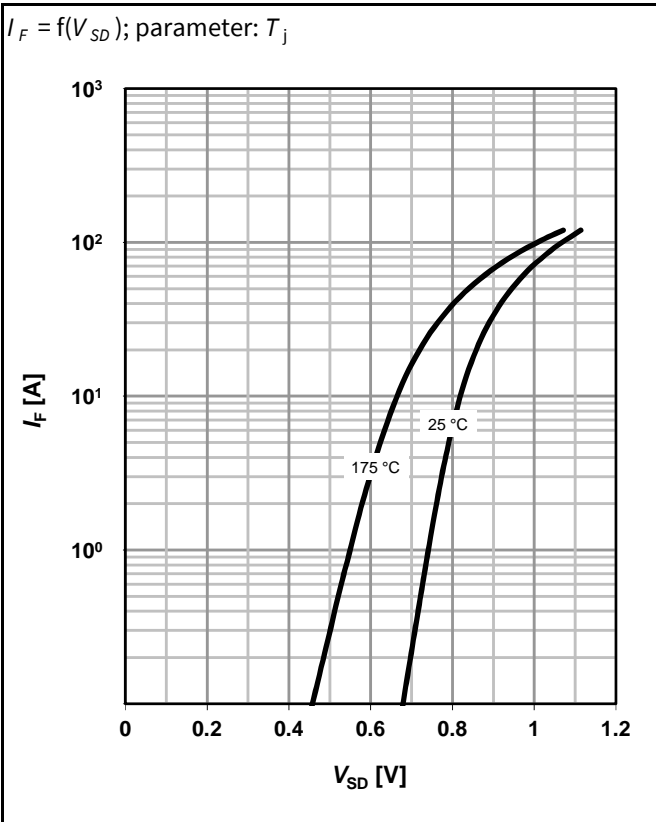
9 Typ. gate threshold voltage



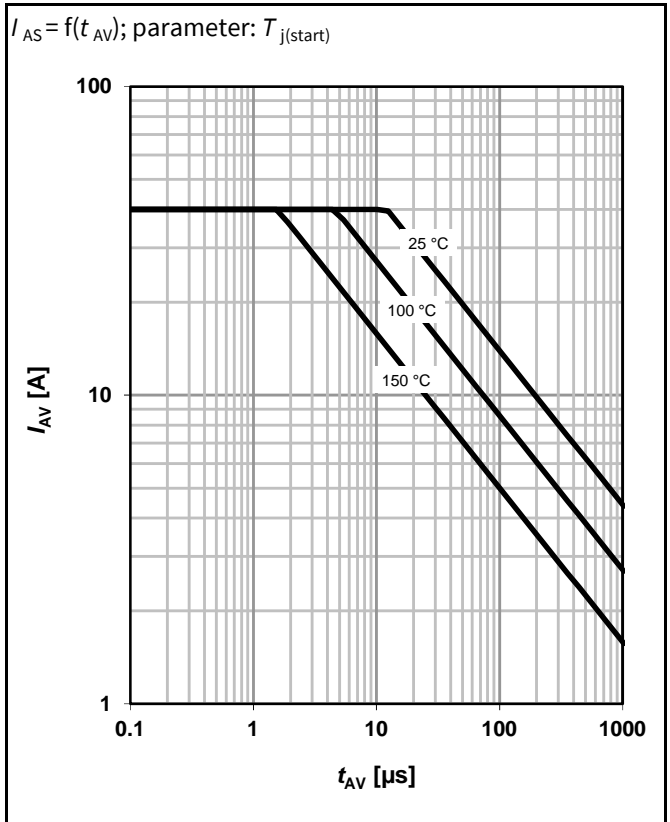
10 Typ. capacitances



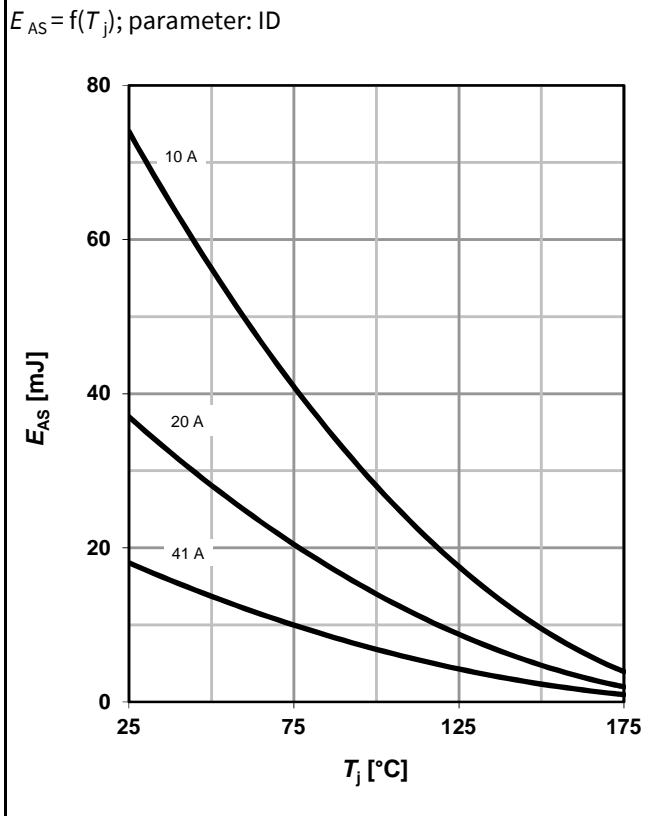
11 Typical forward diode characteristics



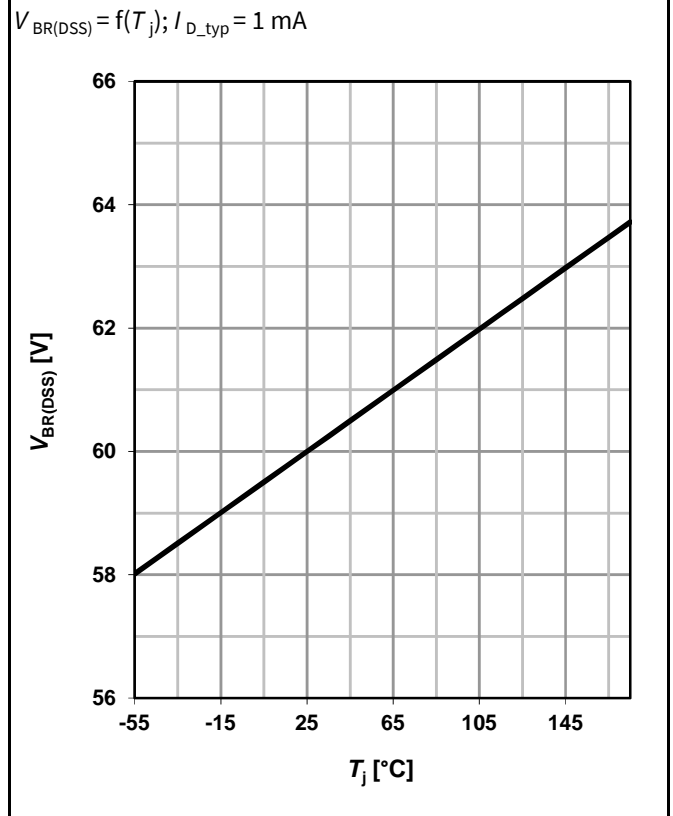
12 Typ. avalanche characteristics



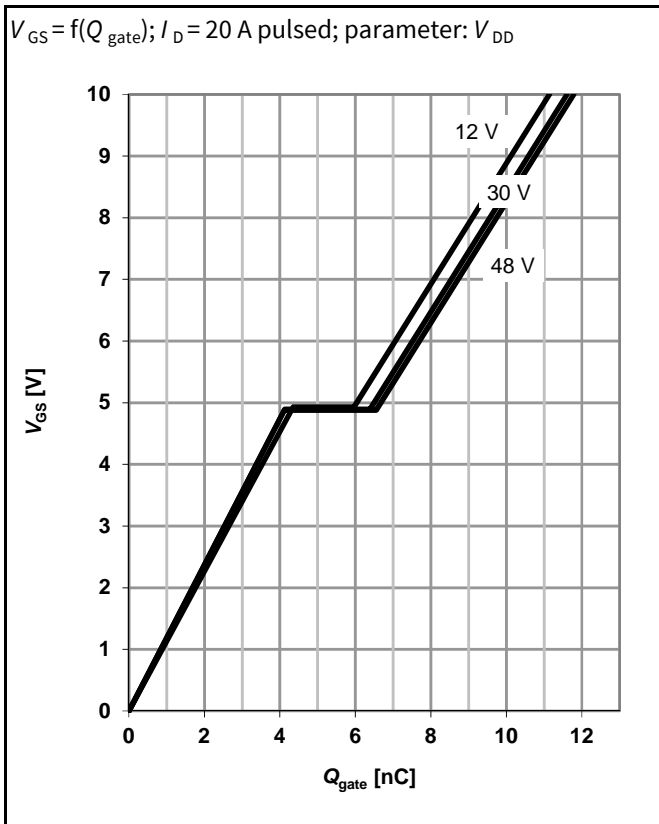
13 Typical avalanche energy



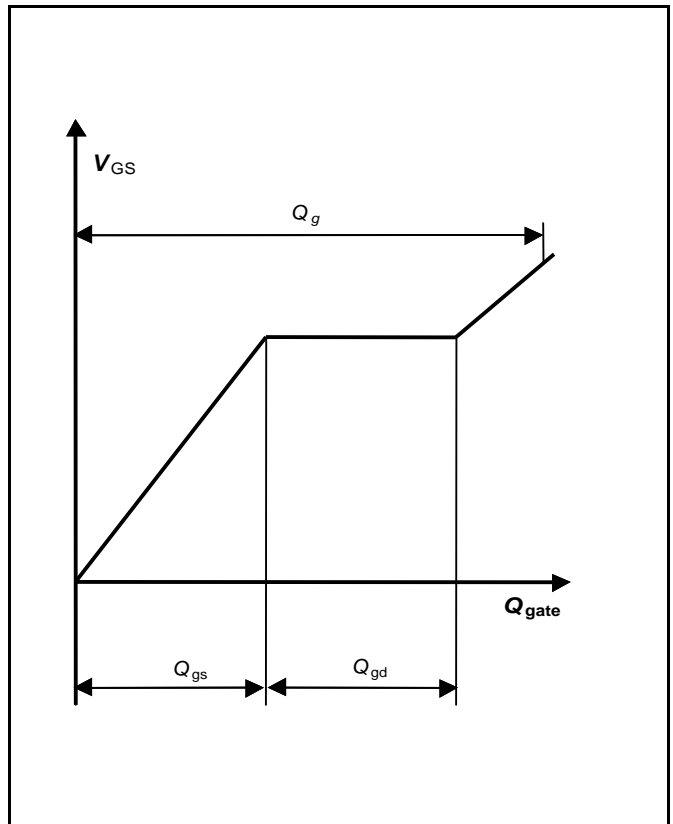
14 Drain-source breakdown voltage



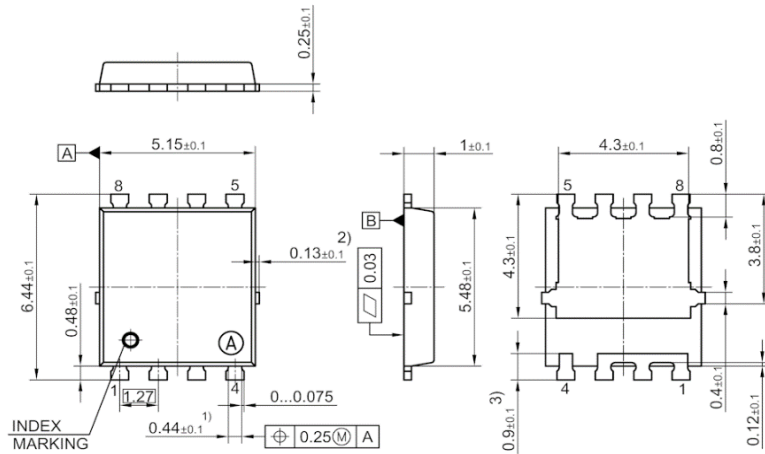
15 Typ. gate charge



16 Gate charge waveforms

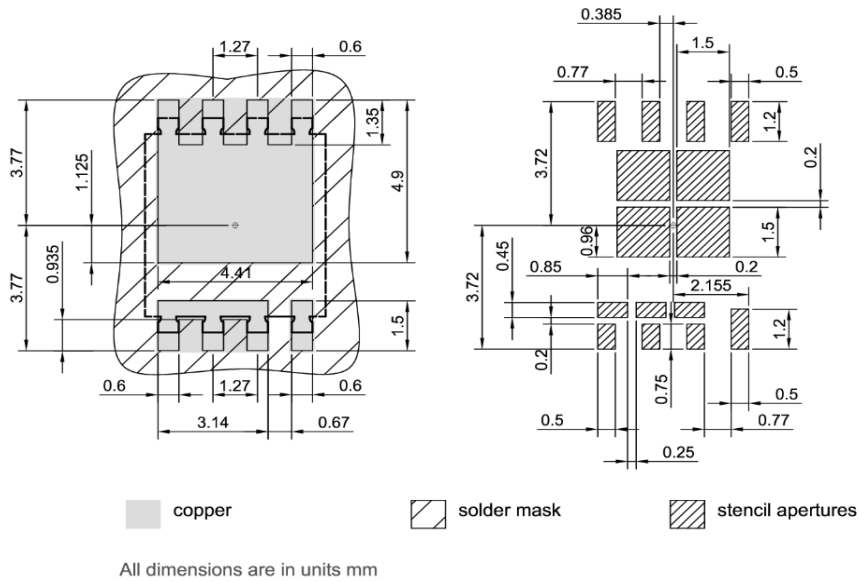


Package Outline

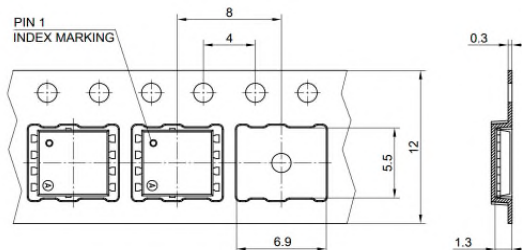


- 1) EXCLUDE MOLD FLASH
 - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 - 3) LEAD LENGTH UP TO ANTI FLASH LINE
 - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Footprint



Packaging



ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Revision History

Revision	Date	Changes
Revision 1.0	04.05.2021	final data sheet
Revision 1.1	14.02.2022	update image of pin layout (page 1)

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