

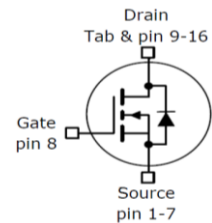
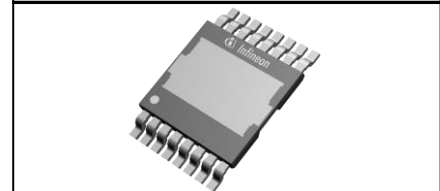
OptiMOS™-5 Power-Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

| | | |
|--------------|-----|----|
| V_{DS} | 100 | V |
| $R_{DS(on)}$ | 1.9 | mΩ |
| I_D | 260 | A |

PG-HDSOP-16-2


| Type | Package | Marking |
|-------------------|-------------------------------|---------|
| IAUS260N10S5N019T | PG-HDSOP-16-2 | 5N10019 |

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|--------------|------|
| Continuous drain current | I_D | $V_{GS}=10\text{ V}$, Chip limitation ^{1,2)} | 260 | A |
| | | $V_{GS}=10\text{V}$, DC current | 260 | |
| | | $T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)} | 91 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$ | 995 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D=130\text{ A}$ | 400 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 220 | A |
| Gate source voltage | V_{GS} | - | ±20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 300 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|----------------------|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics²⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | Top | - | - | 0.5 | K/W |
| | | Bottom (Pin 1-7) | - | 9 | - | |
| | | Bottom (Pin 9-16) | - | 3 | - | |
| Thermal resistance, junction - ambient ⁴⁾ | R_{thJA} | Top | - | 2.8 | - | |
| | | Bottom (through PCB) | - | 40 | - | |

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|---------------|---|-----|-----|-----|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ | 100 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}$, $I_D=210\text{ }\mu\text{A}$ | 2.2 | 3.0 | 3.8 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ | - | 0.1 | 1 | μA |
| | | $V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ °C}^{2)}$ | - | 1 | 20 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=6\text{ V}$, $I_D=65\text{ A}$ | - | 2.0 | 2.6 | m Ω |
| | | $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ | - | 1.6 | 1.9 | |
| Gate resistance ²⁾ | R_G | - | - | 1.2 | - | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|--|---|------|-------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$ | - | 9100 | 11830 | pF |
| Output capacitance | C_{oss} | | - | 1386 | 1801 | |
| Reverse transfer capacitance | C_{rss} | | - | 61 | 92 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=100\text{ A}, R_G=3.5\ \Omega$ | - | 21 | - | ns |
| Rise time | t_r | | - | 11 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 49 | - | |
| Fall time | t_f | | - | 38 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=50\text{ V}, I_D=100\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$ | - | 41 | 54 | nC |
| Gate to drain charge | Q_{gd} | | - | 28 | 42 | |
| Gate charge total | Q_g | | - | 128 | 166 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 4.5 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|---|-----|------|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 260 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | $T_C=25\text{ }^\circ\text{C}, t_p=100\ \mu\text{s}$ | - | - | 2000 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ }^\circ\text{C}$ | - | 0.9 | 1.3 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$ | - | 79 | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 177 | - | nC |

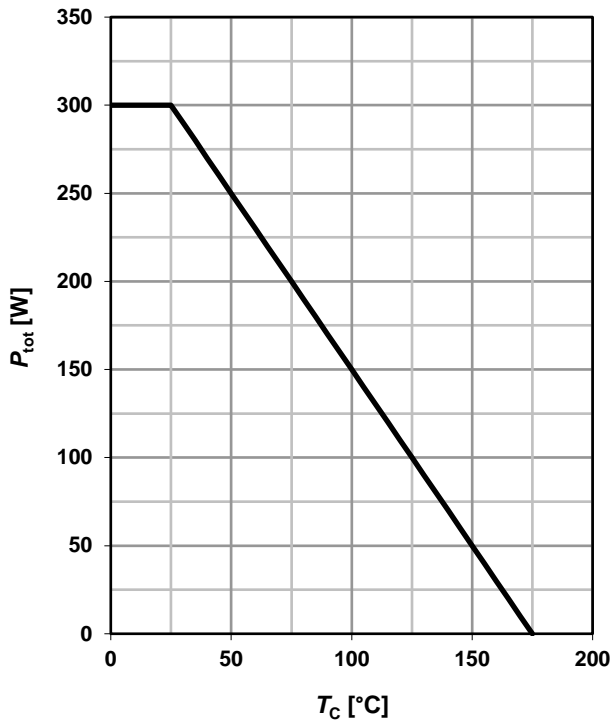
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production testing – specified by design.

⁴⁾ Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100 μm thick and has a conductivity of 0.7 W/mK. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

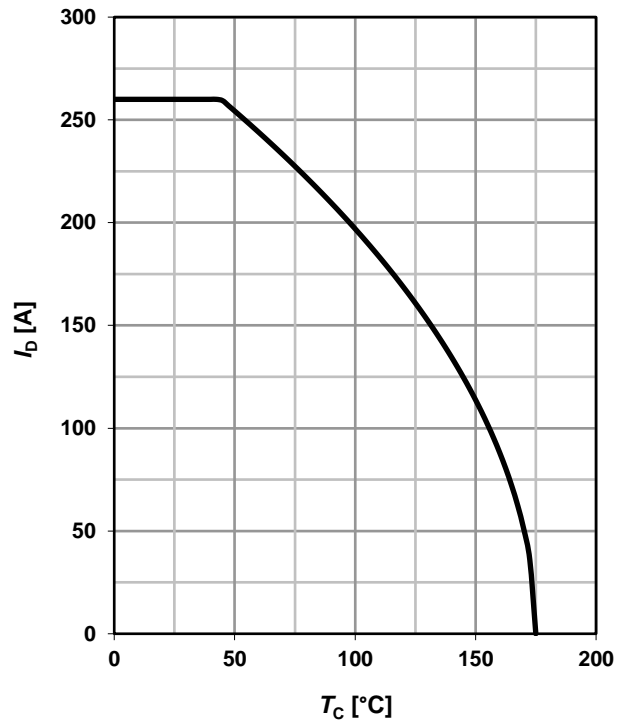
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}$



2 Drain current

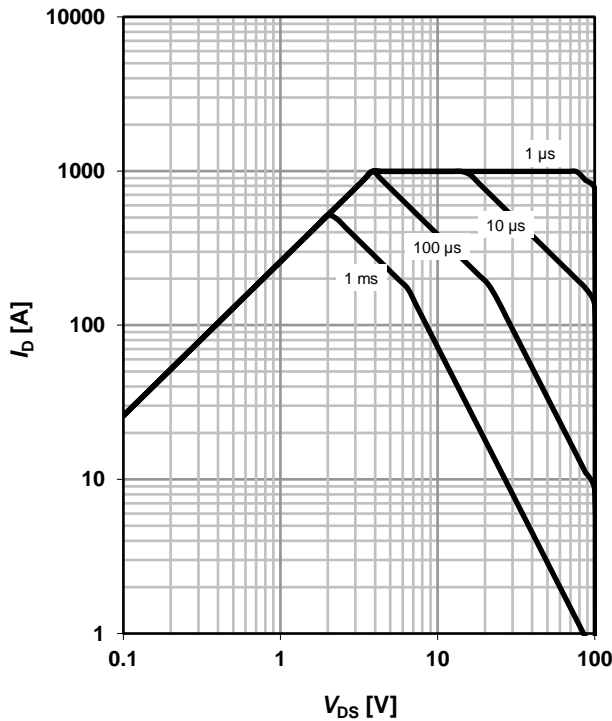
$I_D = f(T_C); V_{GS} \geq 6\text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

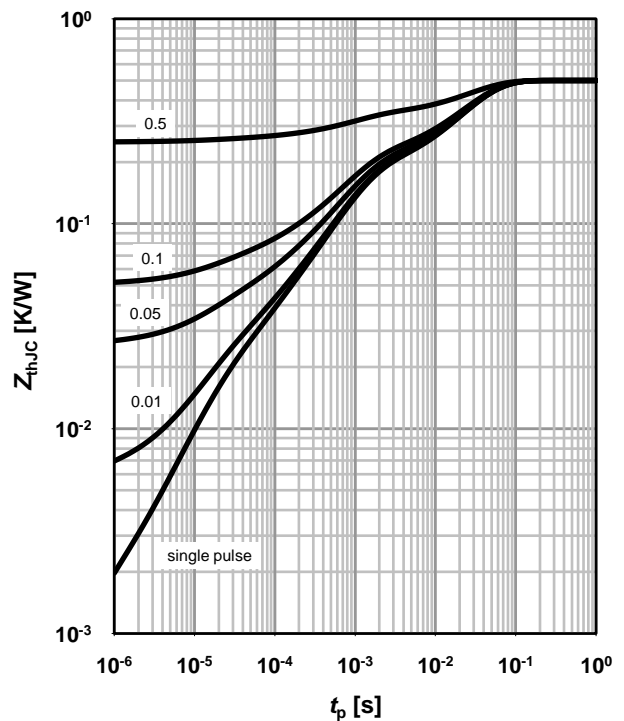
parameter: t_p



4 Max. transient thermal impedance

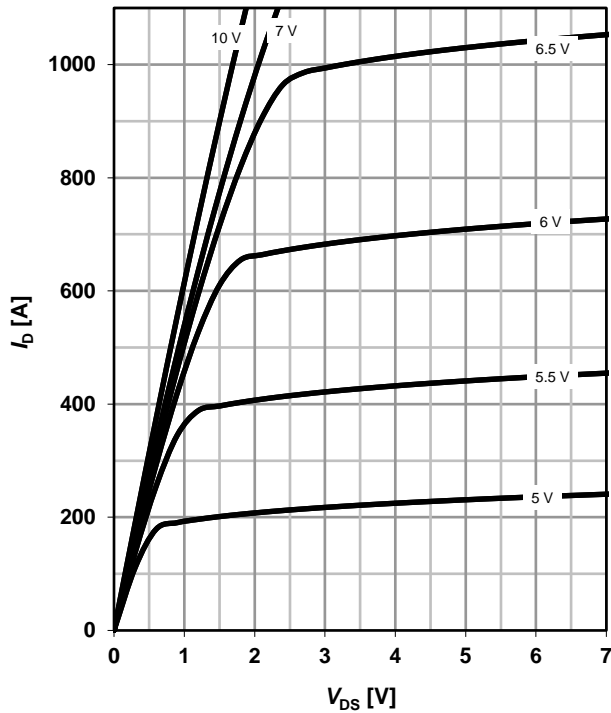
$Z_{thJC} = f(t_p)$

parameter: $D = t_p/T$

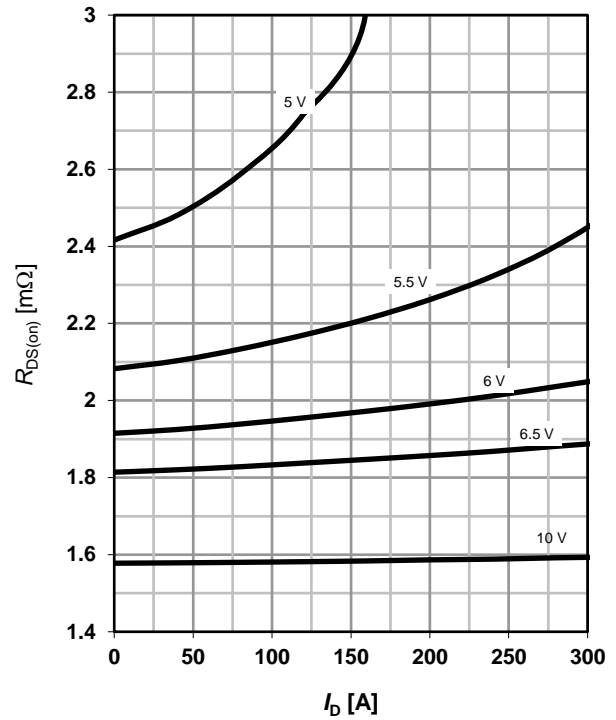


5 Typ. output characteristics

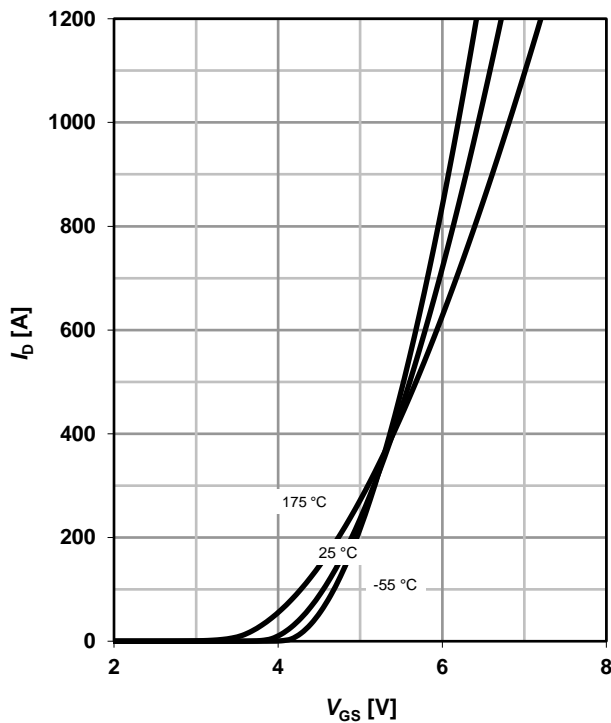
$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance

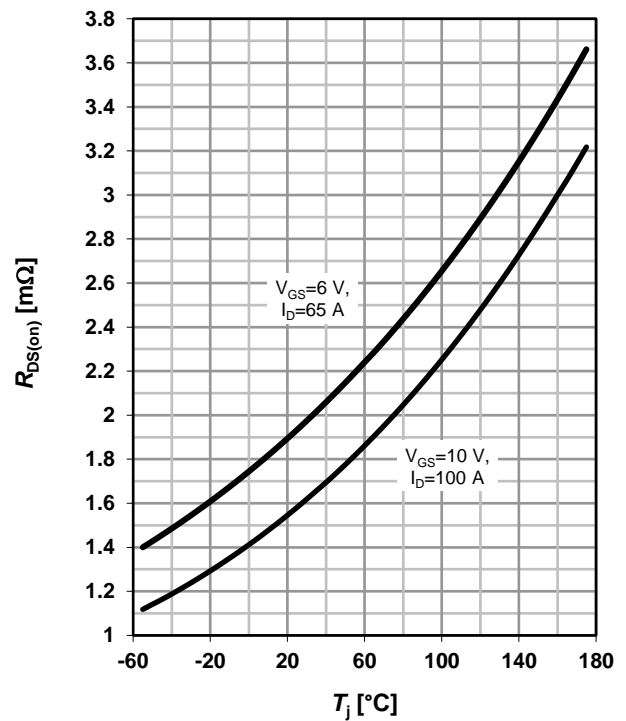
$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

 parameter: T_j

8 Typ. drain-source on-state resistance

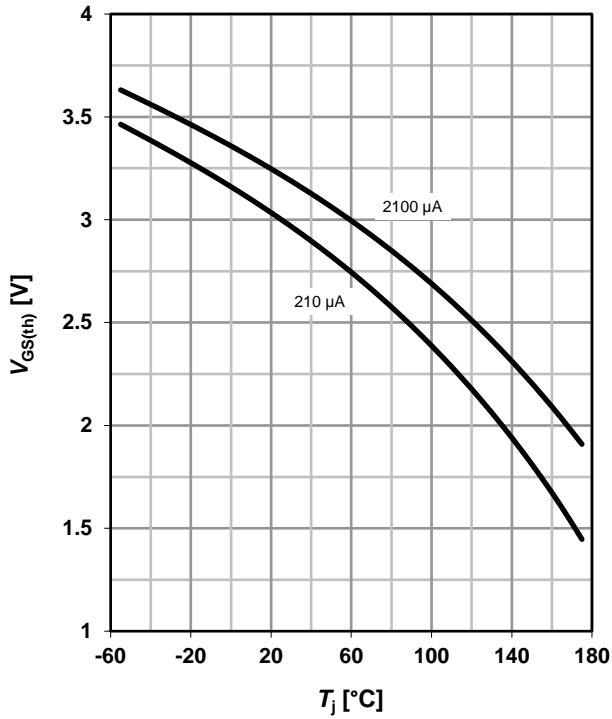
$$R_{DS(on)} = f(T_j)$$

 parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

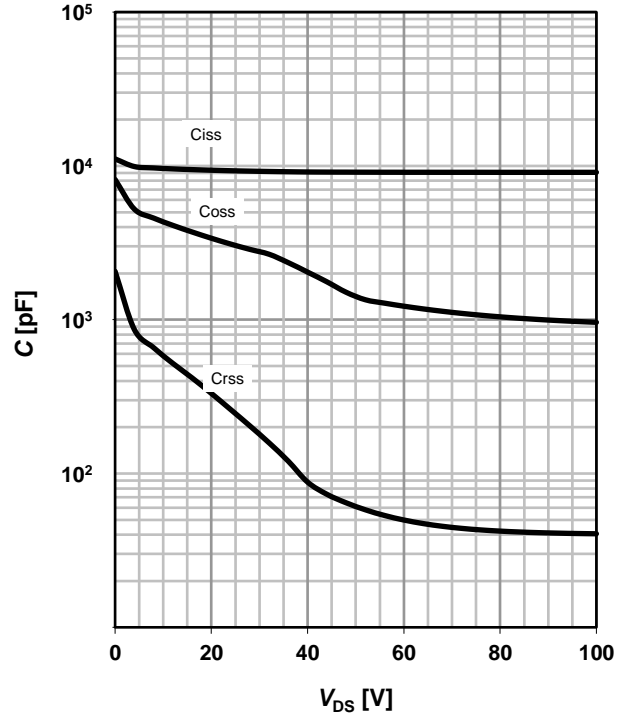
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

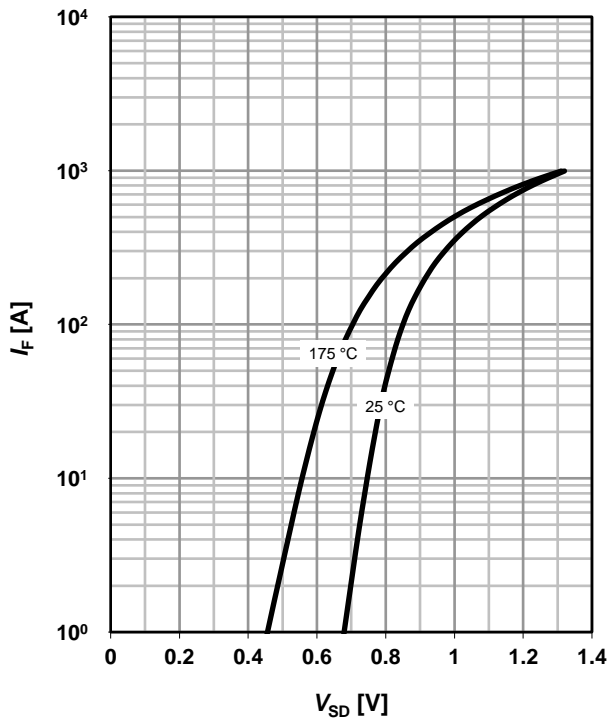
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

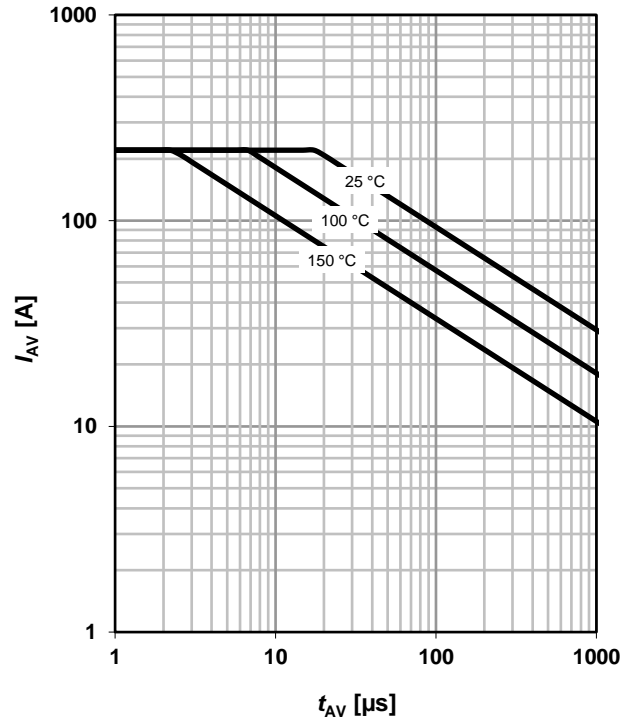
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

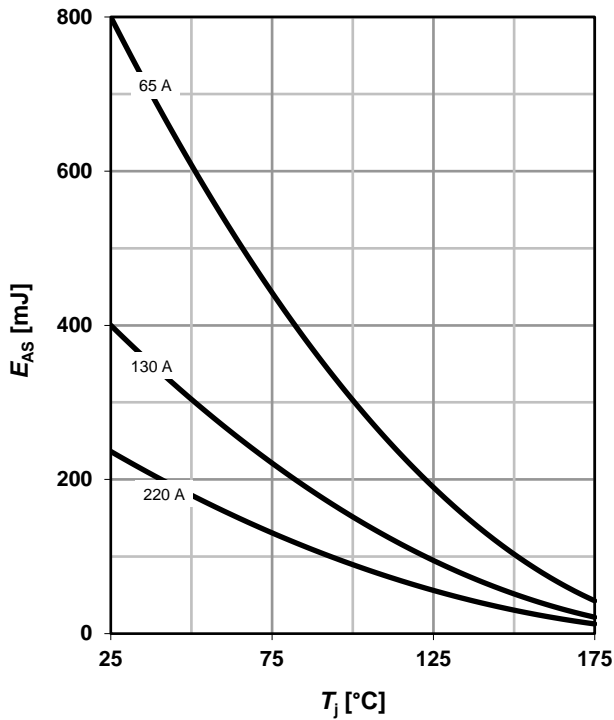
parameter: $T_{j(start)}$



13 Typical avalanche energy

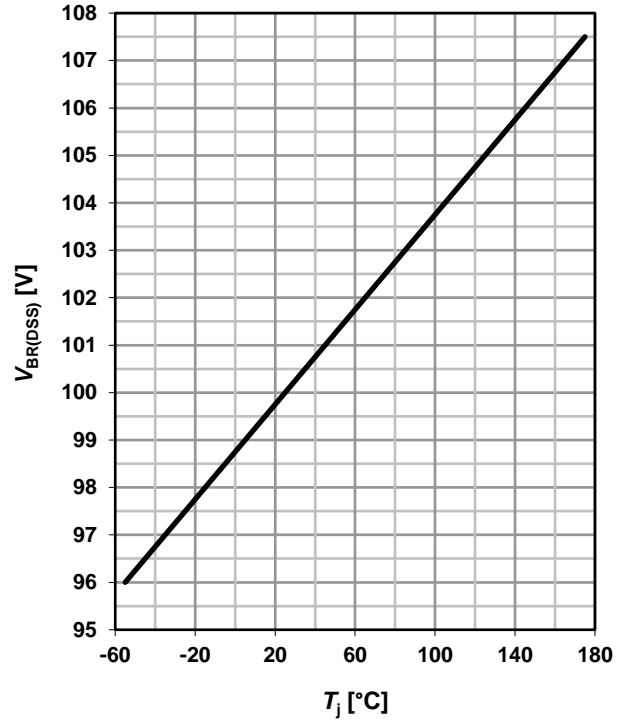
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

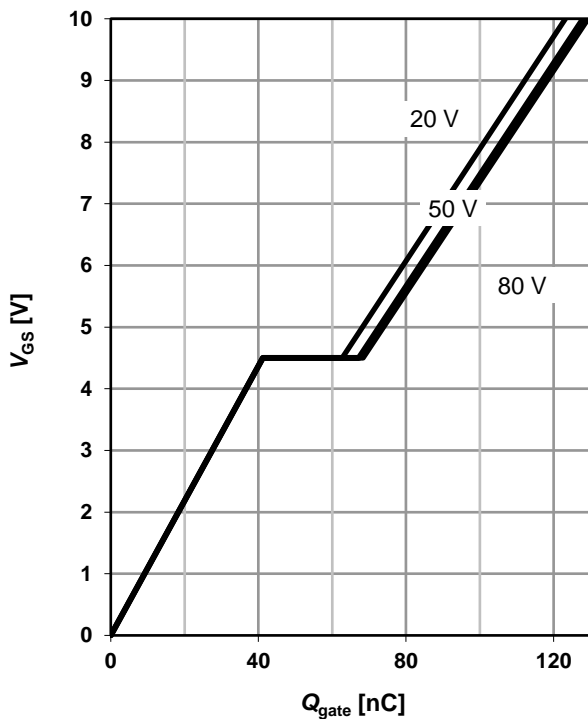
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



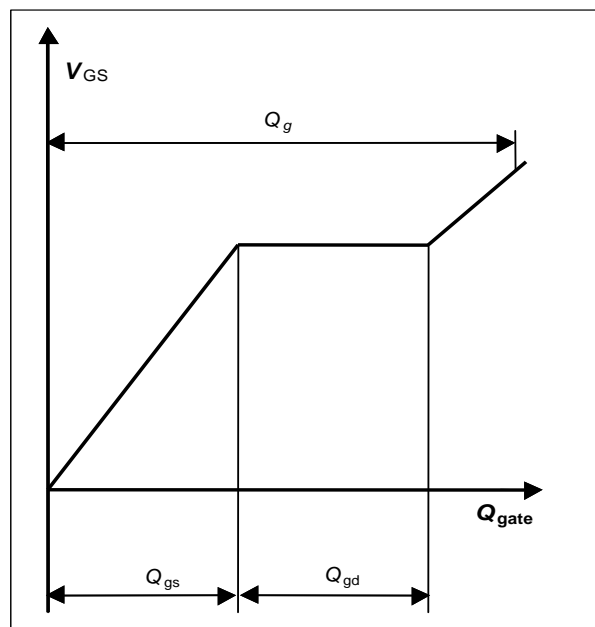
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 100 \text{ A pulsed}$$

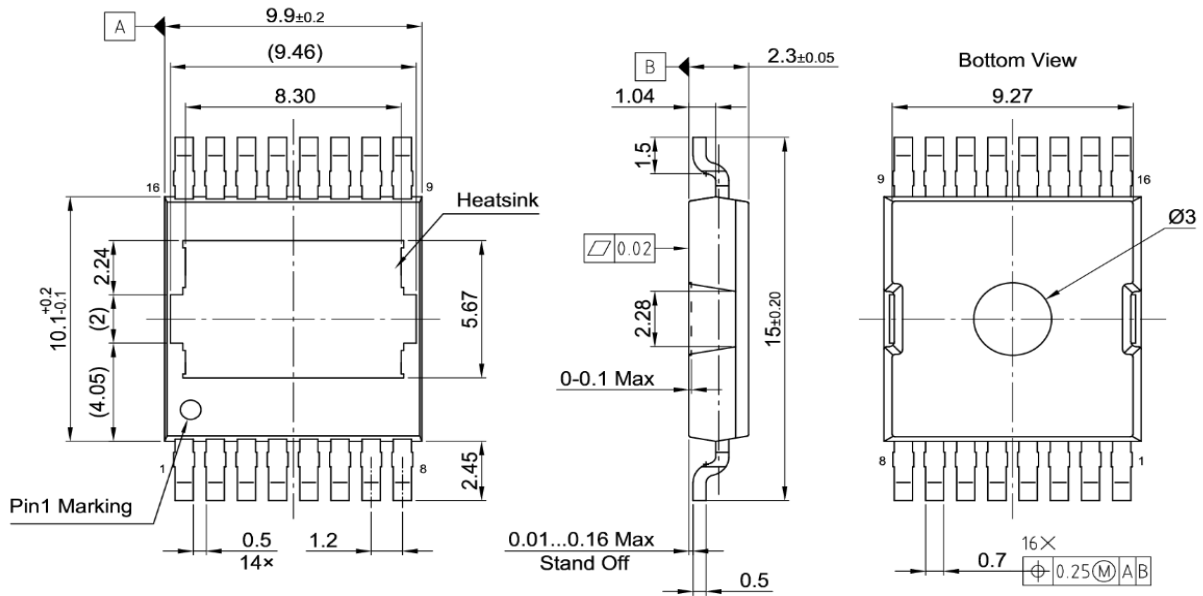
parameter: V_{DD}



16 Gate charge waveforms

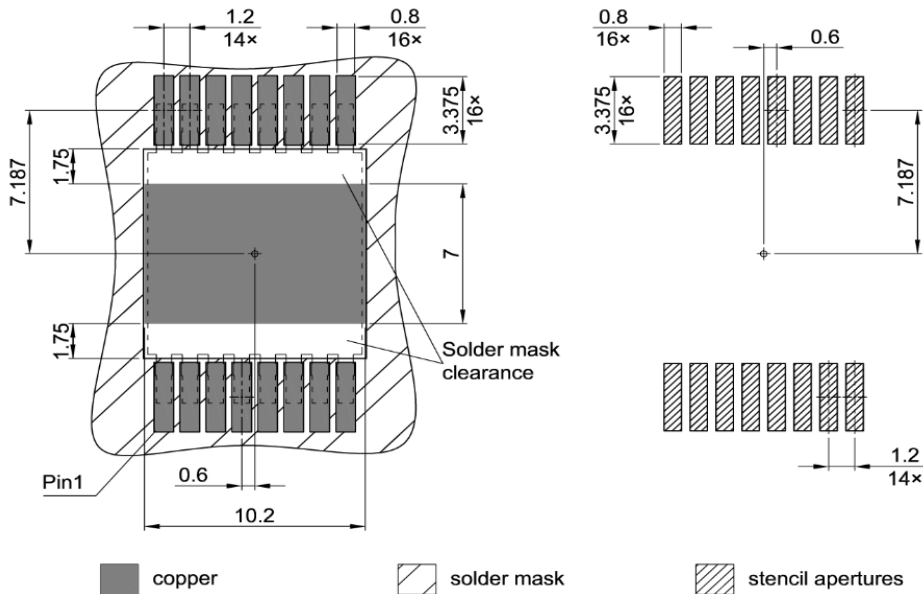


Package Outline



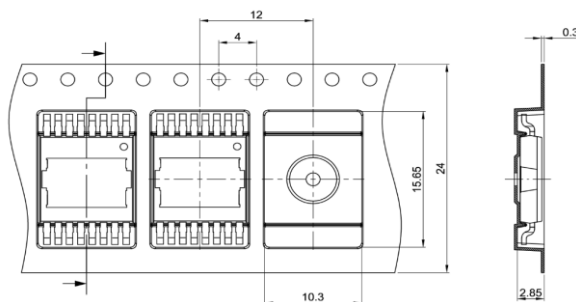
All metal surfaces tin plated except area of cut and heatsink
 All dimensions are in units mm
 The drawing is in compliance with ISO 128-30, Projection Method 1 []

Footprint



Based on stencil thickness 0.20 mm
 All dimensions are in units mm

Packaging



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Revision History

| Version | Date | Changes |
|-------------|------------|-----------------|
| Version 1.0 | 01.10.2020 | Final Datasheet |

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