

# Fixed Frequency 700 V/800 V CoolSET™ - in DIP-7 Package

## Product highlights

- Integrated 700 V/ 800 V avalanche rugged CoolMOS™
- Enhanced Active Burst Mode with selectable entry and exit standby power to reach the lowest standby power <100 mW
- Digital frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- Frequency jitter and soft gate driving for low EMI
- Integrated error amplifier
- Comprehensive protection
- Pb-free lead plating, halogen-free mold compound, RoHS compliant



## Features

- Integrated 700 V/ 800 V avalanche rugged CoolMOS™
- Enhanced Active Burst Mode with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- DCM and CCM operation with slope compensation
- Frequency jitter and soft gate driving for low EMI
- Built-in digital soft start
- Integrated error amplifier to support direct feedback in non-isolated flyback
- Comprehensive protection with  $V_{CC}$  over voltage,  $V_{CC}$  under voltage, overload/open loop, over temperature
- All protections are in auto restart mode
- Limited charging current for  $V_{CC}$  short to GND

## Applications

- Auxiliary power supply for home appliances/white goods, TV, PC & server
- Blu-ray player, set-top box & LCD/LED monitor

## Product validation

Product qualified according to JEDEC Standard

## Description

The ICE5ARxxxxBZS is the 5<sup>th</sup> generation of fixed frequency integrated power IC (CoolSET™) optimized for off-line switch mode power supply in cascode configuration. The CoolSET™ package has 2 separate chips inside; one is controller chip and the other is a 700 V/ 800 V CoolMOS™ chip. The cascode configuration helps achieve fast startup. The frequency reduction with soft gate driving and frequency jitter operation offers lower EMI and better efficiency between light load and 50% load. The selectable entry and exit standby power ABM enables flexibility and ultra-low power consumption at standby mode with small and controllable output voltage ripple. The product has a wide operating range (10.0 ~ 25.5 V) of IC power supply and lower power consumption. The numerous protection functions support the power supply system in failure situations. All these make the 5<sup>th</sup> generation CoolSET™ series an outstanding integrated power stage fixed frequency flyback converter in the market.



Pin configuration and functionality

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## Pin configuration and functionality

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Pin configuration and functionality

# 1 Pin configuration and functionality

The pin configuration is shown in Figure 3 and the functions are described in Table 2.

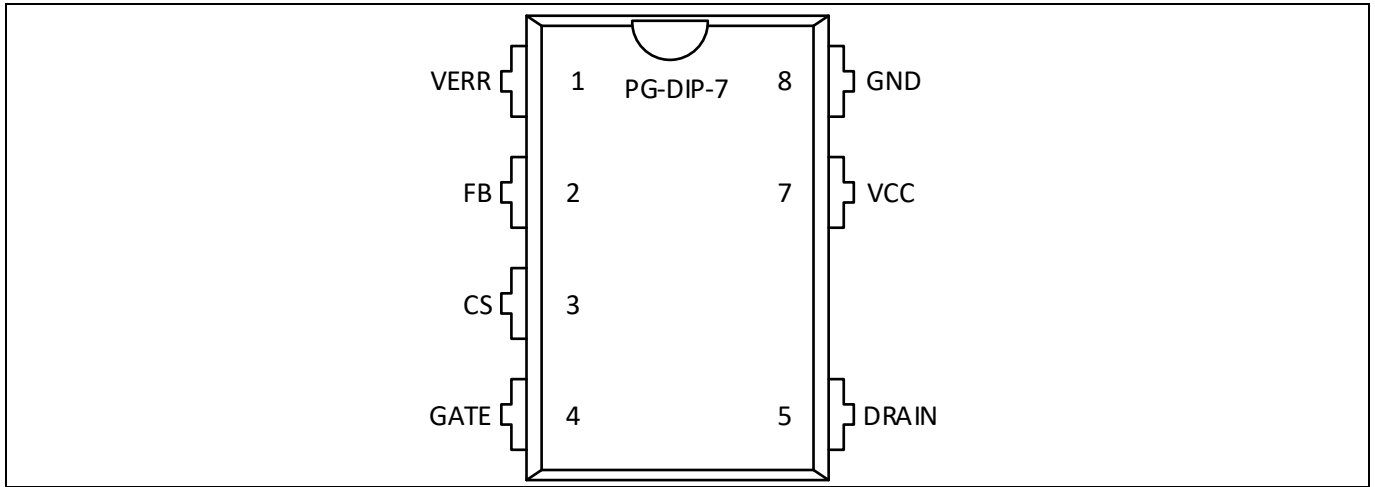


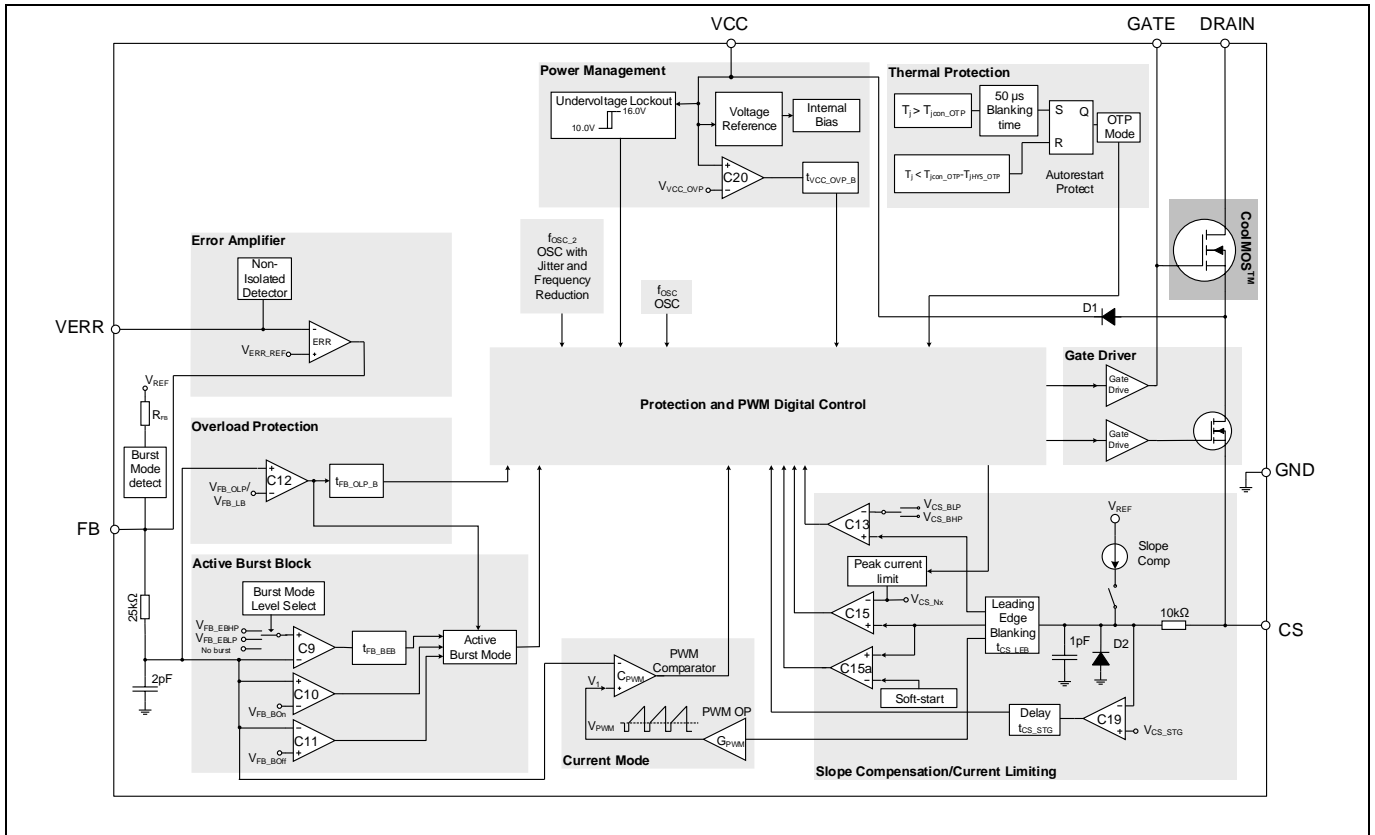
Figure 3 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	VERR	Error amplifier VERR pin is internally connected to the transconductance error amplifier for non-isolated flyback application. Connect this pin to GND for isolated flyback application.
2	FB	Feedback and ABM entry/exit control FB pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
3	CS	Current sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.
4	GATE	Gate driver output The GATE pin is connected to the Gate of the internal CoolMOS™ and additionally, a pull up resistor is connected from bus voltage to turn on the internal CoolMOS™ for charging up the V <sub>CC</sub> capacitor during startup.
5	DRAIN	DRAIN(Drain of integrated CoolMOS™) The DRAIN pin is connected to the drain of the integrated CoolMOS™.
7	VCC	VCC(Positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V <sub>VCC_OFF</sub> and V <sub>VCC_OVP</sub> .
8	GND	Ground The GND pin is the common ground of the controller.

Representative block diagram

## 2 Representative block diagram



**Figure 4** Representative block diagram

*Note:* Junction temperature of the controller chip is sensed for over temperature protection. The CoolMOS™ is a separate chip from the controller chip in the same package. Please refer to the design guide and/or consult a technical expert for the proper thermal design.

Functional description

### 3 Functional description

#### 3.1 V<sub>CC</sub> pre-charging and typical V<sub>CC</sub> voltage during start-up

As shown in Figure 1, once the line input voltage is applied, a rectified voltage appears across the capacitor C<sub>BUS</sub>. The pull up resistor R<sub>STARTUP</sub> provides a current to charge the C<sub>iss</sub> (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over C<sub>iss</sub> is high enough, CoolMOS™ on and V<sub>CC</sub> capacitor will be charged through primary inductance of transformer L<sub>P</sub>, CoolMOS™ and internal diode D<sub>1</sub> with two steps constant current source I<sub>VCC\_Charge1</sub><sup>1</sup> and I<sub>VCC\_Charge3</sub><sup>1</sup>.

A very small constant current source (I<sub>VCC\_Charge1</sub>) is charged to the V<sub>CC</sub> capacitor till V<sub>CC</sub> reach V<sub>VCC\_SCP</sub> to protect the controller from V<sub>CC</sub> pin short to ground during the start up. After this, the second step constant current source (I<sub>VCC\_Charge3</sub>) is provided to charge the V<sub>CC</sub> capacitor further, until the V<sub>CC</sub> voltage exceeds the turned-on threshold V<sub>VCC\_ON</sub>. As shown in the time phase I in Figure 5, the V<sub>CC</sub> voltage increase almost linearly with two steps.

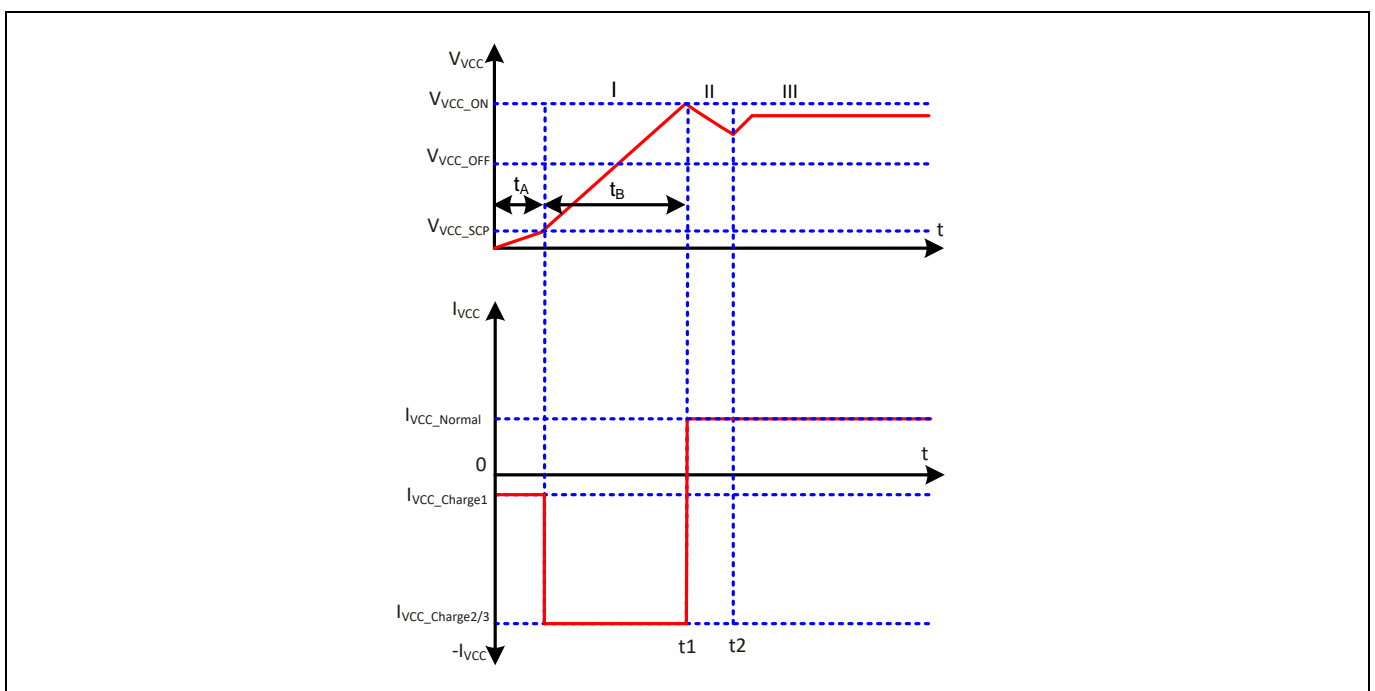


Figure 5 V<sub>CC</sub> voltage and current at startup

The time taking for the V<sub>CC</sub> pre-charging can then be approximately calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \tag{1}$$

When the V<sub>CC</sub> voltage exceeds the V<sub>CC</sub> turn on threshold V<sub>VCC\_ON</sub> at time t<sub>1</sub>, the IC begins to operate with soft-start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V<sub>CC</sub> capacitor before the output voltage is built up, the V<sub>CC</sub> voltage drops (Phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V<sub>CC</sub> capacitor from the time t<sub>2</sub> onward and delivering the I<sub>VCC\_Normal</sub><sup>2</sup> to the CoolSET™. The V<sub>CC</sub> then will reach a constant value depending on output load.

<sup>1</sup> I<sub>VCC\_Charge1/2/3</sub> is charging current from the controller to VCC capacitor during start up

<sup>2</sup> I<sub>VCC\_Normal</sub> is supply current from VCC capacitor or auxiliary winding to the CoolSET™ during normal operation

## Functional description

### 3.2 Soft-start

As shown in Figure 6, the IC begins to operate with a soft-start at time  $t_{on}$ . The switching stresses on the power MOSFET, diode and transformer are minimized during soft-start. The soft-start implemented in ICE5ARxxxBZS is a digital time-based function. The preset soft-start time is  $t_{ss}$  (12 ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to  $V_{CS\_N}$  (0.8 V) finally. The normal feedback loop will take over the control when the output voltage reaches its regulated value.

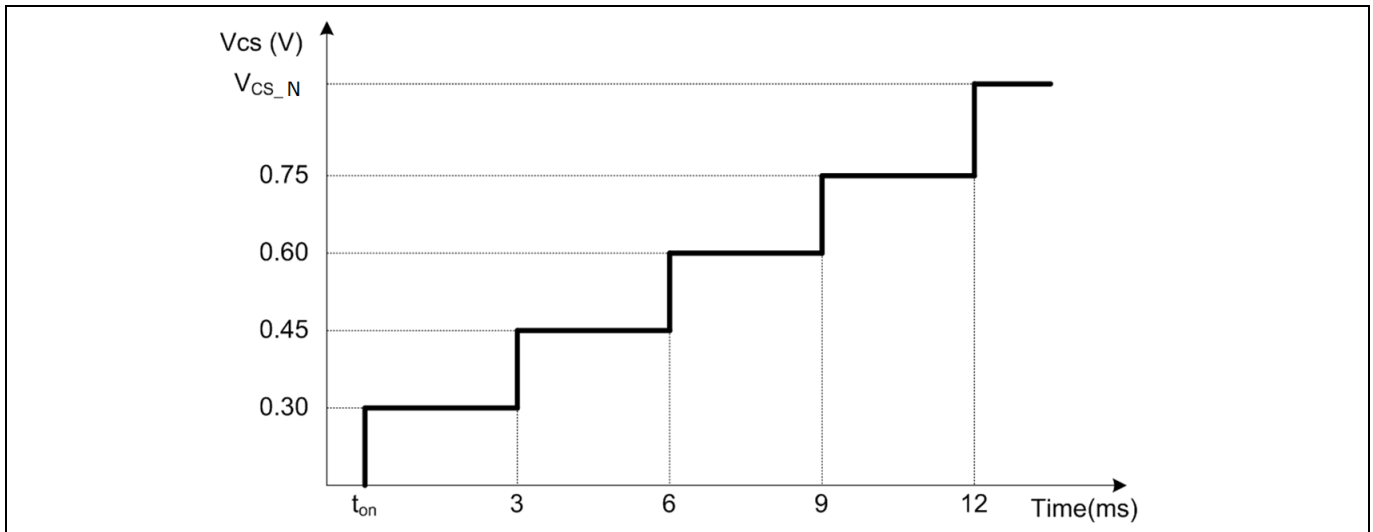


Figure 6 Maximum current sense voltage during soft start

### 3.3 Normal operation

The PWM controller during normal operation consists of a digital signal processing circuit including regulation control and an analog circuit including a current measurement unit and a comparator. Details about the full operation of the CoolSET™ in normal operation are illustrated in the following paragraphs.

#### 3.3.1 PWM operation and peak current mode control

##### 3.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator with a switching frequency  $f_{sw}$  that corresponds to the voltage level  $V_{FB}$  (see Figure 8).

##### 3.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage  $V_1$  (see Figure 4) which is the representation of the instantaneous current of the power MOSFET. When  $V_1$  exceeds  $V_{FB}$ , the PWM comparator sends a signal to switch off the GATE of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the feedback voltage  $V_{FB}$  (see Figure 7).

At switch on transient of the power MOSFET, a voltage spike across  $R_{CS}$  can cause  $V_1$  to increase and exceed  $V_{FB}$ . To avoid a false switch off, the IC has a blanking time  $t_{CS\_LEB}$  before detecting the voltage across  $R_{CS}$  to mask the voltage spike. Therefore, the minimum turn on time of the power MOSFET is  $t_{CS\_LEB}$ .

For some reason that the voltage level at  $V_1$  takes long time to exceed  $V_{FB}$ , the IC has implemented a maximum duty cycle control to force the power MOSFET to switch off when  $D_{MAX} = 0.75$  is reached.



Functional description

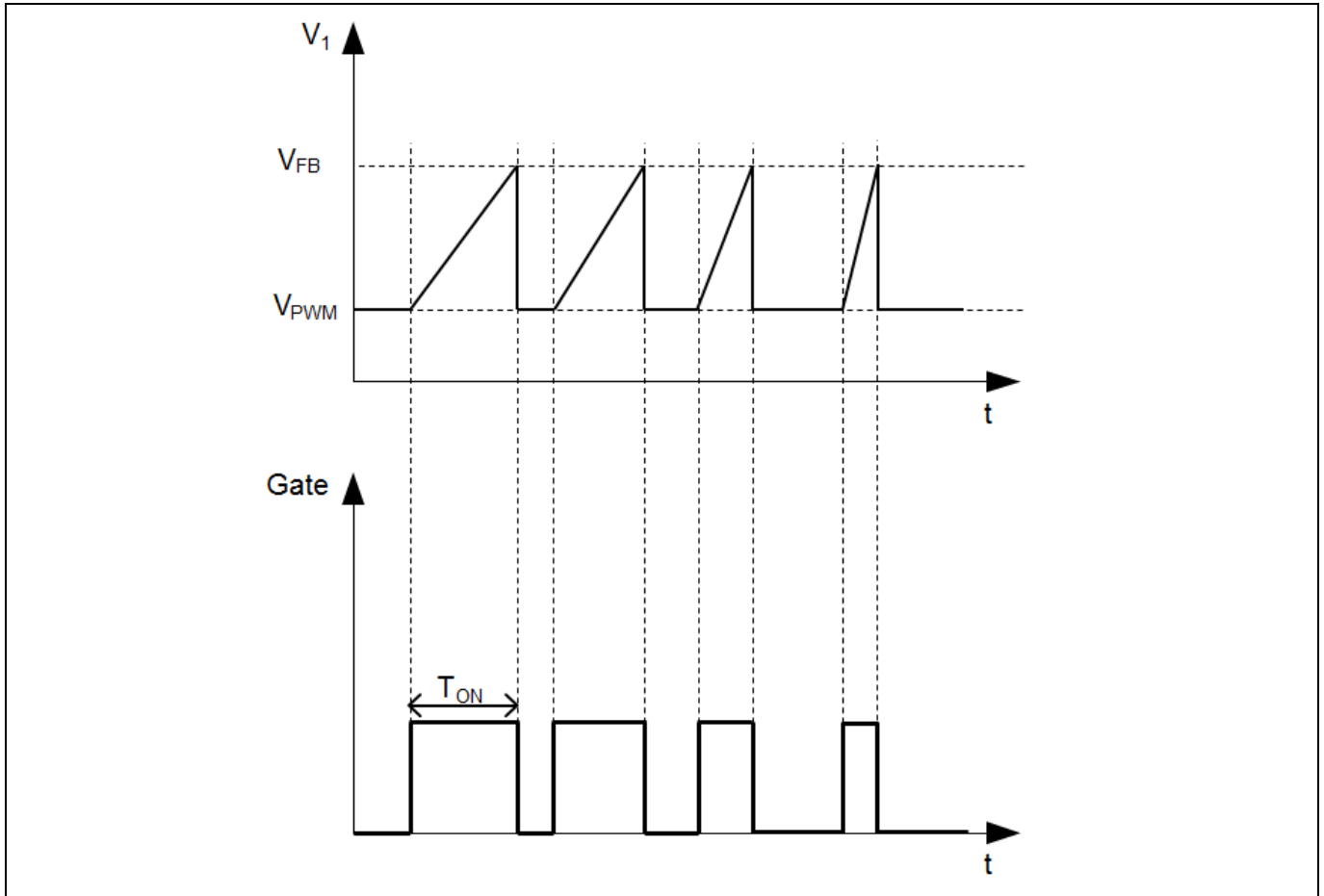


Figure 7 Pulse width modulation

3.3.2 Current sense

The power MOSFET current generates a voltage  $V_{CS}$  across the current sense resistor  $R_{CS}$  connected between the CS pin and the GND pin.  $V_{CS}$  is amplified with gain  $G_{PWM}$ , then, added with an offset  $V_{PWM}$  to become  $V_1$  as described below in below equation 3.

$$V_{CS} = I_D \times R_{CS} \tag{2}$$

$$V_1 = V_{CS} * G_{PWM} + V_{PWM} \tag{3}$$

- where,  $V_{CS}$  : CS pin voltage
- $I_D$  : power MOSFET current
- $R_{CS}$  : resistance of the current sense resistor
- $V_1$  : voltage level compared to  $V_{FB}$  as described in section 3.3.1.2
- $G_{PWM}$  : PWM-OP gain
- $V_{PWM}$  : offset for voltage ramp

If the voltage at the current sense pin is lower than the preset threshold  $V_{CS\_STG}$  after the time  $t_{CS\_STG\_SAM}$  for three consecutive pulses during on-time of the power switch, this abnormal  $V_{CS}$  will trigger IC into auto restart mode.

Functional description

### 3.3.3 Frequency reduction

Frequency reduction is implemented in ICE5ARxxxxBZS to achieve a better efficiency during the light load. At light load, the reduced switching frequency  $F_{SW}$  improves efficiency by reducing the switching losses.

When load decreases,  $V_{FB}$  decreases as well.  $F_{SW}$  is dependent on the  $V_{FB}$  as shown in Figure 8. Therefore,  $F_{SW}$  decreases as the load decreases.

Typically,  $F_{SW}$  at high load is 100 kHz and starts to decrease at  $V_{FB} = 1.7V$ . There is no further frequency reduction once it reached the  $f_{OSC4\_MIN}$  even the load is further reduced.

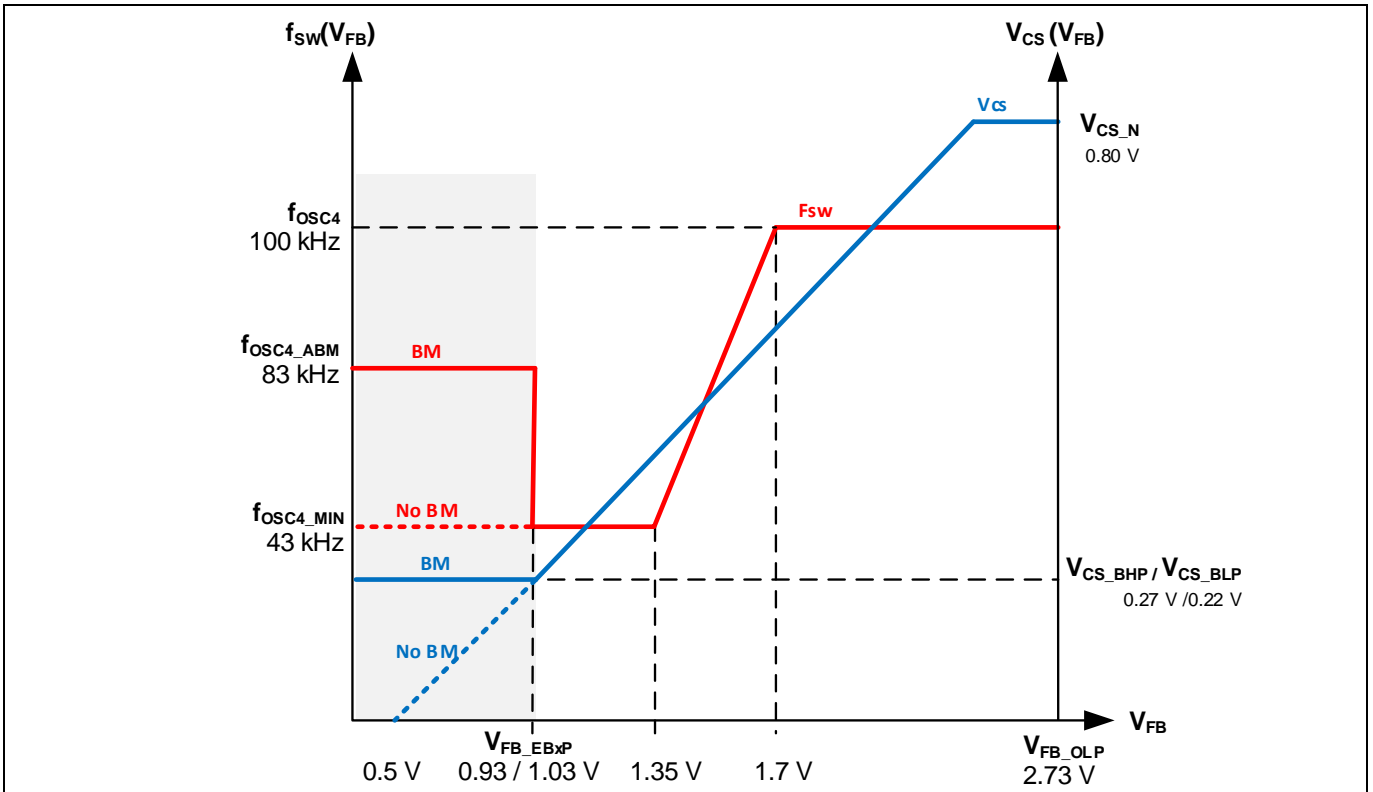


Figure 8 Frequency reduction curve

### 3.3.4 Slope compensation

ICE5ARxxxxBZS can operate at Continuous Conduction Mode (CCM). At CCM operation, duty cycle greater than 50% may generate a sub-harmonic oscillation. To avoid the sub-harmonic oscillation, slope compensation is added to  $V_{CS}$  pin when the gate of the power MOSFET is turned on for more than 40% of the switching cycle period. The relationship between  $V_{FB}$  and the  $V_{CS}$  for CCM operation is described in below equation 4:

$$V_{FB} = V_{CS} * G_{PWM} + V_{PWM} + M_{COMP} * (T_{ON} - 40\% * T_{PERIOD}) \tag{4}$$

where,  $T_{ON}$  : gate turn on time of the power MOSFET

$M_{COMP}$  : slope compensation rate

$T_{PERIOD}$  : switching cycle period

Slope compensation circuit is disabled and no slope compensation is added into the  $V_{CS}$  pin during active burst mode to save the power consumption.

Functional description

### 3.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 100 kHz with frequency jittering of ±4% at a jittering period of  $T_{JITTER}$  (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

### 3.3.6 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of driver (see Figure 9). Thus the leading switch spike during turn on is minimized.

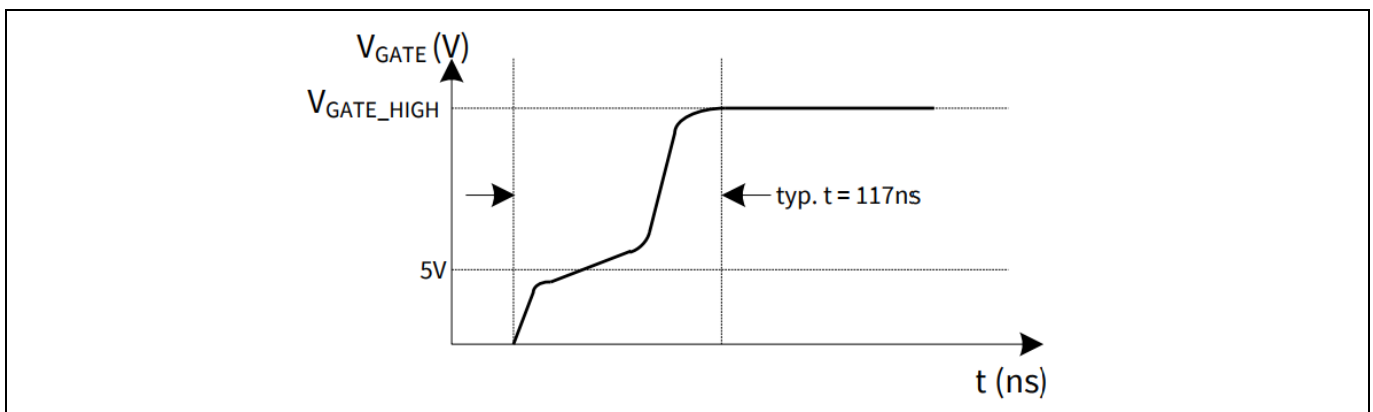


Figure 9 Gate rising waveform

## 3.4 Peak current limitation

There is a cycle by cycle peak current limitation realized by the current limit comparator to provide primary over-current protection. The primary current generates a voltage  $V_{CS}$  across the current sense resistor  $R_{CS}$  connected between the CS pin and the GND pin. If the voltage  $V_{CS}$  exceeds an internal voltage limit  $V_{CS\_N}$ , the comparator immediately turns off the gate drive.

The primary peak current  $I_{PEAK\_PRI}$  can be calculated as below:

$$I_{PEAK\_PRI} = V_{CS\_N} / R_{CS} \tag{5}$$

To avoid mistriggering caused by MOSFET switch on transient voltage spikes, a leading edge blanking time ( $t_{CS\_LEB}$ ) is integrated in the current sensing path.

### 3.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the  $V_{CS}$  to switching the power MOSFET off. An overshoot on the peak current  $I_{peak}$  caused by the delay depends on the ratio of  $di/dt$  of the primary current (see Figure 10).

Functional description

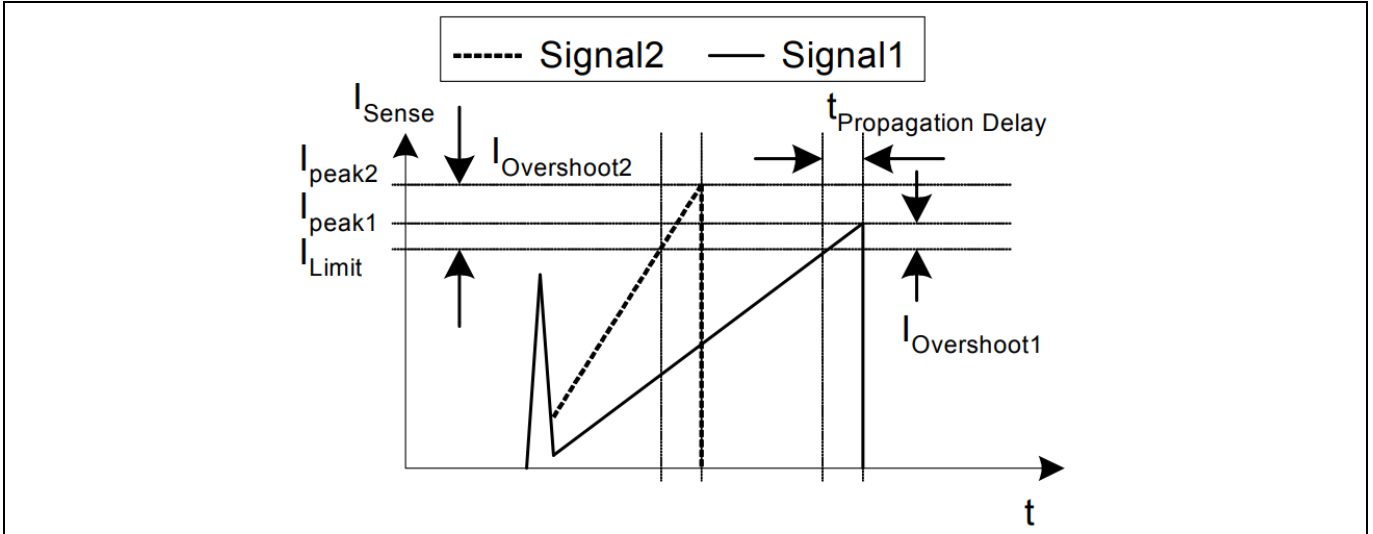


Figure 10 Current limiting

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to  $di/dt$  of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold  $V_{CS\_N}$  and the switching off of the power MOSFET is compensated over wide bus voltage range. Current limiting becomes more accurate which will result in a minimum difference of overload protection triggering power between low and high AC line input voltage.

Under CCM operation, the same  $V_{CS}$  do not result in the same power. In order to achieve a close overload triggering level for CCM, ICE5ARxxxxBZS has implemented a 2 compensation curve as shown Figure 11. One of the curve is used for  $T_{ON}$  greater than 0.40 duty cycle and the other is for lower than 0.40 duty cycle.

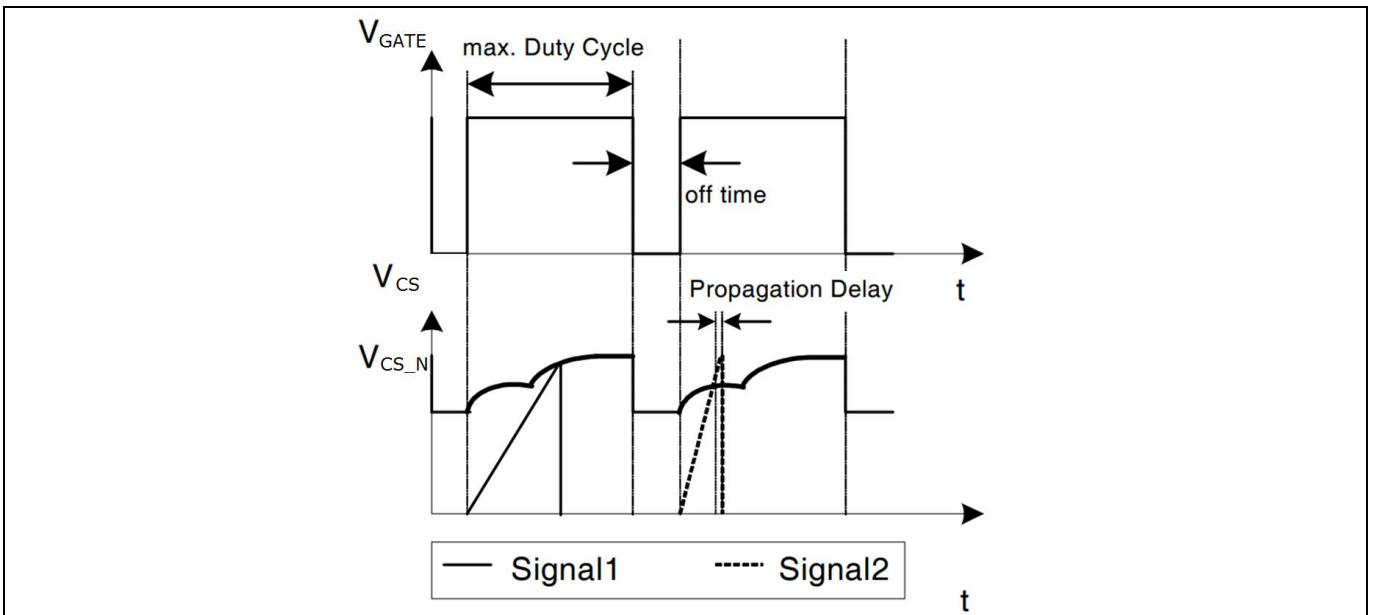


Figure 11 Dynamic voltage threshold  $V_{CS\_N}$

Similarly, the same concept of propagation delay compensation is also implemented in ABM with reduced level. With this implementation, the entry and exit burst mode power can be close between low and high AC line input voltage.

## Functional description

### 3.5 Active Burst Mode (ABM) with selectable power level

At light load condition, the IC enters ABM operation to minimize the power consumption. Details about ABM operation are explained in the following paragraphs.

#### 3.5.1 Entering ABM operation

The system will enter into ABM operation when two conditions below are met:

- the FB voltage is lower than the threshold of  $V_{FB\_EBLP}/V_{FB\_EBHP}$  depending on burst configuration option setup
- and a certain blanking time  $t_{FB\_BEB}$

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of entering ABM operation, so that the controller enters ABM operation only when the output power is really low.

#### 3.5.2 During ABM operation

After entering ABM, the PWM section will be inactive making the  $V_{OUT}$  start to decrease. As the  $V_{OUT}$  decreases,  $V_{FB}$  rises. Once  $V_{FB}$  exceeded  $V_{FB\_BON}$ , the internal circuit is again activated by the internal bias to start with the switching.

If the PWM is still operating and the output load is still low,  $V_{OUT}$  increases and  $V_{FB}$  signal starts to decrease. When  $V_{FB}$  reaches the low threshold  $V_{FB\_BOFF}$ , the internal bias is reset again and the PWM section is disabled with no switching until  $V_{FB}$  increases back to exceed  $V_{FB\_BON}$  threshold.

In ABM,  $V_{FB}$  is like a sawtooth waveform swinging between  $V_{FB\_BOFF}$  and  $V_{FB\_BON}$  shown in Figure 12.

During ABM, the switching frequency  $f_{OSC4\_ABM}$  is 83 kHz. The peak current  $I_{PEAK\_ABM}$  of the power MOSFET is defined by:

$$I_{PEAK\_ABM} = V_{CS\_BXP} / R_{CS} \quad (6)$$

where  $V_{CS\_BXP}$  is the peak current limitation in ABM

#### 3.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When  $V_{FB}$  exceeds  $V_{FB\_LB}$ , it will leave ABM and the peak current limitation threshold voltage will return back to  $V_{CS\_N}$  immediately.

Functional description

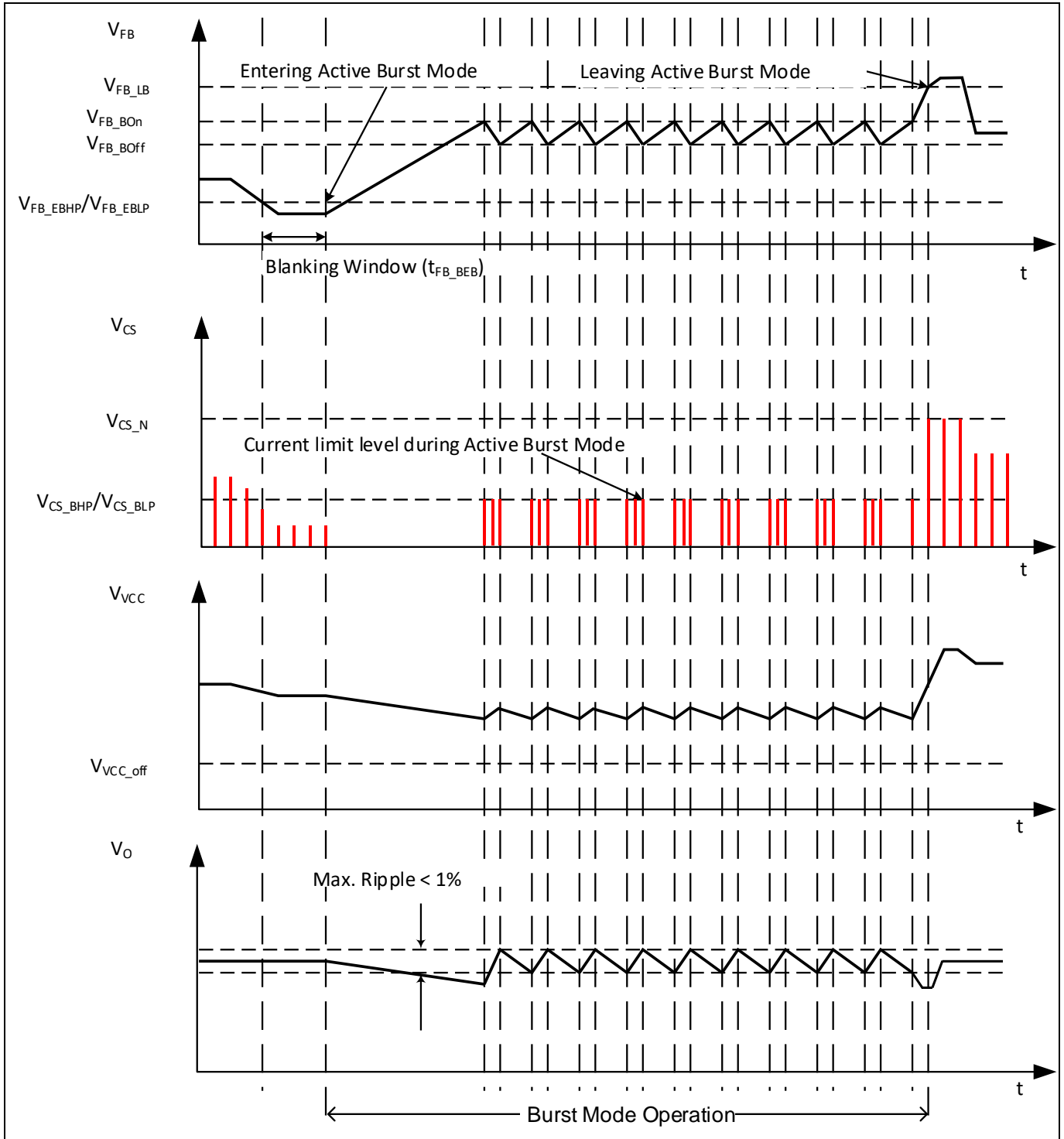


Figure 12 Signals in Active Burst Mode

Functional description

3.5.4 ABM configuration

The burst mode entry level can be selected by changing the different resistance  $R_{sel}$  at FB pin. There are 3 configuration options depending on  $R_{sel}$  which corresponds to the options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit level with the FB voltage.

Table 3 ABM configuration option setup

Option	$R_{sel}$	$V_{FB}$	$V_{CS\_BxP}$	Entry level	Exit level
				$V_{FB\_EBxP}$	$V_{FB\_LB}$
1	<470 k $\Omega$	$V_{FB} < V_{FB\_P\_BIAS1}$	-	No ABM	No ABM
2	720 k $\Omega$ ~ 790 k $\Omega$	$V_{FB\_P\_BIAS1} < V_{FB} < V_{FB\_P\_BIAS2}$	0.22V	0.93 V	2.73 V
3(Default)	>1210 k $\Omega$	$V_{FB} > V_{FB\_P\_BIAS2}$	0.27V	1.03 V	2.73 V

During IC first startup, the controller preset the ABM selection to Option 3, the FB resistor ( $R_{FB}$ ) is turned off by internal switch  $S_2$  (see Figure 13) and a current source  $I_{sel}$  is turned on instead. From  $V_{CC} = 4.44$  V to  $V_{CC}$  on threshold, the FB pin will start to charge resistor  $R_{sel}$  with current  $I_{sel}$  to a certain voltage level. When  $V_{CC}$  reaches  $V_{CC}$  on threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option and the current source ( $I_{sel}$ ) is turned off while the FB resistor ( $R_{FB}$ ) is connected back to the circuit (Figure 13).

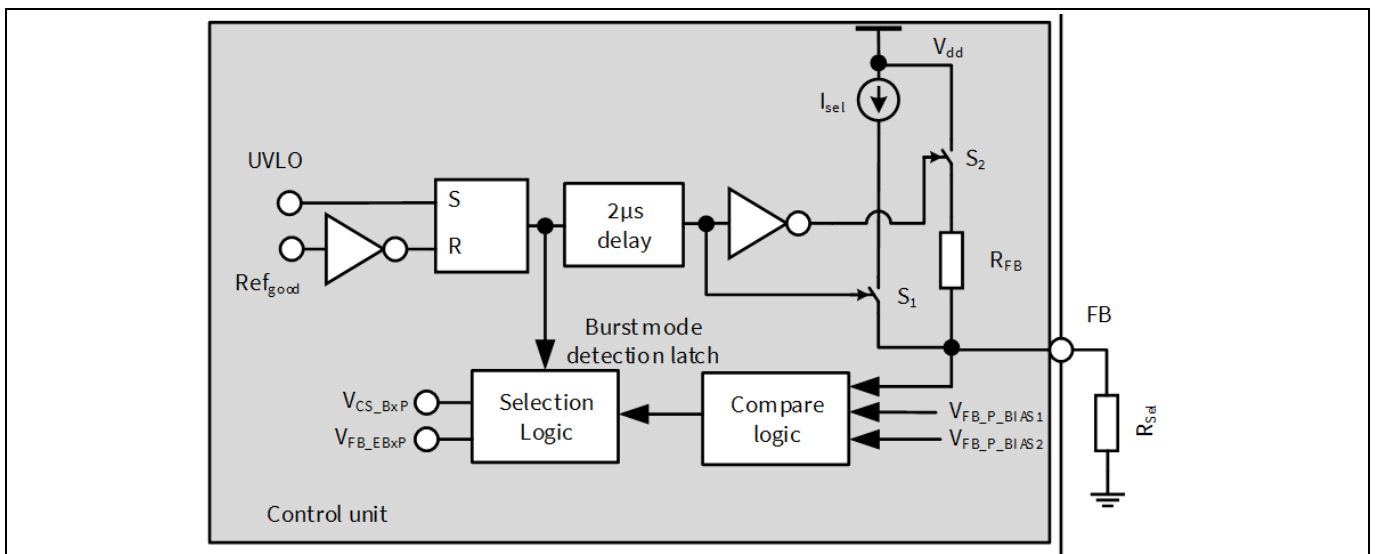


Figure 13 ABM detect and adjust

3.6 Non-isolated/isolated configuration

ICE5ARxxxxBZS has a VERR Pin, which is connected to the input of an integrated error amplifier to support non-isolated flyback application (see Figure 2). When  $V_{CC}$  is charging and before reaching the  $V_{CC}$  on threshold, a current source  $I_{ERR\_P\_BIAS}$  from VERR pin together with  $R_{F1}$  and  $R_{F2}$  will generate a voltage across it. If VERR voltage is more than  $V_{ERR\_P\_BIAS}$  (0.2 V), non-isolated configuration is selected, otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

In case of non-isolated configuration, the voltage divider  $R_{F1}$  and  $R_{F2}$  is used to sense the output voltage and compared with the internal reference voltage  $V_{ERR\_REF}$ . The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

Functional description

### 3.7 Protection functions

The ICE5ARxxxBZS provides numerous protection functions which considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions and the corresponding protection mode whether as a non switch auto restart, auto restart or odd skip auto restart mode. Refer to Figure 14, Figure 15 and Figure 16 for the waveform illustration of protection modes.

**Table 4 Protection functions**

Protection Functions	Normal Mode	Burst Mode		Protection Mode
		Burst ON	Burst OFF	
V <sub>CC</sub> over voltage	√	√	NA <sup>1</sup>	Odd skip auto restart
V <sub>CC</sub> under voltage	√	√	√	Auto restart
Overload/ open loop	√	NA <sup>1</sup>	NA <sup>1</sup>	Odd skip auto restart
Over temperature	√	√	√	Non switch auto restart
V <sub>CC</sub> short to GND	√	√	√	No startup

#### 3.7.1 V<sub>CC</sub> over/under voltage

During operation, the V<sub>CC</sub> voltage is continuously monitored. If V<sub>CC</sub> is either below V<sub>VCC\_OFF</sub> for 50 μs (t<sub>VCC\_OFF\_B</sub>) or above V<sub>VCC\_OVP</sub> for 55 μs (t<sub>VCC\_OVP\_B</sub>), the power MOSFET is kept switch off. After the V<sub>CC</sub> voltage falls below the threshold V<sub>VCCoff</sub>, the new start up sequence is activated. The V<sub>CC</sub> capacitor is then charged up. Once the voltage exceeds the threshold V<sub>VCC\_ON</sub>, the IC begins to operate with a new soft-start.

#### 3.7.2 Overload/ open loop

In case of open control loop or output overload, the FB voltage will be pulled up. When V<sub>FB</sub> exceeds V<sub>FB\_OLP</sub> after a blanking time of t<sub>FB\_OLP\_B</sub>, the IC enters odd skip auto restart mode. The blanking time enables the converter to provide a peak power in case the increase in V<sub>FB</sub> is due to a sudden load increase.

#### 3.7.3 Over temperature

If the junction temperature of controller exceeds T<sub>JCON\_OTP</sub>, the IC enters into Over Temperature Protection (OTP) auto restart mode. The IC has also implemented with a 40 °C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature is dropped 40 °C lower than the over temperature trigger point.

#### 3.7.4 V<sub>CC</sub> short to GND

To limit the power dissipation of the startup circuit at V<sub>CC</sub> short to GND condition, the V<sub>CC</sub> charging current is limited to a minimum level of I<sub>VCC\_Charge1</sub>. With such low current, the power loss of the IC is limited to prevent overheating.

#### 3.7.5 Protection modes

All the protections are in auto restart mode with a new soft start sequence. The three auto restart modes are illustrated in the following figures.

<sup>1</sup> Not Applicable



Functional description

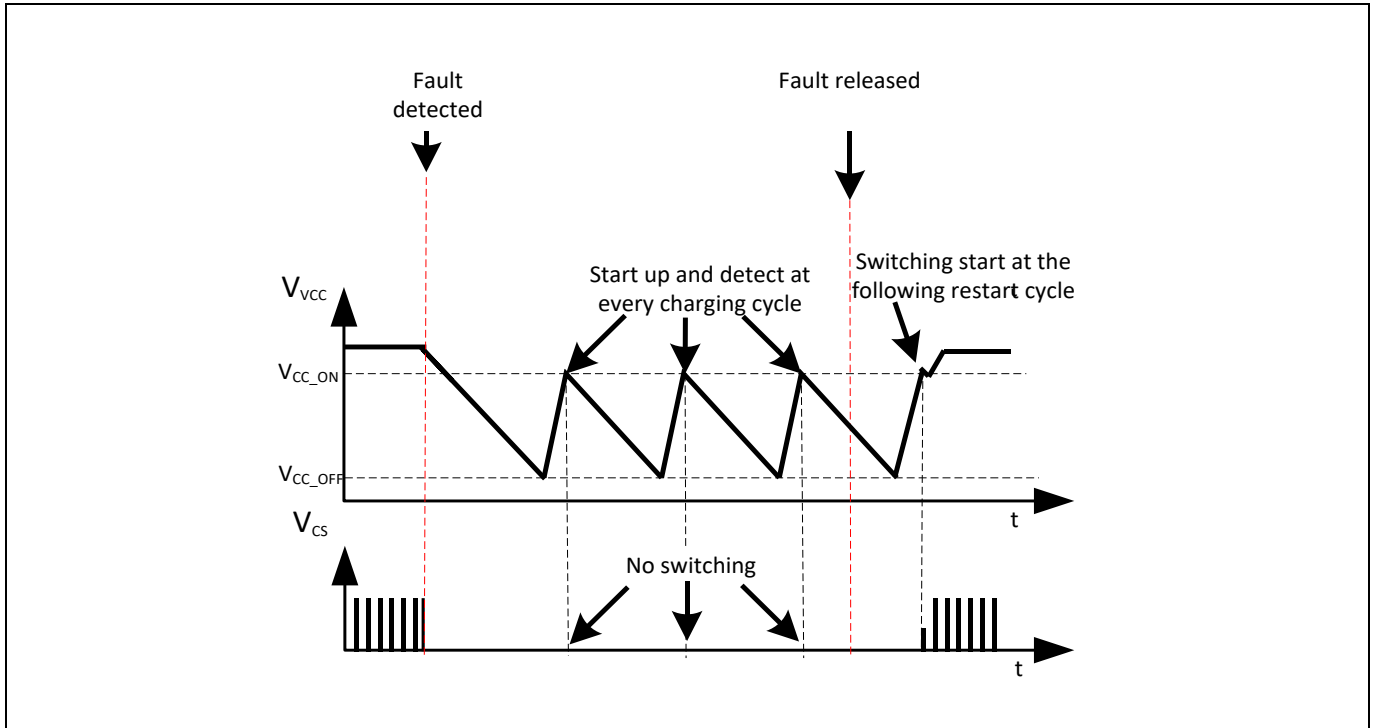


Figure 14 Non switch auto restart mode

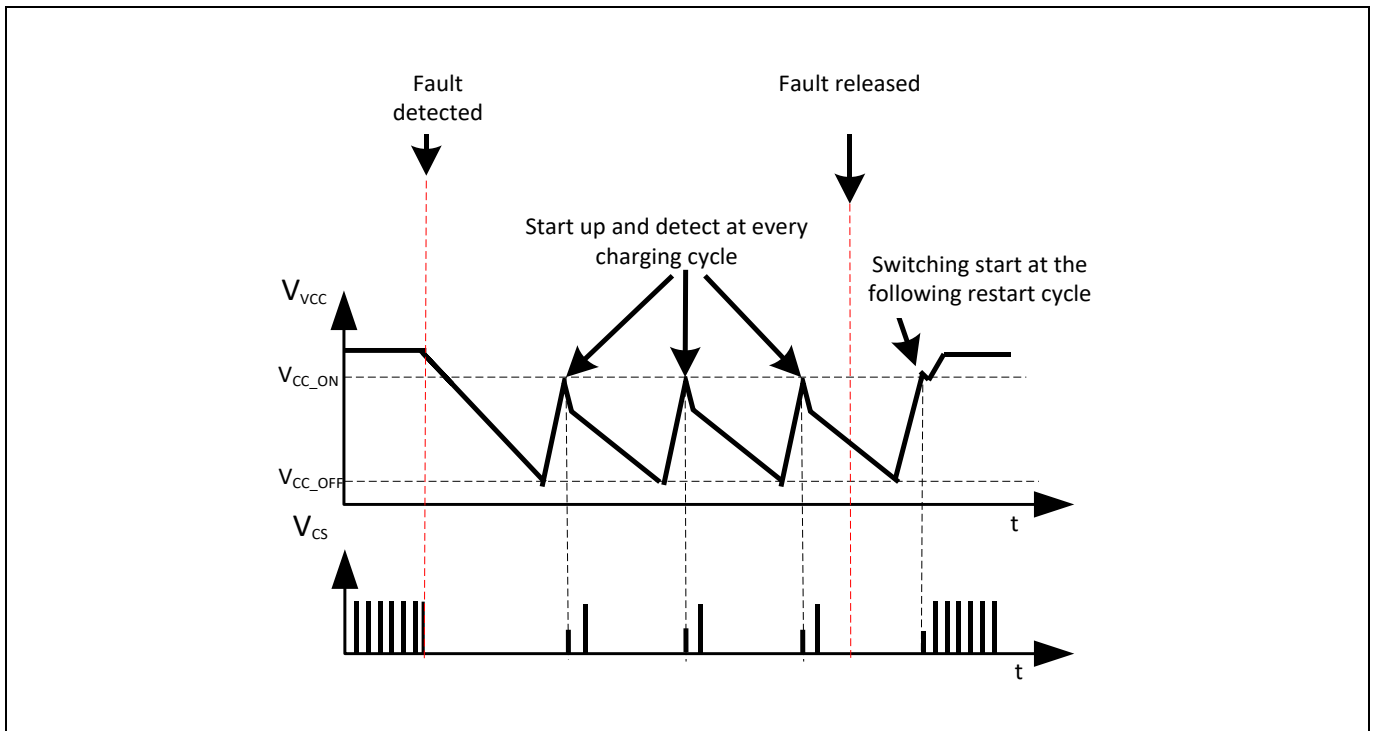


Figure 15 Auto restart mode

Functional description

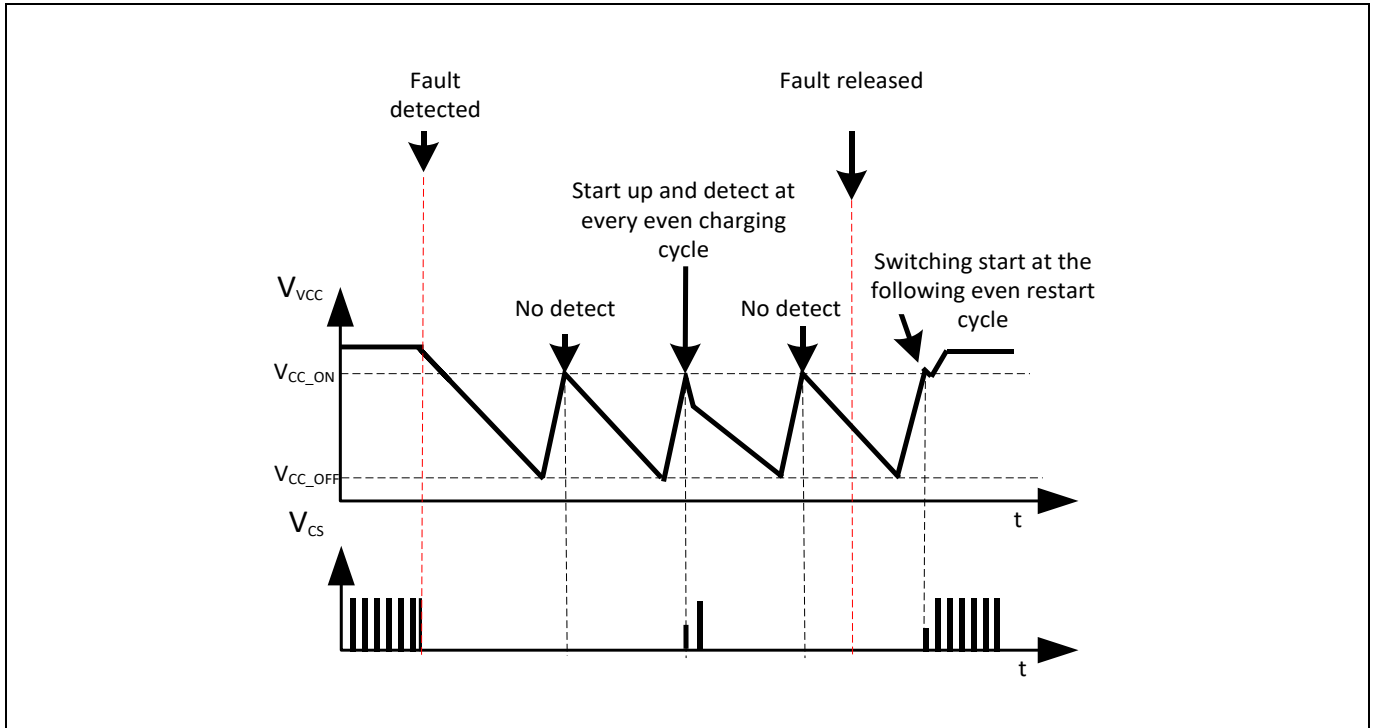


Figure 16 Odd skip auto restart

## Electrical characteristics

## 4 Electrical characteristics

**Attention:** All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

### 4.1 Absolute maximum ratings

**Attention:** Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.  $T_a=25\text{ °C}$  unless otherwise specified.

**Table 5 Absolute maximum ratings**

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
Drain Voltage ICE5ARxx70BZS ICE5ARxx80BZS	$V_{\text{DRAIN}}$	-	700 800	V	$T_j = 25\text{ °C}$
Pulse drain current ICE5AR4770BZS ICE5AR4780BZS ICE5AR0680BZS	$I_{\text{D,Pulse}}$	-	2.2 <sup>1</sup> 2.6 <sup>1</sup> 5.8 <sup>2</sup>	A	
Avalanche energy, repetitive, $t_{\text{AR}}$ limited by max. $T_j=150\text{ °C}$ and $T_{j,\text{Start}} = 25\text{ °C}$ ICE5AR4770BZS ICE5AR4780BZS ICE5AR0680BZS	$E_{\text{AR}}$	-	0.02 0.02 0.22	mJ	$I_{\text{D}}=0.14\text{ A}, V_{\text{DD}}=50\text{ V}$ $I_{\text{D}}=0.20\text{ A}, V_{\text{DD}}=50\text{ V}$ $I_{\text{D}}=1.80\text{ A}, V_{\text{DD}}=50\text{ V}$
Avalanche current, repetitive, $t_{\text{AR}}$ limited by max. $T_j=150\text{ °C}$ and $T_{j,\text{Start}} = 25\text{ °C}$ ICE5AR4770BZS ICE5AR4780BZS ICE5AR0680BZS	$I_{\text{AR}}$	-	0.14 0.20 1.80	A	
VCC Supply Voltage	$V_{\text{CC}}$	-0.3	27.0	V	
GATE Voltage	$V_{\text{GATE}}$	-0.3	27.0	V	
FB Voltage	$V_{\text{FB}}$	-0.3	3.6	V	
VERR Voltage	$V_{\text{ERR}}$	-0.3	3.6	V	
CS Voltage	$V_{\text{CS}}$	-0.3	3.6	V	
Maximum DC current on any pin		-10.0	10.0	mA	Except DRAIN and CS pin

<sup>1</sup> Pulse width  $t_p$  limited by  $T_{j,\text{max}}$

<sup>2</sup> Pulse width  $t_p = 20\text{ }\mu\text{s}$  and limited by  $T_{j,\text{max}}$

**Electrical characteristics**

ESD robustness HBM	$V_{ESD\_HBM}$	-	2000	V	According to EIA/JESD22
ESD robustness CDM	$V_{ESD\_CDM}$	-	500	V	
Junction temperature range	$T_J$	-40	150	°C	Controller & CoolMOS
Storage Temperature	$T_{STORE}$	-55	150	°C	
Thermal Resistance (Junction- Ambient)	$R_{thJA}$			K/W	Setup according to the JEDEC standard JESD51 and using minimum drain pin copper area in a 2 oz copper single sided PCB
ICE5AR4770BZS		-	106		
ICE5AR4780BZS		-	107		
ICE5AR0680BZS		-	100		

**4.2 Operating range**

Note: Within the operating range, the IC operates as described in the functional description.

**Table 6 Operating range**

Parameter	Symbol	Limit Values		Unit	Remark
		Min.	Max.		
VCC Supply Voltage	$V_{VCC}$	$V_{VCC\_OFF}$	$V_{VCC\_OVP}$		
Junction Temperature of controller	$T_{JCon\_op}$	-40	$T_{JCon\_OTP}$	°C	Max value limited due to OTP of controller chip
Junction Temperature of CoolMOS	$T_{JCoolMOS\_op}$	-40	150	°C	

**4.3 Operating conditions**

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range  $T_J$  from - 40 °C to 125 °C. Typical values represent the median values, which are related to 25 °C. If not otherwise stated, a supply voltage of  $V_{CC} = 18 V$  is assumed.

**Table 7 Operating conditions**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Charge Current	$I_{VCC\_Charge1}$	-0.35	-0.20	-0.09	mA	$V_{VCC}=0 V, R_{StartUp}=50 M\Omega$ and $V_{DRAIN}=90 V$
	$I_{VCC\_Charge2}$	-	-3.2	-	mA	$V_{VCC}=3 V, R_{StartUp}=50 M\Omega$ and $V_{DRAIN}=90 V$
	$I_{VCC\_Charge3}$	-5	-3	-1	mA	$V_{VCC}=15 V, R_{StartUp}=50 M\Omega$ and $V_{DRAIN}=90 V$
Current Consumption, Startup Current	$I_{VCC\_Startup}$	-	0.25	-	mA	$V_{VCC}=15 V$
Current Consumption, Normal	$I_{VCC\_Normal}$	-	0.9	-	mA	$I_{FB}=0 A$ (No gate switching)
Current Consumption, Auto Restart	$I_{VCC\_AR}$	-	410	-	µA	
Current Consumption, Burst Mode – Isolated	$I_{VCC\_Burst Mode\_ISO}$	-	0.54	-	mA	
Current Consumption, Burst Mode – Non-Isolated	$I_{VCC\_Burst Mode\_NISO}$	-	0.61	-	mA	

**Electrical characteristics**

VCC Turn-on Threshold Voltage	$V_{VCC\_ON}$	15.3	16.0	16.5	V	
VCC Turn-off Threshold Voltage	$V_{VCC\_OFF}$	9.4	10.0	10.4	V	
VCC Short Circuit Protection	$V_{VCC\_SCP}$	-	1.1	1.9	V	
VCC Turn-off blanking	$t_{VCC\_OFF\_B}$	-	50	-	μs	

**4.4 Internal voltage reference**

**Table 8 Internal voltage reference**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Internal Reference Voltage	$V_{REF}$	3.20	3.30	3.39	V	Measured at pin FB $I_{FB}=0$ A

**4.5 PWM section**

**Table 9 PWM section**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fixed Oscillator Frequency – 100 kHz	$f_{OSC3}$	92	100	108	k H z	
	$f_{OSC4}$	94	100	106	k H z	$T_j = 25\text{ °C}$
Fixed Oscillator Frequency – 100 kHz (Active Burst Mode)	$f_{OSC4\_ABM}$	71	83	94	k H z	$T_j = 25\text{ °C}$
Fixed Oscillator Frequency – 100 kHz (Minimum Fsw)	$f_{OSC4\_MIN}$	36	43	51	k H z	$T_j = 25\text{ °C}$
Frequency Jittering Range	$F_{JITTER}$	-	+/- 4	-	%	$T_j = 25\text{ °C}$
Frequency Jittering period	$T_{JITTER}$	-	4	-	m s	$T_j = 25\text{ °C}$
Maximum Duty Cycle	$D_{MAX}$	70	75	80	%	
Feedback Pull-Up Resistor	$R_{FB}$	11	15	20	k Ω	
PWM-OP Gain	$G_{PWM}$	1.91	2.03	2.16		
Offset for Voltage Ramp	$V_{PWM}$	0.42	0.50	0.58	V	
Slope Compensation rate - 100 kHz	$M_{COMP}$	41	50	58	mV/μs	$V_{CS}=0$ V

**4.6 Error amplifier**

**Table 10 Error amplifier**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transconductance	$G_{ERR\_M}$	2.14	2.80	3.44	m A / V	
Transconductance – Burst Mode	$G_{ERR\_BM}$	6.9	9.2	11.6	m A / V	
Error Amplifier Source Current	$I_{ERR\_SOURCE}$	85	150	223	μ A	
Error Amplifier Sink Current	$I_{ERR\_SINK}$	85	150	223	μ A	
Error Amplifier Reference Voltage	$V_{ERR\_REF}$	1.76	1.80	1.84	V	

**Electrical characteristics**

Error Amplifier Output Dynamic Range of Transconductance	$V_{ERR\_DYN}$	0.05	-	3.15	V	
Error Amplifier Mode Bias Current	$I_{ERR\_P\_BIAS}$	9.5	14.0	18.5	$\mu A$	
Error Amplifier Mode Threshold	$V_{ERR\_P\_BIAS}$	0.16	0.20	0.24	V	

**4.7 Current sense**

**Table 11 Current sense**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	$V_{CS\_N}$	0.72	0.80	0.88	V	$dv_{sense}/dt = 0.41V/\mu s$
Peak current limitation in normal operation, 15% of $T_{ON}$	$V_{CS\_N15}$	0.74	0.79	0.84	V	
Leading Edge Blanking time	$t_{CS\_LEB}$	70	220	365	ns	
Peak Current Limitation in Active Burst Mode - High Power	$V_{CS\_BHP}$	0.23	0.27	0.31	V	
Peak Current Limitation in Active Burst Mode - Low Power	$V_{CS\_BLP}$	0.18	0.22	0.26	V	
Abnormal CS voltage threshold	$V_{CS\_STG}$	0.06	0.10	0.15	V	
Abnormal CS voltage Consecutive Trigger	$P_{CS\_STG}$	-	3	-	cycle	
Abnormal CS voltage Sample period	$t_{CS\_STG\_SAM}$	$t_{PERIOD}^*$ 0.36	$t_{PERIOD}^*$ 0.4	$t_{PERIOD}^*$ 0.44	$\mu s$	

**4.8 Soft start**

**Table 12 Soft start**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Soft-Start time	$t_{SS}$	7.3	12.0	-	ms	
Soft-start time step	$t_{SS\_S}^1$	-	3	-	ms	
CS peak voltage at first step of soft start	$V_{SS1}^1$	-	0.30	-	V	CS peak voltage
Step increment of CS peak voltage in soft start	$V_{SS\_S}^1$	-	0.15	-	V	CS peak voltage

**4.9 Active Burst Mode**

**Table 13 Active Burst Mode**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		

<sup>1</sup> The parameter is not subjected to production test - verified by design/characterization

**Electrical characteristics**

Charging current to select burst mode	$I_{sel}$	2.5	3.0	3.5	μA	
Burst mode selection reference voltage Threshold	$V_{FB\_P\_BIAS1}$	1.65	1.73	1.80	V	
Burst mode selection reference voltage Threshold	$V_{FB\_P\_BIAS2}$	2.76	2.89	3.01	V	
Feedback voltage for entering ABM for high power	$V_{FB\_EBHP}$	0.98	1.03	1.08	V	
Feedback voltage for entering ABM for low power	$V_{FB\_EBLP}$	0.88	0.93	0.98	V	
Blanking time for entering Active Burst Mode	$t_{FB\_BEB}$	-	36	-	ms	
Feedback voltage for leaving Active Burst Mode	$V_{FB\_LB}$	2.63	2.73	2.83	V	
Feedback voltage for burst-on – Isolated Case	$V_{FB\_Bon\_ISO}$	2.26	2.35	2.45	V	
Feedback voltage for burst-off – Isolated Case	$V_{FB\_Boff\_ISO}$	1.88	2.00	2.05	V	
Feedback voltage for burst-on – Non-Isolated Case	$V_{FB\_Bon\_NISO}$	1.88	1.95	2.05	V	
Feedback voltage for burst-off – Non-Isolated Case	$V_{FB\_Boff\_NISO}$	1.50	1.55	1.64	V	

**4.10 V<sub>CC</sub> over voltage protection**

**Table 14 V<sub>CC</sub> over voltage protection**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Over Voltage threshold	$V_{VCC\_OVP}$	24.0	25.5	27.0	V	
VCC Over Voltage blanking	$t_{VCC\_OVP\_B}$	-	55	-	μs	

**4.11 Overload protection**

**Table 15 Overload protection**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over Load Detection threshold for OLP protection at FB pin	$V_{FB\_OLP}$	2.63	2.73	2.83	V	
Over Load Protection Blanking Time	$t_{FB\_OLP\_B}$	30	54	-	ms	

**4.12 Thermal protection**

**Table 16 Thermal protection**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		

**Electrical characteristics**

Over temperature protection	$T_{jcon\_OTP}^1$	129	140	150	°C	Junction temperature of the controller chip (not the CoolMOS™ chip)
Over temperature Hysteresis	$T_{jhys\_OTP}$	-	40	-	°C	
Over temperature Blanking Time	$T_{jcon\_OTP\_B}$	-	50	-	µs	

**4.13 CoolMOS™ section**

**Table 17 ICE5ARxxxxBZS**

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain Source Breakdown Voltage ICE5ARxx70BZS ICE5ARxx80BZS	$V_{(BR)DSS}$	700 800	- -	- -	V	$T_j = 25^\circ\text{C}$
Drain Source On-Resistance (inclusive of low side MOSFET) ICE5AR4770BZS ICE5AR4780BZS ICE5AR0680BZS	$R_{DSon}$	- - - -	4.73 8.73 <sup>2</sup> 4.13 8.69 <sup>1</sup>	5.18 - 4.85 -	Ω	$T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ at $I_D = 0.4\text{A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ at $I_D = 0.4\text{A}$ $T_j = 25^\circ\text{C}$ $T_j = 125^\circ\text{C}$ at $I_D = 2\text{A}$
Effective output capacitance, energy related <sup>1</sup> ICE5AR4770BZS ICE5AR4780BZS ICE5AR0680BZS	$C_{o(er)}$	- - -	3.4 3 24	- - -	pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 0 \sim 480\text{V}$ $V_{GS} = 0\text{V}$ , $V_{DS} = 0 \sim 500\text{V}$ $V_{GS} = 0\text{V}$ , $V_{DS} = 0 \sim 500\text{V}$
Rise Time	$t_{rise}^3$	-	30	-	ns	
Fall Time	$t_{fall}^2$	-	30	-	ns	

<sup>1</sup>The parameter is not subjected to production test - verified by design/characterization

<sup>2</sup>The parameter is not subjected to production test - verified by design/characterization

<sup>3</sup>Measured in a typical flyback converter application



CoolMOS™ performance characteristics

### 5 CoolMOS™ performance characteristics

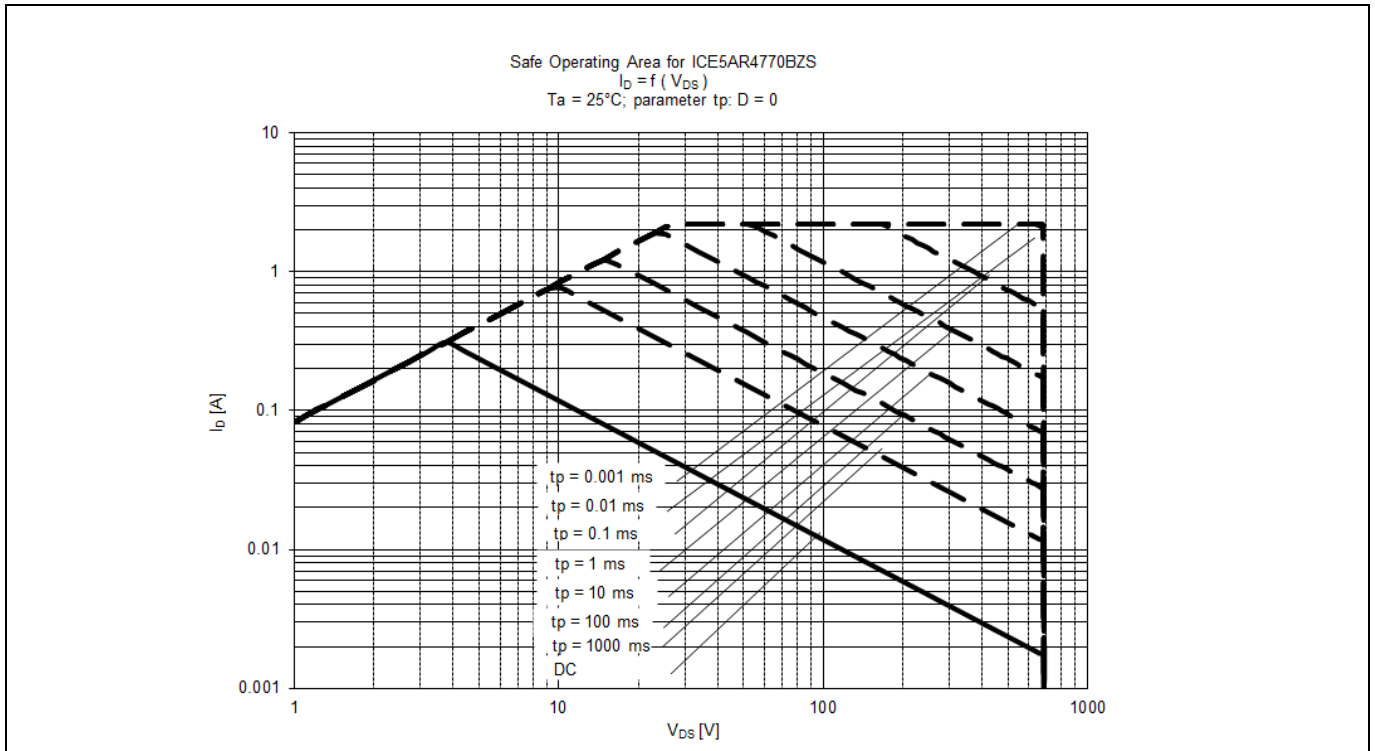


Figure 17 Safe Operating Area (SOA) curve for ICE5AR4770BZS

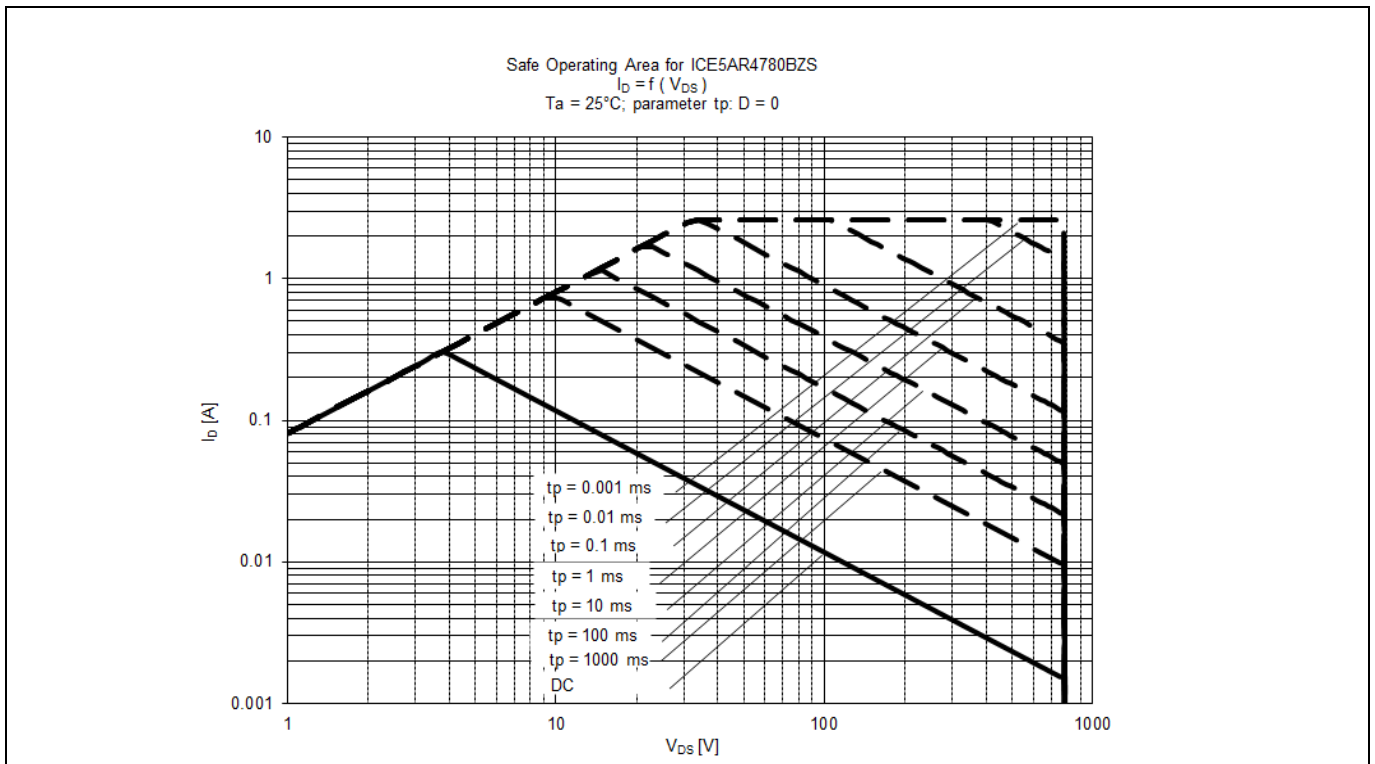


Figure 18 Safe Operating Area (SOA) curve for ICE5AR4780BZS

CoolMOS™ performance characteristics

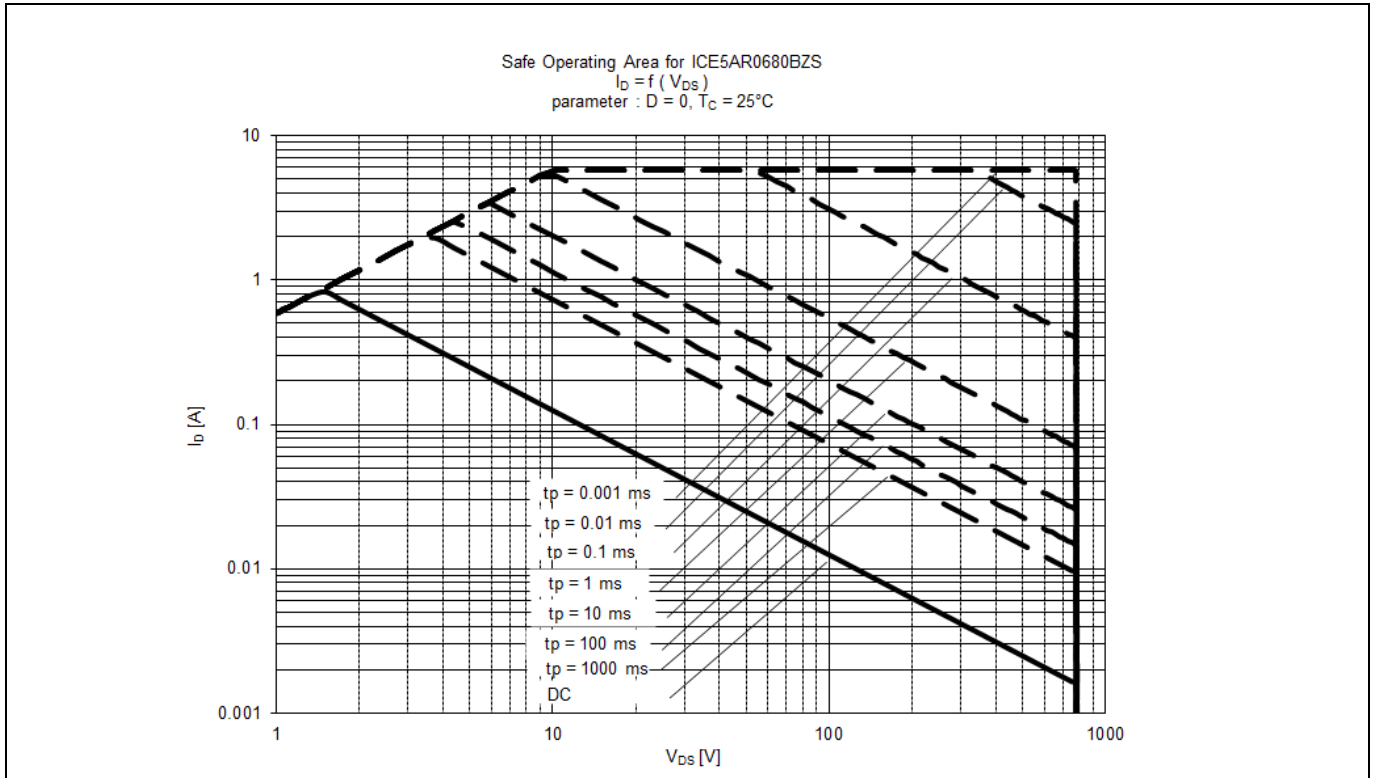


Figure 19 Safe Operating Area (SOA) curve for ICE5AR0680BZS

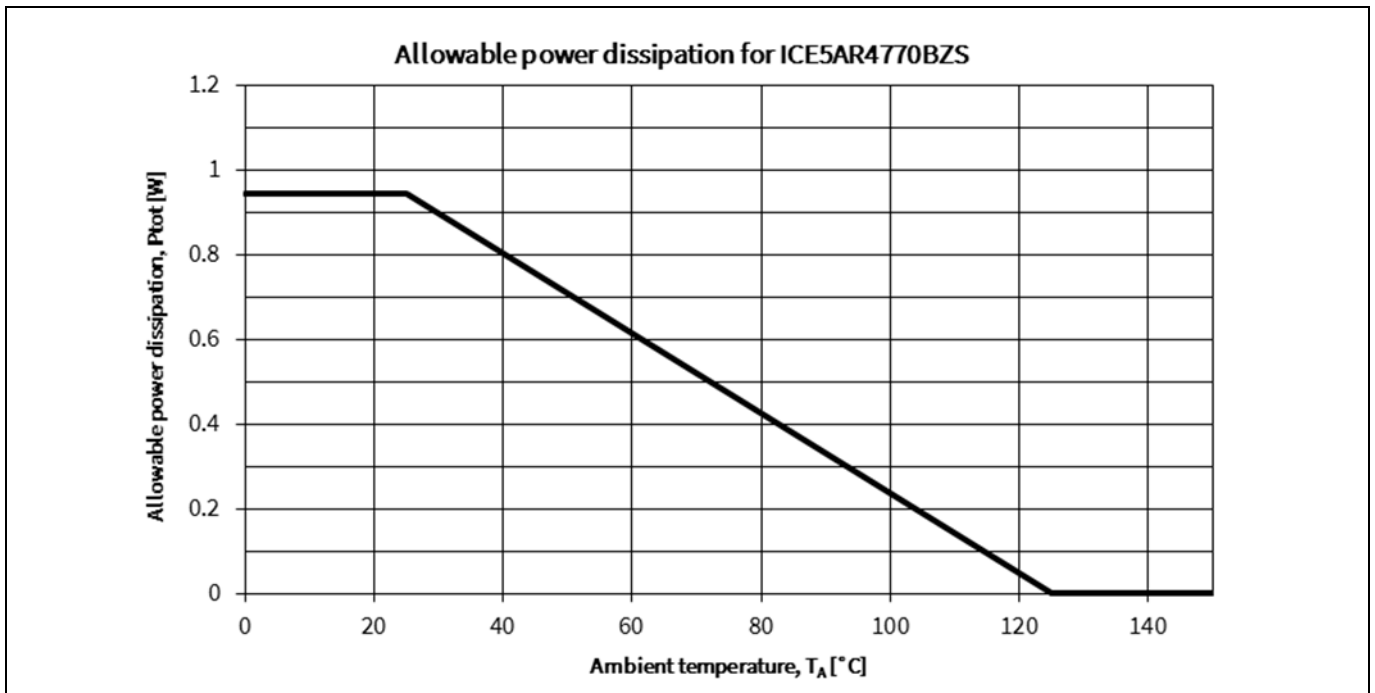


Figure 20 Power dissipation of ICE5AR4770BZS;  $P_{tot}=f(T_a)$ , (Maximum ratings as given in section 4.1 must not be exceeded)

CoolMOS™ performance characteristics

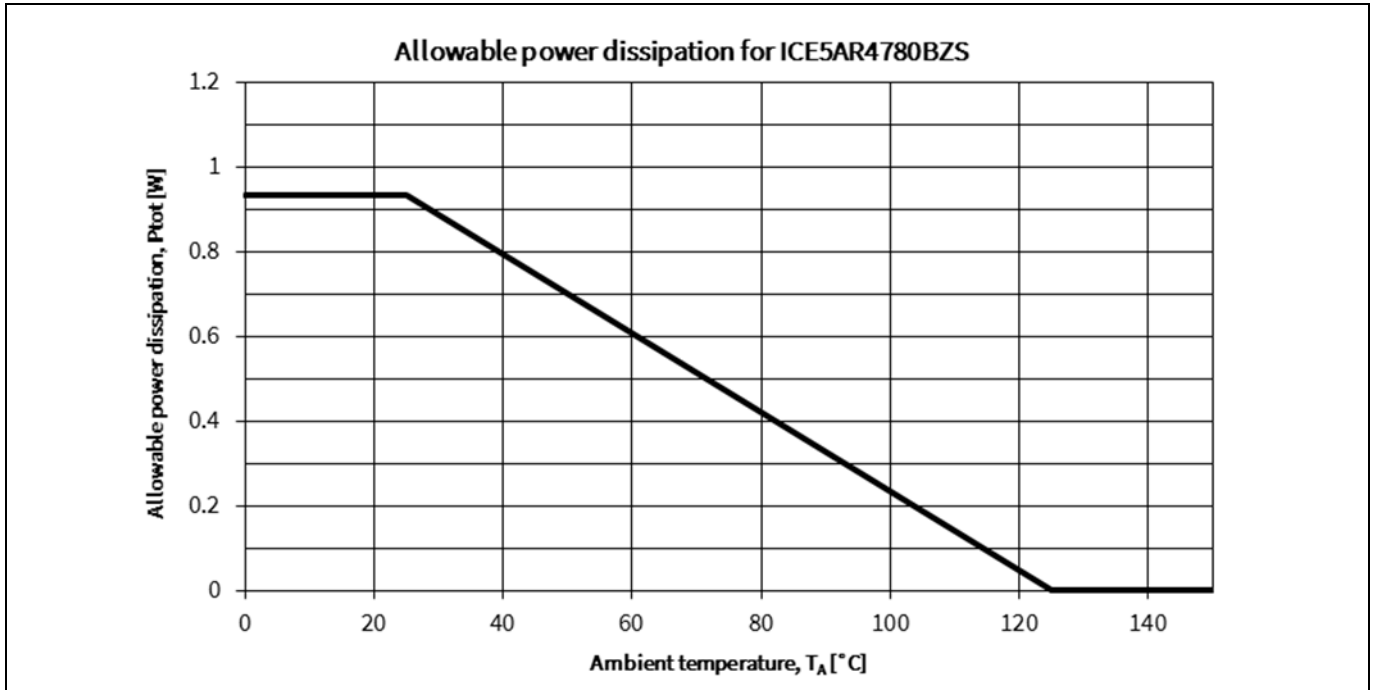


Figure 21 Power dissipation of ICE5AR4780BZS;  $P_{tot}=f(T_a)$ , (Maximum ratings as given in section 4.1 must not be exceeded)

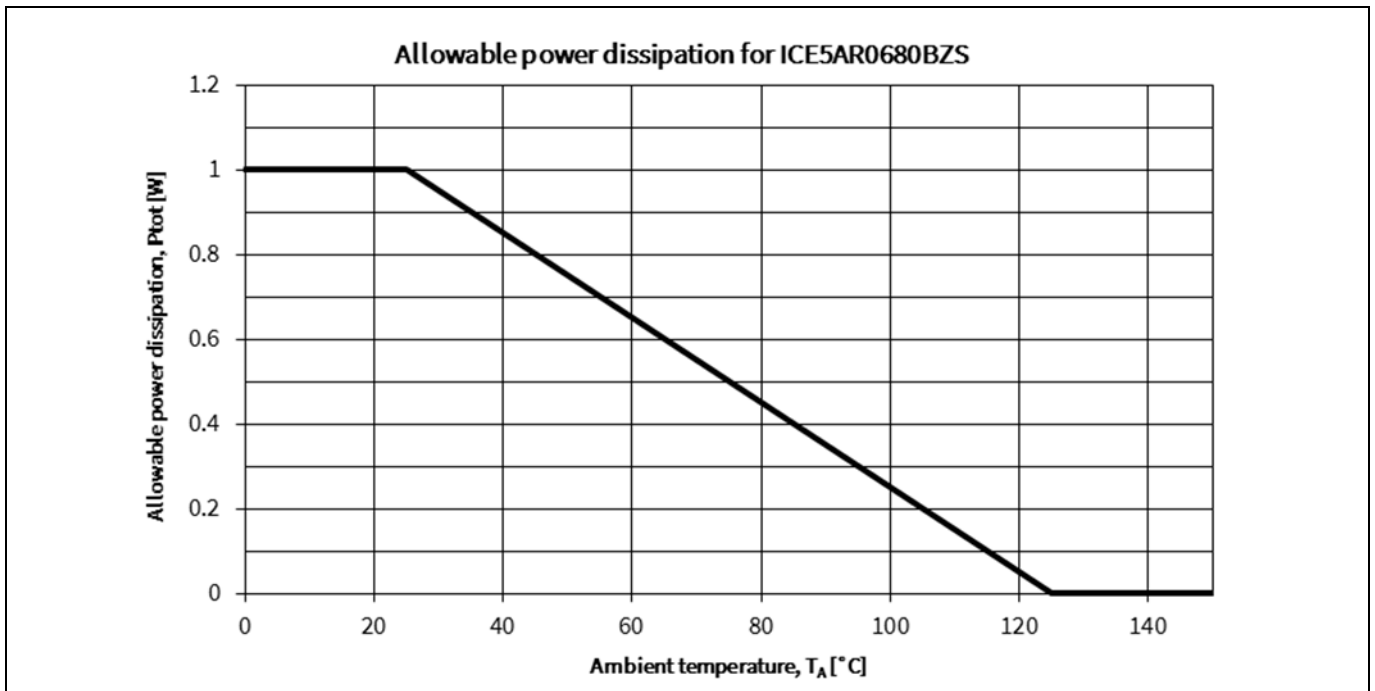


Figure 22 Power dissipation of ICE5AR0680BZS;  $P_{tot}=f(T_a)$ , (Maximum ratings as given in section 4.1 must not be exceeded)

CoolMOS™ performance characteristics

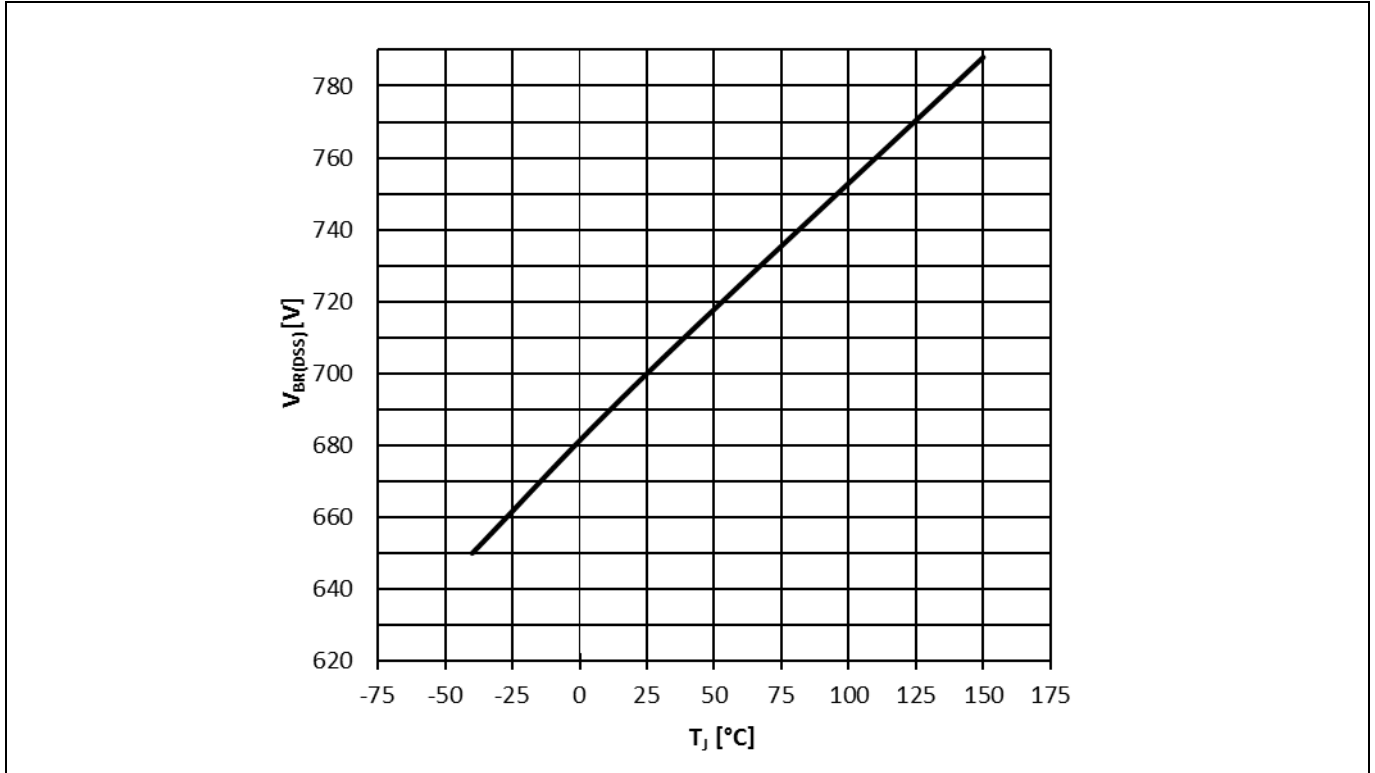


Figure 23 Drain-source breakdown voltage ICE5ARxx70BZS;  $V_{BR(DSS)}=f(T_J)$ ,  $I_D=1$  mA

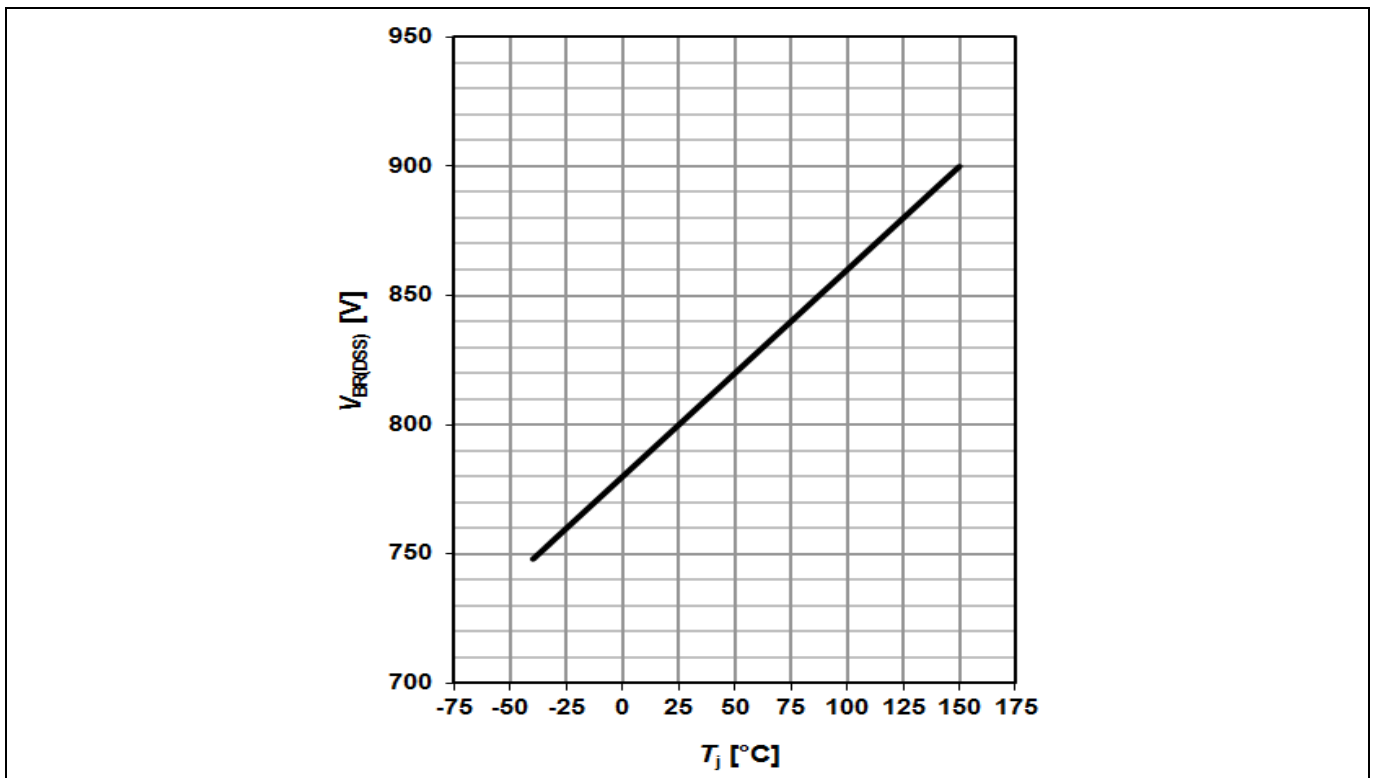


Figure 24 Drain-source breakdown voltage ICE5ARxx80BZS;  $V_{BR(DSS)}=f(T_J)$ ,  $I_D=1$  mA

CoolMOS™ performance characteristics

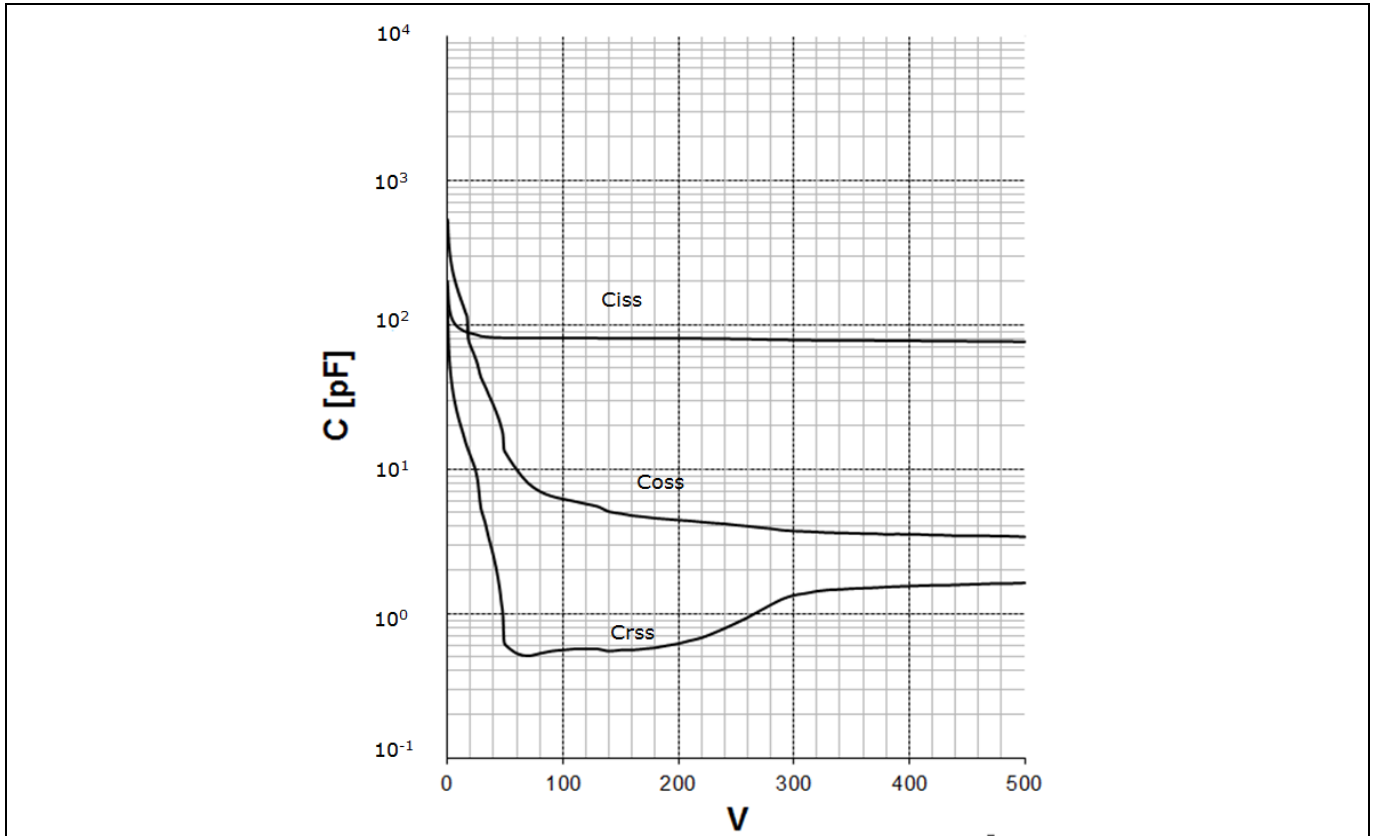


Figure 25 Typical CoolMOS™ capacitances of ICE5AR4770BZS ( $C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$ )

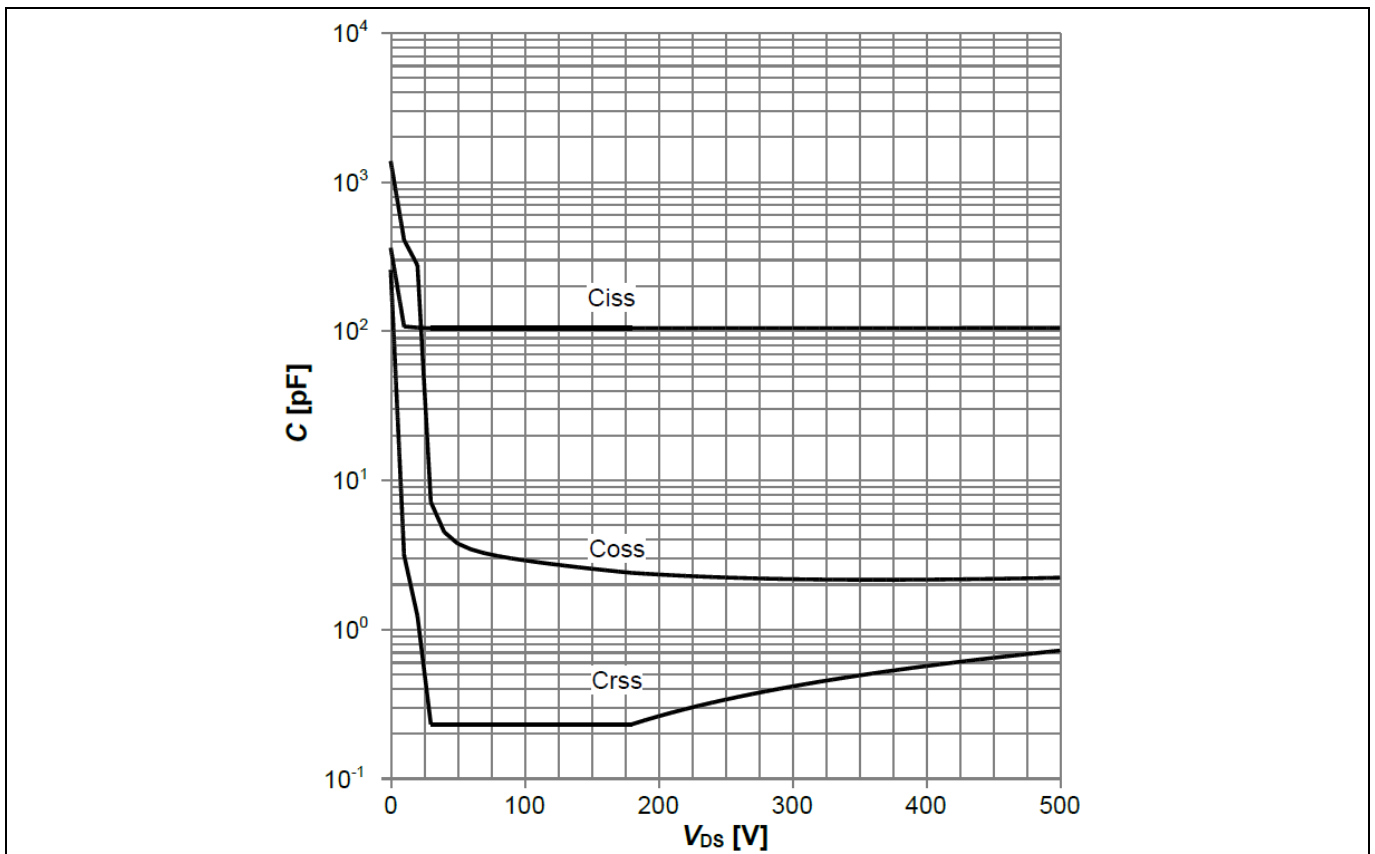


Figure 26 Typical CoolMOS™ capacitances of ICE5AR4780BZS ( $C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$ )

CoolMOS™ performance characteristics

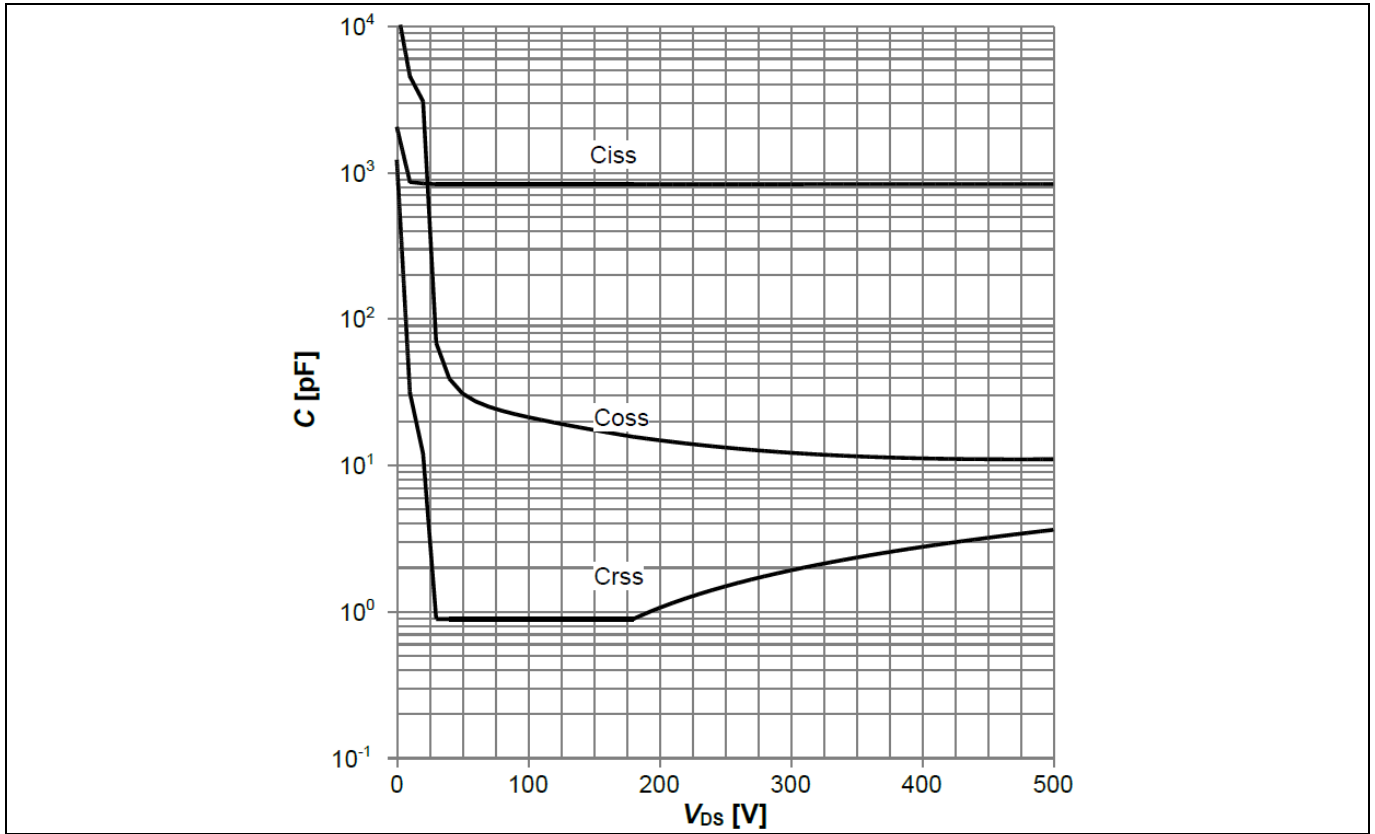


Figure 27 Typical CoolMOS™ capacitances of ICE5AR0680BZS (C=f(V<sub>DS</sub>);V<sub>GS</sub>=0 V; f=250 kHz)

Output power curve

## 6 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM/CCM flyback in an open frame design setting the maximum  $T_J$  of the integrated CoolMOS™ at 125 °C, using minimum drain pin copper area in a 2 oz copper single sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for selection purpose only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in section 4.1.

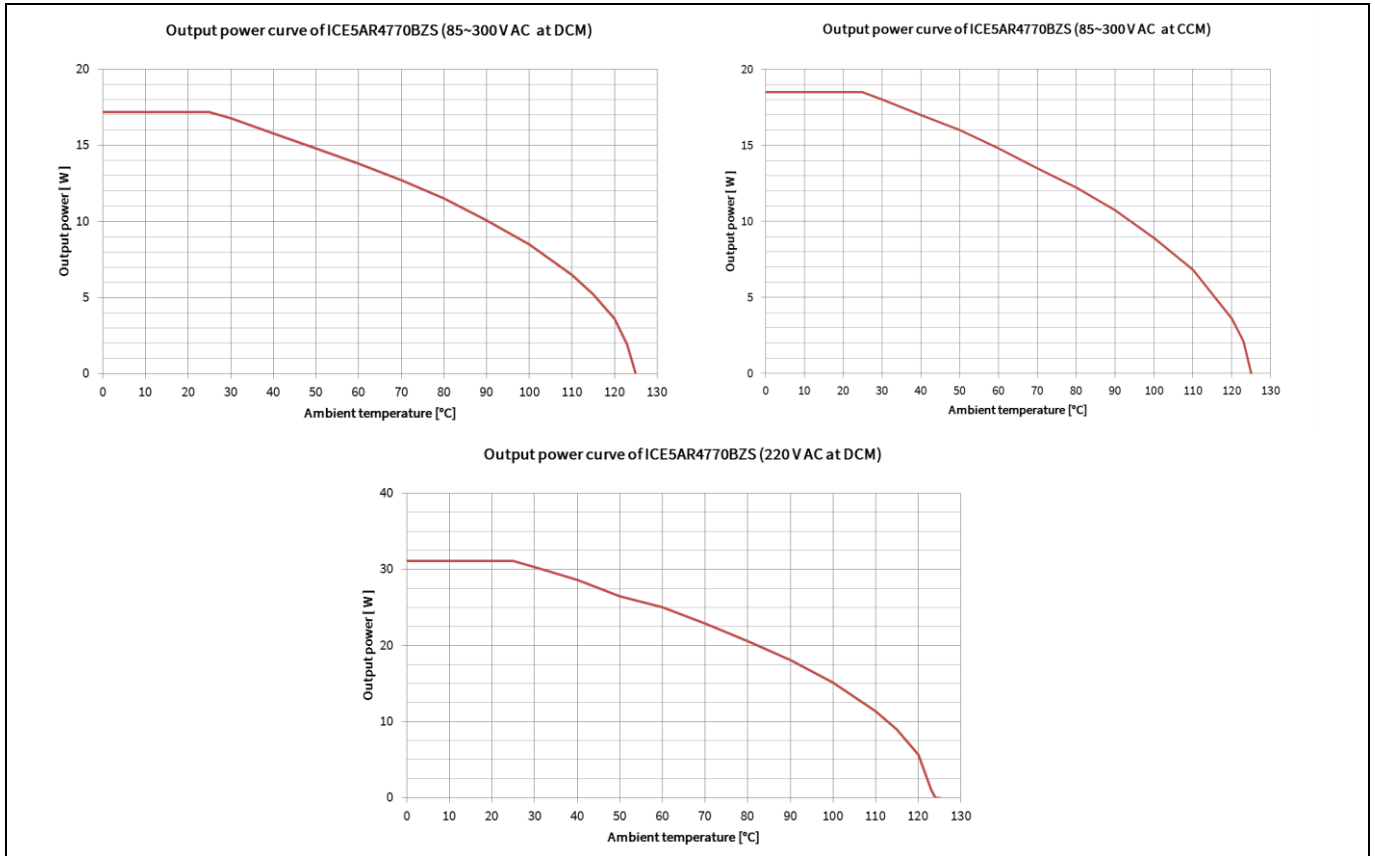


Figure 28 Output power curve of ICE5AR4770BZS

Output power curve

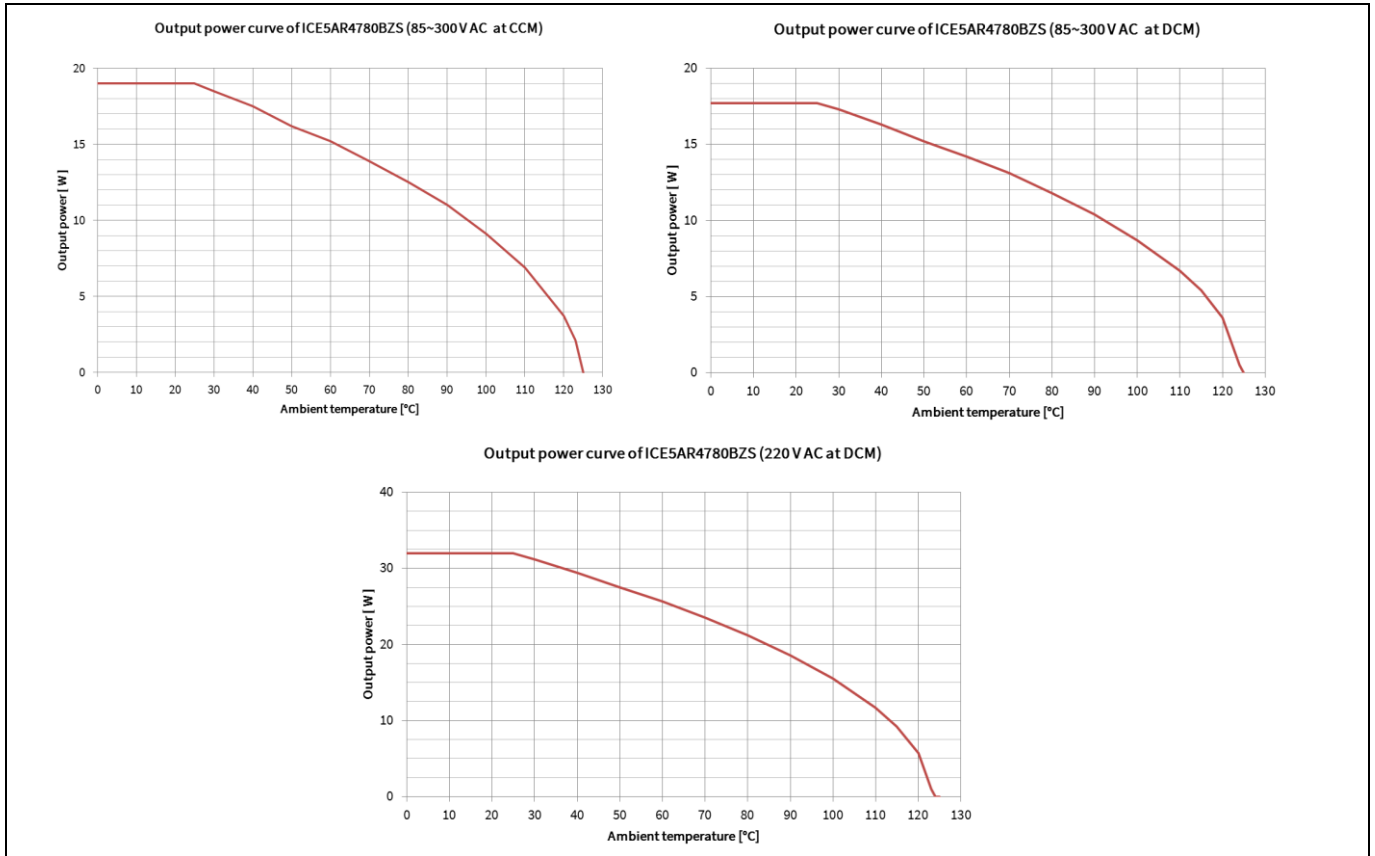


Figure 29 Output power curve of ICE5AR4780BZS

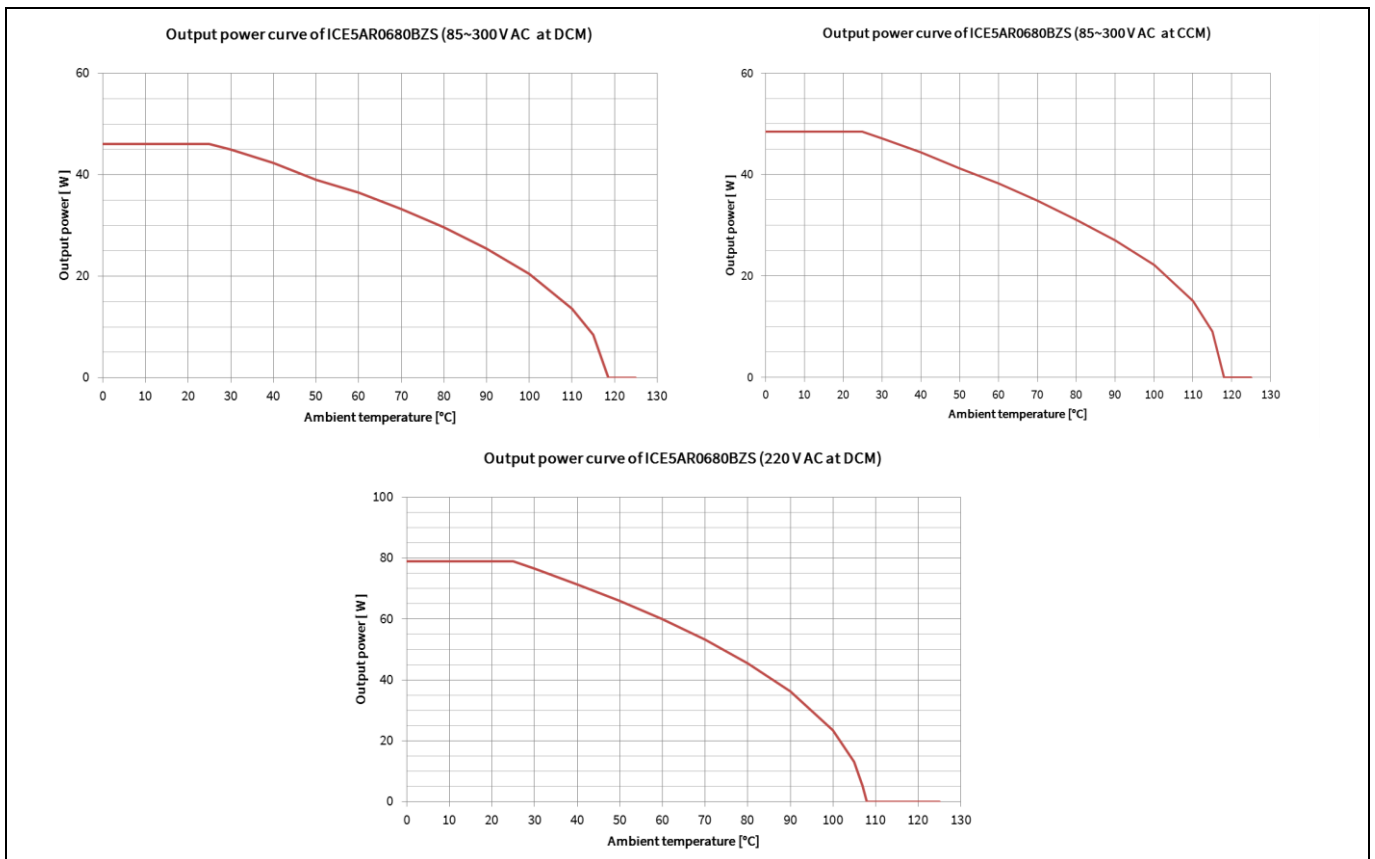


Figure 30 Output power curve of ICE5AR0680BZS



Outline dimension

7 Outline dimension

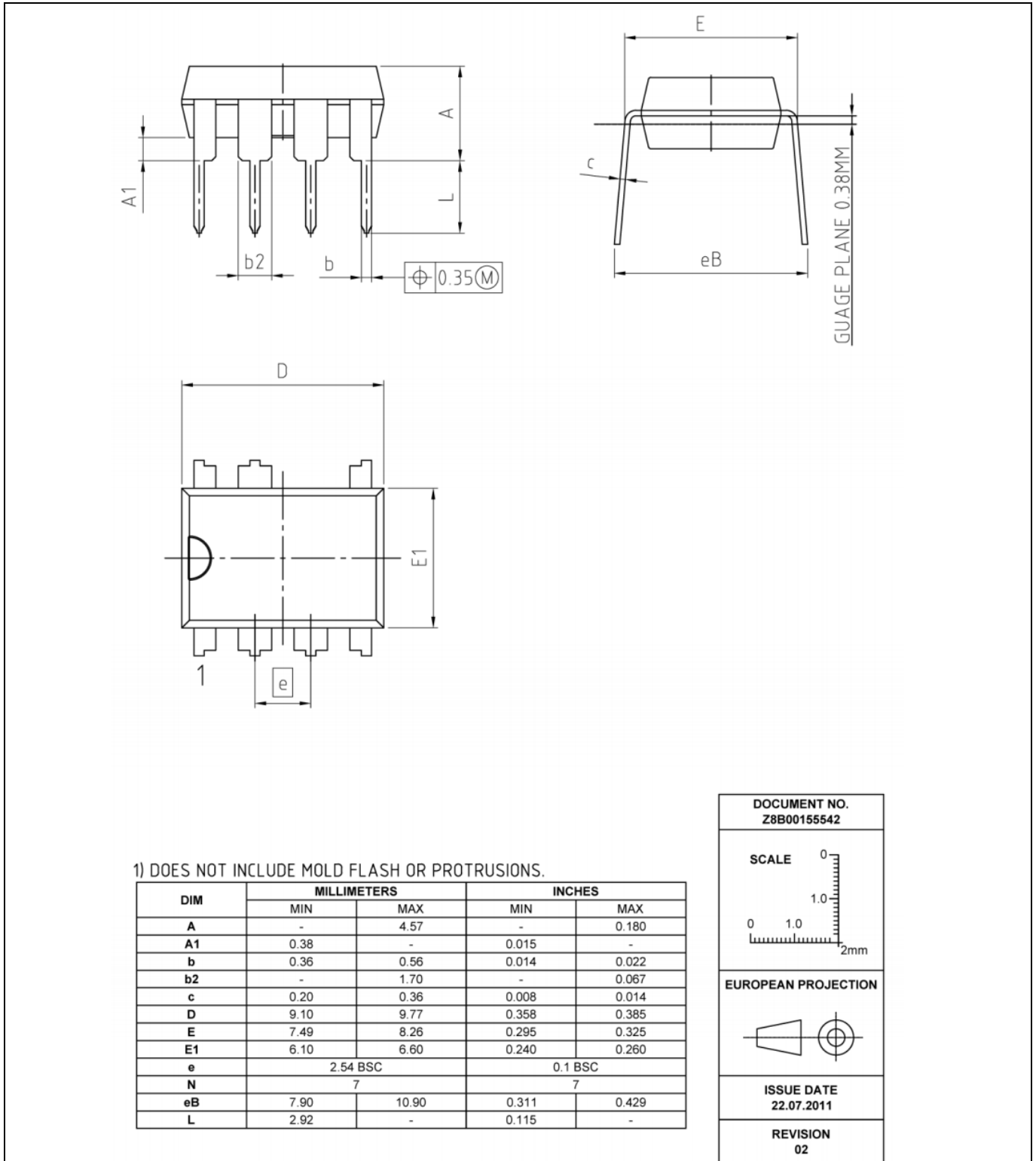


Figure 31 PG-DIP-7

Marking

8 Marking

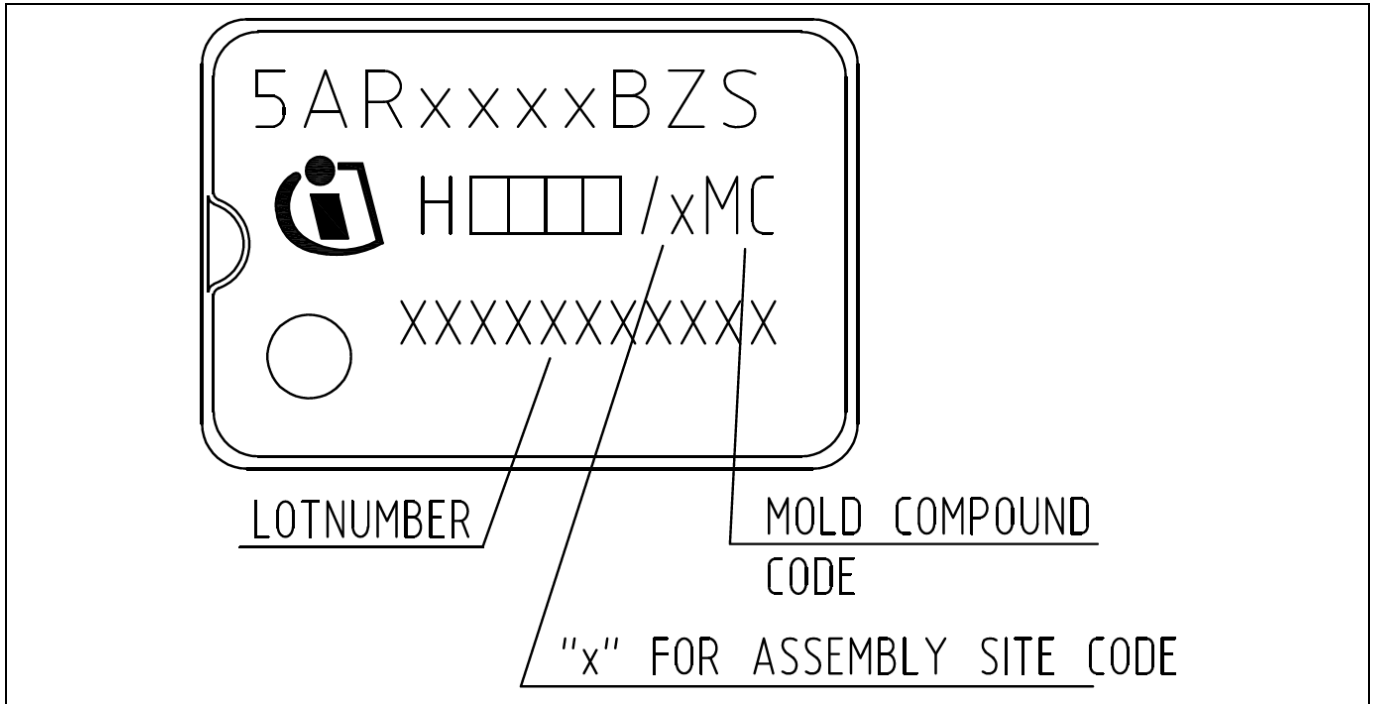


Figure 32 Marking of PG-DIP-7

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## Revision history

### Revision history

Document version	Date of release	Description of changes
V 2.0	21 Nov 2017	First release
V 2.1	27 Feb 2018	Page 1 Product validation text content revised
V 2.2	2 Oct 2019	Page 34 Update marking with reference to PCN 2019-142-A
V 2.3	3 Feb 2020	Update of CS pin function and description (refer to errata sheet ES_2001_PL83_2002_024629)

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**Document reference**

**ICE5ARxxxxBZS**

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