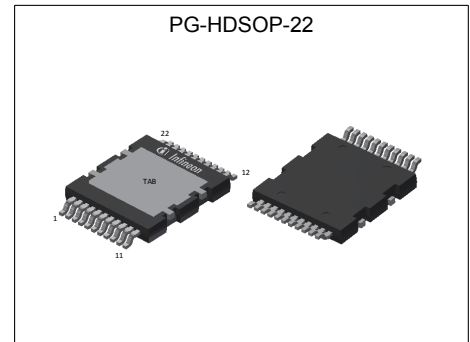


# MOSFET

## CoolSiC™ Power Device 750 V G1

The 750 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 750V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.



### Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class  $R_{DS(on)} \times Q_{fr}$
- Excellent  $R_{DS(on)} \times Q_{oss}$  and  $R_{DS(on)} \times Q_G$
- Unique combination of low  $C_{rfs}/C_{iss}$  and high  $V_{GS(th)}$
- Infineon proprietary die attach technology
- Cutting edge top side cooling package (QDPAK)
- Driver source pin available

### Benefits

- Enhanced robustness to withstand bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

### Potential applications

- EV charging infrastructure
- Solar PV inverters
- UPS (uninterruptable power supplies)
- Energy storage and battery formation
- Telecom and Server SMPS

### Product validation

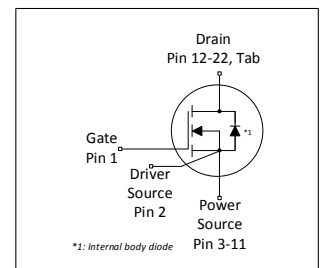
Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DSS}$ over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	40	mΩ
$R_{DS(on),max}$	52	mΩ
$Q_{G,typ}$	34	nC
$I_{DM,max}$	134	A
$Q_{oss,typ} @ 500 V$	68	nC
$E_{oss,typ} @ 500 V$	12.2	μJ

Type / Ordering Code	Package	Marking	Related Links
IMDQ75R040M1H	PG-HDSOP-22	75R040M1	see Appendix A



RoHS

## Table of Contents

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## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current <sup>1)</sup>	$I_{\text{DDC}}$	-	-	47 33	A	$T_C = 25\text{ °C}$ $T_C = 100\text{ °C}$
Peak drain current <sup>2)</sup>	$I_{\text{DM}}$	-	-	134	A	$T_C = 25\text{ °C}$ , $V_{\text{GS}} = 18\text{ V}$
Avalanche energy, single pulse	$E_{\text{AS}}$	-	-	170	mJ	$I_{\text{D}} = 6.4\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11
Avalanche energy, repetitive	$E_{\text{AR}}$	-	-	0.85	mJ	$I_{\text{D}} = 6.4\text{ A}$ , $V_{\text{DD}} = 50\text{ V}$ ; see table 11
Avalanche current, single pulse	$I_{\text{AS}}$	-	-	6.4	A	-
MOSFET $dv/dt$ ruggedness	$dv/dt$	-	-	200	V/ns	$V_{\text{DS}} = 0\text{...}500\text{ V}$
Gate source voltage (static) <sup>3)</sup>	$V_{\text{GS}}$	-5	-	23	V	-
Gate source voltage (transient)	$V_{\text{GS}}$	-10	-	25	V	$t_p \leq 500\text{ ns}$ , duty cycle $\leq 1\%$
Power dissipation	$P_{\text{tot}}$	-	-	211	W	$T_C = 25\text{ °C}$
Storage temperature	$T_{\text{stg}}$	-55	-	150	°C	-
Operating junction temperature	$T_j$	-55	-	175	°C	-
Mounting torque	-	-	-	n. a.	Ncm	-
Continuous reverse drain current <sup>1)</sup>	$I_{\text{SDC}}$	-	-	47 37	A	$V_{\text{GS}} = 18\text{ V}$ , $T_C = 25\text{ °C}$ $V_{\text{GS}} = 0\text{ V}$ , $T_C = 25\text{ °C}$
Peak reverse drain current <sup>2)</sup>	$I_{\text{SM}}$	-	-	134 43	A	$T_C = 25\text{ °C}$ , $t_p \leq 250\text{ ns}$ $T_C = 25\text{ °C}$
Insulation withstand voltage	$V_{\text{ISO}}$	-	-	n. a.	V	$V_{\text{rms}}$ , $T_C = 25\text{ °C}$ , $t = 1\text{ min}$

<sup>1)</sup> Limited by  $T_{j,\text{max}}$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,\text{max}}$

<sup>3)</sup> The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	0.71	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL3

## 3 Operating range

**Table 4 Operating range**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots <sup>1)</sup>	$V_{GS}$	-2	-	20	V	-
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

<sup>1)</sup> **Important notice:** If the gate source voltage of the device in application exceeds the operating range (Table 4), the device  $R_{DS(on)}$  and  $V_{GS(th)}$  might exceed the maximum value stated in the datasheet at the end of the lifetime of the device. In order to ensure sound operation of the device over the planned lifetime, the maximum ratings (Table 2) and the application note AN2018-09 must be considered.

## 4 Electrical characteristics

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 5 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source voltage <sup>1)</sup>	$V_{DSS}$	750	-	-	V	$V_{GS} = 0\text{ V}$ , $I_D = 0.60\text{ mA}$ , $T_j = -55\text{ °C}$ to $175\text{ °C}$
Gate threshold voltage <sup>2)</sup>	$V_{GS(th)}$	3.5	4.3	5.6	V	$V_{DS} = V_{GS}$ , $I_D = 6.0\text{ mA}$
Zero gate voltage drain current	$I_{DSS}$	-	1 10	75 -	$\mu\text{A}$	$V_{DS} = 750\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 25\text{ °C}$ $V_{DS} = 750\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_j = 175\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	49 40 37 72	- 52 -	m $\Omega$	$V_{GS} = 15\text{ V}$ , $I_D = 16.6\text{ A}$ , $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $T_j = 25\text{ °C}$ $V_{GS} = 20\text{ V}$ , $I_D = 16.6\text{ A}$ , $T_j = 25\text{ °C}$ $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $T_j = 175\text{ °C}$
Internal gate resistance	$R_{G,int}$	-	6	-	$\Omega$	$f = 1\text{ MHz}$

**Table 6 Dynamic characteristics**

External parasitic elements (PCB layout) influence switching behavior significantly.

Stray inductances and coupling capacitances must be minimized.

For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1135	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 500\text{ V}$ , $f = 250\text{ kHz}$
Reverse transfer capacitance	$C_{riss}$	-	7.2	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 500\text{ V}$ , $f = 250\text{ kHz}$
Output capacitance <sup>3)</sup>	$C_{oss}$	-	76	99	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 500\text{ V}$ , $f = 250\text{ kHz}$
Output charge <sup>3)</sup>	$Q_{oss}$	-	68	89	nC	calculation based on $C_{oss}$
Effective output capacitance, energy related <sup>4)</sup>	$C_{o(er)}$	-	98	-	pF	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0...500\text{ V}$
Effective output capacitance, time related <sup>5)</sup>	$C_{o(tr)}$	-	137	-	pF	$I_D = \text{constant}$ , $V_{GS} = 0\text{ V}$ , $V_{DS} = 0...500\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD} = 500\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Rise time	$t_r$	-	12	-	ns	$V_{DD} = 500\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Turn-off delay time	$t_{d(off)}$	-	20	-	ns	$V_{DD} = 500\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10
Fall time	$t_f$	-	8	-	ns	$V_{DD} = 500\text{ V}$ , $V_{GS} = 18\text{ V}$ , $I_D = 16.6\text{ A}$ , $R_G = 1.8\text{ }\Omega$ ; see table 10

<sup>1)</sup> Tested at  $T_j = 25\text{ °C}$ , minimum  $V_{DSS}$  verified by design over full junction temperature range.

<sup>2)</sup> Tested after 1 ms pulse at  $V_{GS} = +20\text{ V}$ .

<sup>3)</sup> Maximum specification is defined by calculated six sigma upper confidence bound.

<sup>4)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500 V.

<sup>5)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 500 V.

**Table 7 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	9.1	-	nC	$V_{DD} = 500\text{ V}$ , $I_D = 16.6\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Gate to drain charge	$Q_{GD}$	-	8.6	-	nC	$V_{DD} = 500\text{ V}$ , $I_D = 16.6\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$
Total gate charge	$Q_G$	-	34	-	nC	$V_{DD} = 500\text{ V}$ , $I_D = 16.6\text{ A}$ , $V_{GS} = 0\text{ to }18\text{ V}$

**Table 8 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	$V_{SD}$	-	3.9	5.3	V	$V_{GS} = 0\text{ V}$ , $I_S = 16.6\text{ A}$ , $T_j = 25\text{ °C}$
MOSFET forward recovery time	$t_{fr}$	-	19 10	-	ns	$V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9 $V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET forward recovery charge <sup>1)</sup>	$Q_{fr}$	-	75 115	-	nC	$V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9 $V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9
MOSFET peak forward recovery current	$I_{frm}$	-	7.7 22	-	A	$V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 1000\text{ A}/\mu\text{s}$ ; see table 9 $V_{DD} = 500\text{ V}$ , $I_S = 16.6\text{ A}$ , $di_S/dt = 4000\text{ A}/\mu\text{s}$ ; see table 9

<sup>1)</sup>  $Q_{fr}$  includes  $Q_{oss}$

## 5 Electrical characteristics diagrams

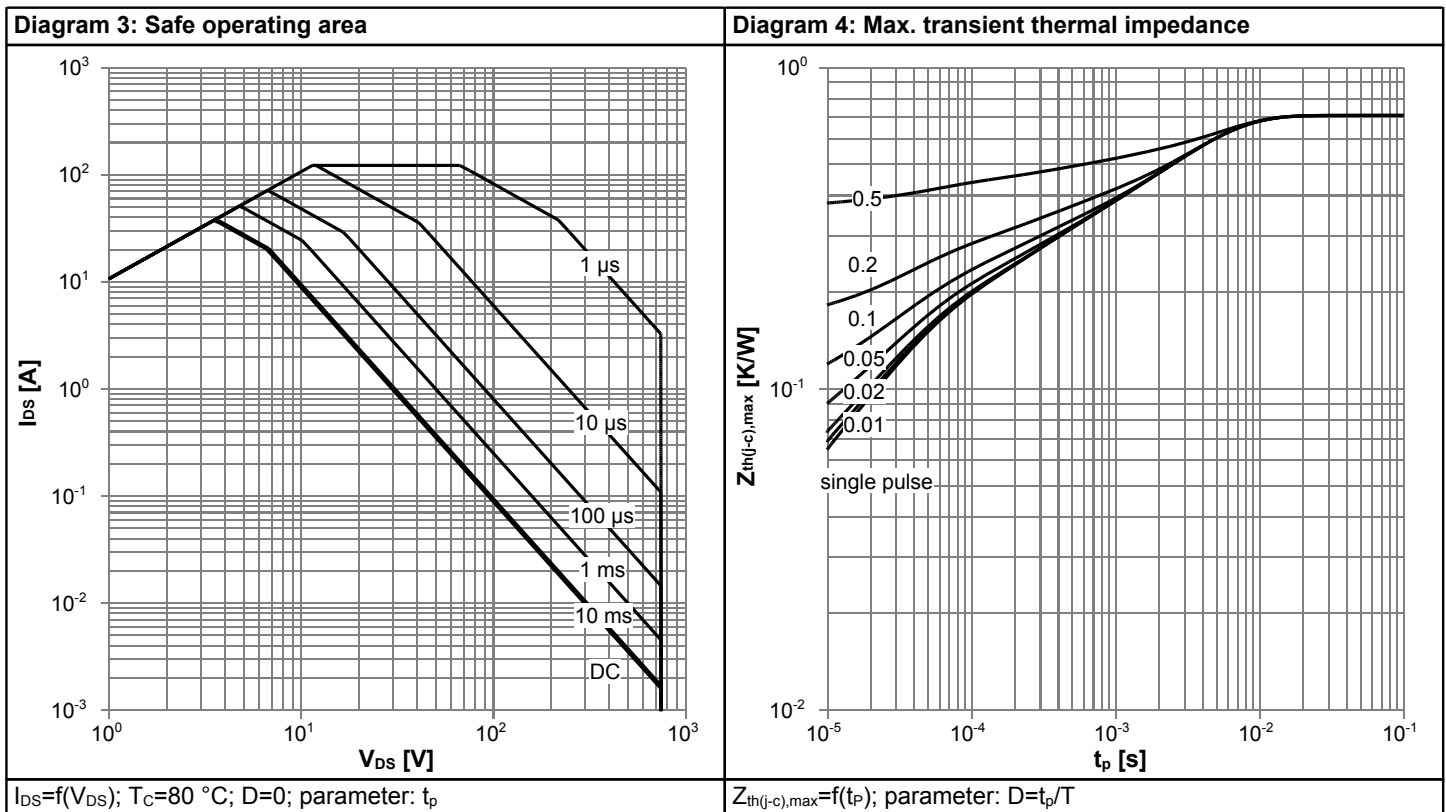
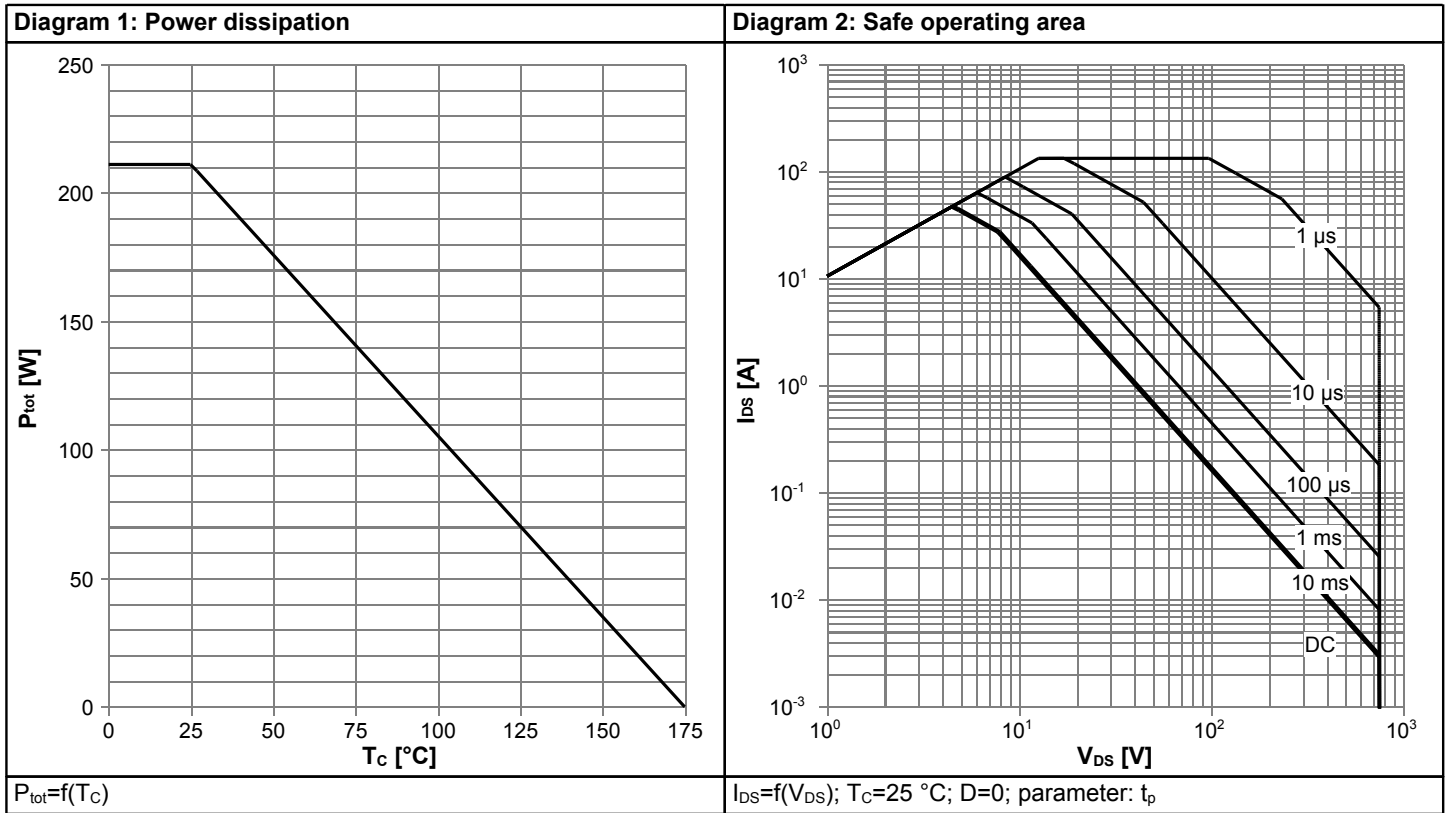
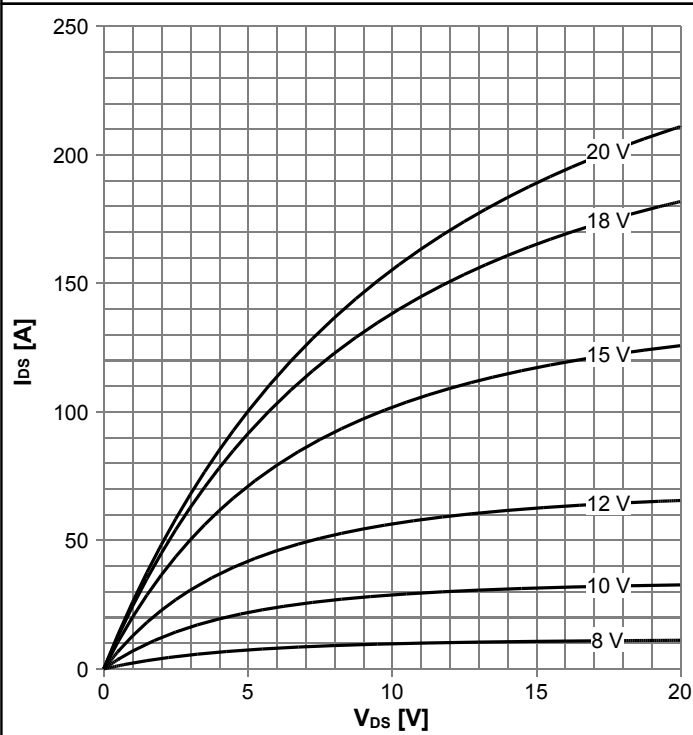
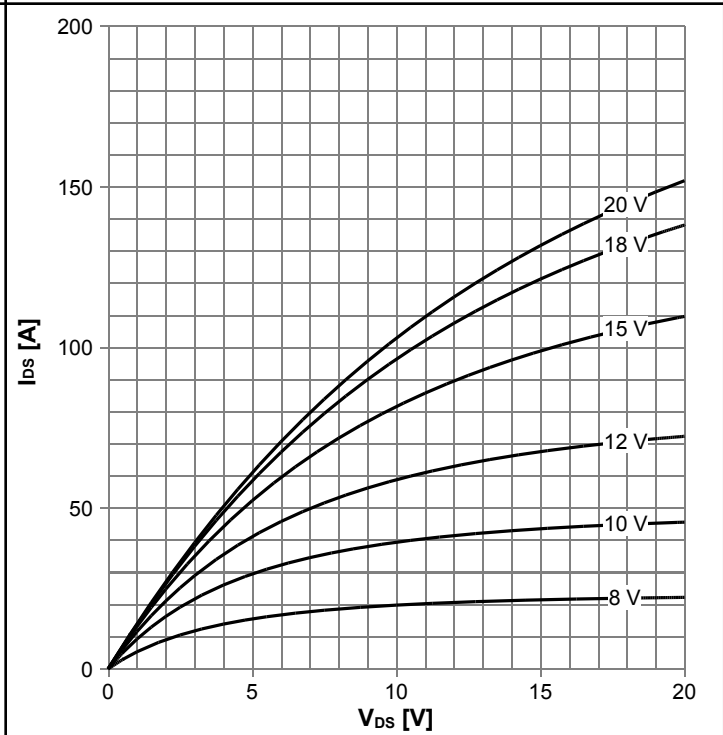


Diagram 5: Typ. output characteristics



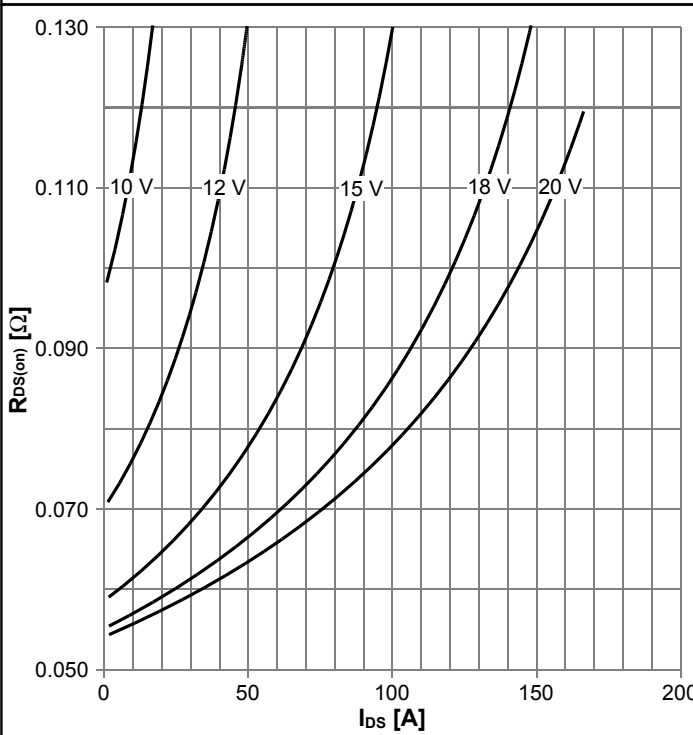
$I_{DS}=f(V_{DS}); T_J=25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics



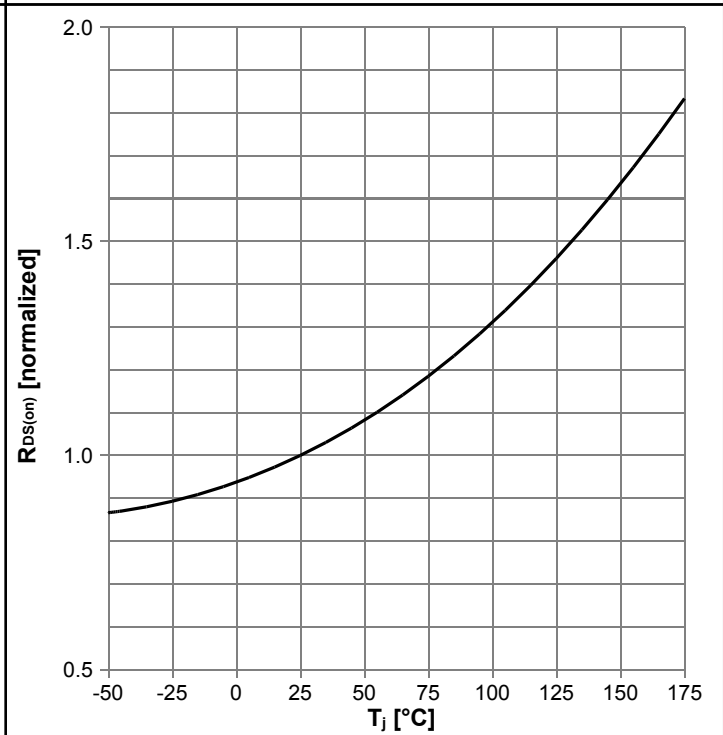
$I_{DS}=f(V_{DS}); T_J=175\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_{DS}); T_J=125\text{ °C}; \text{parameter: } V_{GS}$

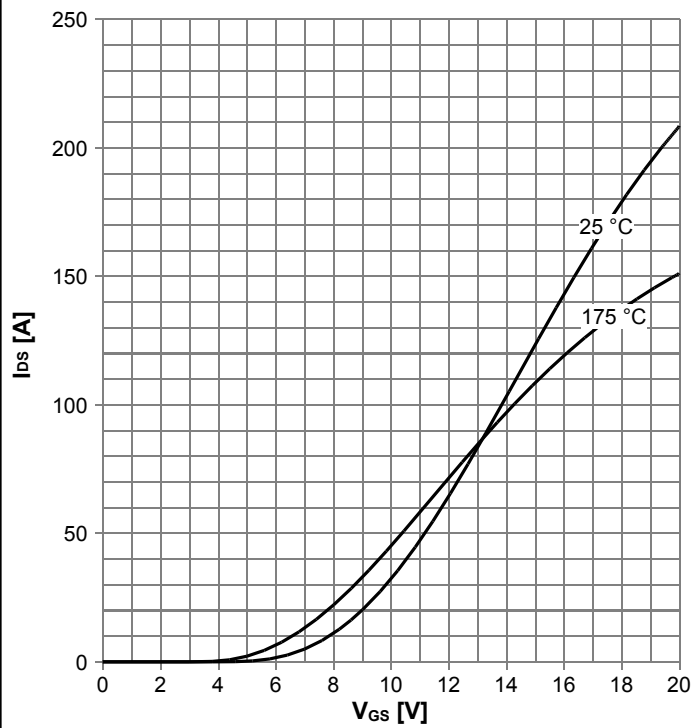
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_J); I_D=16.6\text{ A}; V_{GS}=18\text{ V}$

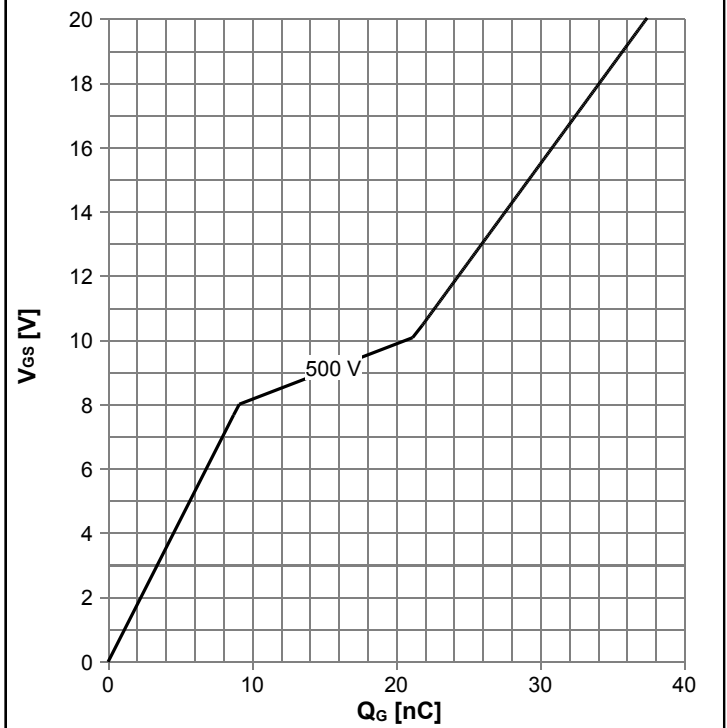


**Diagram 9: Typ. transfer characteristics**



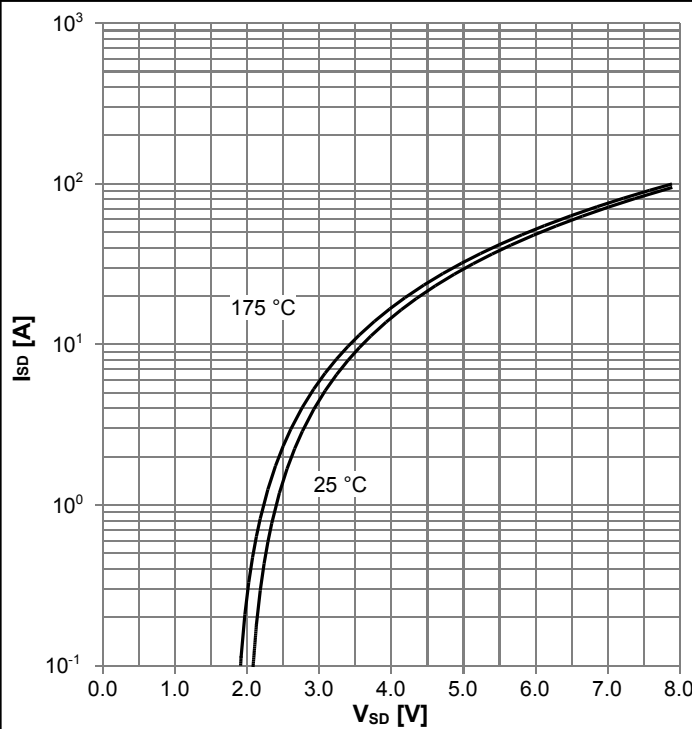
$I_{DS}=f(V_{GS})$ ;  $V_{DS}=20$  V; parameter:  $T_j$

**Diagram 10: Typ. gate charge**



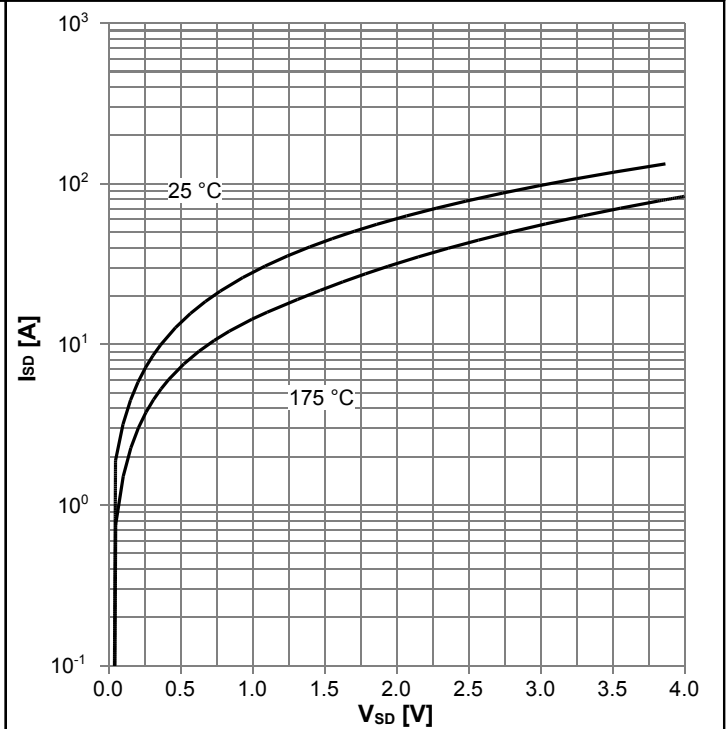
$V_{GS}=f(Q_G)$ ;  $I_{DS}=16.6$  A pulsed; parameter:  $V_{DD}$

**Diagram 11: Typ. reverse drain current characteristics**

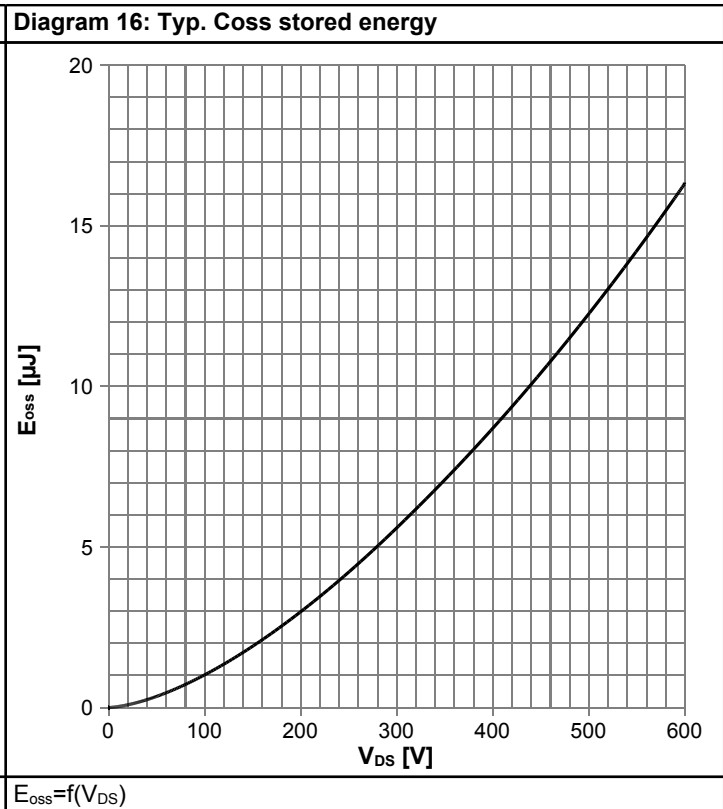
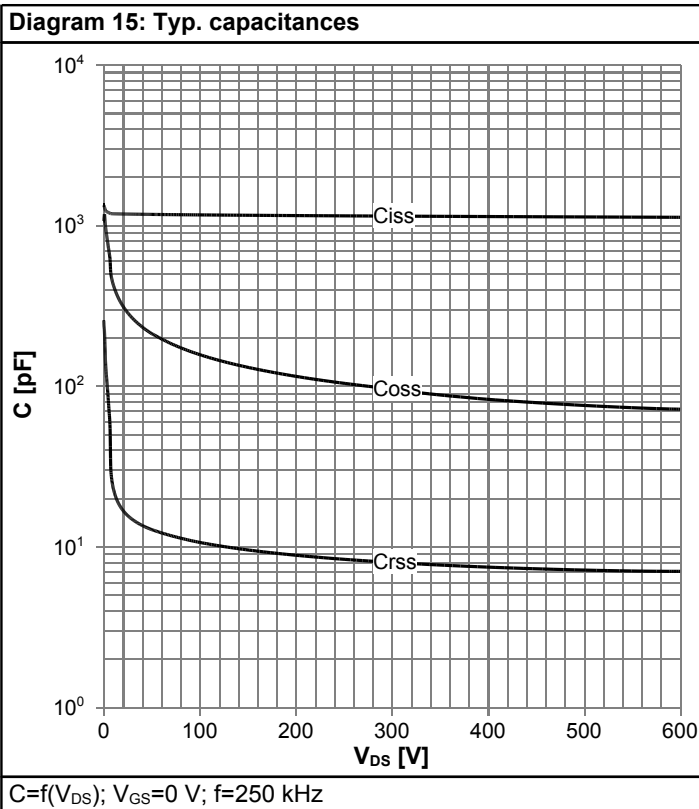
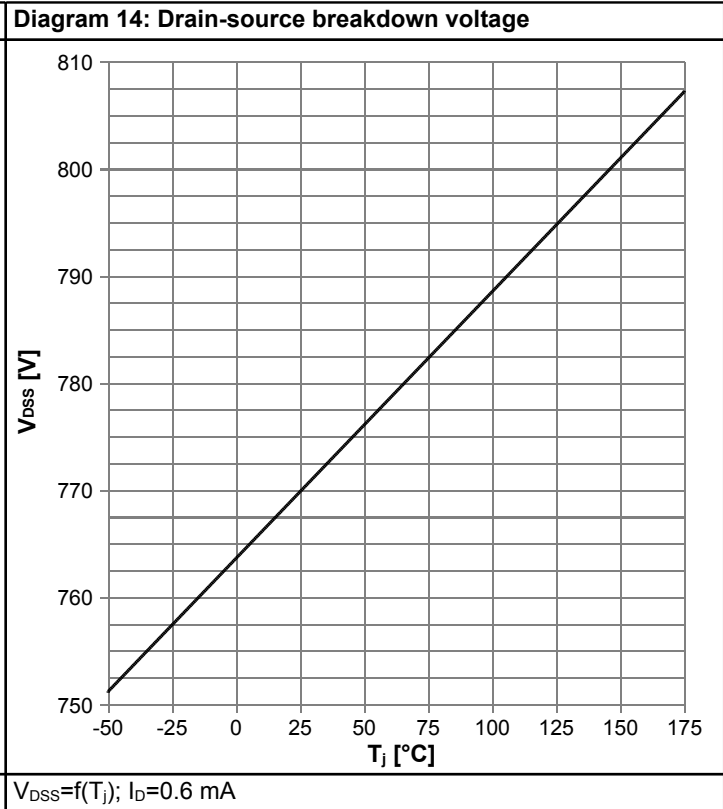
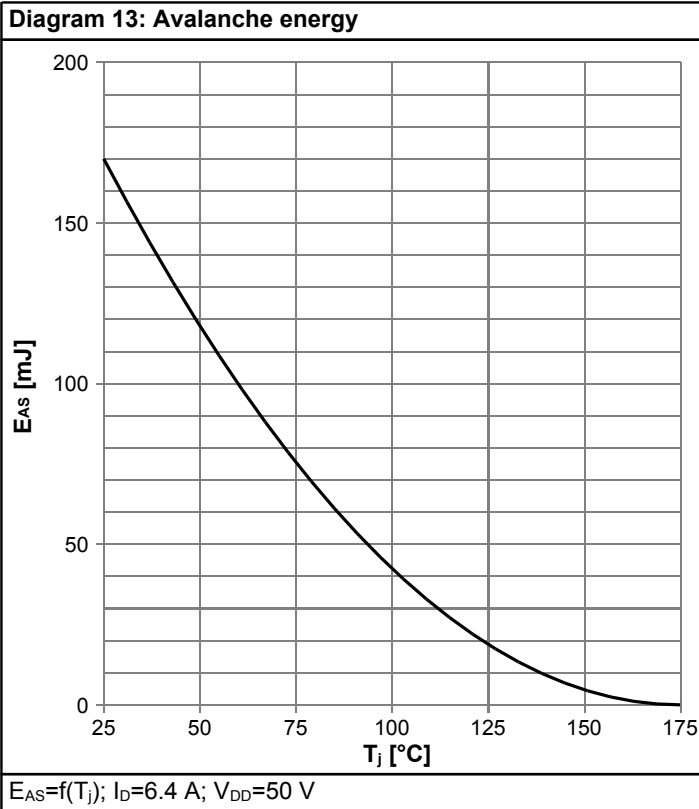


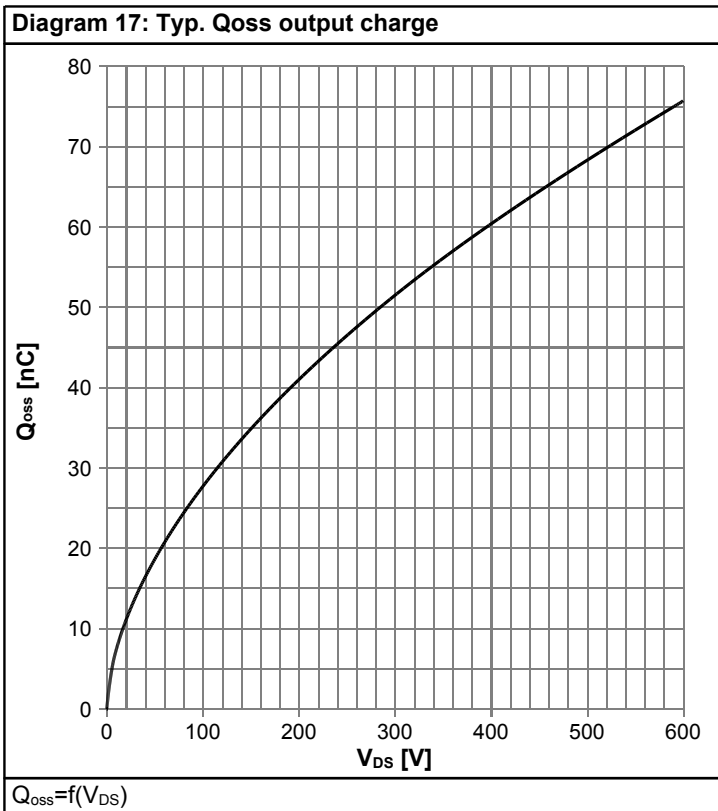
$I_{SD}=f(V_{SD})$ ;  $V_{GS}=0$  V; parameter:  $T_j$

**Diagram 12: Typ. reverse drain current characteristics**



$I_{SD}=f(V_{SD})$ ;  $V_{GS}=18$  V; parameter:  $T_j$





## 6 Test Circuits

**Table 9 Body diode characteristics**

Test circuit for body diode characteristics	Body diode recovery waveform

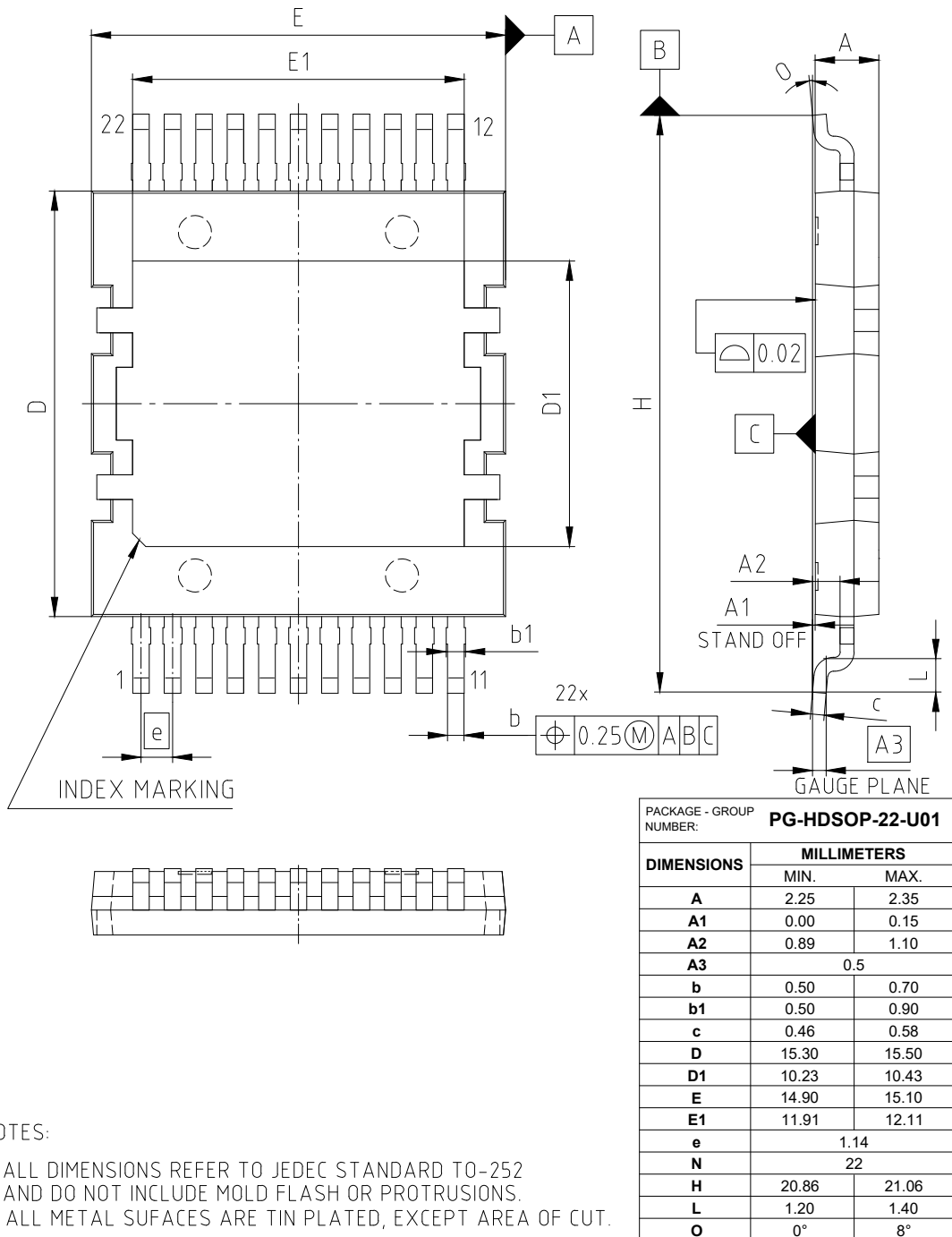
**Table 10 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 11 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 7 Package Outlines



**Figure 1 Outline PG-HDSOP-22, dimensions in mm**

## **8 Appendix A**

### **Table 12 Related Links**

- IFX CoolSiC CoolSiC™ Power Device 750 V G1 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC CoolSiC™ Power Device 750 V G1 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolSiC CoolSiC™ Power Device 750 V G1 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IMDQ75R040M1H

**Revision: 2023-08-28, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-08-28	Release of final version

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[C3M0120090J](#) [C3M0065090J](#) [C3M0280090J](#) [SCT2750NYTB](#) [SCT2H12NYTB](#) [C3M0021120D](#) [C3M0016120K](#) [C3M0045065D](#)  
[C3M0045065K](#) [E3M0120090J](#) [C3M0065090J-TR](#) [C3M0120100J](#) [C3M0075120J](#) [DMWS120H100SM4](#) [DMWSH120H28SM4](#)  
[DMWSH120H90SM4](#) [DMWSH120H90SM4Q](#) [DMWSH120H28SM4Q](#) [DMWSH120H90SCT7Q](#) [DMWSH120H28SM3](#)  
[DMWSH120H43SM3](#) [DMWSH120H90SM3](#) [DMWSH120H28SM3Q](#) [DMWSH120H90SM3Q](#) [DIF120SIC053-AQ](#) [DIW120SIC059-AQ](#)  
[G2R1000MT17D](#) [G3R60MT07K](#) [G2R50MT33K](#) [G3R12MT12K](#) [G3R160MT12D](#) [G3R160MT12J-TR](#) [G3R160MT17D](#) [G3R160MT17J-TR](#)  
[G3R20MT12K](#) [G3R20MT12N](#) [G3R20MT17K](#) [G3R20MT17N](#) [G3R30MT12J-TR](#) [G3R30MT12K](#) [G3R350MT12D](#) [G3R40MT12D](#)  
[G3R40MT12J](#)