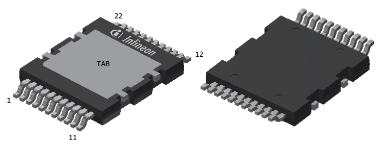
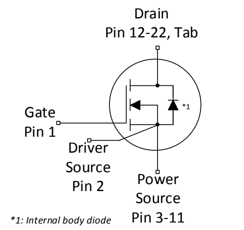
MOSFET

CoolSiC™ Power Device 750 V G1

The 750 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 750V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.

PG-HDSOP-22





Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class $R_{DS(on)}$ x Q_{fr}
- Excellent $R_{DS(on)}$ x Q_{oss} and $R_{DS(on)}$ x Q_G
- Unique combination of low C_{rss}/C_{iss} and high $V_{GS(th)}$
- Infineon proprietary die attach technology
- Cutting edge top side cooling package (QDPAK)
- Driver source pin available

Benefits

- Enhanced robustness to withstand bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

Potential applications

- EV charging infrastructure
- Solar PV inverters
- UPS (uninterruptable power supplies)
- Energy storage and battery formation
- Telecom and Server SMPS

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	140	mΩ
$R_{DS(on),max}$	182	mΩ
$Q_{G,typ}$	12	nC
$I_{DM,max}$	38	A
$Q_{oss,typ}$ @ 500 V	28	nC
$E_{oss,typ}$ @ 500 V	5.1	µJ

Type / Ordering Code	Package	Marking	Related Links
IMDQ75R140M1H	PG-HDSOP-22	75R140M1	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current[1]	I_{DDC}	- -	- -	17 12	A	T_C = 25 °C T_C = 100 °C
Peak drain current[2]	I_{DM}	-	-	38	A	T_C = 25 °C, V_{GS} = 18 V
Avalanche energy, single pulse	E_{AS}	-	-	48	mJ	I_D = 1.8 A, V_{DD} = 50 V; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.24	mJ	I_D = 1.8 A, V_{DD} = 50 V; see table 11
Avalanche current, single pulse	I_{AS}	-	-	1.8	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	V_{DS}= 0...500 V
Gate source voltage (static)[3]	V_{GS}	-5	-	23	V	-
Gate source voltage (transient)	V_{GS}	-10	-	25	V	$t_p \leq$ 500 ns, duty cycle $\leq$ 1%
Power dissipation	P_{tot}	-	-	100	W	T_C = 25 °C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	175	°C	-
Mounting torque	-	-	-	n. a.	Ncm	-
Continuous reverse drain current[1]	I_{SDC}	- -	- -	17 12	A	V_{GS} = 18 V, T_C = 25 °C V_{GS} = 0 V, T_C = 25 °C
Peak reverse drain current[2]	I_{SM}	- -	- -	38 13	A	T_C = 25 °C, $t_p \leq$ 250 ns T_C = 25 °C
Insulation withstand voltage	V_{ISO}	-	-	n. a.	V	V_{rms}, T_C = 25 °C, t = 1 min

[1] Limited by $T_{j,max}$
[2] Pulse width t_p limited by $T_{j,max}$
[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	1.5	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL3

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots[1)]	V_{GS}	-2	-	20	V	-
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

[1)] **Important notice:** If the gate source voltage of the device in application exceeds the operating range (Table 4), the device $R_{DS(on)}$ and $V_{GS(th)}$ might exceed the maximum value stated in the datasheet at the end of the lifetime of the device. In order to ensure sound operation of the device over the planned lifetime, the maximum ratings (Table 2) and the application note AN2018-09 must be considered.

4 Electrical characteristics

at T_j = 25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source voltage[1]	V_{DSS}	750	-	-	V	V_{GS} = 0 V, I_D = 0.17 mA, T_j = -55 °C to 175 °C
Gate threshold voltage[2]	$V_{GS(th)}$	3.5	4.3	5.6	V	V_{DS} = V_{GS}, I_D = 1.7 mA
Zero gate voltage drain current	I_{DSS}	- -	1 10	75 -	µA	V_{DS} = 750 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 750 V, V_{GS} = 0 V, T_j = 175 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS} = 20 V, V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	- - - -	172 140 129 252	- 182 - -	mΩ	V_{GS} = 15 V, I_D = 4.7 A, T_j = 25 °C V_{GS} = 18 V, I_D = 4.7 A, T_j = 25 °C V_{GS} = 20 V, I_D = 4.7 A, T_j = 25 °C V_{GS} = 18 V, I_D = 4.7 A, T_j =175 °C
Internal gate resistance	$R_{G,int}$	-	16	-	Ω	f = 1 MHz

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	351	-	pF	V_{GS} = 0 V, V_{DS} = 500 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}	-	2.5	-	pF	V_{GS} = 0 V, V_{DS} = 500 V, f = 250 kHz
Output capacitance[3]	C_{oss}	-	32	41	pF	V_{GS} = 0 V, V_{DS} = 500 V, f = 250 kHz
Output charge[3]	Q_{oss}	-	28	37	nC	calculation based on C_{oss}
Effective output capacitance, energy related[4]	$C_{o(er)}$	-	41	-	pF	V_{GS} = 0 V, V_{DS} = 0...500 V
Effective output capacitance, time related[5]	$C_{o(tr)}$	-	57	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0...500 V
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	V_{DD} = 500 V, V_{GS} = 18 V, I_D = 4.7 A, R_G = 1.8 Ω; see table 10
Rise time	t_r	-	7	-	ns	V_{DD} = 500 V, V_{GS} = 18 V, I_D = 4.7 A, R_G = 1.8 Ω; see table 10
Turn-off delay time	$t_{d(off)}$	-	13	-	ns	V_{DD} = 500 V, V_{GS} = 18 V, I_D = 4.7 A, R_G = 1.8 Ω; see table 10
Fall time	t_f	-	13	-	ns	V_{DD} = 500 V, V_{GS} = 18 V, I_D = 4.7 A, R_G = 1.8 Ω; see table 10

[1] Tested at T_j = 25 °C, minimum V_{DSS} verified by design over full junction temperature range.
[2] Tested after 1 ms pulse at V_{GS} = +20 V.
[3] Maximum specification is defined by calculated six sigma upper confidence bound.
[4] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500 V.
[5] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500 V.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	2.8	-	nC	V_{DD} = 500 V, I_D = 4.7 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{GD}	-	3.1	-	nC	V_{DD} = 500 V, I_D = 4.7 A, V_{GS} = 0 to 18 V
Total gate charge	Q_G	-	12	-	nC	V_{DD} = 500 V, I_D = 4.7 A, V_{GS} = 0 to 18 V

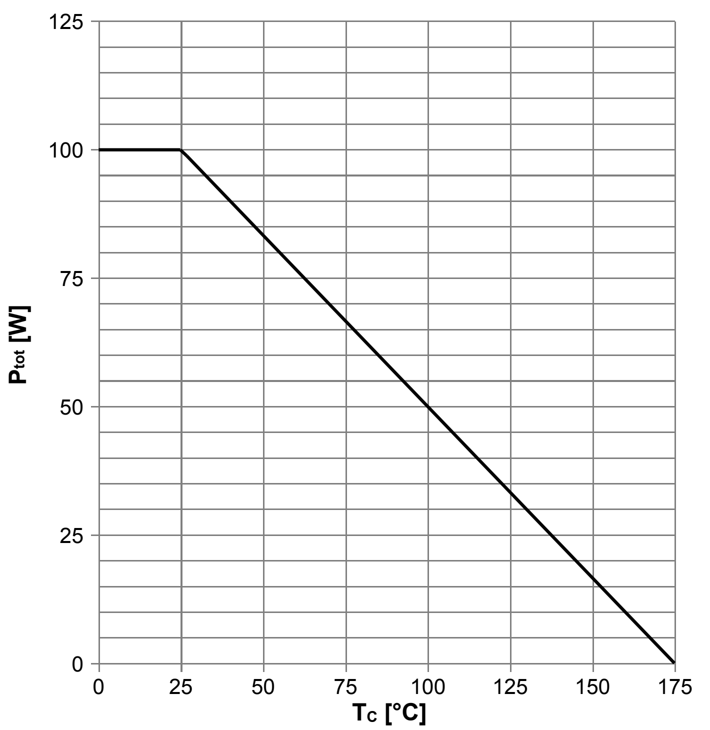
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	3.9	5.3	V	V_{GS} = 0 V, I_S = 4.7 A, T_j = 25 °C
MOSFET forward recovery time	t_{fr}	- -	20 7	- -	ns	V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 1000 A/µs; see table 9 V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 4000 A/µs; see table 9
MOSFET forward recovery charge[1)]	Q_{fr}	- -	46 57	- -	nC	V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 1000 A/µs; see table 9 V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 4000 A/µs; see table 9
MOSFET peak forward recovery current	I_{frm}	- -	4.6 16	- -	A	V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 1000 A/µs; see table 9 V_{DD} = 500 V, I_S = 4.7 A, di_S/dt = 4000 A/µs; see table 9

1) Q_{fr} includes Q_{oss}

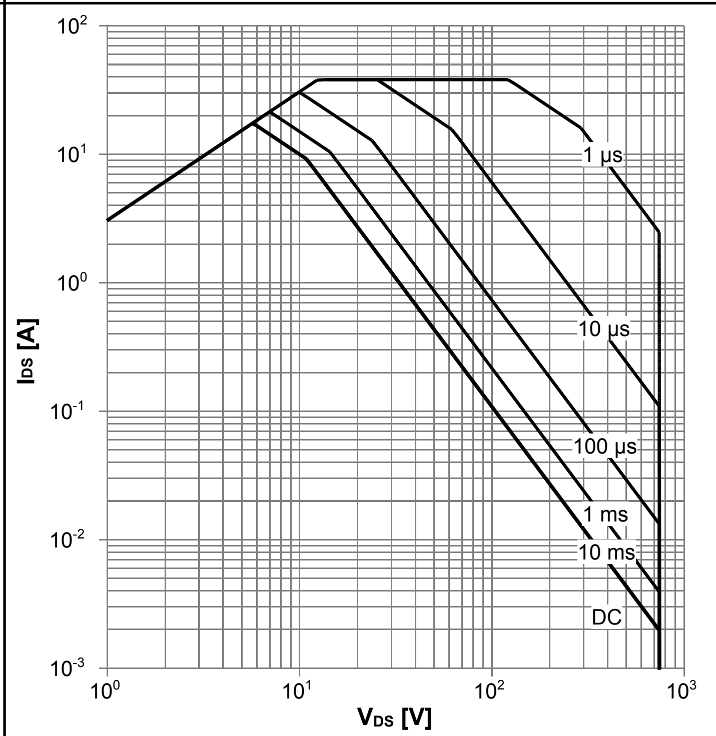
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



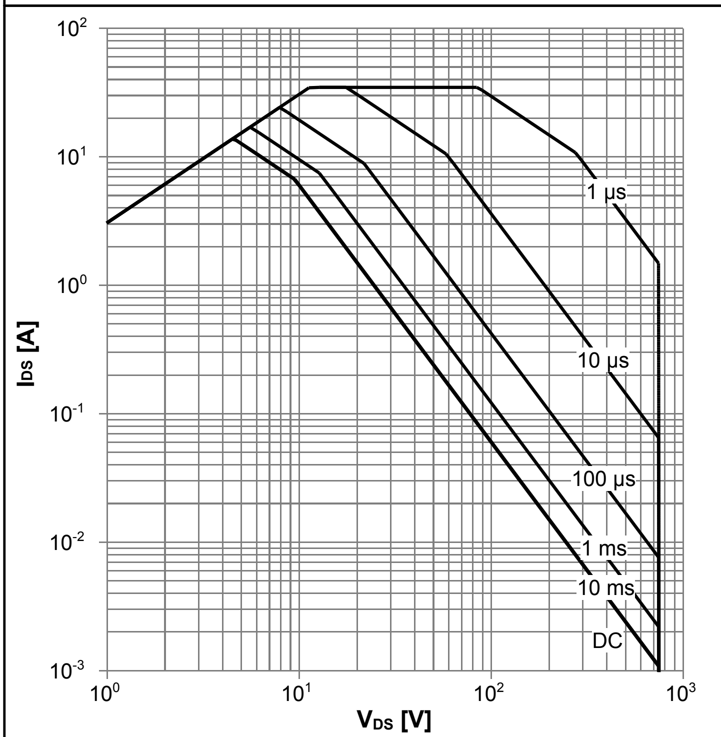
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



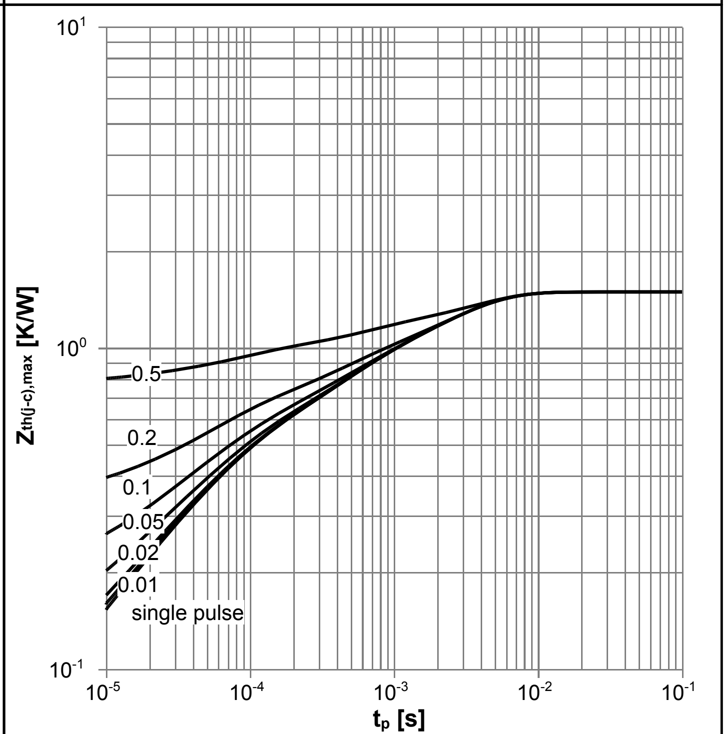
$I_{DS}=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



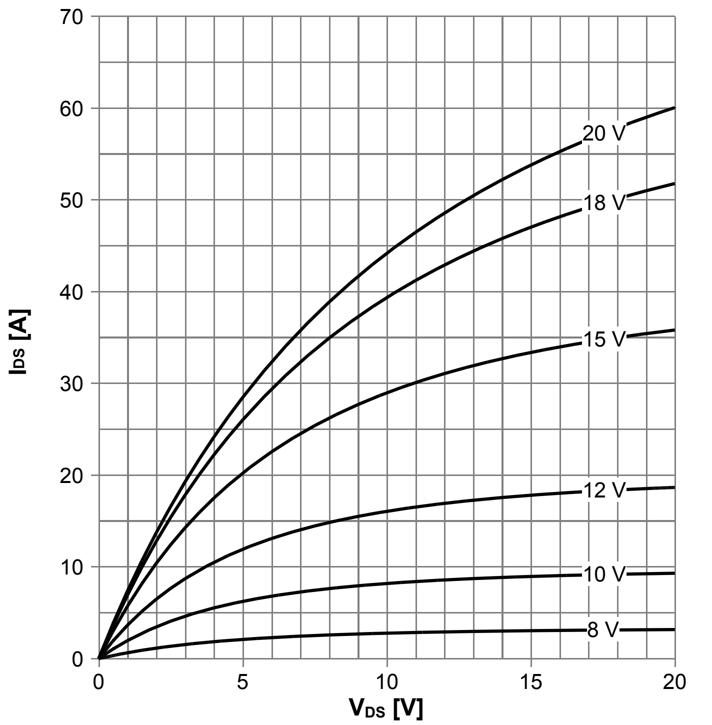
$I_{DS}=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



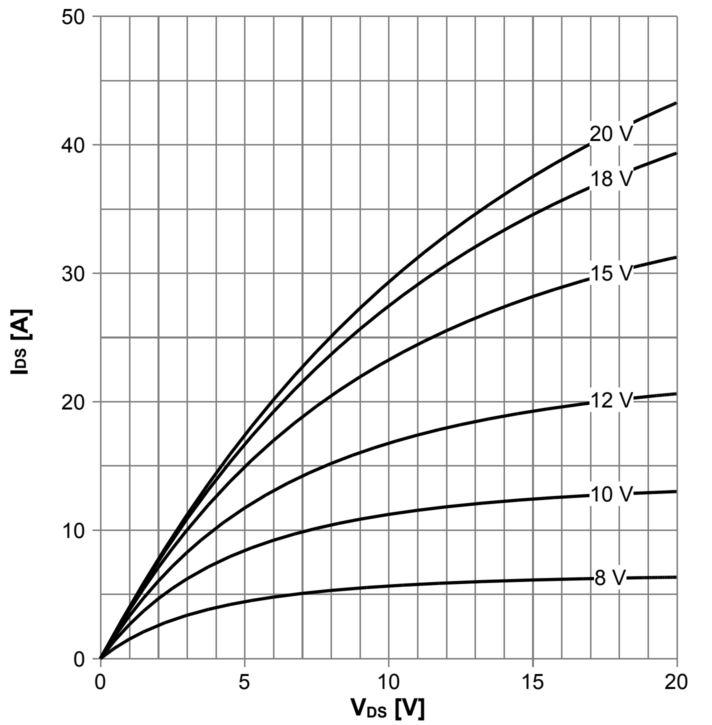
$Z_{th(j-c),max}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



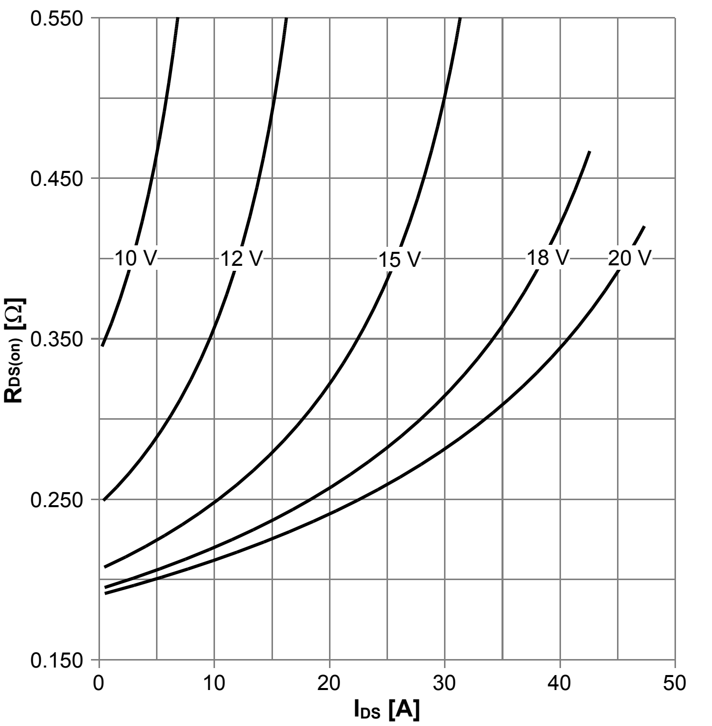
$I_{DS}=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



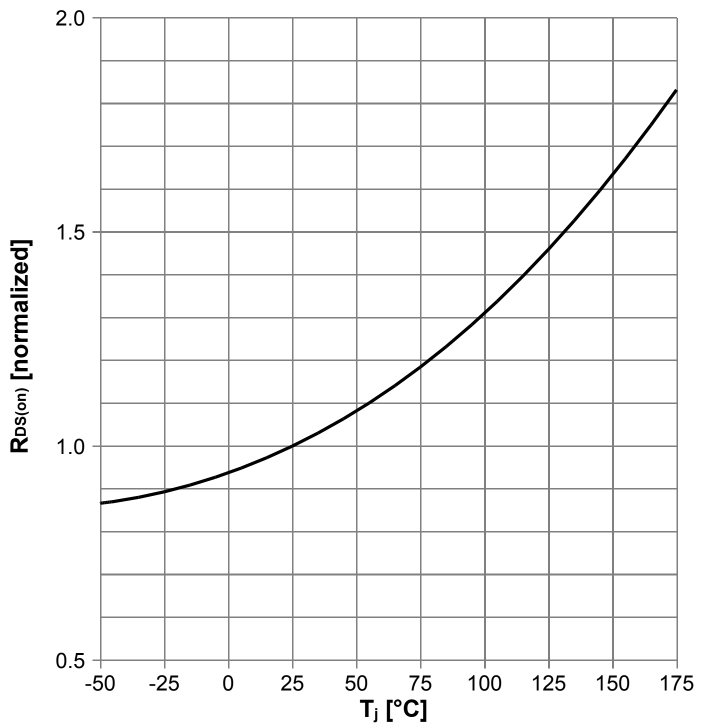
$I_{DS}=f(V_{DS})$; $T_j=175$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



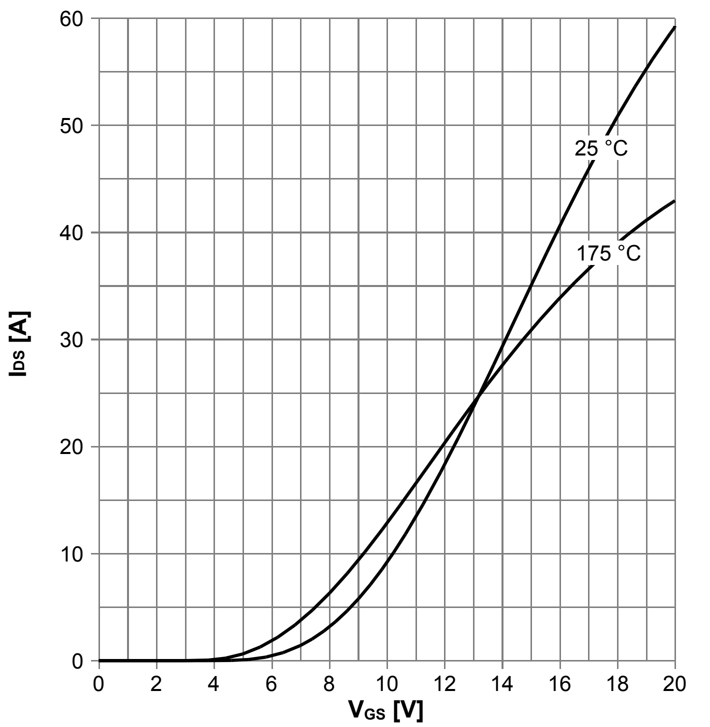
$R_{DS(on)}=f(I_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



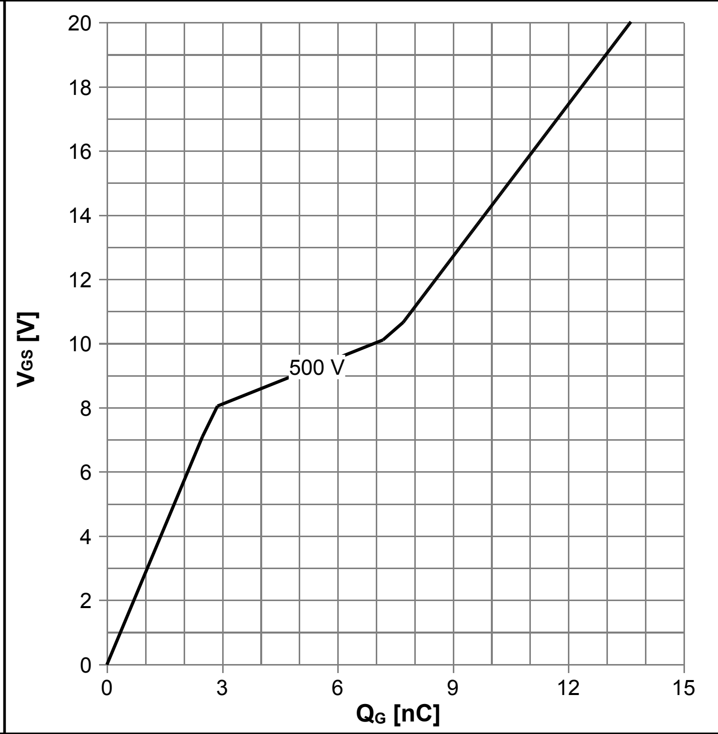
$R_{DS(on)}=f(T_j)$; $I_D=4.7$ A; $V_{GS}=18$ V

Diagram 9: Typ. transfer characteristics



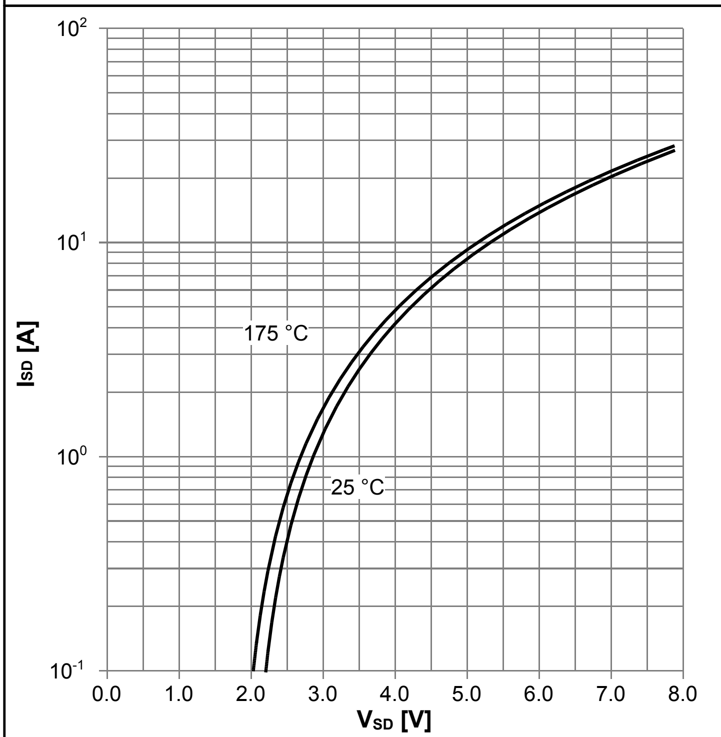
I_{DS}=f(V_{GS}); V_{DS}=20 V; parameter: T_j

Diagram 10: Typ. gate charge



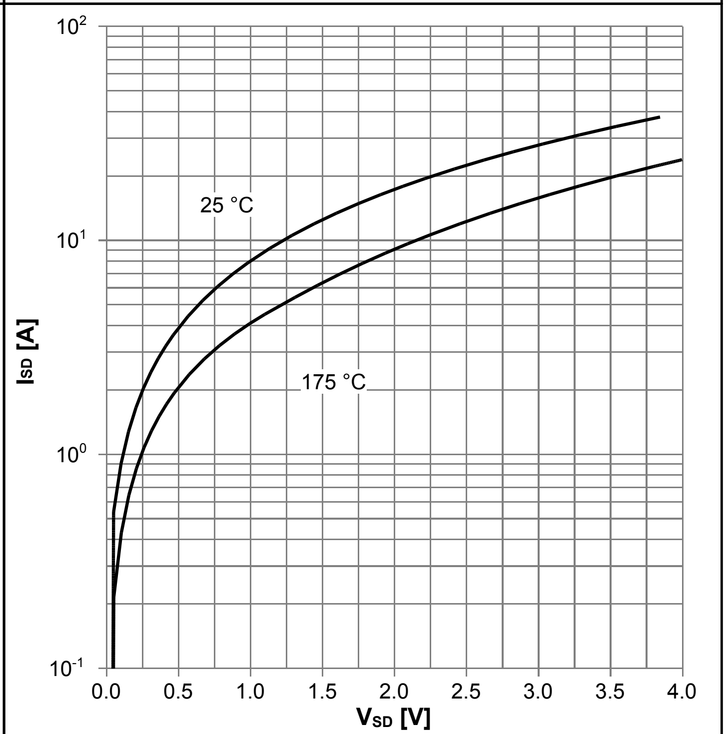
V_{GS}=f(Q_G); I_D=4.7 A pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse drain current characteristics



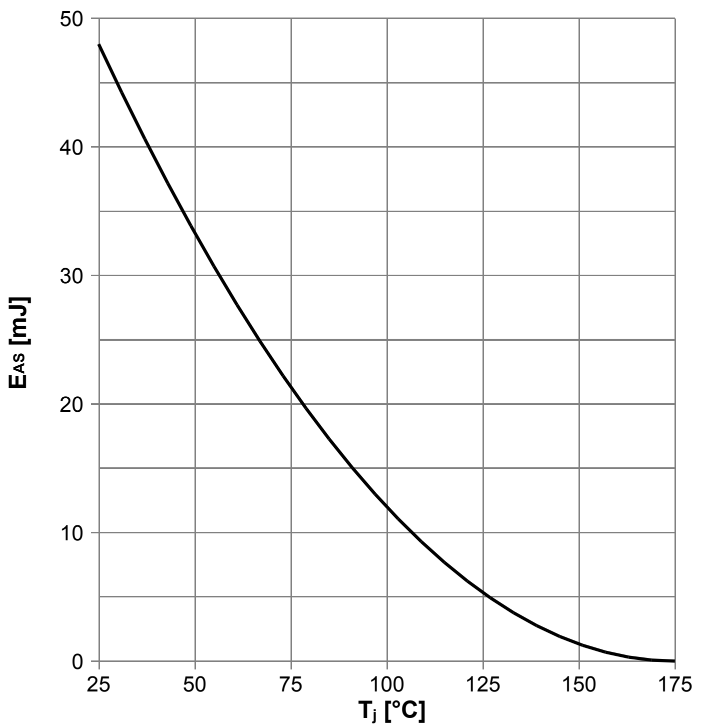
I_{SD}=f(V_{SD}); V_{GS}=0 V; parameter: T_j

Diagram 12: Typ. reverse drain current characteristics



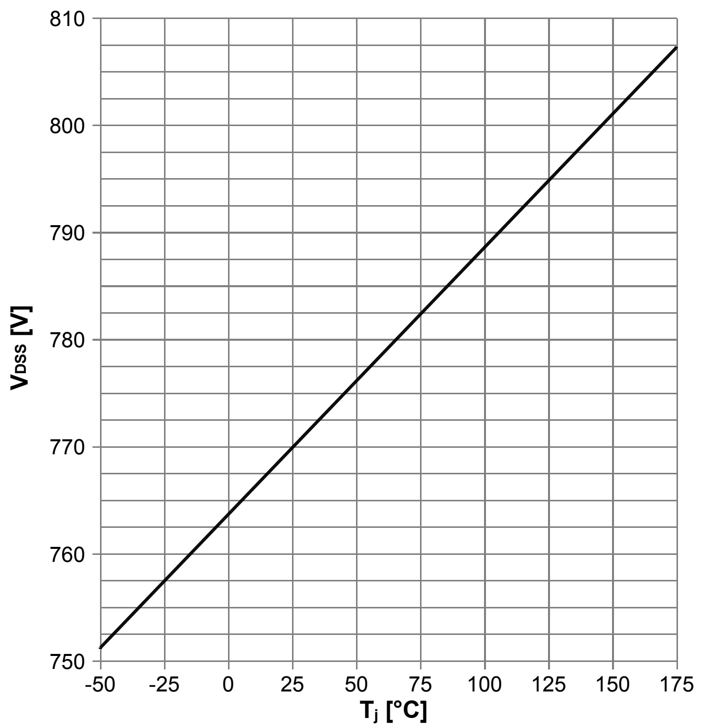
I_{SD}=f(V_{SD}); V_{GS}=18 V; parameter: T_j

Diagram 13: Avalanche energy



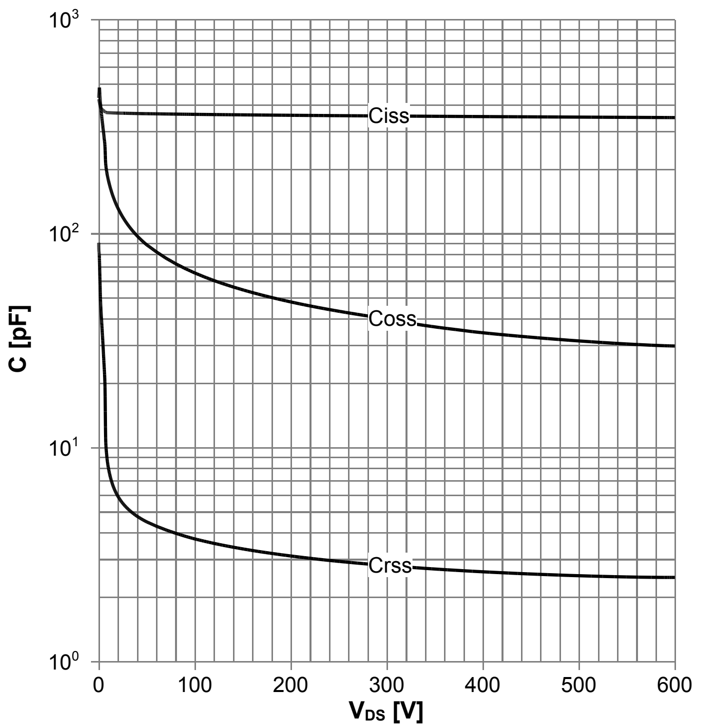
$E_{AS}=f(T_j)$; $I_D=1.8$ A; $V_{DD}=50$ V

Diagram 14: Drain-source breakdown voltage



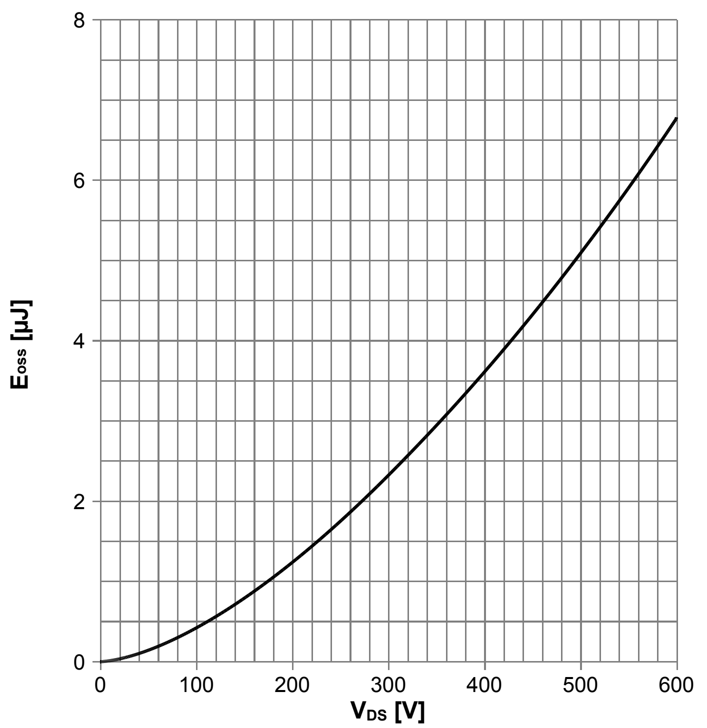
$V_{DSS}=f(T_j)$; $I_D=0.17$ mA

Diagram 15: Typ. capacitances

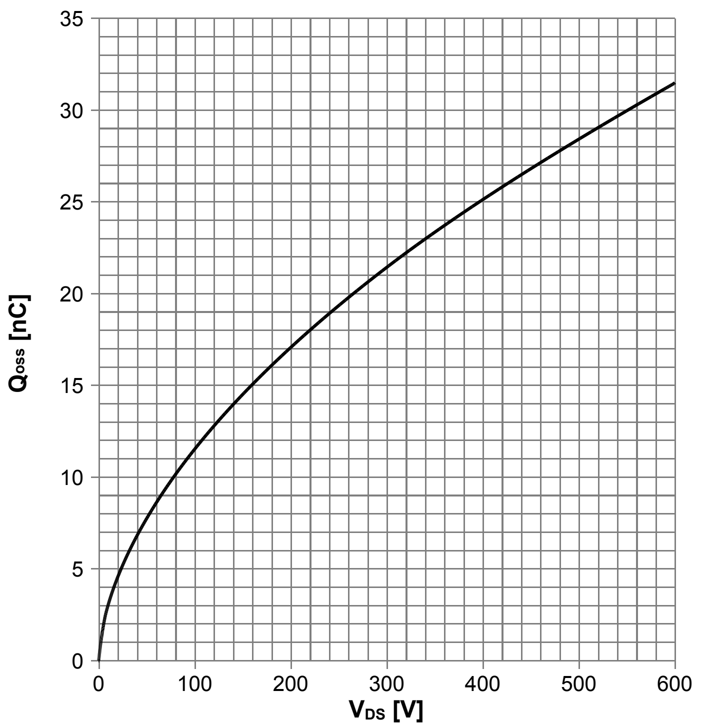


$C=f(V_{DS})$; $V_{GS}=0$ V; f=250 kHz

Diagram 16: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge

$Q_{oss}=f(V_{DS})$

6 Test Circuits

Table 9 Body diode characteristics

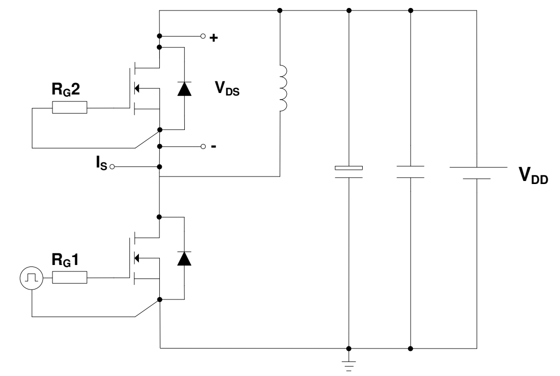
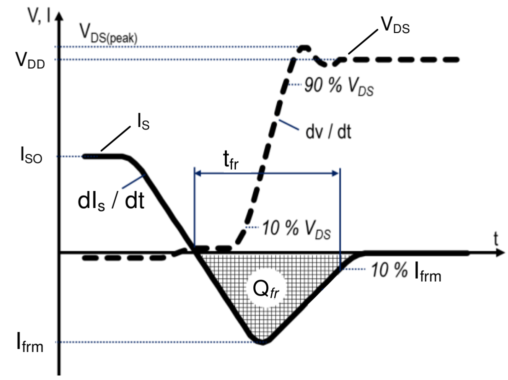
Test circuit for body diode characteristics	Body diode recovery waveform
	

Table 10 Switching times

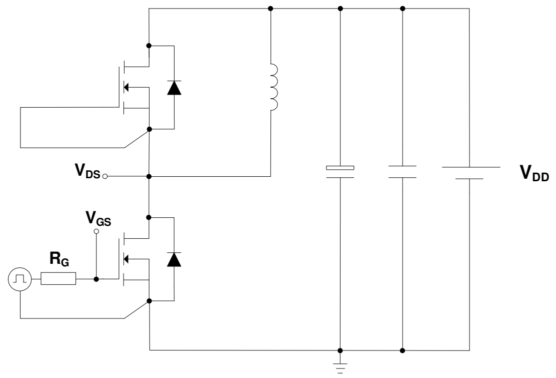
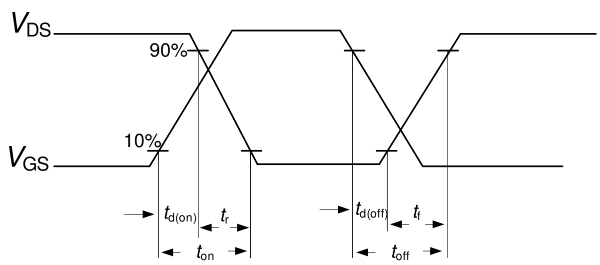
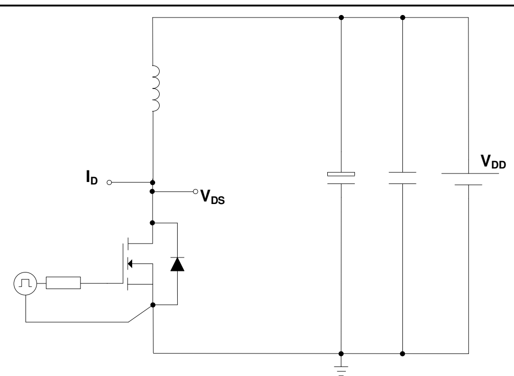
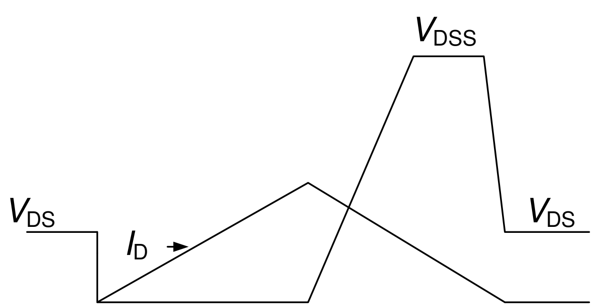
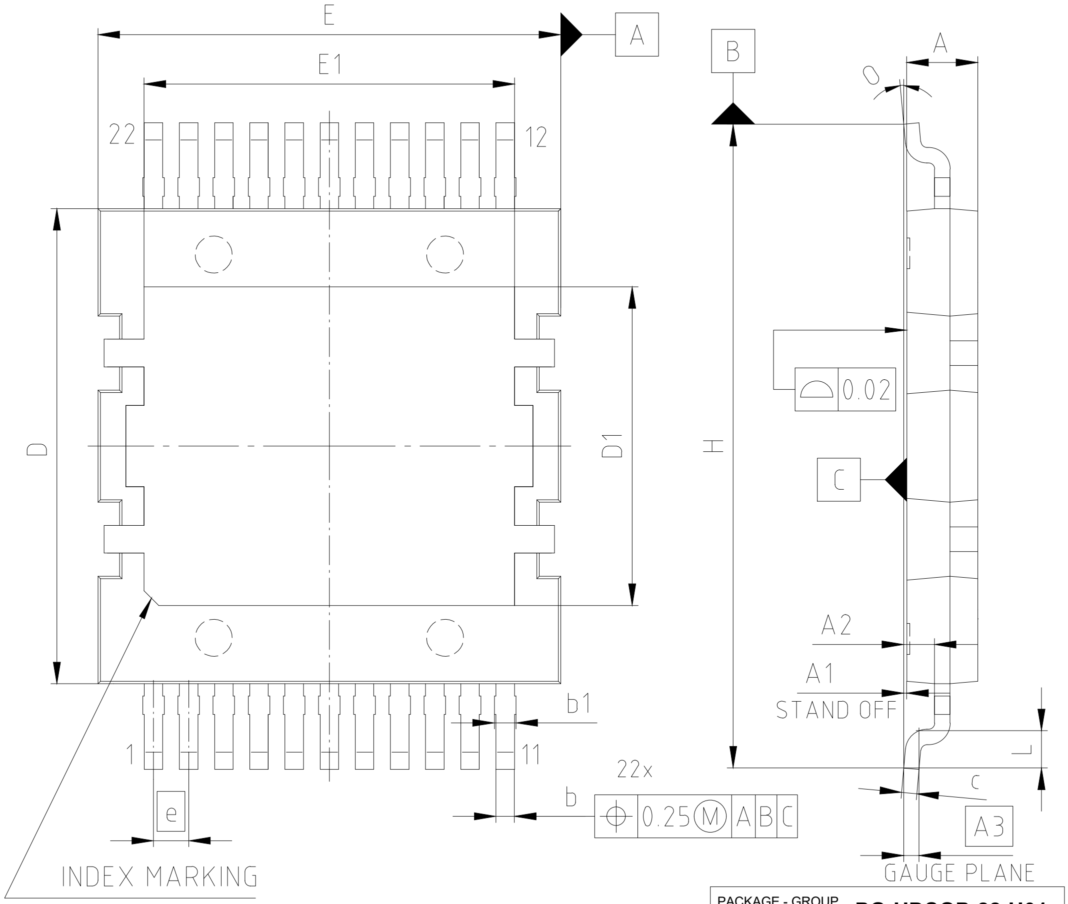
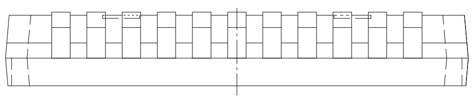
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines





PACKAGE - GROUP NUMBER:	PG-HDSOP-22-U01	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.89	1.10
A3	0.5	
b	0.50	0.70
b1	0.50	0.90
c	0.46	0.58
D	15.30	15.50
D1	10.23	10.43
E	14.90	15.10
E1	11.91	12.11
e	1.14	
N	22	
H	20.86	21.06
L	1.20	1.40
O	0°	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. ALL METAL SUFACES ARE TIN PLATED, EXCEPT AREA OF CUT.

Figure 1 Outline PG-HDSOP-22, dimensions in mm

8 Appendix A

Table 12 Related Links

- **IFX CoolSiC CoolSiC™ Power Device 750 V G1 Webpage:** www.infineon.com
- **IFX CoolSiC CoolSiC™ Power Device 750 V G1 application note:** www.infineon.com
- **IFX CoolSiC CoolSiC™ Power Device 750 V G1 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IMDQ75R140M1H

Revision: 2023-10-10, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-08-28	Release of final version
2.1	2023-10-10	Updated (reduced) Ciss, Crss, Coss, Qoss, Eoss, Qgs(pl), Qgd, and corresponding diagrams.

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The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.