CoolSiC™ 1200 V SiC Trench MOSFET : Silicon Carbide MOSFET with .XT interconnection technology

Halogen-free
Green
Lead-free
RoHS

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 55 A at T_c = 25°C
- $R_{DS(on)}$ = 39 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Short circuit withstand time 3 µs
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance

Potential applications

- General purpose drives (GPD)
- EV-Charging
- Online UPS/Industrial UPS
- String inverter
- Solar power optimizer

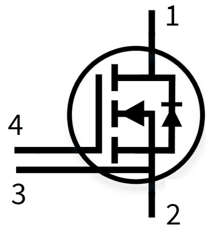
Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

1 – drain
2 – source
3 – Kelvin sense contact
4 – gate

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	**Package**	**Marking**
IMZA120R040M1H	PG-TO247-4-STD-NT3.7	12M1H040

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	wave soldering 1.6 mm (0.063 in.) from case for 10 s			260	°C
Mounting torque	M	M3 screw, Maximum of mounting processes: 3			0.6	Nm
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			0.51	0.66	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	55	A
			$T_c = 100$ °C	39	
Peak drain current, t_p limited by $T_{vj(max)}$	I_{DM}	$V_{GS} = 18$ V		117	A
Gate-source voltage, max. transient voltage[1)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10/23	V
Gate-source voltage, max. static voltage	V_{GS}			-7/20	V
Avalanche energy, single pulse	E_{AS}	$I_D = 18.8$ A, $V_{DD} = 50$ V, $L = 1.9$ mH		339	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 18.8$ A, $V_{DD} = 50$ V, $L = 9.5$ µH		1.68	mJ
Short-circuit withstand time	t_{SC}	$V_{DD} \leq 800$ V, $V_{DS,peak} < 1200$ V, $V_{GS(on)} = 15$ V, $T_{vj(start)} = 25$ °C		3	µs
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	227	W
			$T_c = 100$ °C	114	

1) Important note: The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	I_D = 19.3 A	T_{vj} = 25 °C, $V_{GS(on)}$ = 18 V		39	54.4	mΩ
			T_{vj} = 100 °C, $V_{GS(on)}$ = 18 V		54		
			T_{vj} = 175 °C, $V_{GS(on)}$ = 18 V		77		
			T_{vj} = 25 °C, $V_{GS(on)}$ = 15 V		50.4	61.5	
Gate-source threshold voltage	$V_{GS(th)}$	I_D = 8.3 mA, V_{DS} = V_{GS} (tested after 1 ms pulse at V_{GS} = 20 V)	T_{vj} = 25 °C	3.5	4.2	5.2	V
			T_{vj} = 175 °C		3.6		
Zero gate-voltage drain current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V	T_{vj} = 25 °C			150	µA
			T_{vj} = 175 °C		2.6		
Gate leakage current	I_{GSS}	V_{DS} = 0 V	V_{GS} = 23 V			100	nA
			V_{GS} = -10 V			-100	
Forward transconductance	g_{fs}	I_D = 19.3 A, V_{DS} = 20 V			12.9		S
Internal gate resistance	$R_{G,int}$	f = 1 MHz, V_{AC} = 25 mV			2.5		Ω
Input capacitance	C_{iss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			1620		pF
Output capacitance	C_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			75		pF
Reverse transfer capacitance	C_{rss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			11		pF
C_{oss} stored energy	E_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV			30		µJ
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = -2/18 V, turn-on pulse			51		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = -2/18 V, turn-on pulse			12.7		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = -2/18 V, turn-on pulse			10.2		nC

(table continues...)

Table 4 **(continued) Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		17		ns
			T_{vj} = 175 °C		16		
Rise time	t_r	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		6.4		ns
			T_{vj} = 175 °C		7.3		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		20.6		ns
			T_{vj} = 175 °C		21		
Fall time	t_f	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		6.9		ns
			T_{vj} = 175 °C		6.9		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		190		µJ
			T_{vj} = 175 °C		305		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		50		µJ
			T_{vj} = 175 °C		53		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 19.3 A, V_{GS} = 0/18 V, $R_{GS(on)}$ = 1 Ω, $R_{GS(off)}$ = 1 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		270		µJ
			T_{vj} = 175 °C		478		
Virtual junction temperature	T_{vj}			-55		175	°C

Note: *For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.*

The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.

Dynamic test circuit see Fig. F.

3 Body diode (MOSFET)

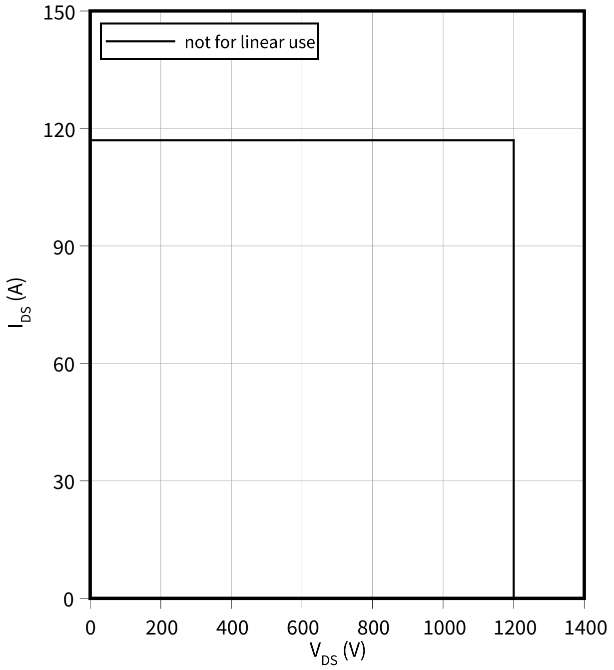
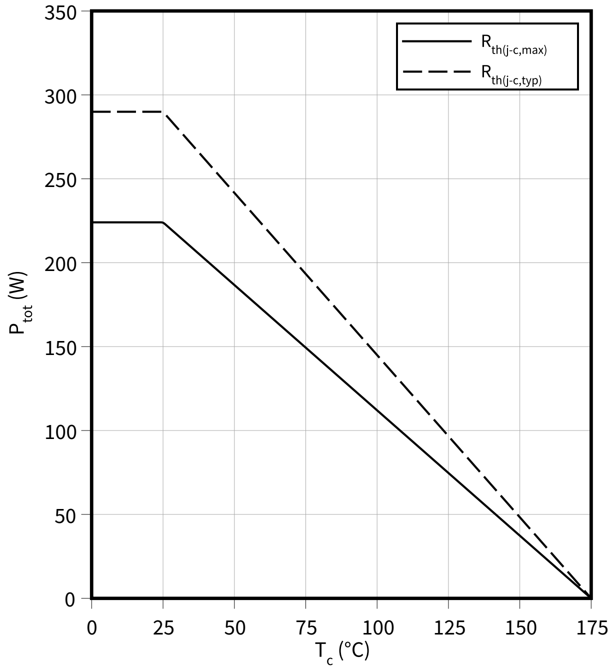
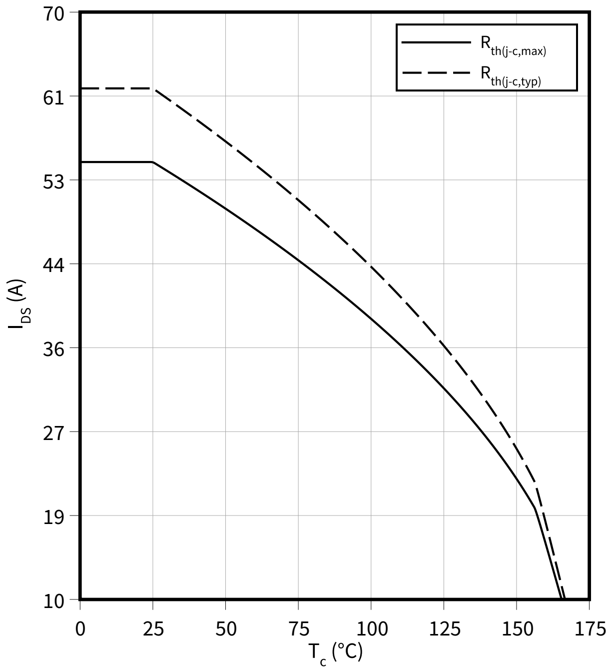
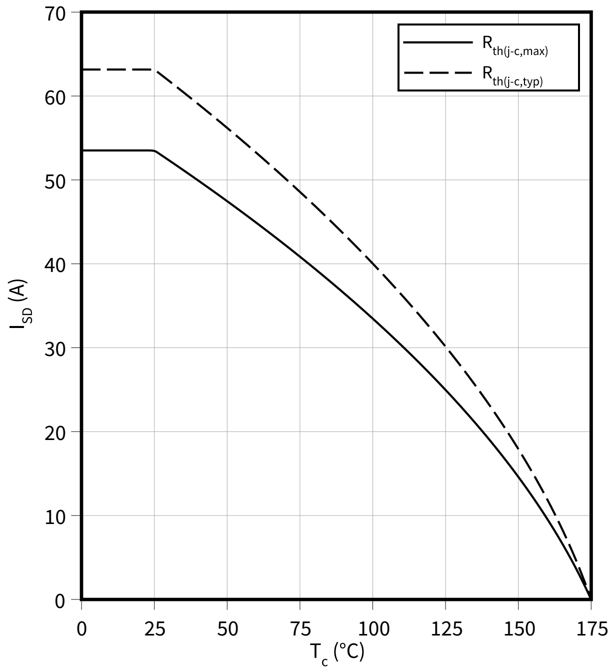
Table 5 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	$V_{GS} = 0$ V	$T_c = 25$ °C	54	A
			$T_c = 100$ °C	33	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	$V_{GS} = 0$ V		117	A

Table 6 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	$I_{SD} = 19.3$ A, $V_{GS} = 0$ V	$T_{vj} = 25$ °C		3.8	5	V
			$T_{vj} = 100$ °C		3.7		
			$T_{vj} = 175$ °C		3.6		
MOSFET forward recovery charge	Q_{fr}	$V_{DD} = 800$ V, $I_{SD} = 19.3$ A, $V_{GS} = 0$ V, $di_{SD}/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		160		nC
			$T_{vj} = 175$ °C		293		
MOSFET peak forward recovery current	I_{frm}	$V_{DD} = 800$ V, $I_{SD} = 19.3$ A, $V_{GS} = 0$ V, $di_{SD}/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		31		A
			$T_{vj} = 175$ °C		50		
MOSFET forward recovery energy	E_{fr}	$V_{DD} = 800$ V, $I_{SD} = 19.3$ A, $V_{GS} = 0$ V, $di_{SD}/dt = 3000$ A/µs, Q_{fr} includes also Q_C	$T_{vj} = 25$ °C		30		µJ
			$T_{vj} = 175$ °C		122		
Virtual junction temperature	T_{vj}			-55		175	°C

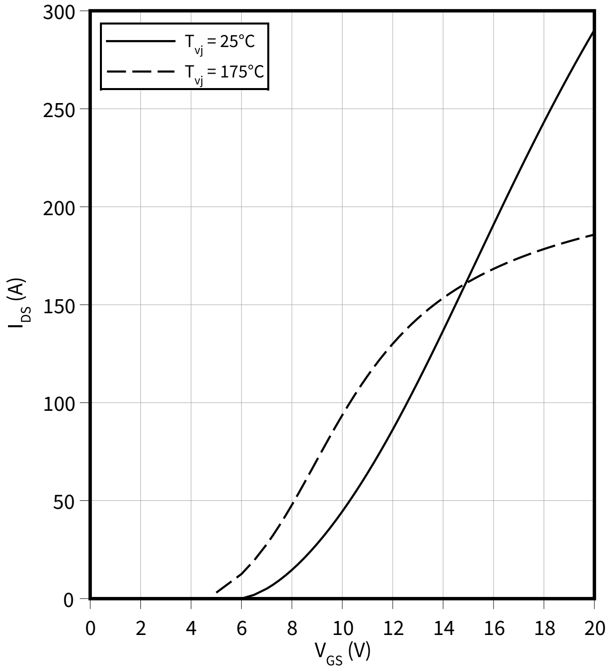
4 Characteristics diagrams

Reverse bias safe operating area (RBSOA) $I_{DS} = f(V_{DS})$ $T_{vj} \leq 175$ °C, $V_{GS} = 0/18$ V, $T_c = 25$ °C	**Power dissipation as a function of case temperature limited by bond wire** $P_{tot} = f(T_c)$
	
Maximum DC drain to source current as a function of case temperature limited by bond wire $I_{DS} = f(T_c)$	**Maximum source to drain current as a function of case temperature limited by bond wire** $I_{SD} = f(T_c)$ $V_{GS} = 0$ V
	

Typical transfer characteristic

$I_{DS} = f(V_{GS})$

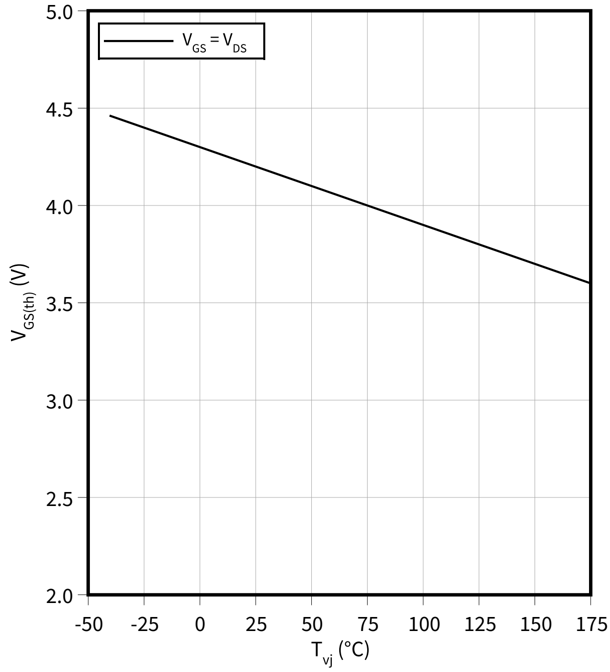
$V_{DS} = 20$ V, $t_p = 20$ µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

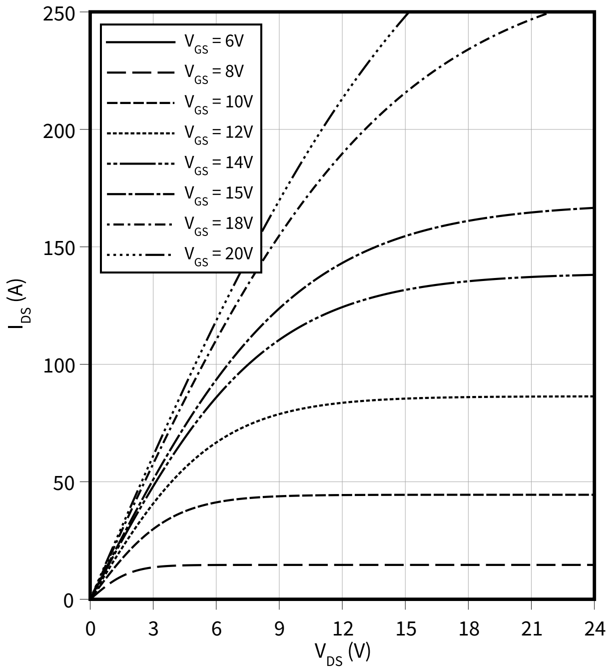
$I_D = 8.3$ mA



Typical output characteristic, V_{GS} as parameter

$I_{DS} = f(V_{DS})$

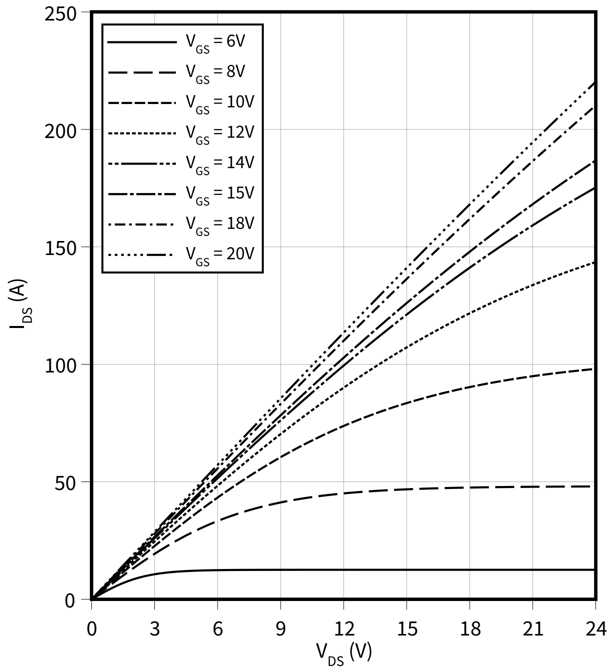
$T_{vj} = 25$ °C, $t_p = 20$ µs



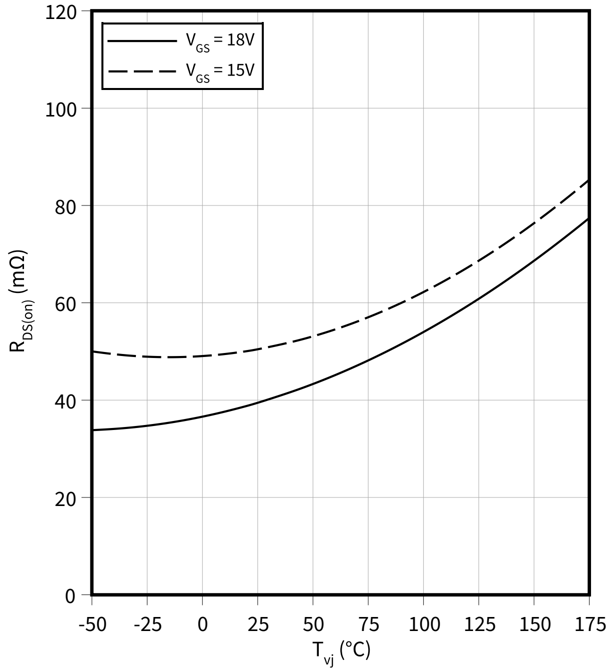
Typical output characteristic, V_{GS} as parameter

$I_{DS} = f(V_{DS})$

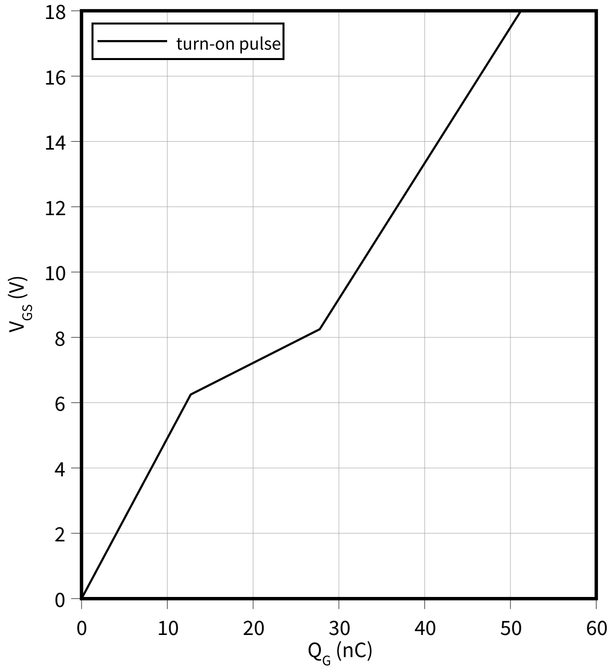
$T_{vj} = 175$ °C, $t_p = 20$ µs



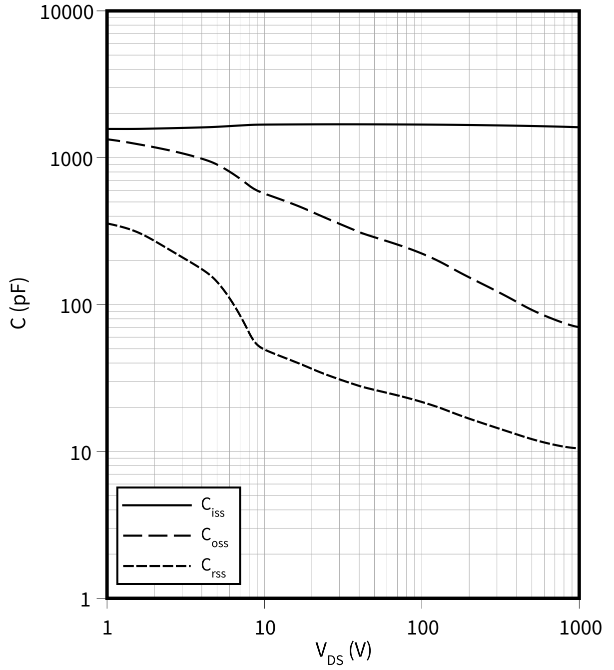
Typical on-state resistance as a function of junction temperature
$R_{DS(on)} = f(T_{vj})$
$I_D = 19.3$ A



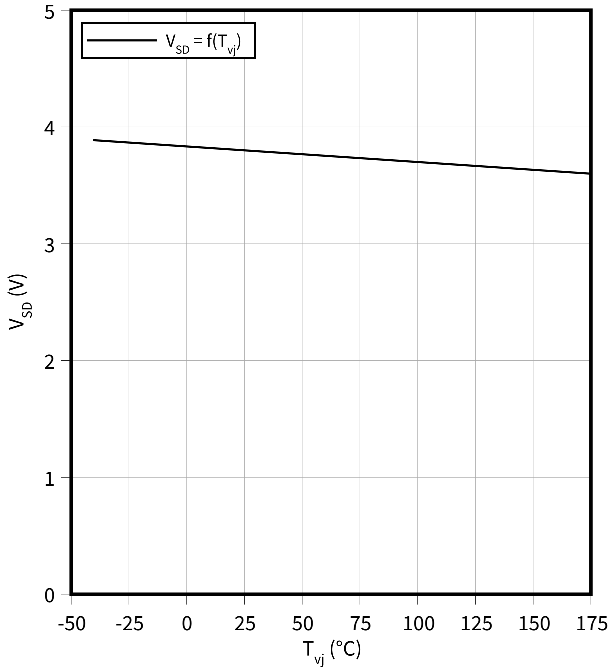
Typical gate charge
$V_{GS} = f(Q_G)$
$I_D = 19.3$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage
$C = f(V_{DS})$
f = 100 kHz, $V_{GS} = 0$ V



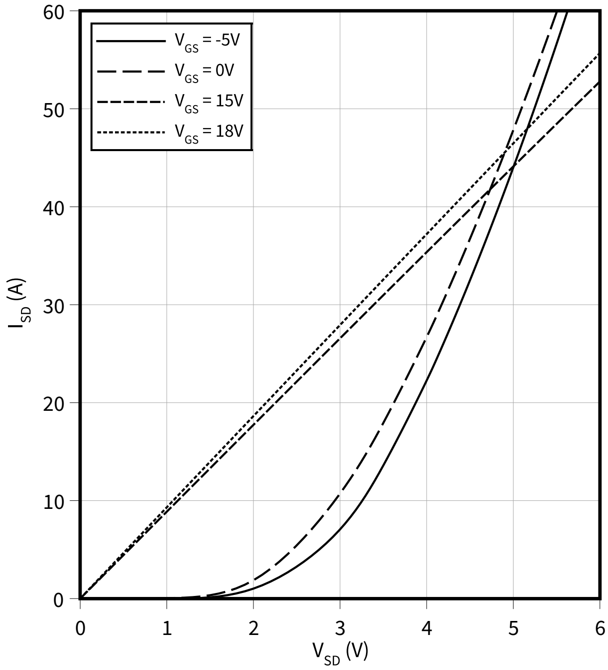
Typical reverse drain voltage as function of junction temperature
$V_{SD} = f(T_{vj})$
$I_{SD} = 19.3$ A, $V_{GS} = 0$ V



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

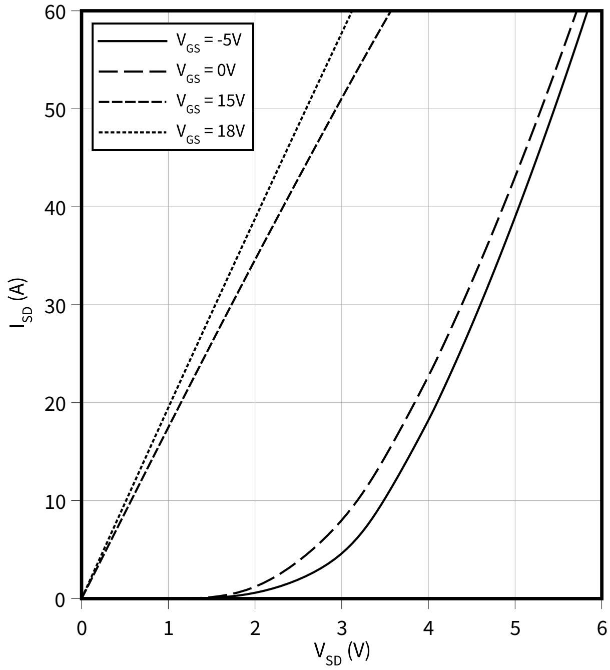
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

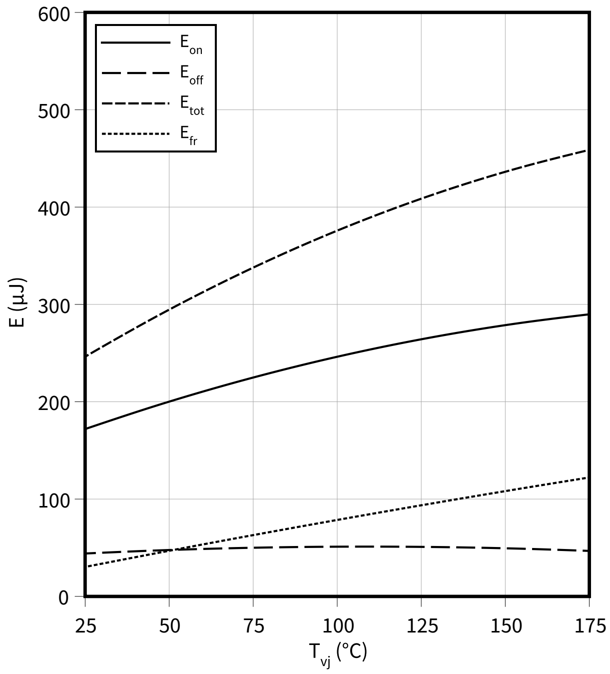
$t_p = 20\ µs$, $T_{vj} = 25\ °C$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V

$E = f(T_{vj})$

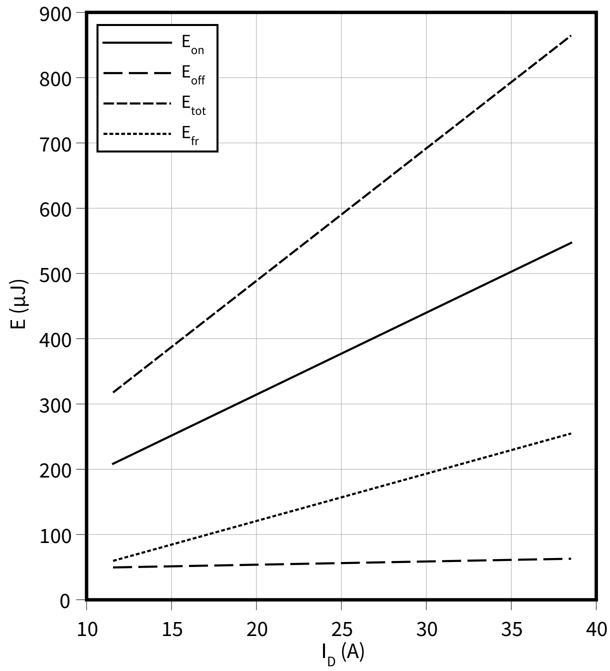
$V_{GS} = 0/18$ V, $I_D = 19.3$ A, $R_{G,ext} = 1\ Ω$, $V_{DD} = 800$ V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V

$E = f(I_D)$

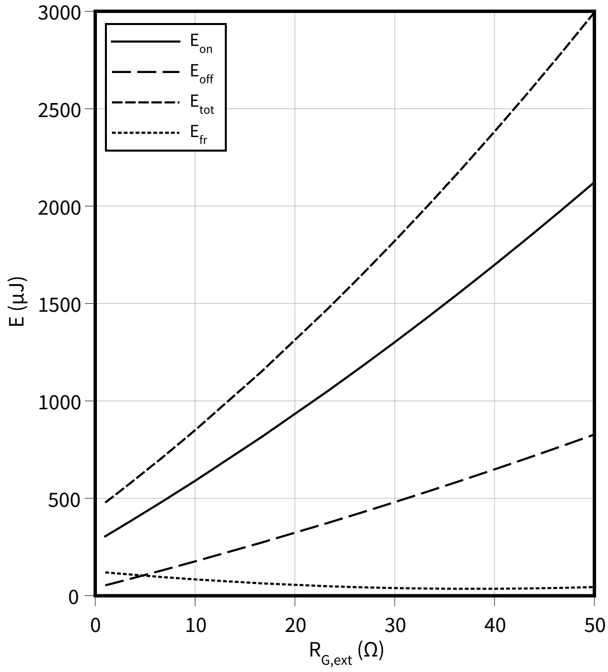
$V_{GS} = 0/18$ V, $T_{vj} = 175\ °C$, $R_{G,ext} = 1\ Ω$, $V_{DD} = 800$ V



Typical switching energy losses as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

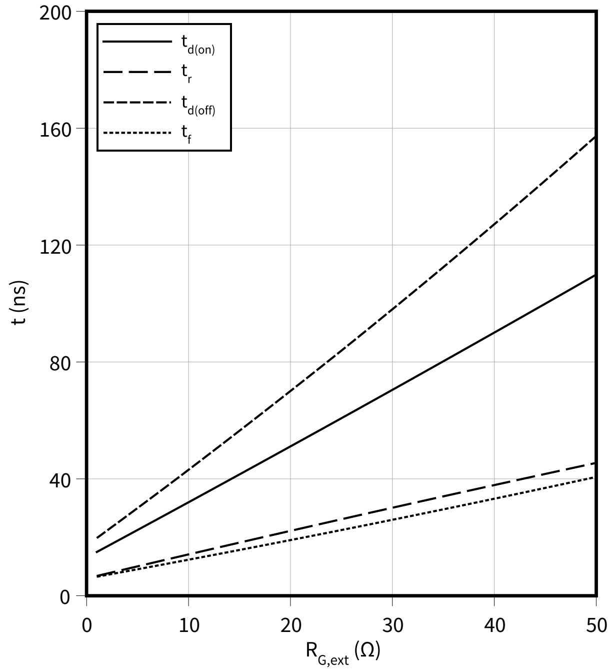
V_{GS} = 0 V, I_D = 19.3 A, T_{vj} = °C, V_{DD} = 800 V



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

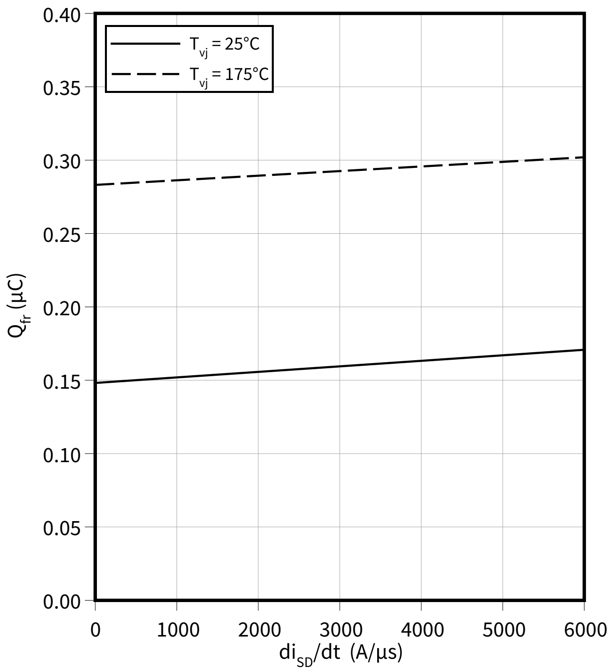
V_{GS} = 0/18 V, I_D = 19.3 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$Q_{fr} = f(di_{SD}/dt)$

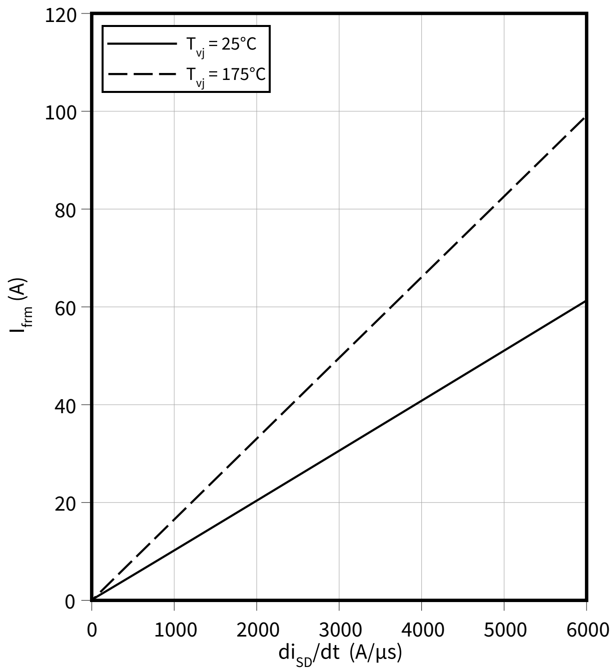
V_{GS} = 0/18 V, I_{SD} = 19.3 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(di_{SD}/dt)$

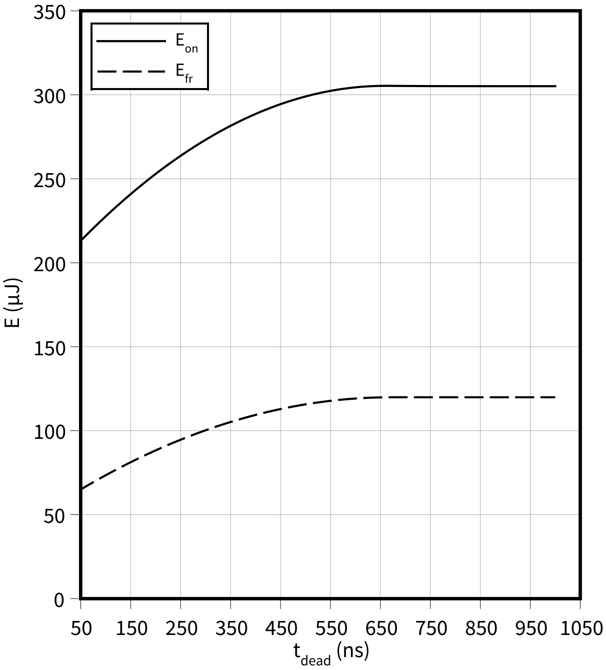
V_{GS} = 0/18 V, I_{SD} = 19.3 A, V_{DD} = 800 V



Typical switching energy losses as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(t_{dead})$

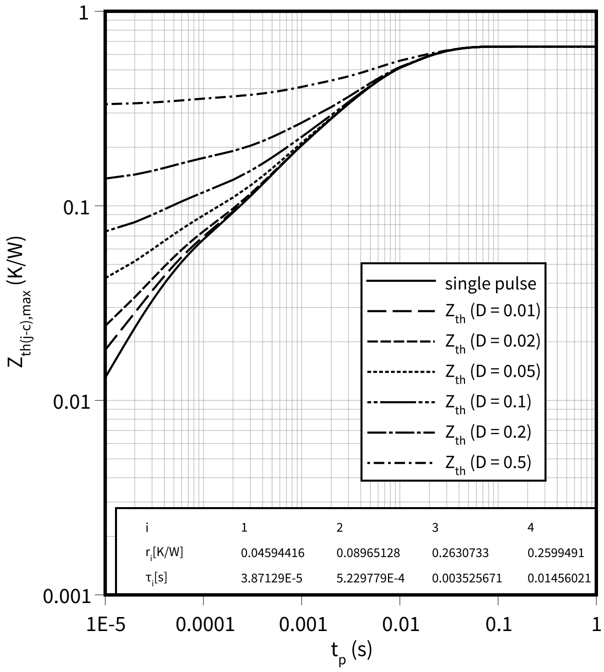
V_{GS} = -5/18 V, I_D = 19.3 A, T_{vj} = 175 °C, V_{DD} = 800 V



Max. transient thermal impedance (MOSFET/diode)

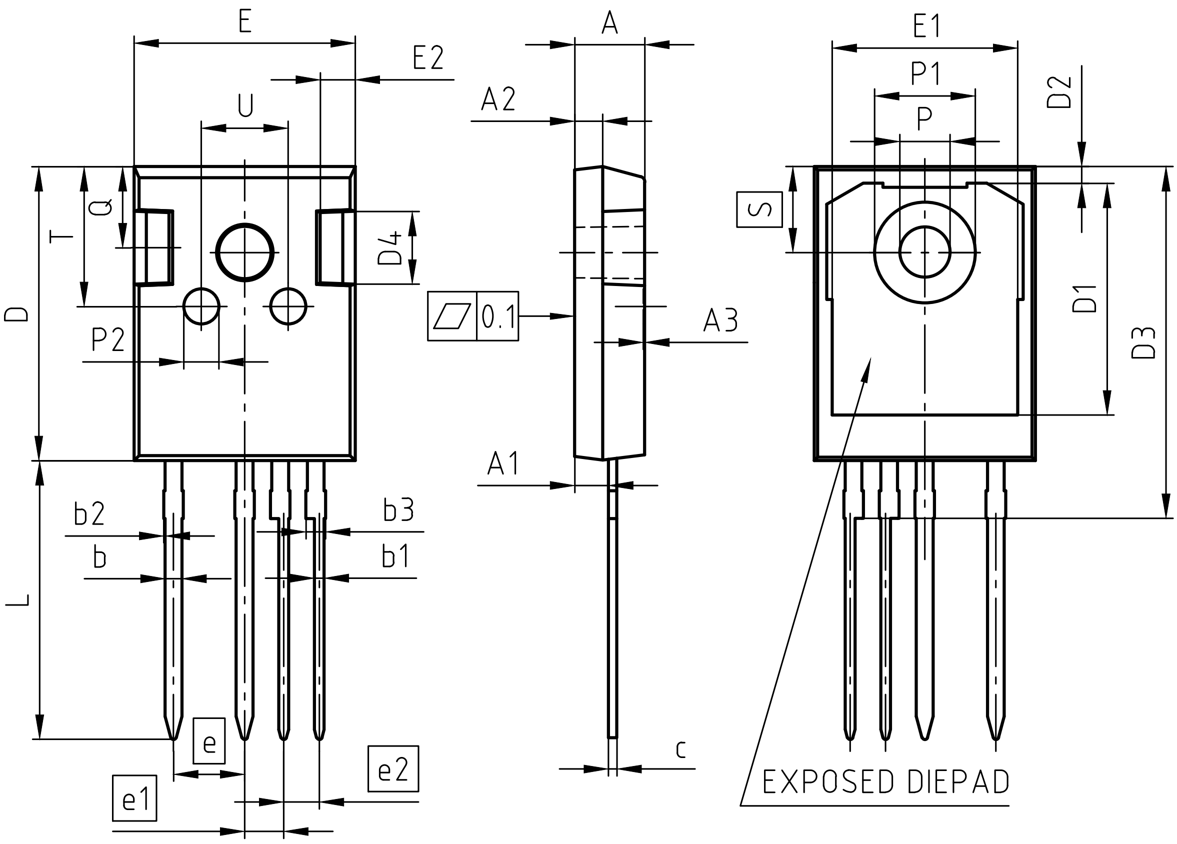
$Z_{th(j\text{-}c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines

PG-TO247-4-STD-NT3.7



NOTES:
ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH
OR PROTRUSIONS.

PACKAGE - GROUP NUMBER:	PG-TO247-4-U02				
DIMENSIONS	**MILLIMETERS**		**DIMENSIONS**	**MILLIMETERS**	
	MIN.	MAX.		MIN.	MAX.
A	4.90	5.10	**E**	15.70	15.90
A1	2.31	2.51	**E1**	13.10	13.50
A2	1.90	2.10	**E2**	2.40	2.60
A3	0.05	0.25	**e**	5.08	
b	1.10	1.30	**e1**	2.79	
b1	0.65	0.79	**e2**	2.54	
b2	---	0.20	**N**	4	
b3	1.34	1.44	**L**	19.80	20.10
c	0.58	0.66	**øP**	3.50	3.70
D	20.90	21.10	**øP1**	7.00	7.40
D1	16.25	16.85	**øP2**	2.40	2.60
D2	1.05	1.35	**Q**	5.60	6.00
D3	24.97	25.27	**S**	6.15	
D4	4.90	5.10	**T**	9.80	10.20
			U	6.00	6.40

Figure 1

6 Testing conditions

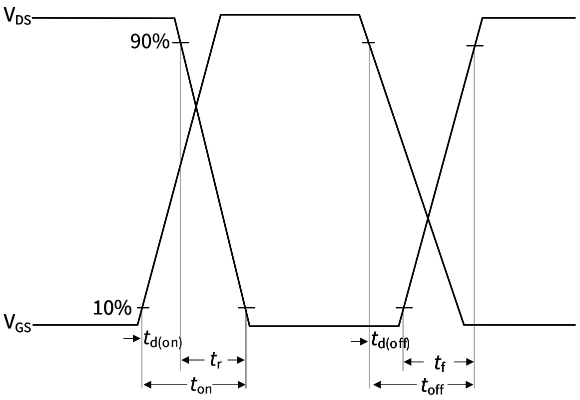


Figure A. **Definition of switching times**

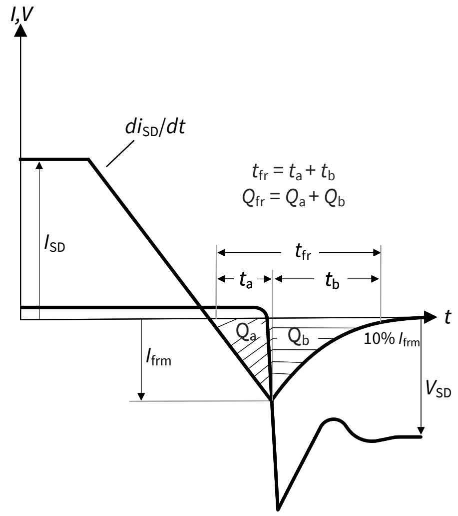


Figure B. **Definition of body diode switching characteristics**

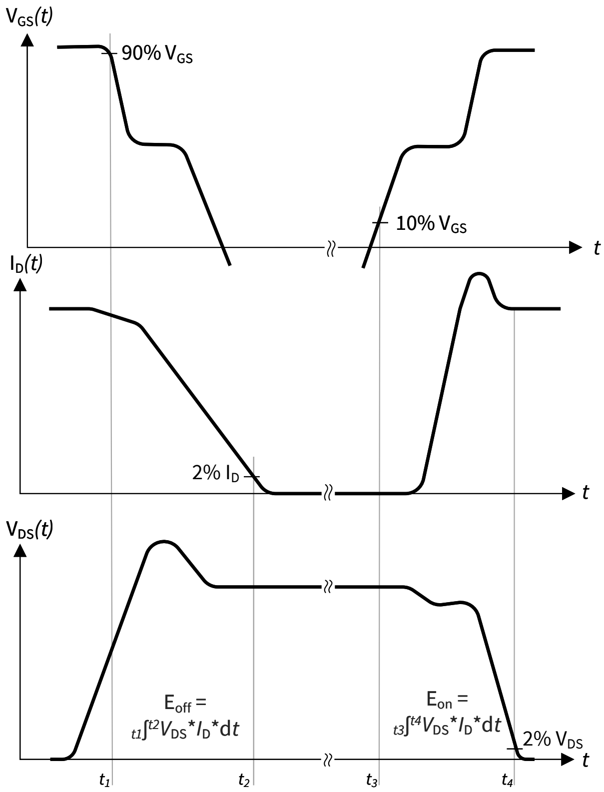


Figure C. **Definition of switching losses**

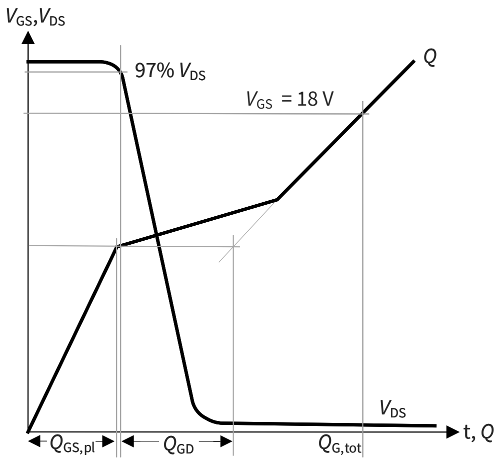


Figure D. **Definition of QGD**

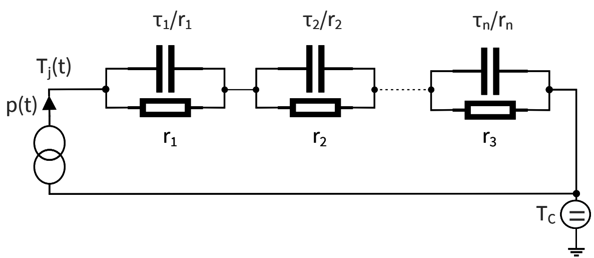


Figure E. **Thermal equivalent circuit**

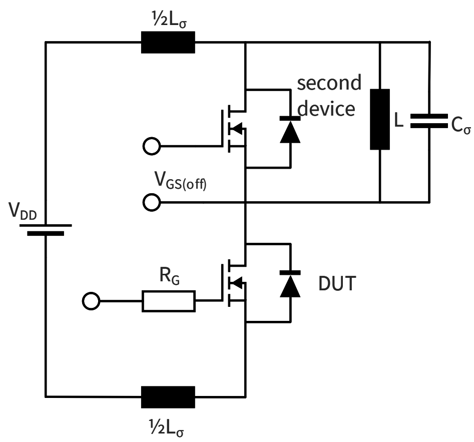


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
1.00	2022-02-03	Final datasheet
1.10	2022-08-11	Change of test condition of dynamic capacitances in Table 4, "Characteristic values" (C_{iss}, C_{oss}, C_{rss}): V_{DD}= 25 V to V_{DD}= 800 V Correction of unit of "Input capacitance" C_{iss} from nF to pF Change of V_{GS} "Gate-source voltage, max. static voltage" in Table 2, "Maximum rated values" from -5/20 V to -7/20 V Editorial changes in "Features" on page 1 Editorial changes in "Package" on page 1 Correction of unit of x-axis at diagram "Max. transient thermal impedance (MOSFET/diode)" from µs to s, on page 13 Correction of diagram "Max. transient thermal impedance (MOSFET/ diode)", on page 13
1.20	2023-05-08	Correction of gate charge values in Table 4 Editorial changes

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