

# MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™ Power-Transistor, 60 V  
IPA029N06N

## Data Sheet

Rev. 2.2  
Final

## 1 Description

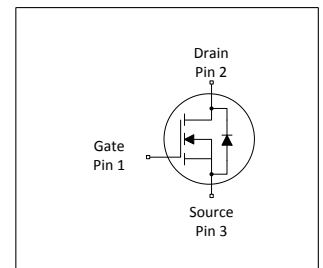
### Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	2.9	m $\Omega$
$I_D$	84	A
$Q_{OSS}$	65	nC
$Q_G(0V..10V)$	56	nC



Type / Ordering Code	Package	Marking	Related Links
IPA029N06N	PG-TO220-FP	029N06N	-

<sup>1)</sup> J-STD20 and JESD22

**Table of Contents**

Description .....	2
Maximum ratings .....	4
Thermal characteristics .....	4
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Package Outlines .....	10
Revision History .....	11
Disclaimer .....	11

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	84 59	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	336	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	140	mJ	$I_D=84\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	38	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	2.9	3.9	K/W	-

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$ , $I_D=75\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.6 3.0	2.9 3.5	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=84\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=21\text{ A}$
Gate resistance <sup>3)</sup>	$R_G$	0.65	1.3	1.95	$\Omega$	-
Transconductance	$g_{fs}$	75	150	-	S	$ V_{DS} >2 I_D /R_{DS(on)max}$ , $I_D=84\text{ A}$

<sup>1)</sup> See figure 3 for more detailed information

<sup>2)</sup> See figure 13 for more detailed information

<sup>3)</sup> Defined by design. Not subject to production test

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	4100	5125	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	980	1225	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	39	78	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=84\text{ A}$ , $R_{G,ext}=3\ \Omega$
Rise time	$t_r$	-	15	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=84\text{ A}$ , $R_{G,ext}=3\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=84\text{ A}$ , $R_{G,ext}=3\ \Omega$
Fall time	$t_f$	-	11	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=84\text{ A}$ , $R_{G,ext}=3\ \Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	19	-	nC	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	11	-	nC	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	10	15	nC	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	18	-	nC	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	56	66	nC	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	$V_{DD}=30\text{ V}$ , $I_D=84\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	49	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	65	82	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	32	A	$T_C=25\text{ }^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$	-	-	336	A	$T_C=25\text{ }^\circ\text{C}$
Diode forward voltage	$V_{SD}$	-	0.85	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=32\text{ A}$ , $T_J=25\text{ }^\circ\text{C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	36	58	ns	$V_R=30\text{ V}$ , $I_F=32\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	31	-	nC	$V_R=30\text{ V}$ , $I_F=32\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

## 5 Electrical characteristics diagrams

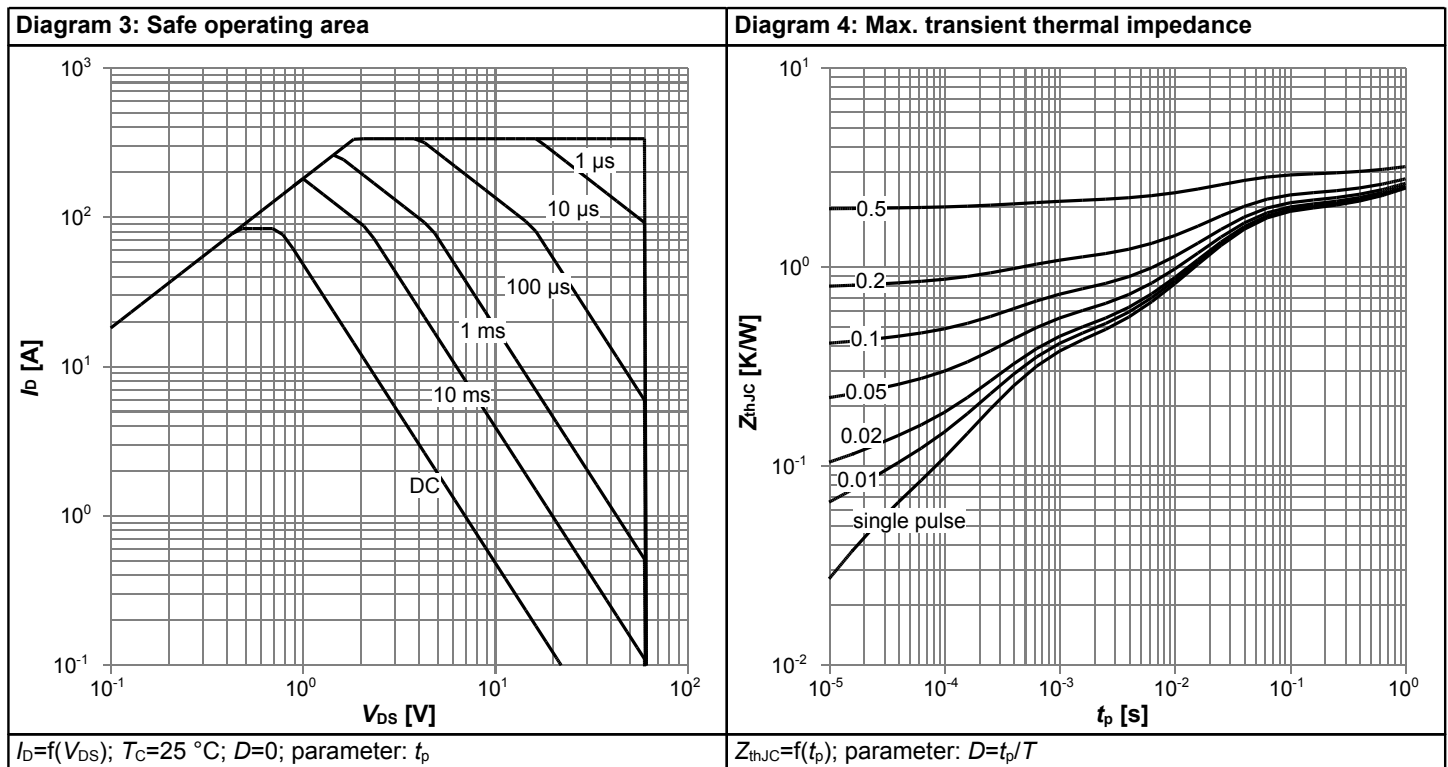
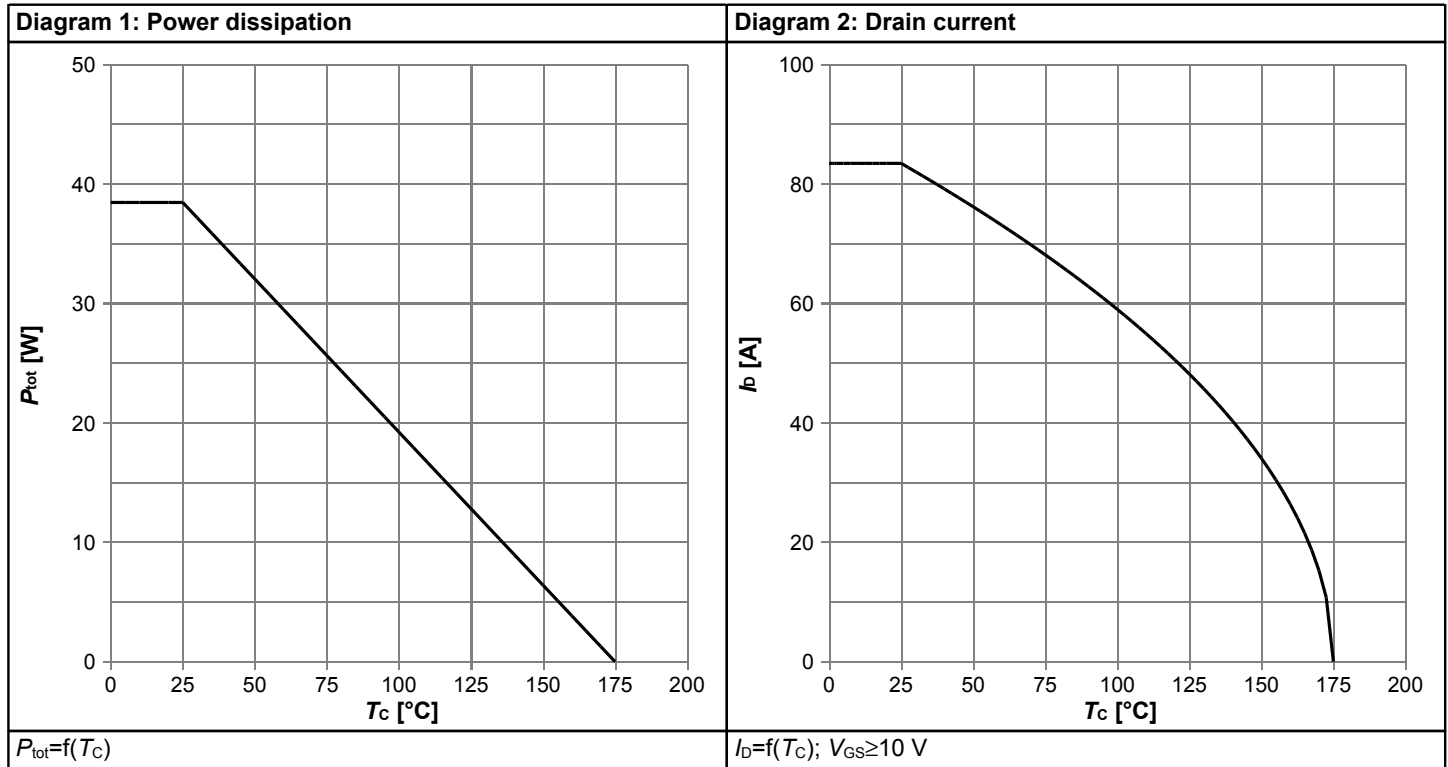
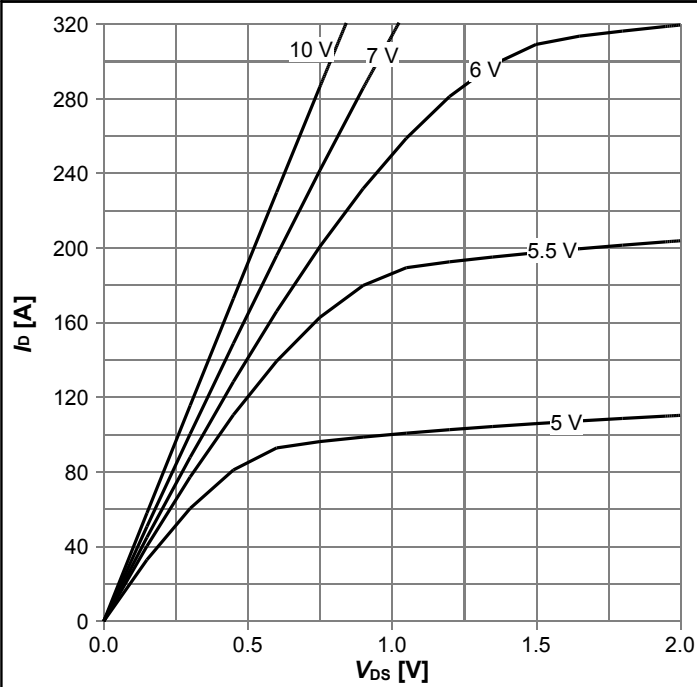
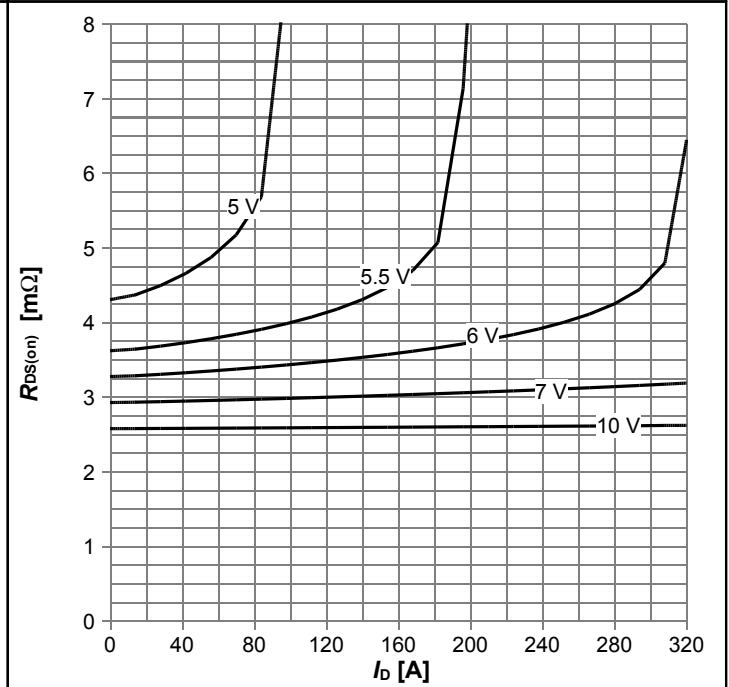


Diagram 5: Typ. output characteristics



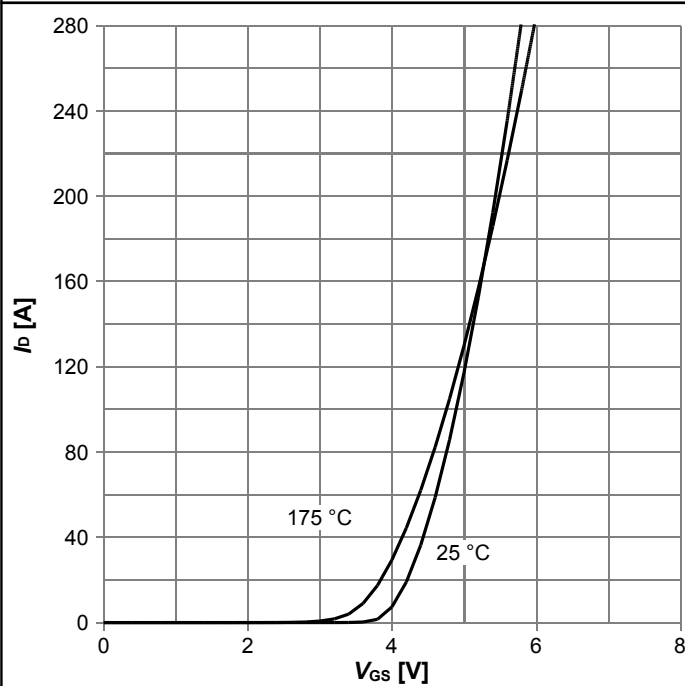
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



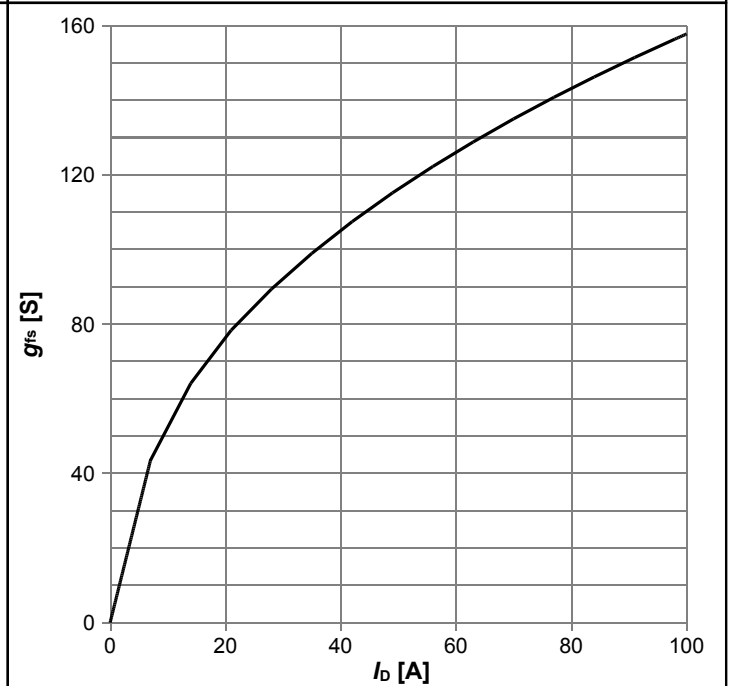
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



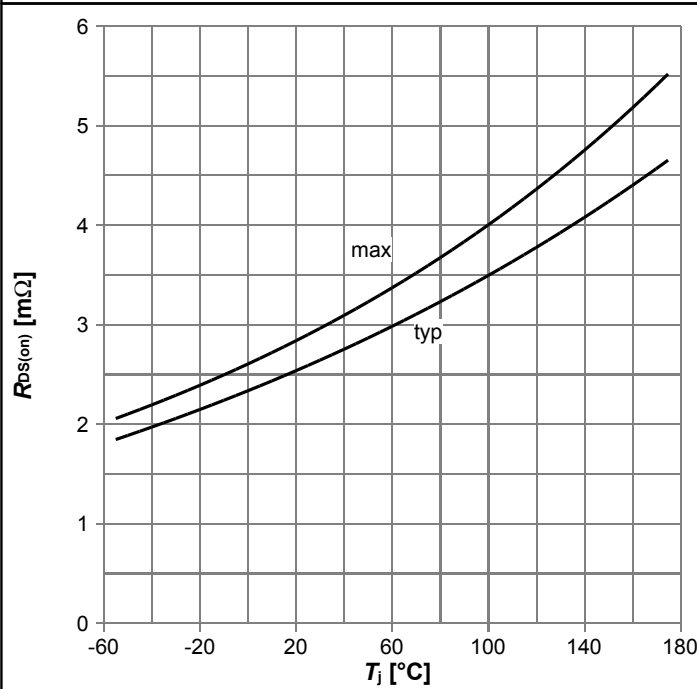
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



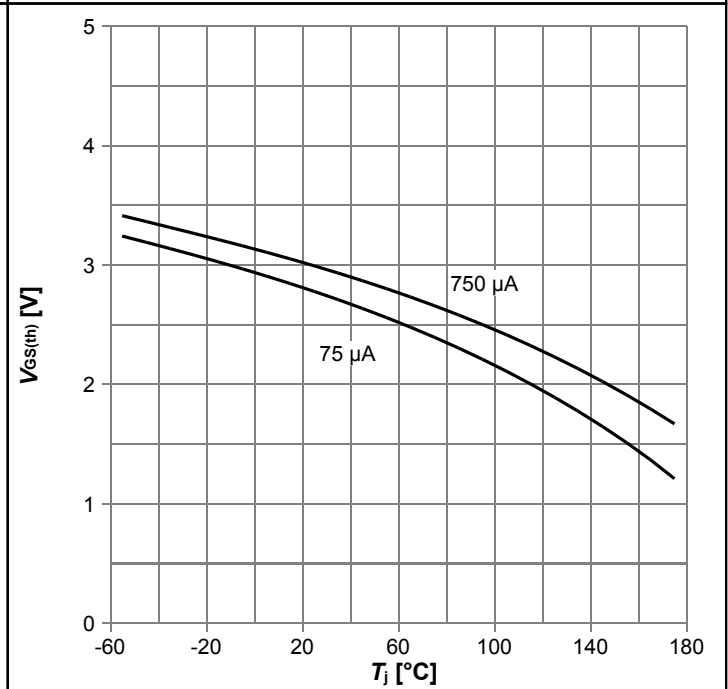
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



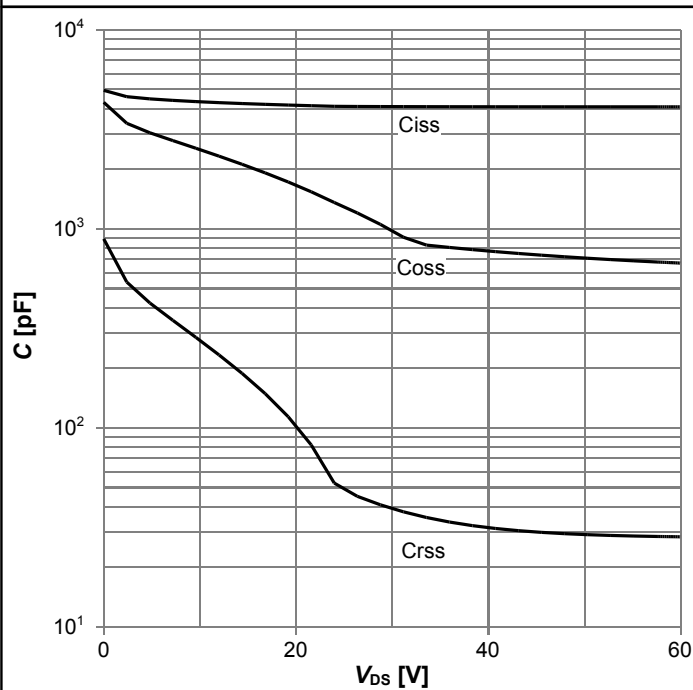
$R_{DS(on)}=f(T_j); I_D=84\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



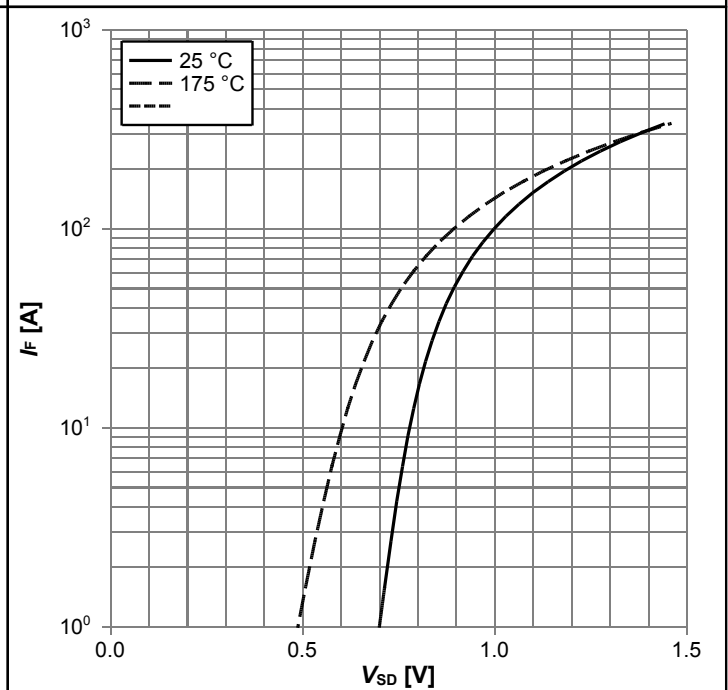
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

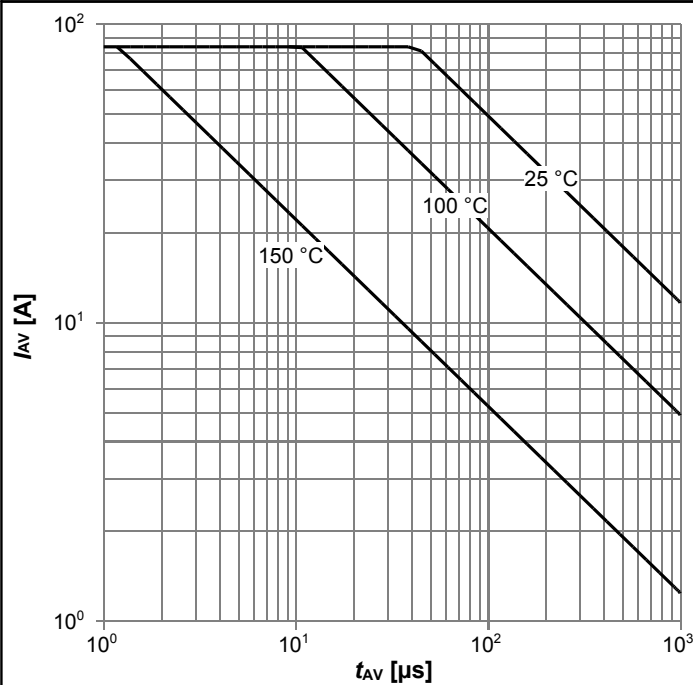
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

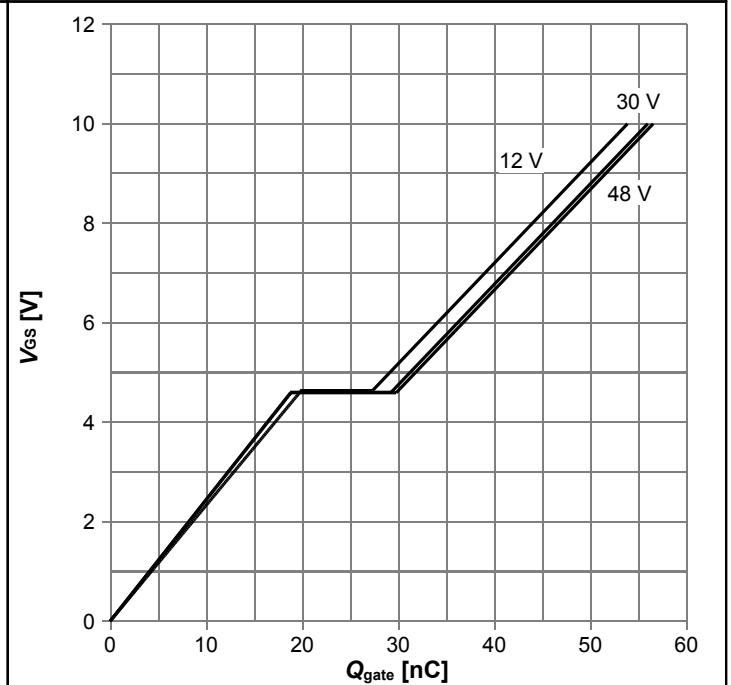


Diagram 13: Avalanche characteristics



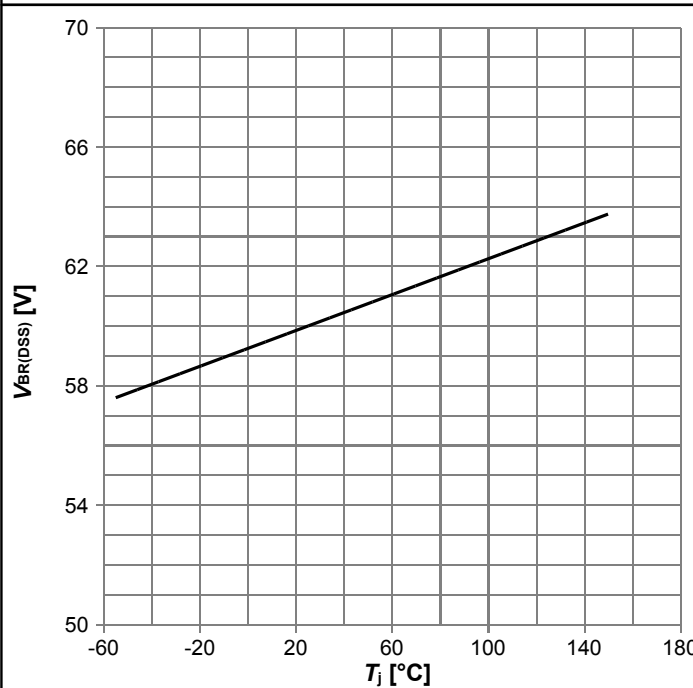
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



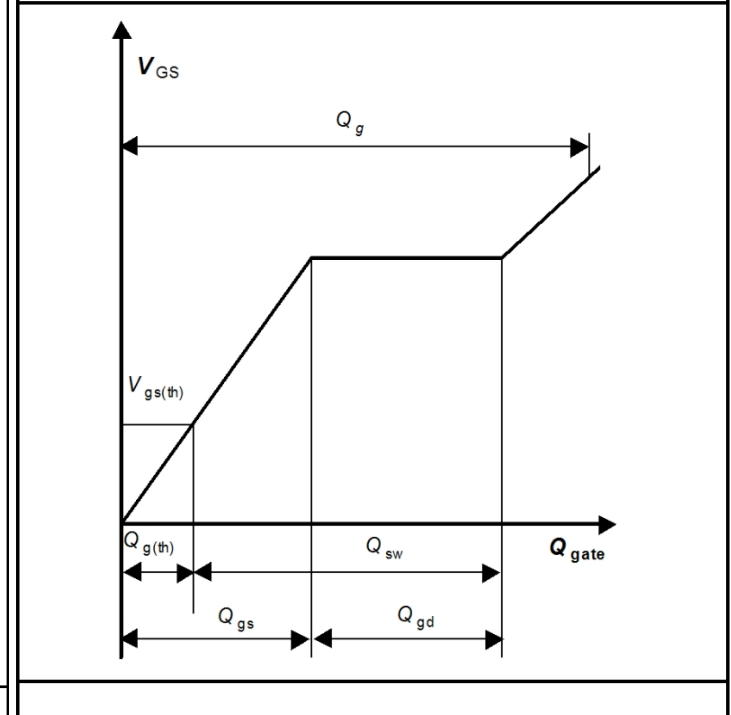
$V_{GS}=f(Q_{gate}); I_D=84$  A pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

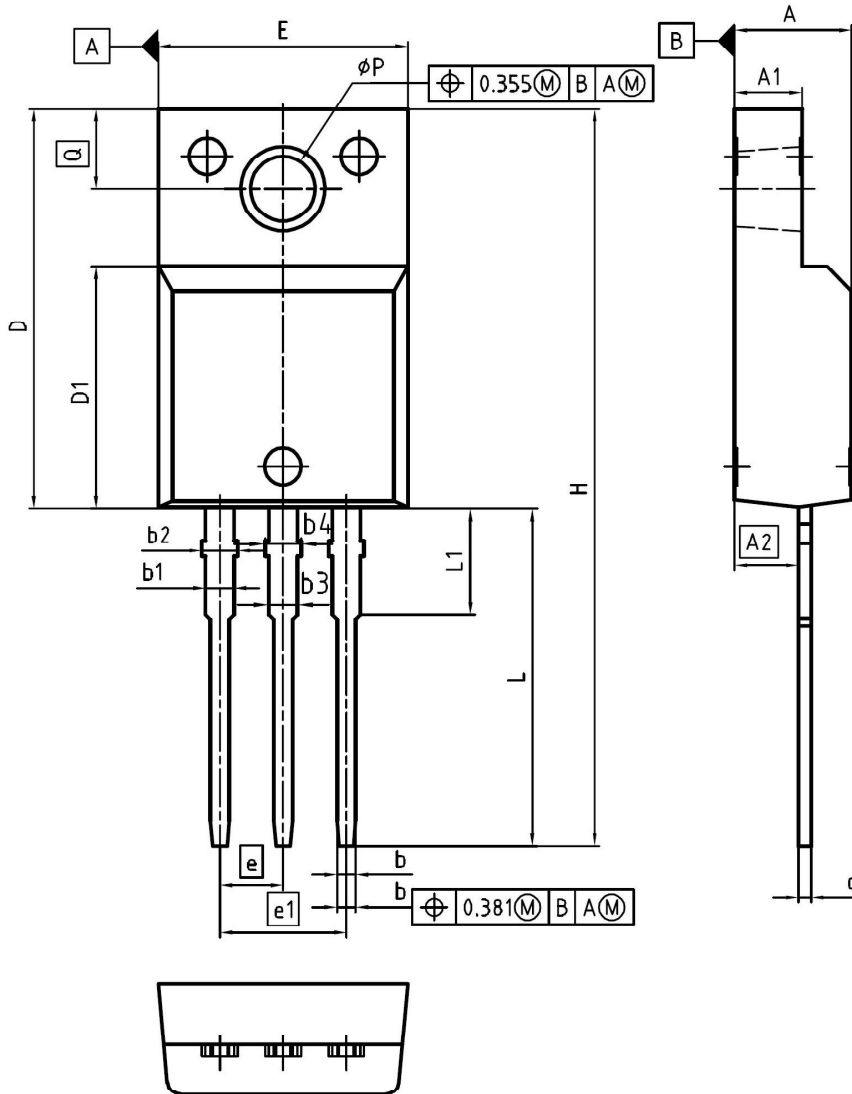


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.55	4.85	0.179	0.191
A1	2.55	2.85	0.100	0.112
A2	2.42	2.72	0.095	0.107
b	0.65	0.85	0.026	0.033
b1	0.95	1.33	0.037	0.052
b2	0.95	1.51	0.037	0.059
b3	0.65	1.33	0.026	0.052
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.85	16.15	0.624	0.636
D1	9.53	9.83	0.375	0.387
E	10.35	10.65	0.407	0.419
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H	29.45	29.75	1.159	1.171
L	13.45	13.75	0.530	0.541
L1	3.15	3.45	0.124	0.136
phi P	2.95	3.20	0.116	0.126
Q	3.15	3.50	0.124	0.138

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REVISION  
03

Figure 1 Outline PG-TO220-FP, dimensions in mm/inches

## Revision History

IPA029N06N

**Revision: 2015-04-09, Rev. 2.2**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2014-06-19	Release of Final Version
2.2	2015-04-09	Rev.2.1

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